# Two-channel, 500-kSPS operation of the ADS8361

**By Tom Hendrick** (Email: t-hendrick@ti.com)
*Data Acquisition Applications*

## Introduction

The ADS8361 is a member of the Texas Instruments (TI) motor control products family of serial analog-to-digital converters (ADCs). The ADS8361 is a 2+2-channel, 16-bit upgrade for the 2+2-channel, 12-bit ADS7861. Its 3.3- to 5-V digital interface is ideally suited for use with the entire TMS320 series of digital signal processors from TI.

The device features two independent 500-kSPS ADC channels, each with its own sample-and-hold circuits and serial data output pin. A user-controllable multiplexer (MUX) allows simultaneous sampling of two 2-channel pairs (4 total channels) at 250 kSPS.

## Hardware pins

The ADS8361 features three hardware pins (M0, M1, and A0) that select various operating modes (see Table 1).

Mode I allows for 2-channel operation at speeds of up to 500 kSPS by utilizing both conversion channels. Mode II reduces the maximum throughput to 250 kSPS by using a single serial output pin (OUTA) to present the simultaneously sampled data from channel pairs Ax and Bx. Toggling the address pin A0 controls the selection of channel pair 0 or 1.

Modes III and IV allow the sequential output of both simultaneously sampled channel pairs A0 and B0, followed by A1 and B1. Since Mode III uses both serial outputs A and B, the maximum throughput can be maintained at 250 kSPS. Mode IV presents all 4 converted channels at the OUTA pins, with a maximum throughput of 125 kSPS.

## Single McBSP operation

With the interface method presented in Reference 1, applications that do not require simultaneous sampling but do need two fast, independent ADCs can benefit from the ADS8361's 2-µs conversion time. An external MUX or bus switch between the serial outputs would allow 1- to 4-channel operation of channel A or B through a single multichannel buffered serial port (McBSP). Each channel can be independently operated at 500 kSPS. This method would require some sort of control over the state of one or more of the hardware pins M0, M1, and A0, adding additional logic to the design.

Applications with 2 channels and simultaneous-sampling rates of 250 kSPS or less also can use a single McBSP. Hardware pins M0 and M1 can be fixed at ground and $V_{CC}$, with A0 controlling the channel pairs to be converted (Mode II). This method uses the internal MUX to switch the conversion results from the A and B channels through OUTA. Tying both M0 and M1 to $V_{CC}$ permits 4-channel, simultaneous-sampling applications to be realized. It also allows sequential presentation of two simultaneously sampled channel pairs, 4 channels in all (Mode IV), for applications needing sampling rates of 125 kSPS or less.

If a second McBSP is available, 2- and 4-channel, simultaneous-sampling operation can be realized with no additional "glue logic" required, at 500-kSPS throughput per channel for 2 channels and 250-kSPS for 4 channels.

## Dual McBSP operation

The simultaneous conversion properties of the ADS8361 allow conversion data from channels Ax and Bx to be presented to the OUTA and OUTB pins at the same time. Both channels use the same conversion start (CONVST) signal and the same conversion clock so that data skew between A and B outputs is minimized.

To achieve full-speed, 2- and 4-channel operation, the transmitter portion (CLKX, FSX and DX lines) of one McBSP can be used to control the conversion speed, timing, and channel selection of the ADS8361. The ADS8361's serial data outputs, along with clock and frame sync

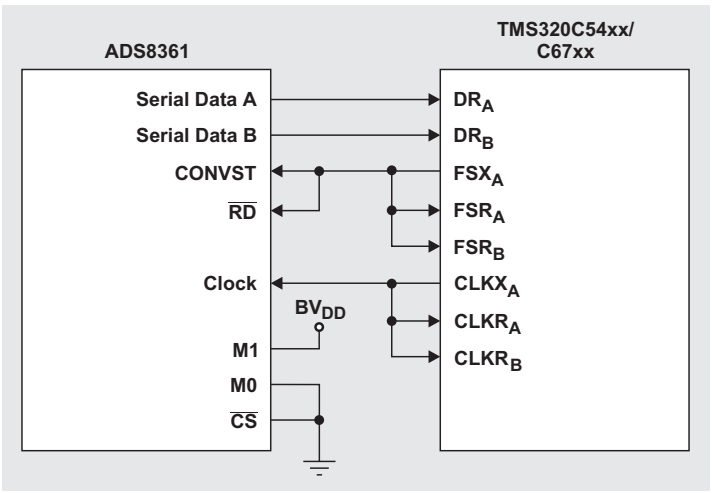
**Table 1. Operating modes of ADS8361 hardware pins**

| MODE | HARDWARE PINS | | | 2-CHANNEL/ 4-CHANNEL OPERATION | DATA ON SERIAL OUTPUTS | CHANNELS CONVERTED | TOTAL THROUGHPUT (kSPS) |
|---|---|---|---|---|---|---|---|
| | M0 | M1 | A0 | | | | |
| I | 0 | 0 | 0 | 2-channel | A and B | A0 and B0 | 500 |
| | 0 | 0 | 1 | 2-channel | A and B | A1 and B1 | 500 |
| II | 0 | 1 | 0 | 2-channel | A only | A0 and B0 | 250 |
| | 0 | 1 | 1 | 2-channel | A only | A1 and B1 | 250 |
| III | 1 | 0 | X | 4-channel | A and B | Sequential | 250 |
| IV | 1 | 1 | X | 4-channel | A only | Sequential | 125 |

return, are then fed to the receiver portions of two McBSPs as shown in Figure 1.

To enhance the control of the ADS8361 further, the unused transmitter section of the second McBSP can be configured as GPIO and connected to the control pins M0, M1, and A0 of the ADS8361. For simultaneous, 2-channel operation at a 500-kSPS-per-channel conversion rate, all that is required is a single GPIO line to toggle A0.

**Figure 1. Hardware interface example**




## Software interface

A project database for this article was developed and compiled with Code Composer Studio™ version 2.20. The most involved portion of writing the code for this simple interface was programming the McBSP. If you wish to receive the project file used in this example, please feel free to send an email to datconvapps@list.ti.com with the title of this article as the subject.

Since the two converters in the ADS8361 share a common interrupt, conversion clock, and conversion start mechanism, the software requirements for the DSP are quite simple. The first McBSP is configured to transmit a frame sync pulse to act as the conversion start signal. $FSR_A$, $DX_A$ (Serial Data A), and $CLKR_A$ are returned to the first McBSP. The ADS8361's BUSY pin acts as an interrupt to the DSP, which in turn reads the serial data. When the second serial output of the ADS8361 is used, FSR, CLKR, and Serial OUTB are returned to the receiver of the second McBSP. This enables the user to configure the transmitter portion as GPIO to control channel 0 or channel 1 selection of the ADS8361 without the use of additional decode circuits.

## Create a .CDB file

Code Composer Studio's graphical user interface for the DSP/BIOS™ configuration (.CDB file) and Chip Support Libraries (CSL) have made it easier than ever to write programs and set up the McBSP.

The first step in creating a project that accommodates the ADS8361 with two McBSPs is to create a .CDB file, then add it to the project. This process creates a .CMD file for the linker, which also needs to be added to the project. Additional DSP/BIOS files are created too, which are added to the project automatically when the .CDB file is loaded. All necessary files and libraries are loaded automatically, based on the DSP/BIOS configuration options set.

By expanding the CSL tab in the .CDB file, the user gains access to the McBSP Configuration Manager. A McBSP configuration is added, and the desired values for clock speed, etc., are set. Once the first configuration is done, it is simply highlighted, copied, and pasted. This creates two copies of the same configuration, each with its own name.

```
MCBSP_Config mcbspCfg0 = {
     0x0000,         /*  Serial Port Control Register 1   */
     0x0220,         /*  Serial Port Control Register 2   */
     0x0060,         /*  Receive Control Register 1   */
     0x0000,         /*  Receive Control Register 2   */
     0x0060,         /*  Transmit Control Register 1   */
     0x0005,         /*  Transmit Control Register 2   */
     0x0109,         /*  Sample Rate Generator Register 1   */
     0x3014,         /*  Sample Rate Generator Register 2   */
     0x0000,         /*  Multichannel Control Register 1   */
     0x0000,         /*  Multichannel Control Register 2   */
     0x2a00,         /*  Pin Control Register   */
};
MCBSP_Config mcbspCfg1 = {
     0x0000,         /*  Serial Port Control Register 1   */
     0x0200,         /*  Serial Port Control Register 2   */
     0x0060,         /*  Receive Control Register 1   */
     0x0000,         /*  Receive Control Register 2   */
     0x0000,         /*  Transmit Control Register 1   */
     0x0000,         /*  Transmit Control Register 2   */
     0x010e,         /*  Sample Rate Generator Register 1   */
     0x3013,         /*  Sample Rate Generator Register 2   */
     0x0000,         /*  Multichannel Control Register 1   */
     0x0000,         /*  Multichannel Control Register 2   */
     0x0a00,         /*  Pin Control Register   */
};
```

## McBSP settings

The McBSPs are configured as shown in the sidebar at left.

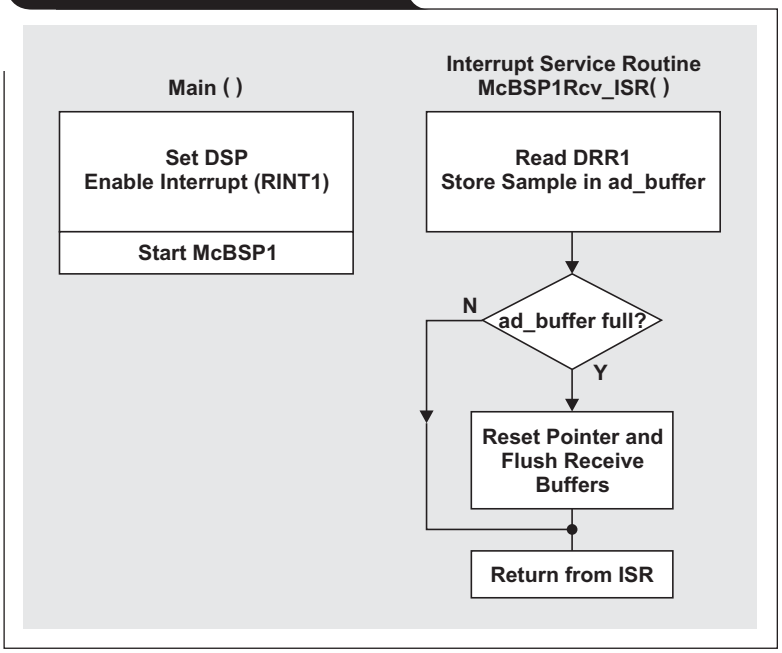
The McBSP is programmed as a serial port in nonstop clock mode (or DSP mode). Frame sync and serial clock signals are output pins. The receiver is set for 16-bit transfers with a 2-bit delay on data receive. The frame sync (FSX1) is generated by the sample-rate generator and is used for both the $\overline{RD}$ and CONVST signals on the ADS8361 by jumper W2 on the evaluation module (EVM).

In the sample code (see sidebar), the ADS8361 is running at 469 kSPS with a serial clock of 9.375 MHz. The C6711 DSP Starter Kit clocks the C6711 DSP at 150 MHz. The sample-rate generator clock source is half the CPU clock, or 75 MHz. The 9.4-MHz clock on CLKX is achieved by setting the CLKGDV bit field in the sample-rate generator register to 8. The formula for calculating the serial clock is

$$\text{CLOCK} = \frac{\frac{\text{CPUCLOCK}}{2}}{\text{CLKDIV} + 1}.$$

By this equation, each clock's cycle is approximately 106.6 ns, triggering a frame-sync pulse every 20 serial clock cycles, which gives a sample rate of 468 kHz. The frame period (FPER) field, in the sample-rate generator register, is where the 20-cycle period is set.

**Figure 2. Software flow chart**




## Software flow

The software presented in this article reads 1024 samples at 469 kHz continuously. As selected in the configuration tool, all the register and peripheral programming is done during initialization. DSP/BIOS pre-initializes all the McBSP registers and other DSP registers before arriving in the main function. As a result, the main function simply enables the interrupt service routine and McBSP1; from then on, the DSP/BIOS and McBSP receive ISR do all the work. When a McBSP1 receive interrupt occurs, `McBSP1Rcv_ISR` reads the port and stores the data in `ad_buffer`. When the buffer is full, it resets the index, `i`, to the beginning and flushes the receive buffer (see Figure 2).

## Conclusion

An EVM is available that provides a platform to demonstrate the functionality of the ADS8361 ADC with various TI DSPs and microcontrollers, while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, visit **www**.ti.com/sc/device/ADS8361 and select Development Tools.

## References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.


| Document Title | TI Lit. # |
|---|---|
| 1. Tom Hendrick, "Interfacing the ADS8361 to the TMS320C6711 DSP," Application Report | slaa164 |
| 2. "Dual, 500kSPS, 16-Bit, 2 + 2 Channel, Simultaneous Sampling Analog-to-Digital Converter," ADS8361 Data Sheet | sbas230 |
| 3. "TMS320C6711, TMS320C6711B, TMS320C6711C Floating-Point Digital Signal Processing," Data Sheet | sprs088 |
| 4. "TMS320C6000 DSP/BIOS User's Guide" | spru303 |
| 5. "TMS320 Cross-Platform Daughtercard Specification, Revision 1.0," Application Report | spra711 |


## Related Web sites

**analog.ti.com**
**www.ti.com/sc/device/***partnumber*
Replace *partnumber* with ADS7861, ADS8361 or TMS320C6711

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