A/D and D/A conversion of PC graphics and component video signals, Part 2: Software and control

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Introduction

The first article of this two-part series, published in the February 2001 issue of *Analog Applications Journal*, discussed the THS8083EVM hardware, a TI evaluation module featuring the THS8083 (a triple 8-bit high-speed ADC with integrated PLL for component video and PC graphics digitizing) and the THS8134 (a triple 8-bit video DAC). Having presented an overview of the features and EVM block diagram in the earlier article, we now turn our attention to the design of the complex programmable logic device (CPLD) on the EVM and the design of the PC-user software.

First we will describe the overall functionality of the CPLD, which operates in combination with the THS8083 to enable the display of a digitized PC graphics or video signal on an LCD flat-panel display connected to the board. Then we will focus on the implementation of the communication protocol between the PC and the EVM that eliminates the need for a microcontroller and therefore is more generally applicable as a methodology for rapid hardware prototyping. We will illustrate some of the EVM and THS8083 features using the PC software graphical user interface (GUI); and, in particular, we will implement an algorithm for white-balance calibration.

CPLD design

While the THS8083 is a contained solution for the digitizing of a PC graphics or component video signal, it does not include the circuitry to generate the synchronization signals for the digital display. In this example, we use a Sharp XGA flat panel that accepts 6-bit R, G, and B data (using the 6 MSBs of each 8-bit bus) over a double-pixel interface bus. Additionally this requires Hsync, Vsync, and Data Enable signals. While the THS8083 does provide an output Hsync, we like to have the option of centering the image, a standard feature on any LCD or CRT computer monitor. This is accomplished by changing the timing of the sync signals with respect to the active video data by feeding both Hsync (from the THS8083 or from the input video signal) and Vsync (from the video input) to the CPLD, where they are used as references to, respectively, a horizontal (pixel) and vertical (line) counter. The horizontal counter is reset by each Hsync and increments with the sample (pixel) clock; the vertical counter is incremented by Hsync and reset by Vsync.

The EVM provides digital output from the ADC to the flat-panel display as well as analog output from a back-to-back connection of ADC and DAC to a computer CRT monitor. To provide image centering on both displays, the CPLD generates two sets of syncs that can be independently controlled. A third set of output sync signals from the CPLD is routed to the THS8083 for test purposes. When these signals are selected via board jumpers, it is possible to use them instead of an external video source for synchronizing the THS8083.

The user can program start and stop values for each set of sync signals (and the data_enable signals for the digital LCD output) in units of pixels (for the horizontal dimension) or lines (for the vertical dimension). Additionally, the polarity of the sync signals is programmable. The programmable logic generates these signals by comparing the programmed start/stop values with the current state of the pixel and line counters.

Note that the data output of the THS8083 is not routed through the CPLD, and therefore it is not possible to implement on-screen display (OSD), image data capture, or other video processing in the digital data path on this board.

The THS8134 DAC can be configured in different modes, depending on the desired color space (RGB vs. YPbPr) and sync insertion features. There are also dedicated inputs to this device to control the timing of the sync insertion. The programmability of these signals is register-controlled through the CPLD.

The CPLD itself is configured via an I^2C interface. The CPLD design contains a full I^2C slave implementation with writeable and readable configuration registers. Since it is only an I^2C slave, the CPLD can respond only to data transfer requests initiated by the host (PC).

Reference 1 fully details the CPLD design. The design was accomplished using schematic entry and, for some functional blocks, via a behavioral description in Altera® High Level Description Language (AHDL). The complete design was compiled with Max+Plus II® version 9.6 and was fitted into an Altera Flex10K30 device, occupying its manufacturer-stated 30K gate capacity for about 50%.

Serial communication interface

Since there is no need for real-time communication between any of the devices on this board outside the video data path, there is no need for a microcontroller in this design. The control communication is only for configuration and status reporting between the PC and EVM and therefore can be run at low speed. We chose to implement a standard I^2C* interface directly onto the PC parallel port.

The I^2C interface consists of bidirectional data (SDA) and clock (SCL) lines, which have been implemented with two terminals of the standard PC LPT1 port's 25-pin connector.

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*The I^2C (inter-IC) communication bus is an industry-standard control bus and specifies a 2-wire physical interface that is shared by I^2C-compatible devices. The bus protocol is widely used for consumer video ICs. See Reference 2 for specifications.

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Figure 1 shows the bidirectional communication. The I^2C bus is an open-collector type (to enable a wired-AND operation inherent to the bus specification) and requires the use of open-collector buffer inverters to transform the unidirectional LPT1 port communication into bidirectional communication on the EVM.

On the THS8083EVM, both the THS8083 and the CPLD are slave devices connected to the (SCL1,SDA1) bus. The second I^2C bus is unused on this EVM but was provided to control other boards from the same host PC (via an extension connector) in the future.

THS8083EVM PC software

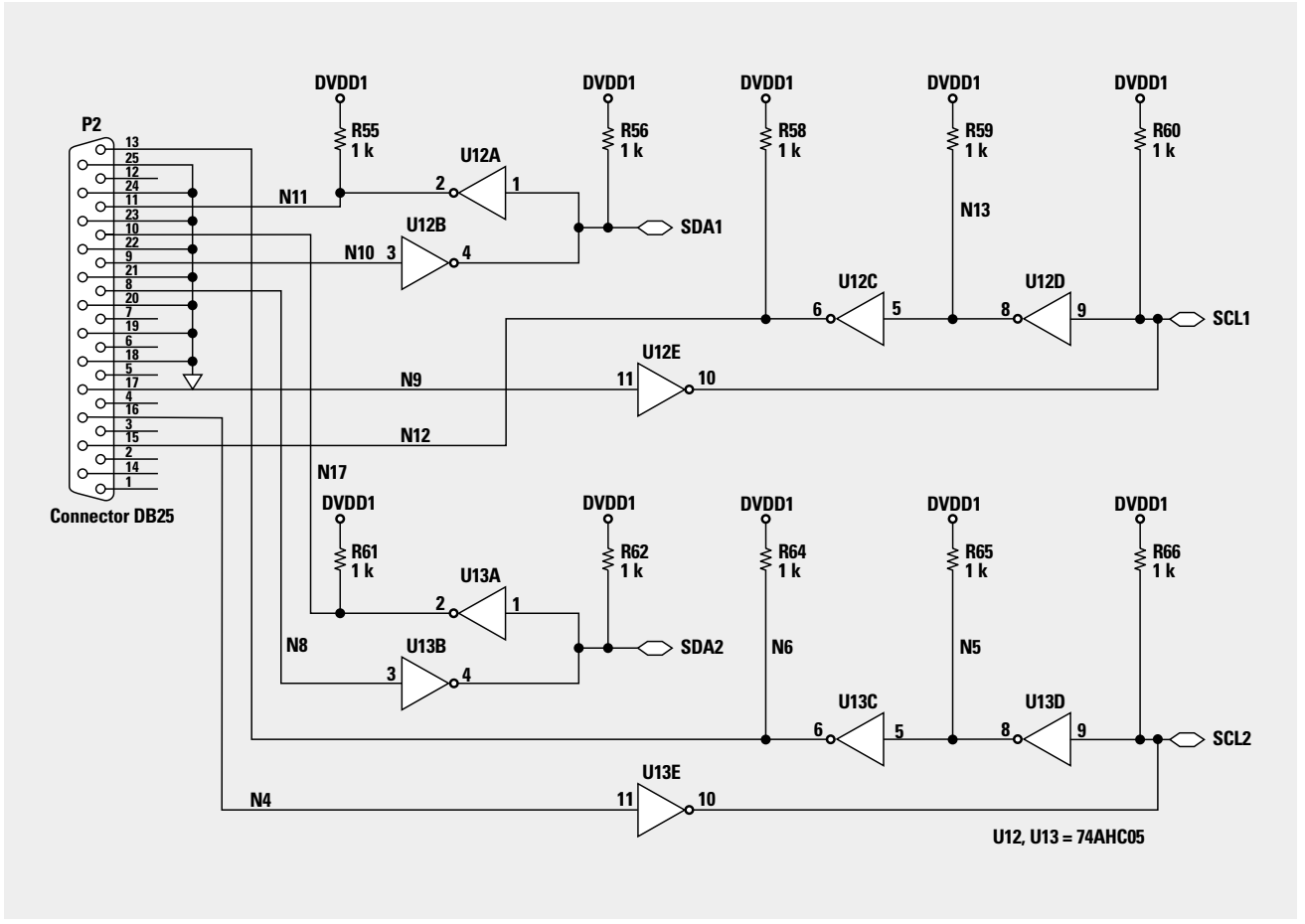
The PC software consists of a (shareware) parallel-port driver and the THS8083EVM graphical user interface (GUI).

Before the EVM can be used, the port driver needs to be installed. This will set up a Windows™ dynamic link library (DLL) that enables data I/O on LPT1 under both Windows 98 and Windows NT™ platforms. Once installed, this DLL is called transparently by the EVM's GUI.

As shown in Figure 2, the user interface is implemented as a property sheet, or tabbed dialog box, that groups logically related controls on the same page. For each video mode, a set of default settings can be selected via the "combo" box in the lower left of the main window. The user can change and re-save these defaults to disk for later use. Furthermore, each individual setting can be changed with the high-level controls on the different property pages. The I^2C register map of the THS8083 and/or the CPLD, as shown in Figure 2, immediately adapts to the new setting. Which device implements each software function is transparent to the user. The software keeps track of changes versus the previous device settings and will update only those registers that have been affected.

Additional control buttons are available for checking the I^2C status (a data pattern is written to and read from each I^2C device and compared for equality) or for the retrieval of settings currently loaded in the devices. Furthermore, using an automatic PC interrupt invoked by the GUI, the software automatically polls the I^2C bus every 3 seconds for status indicators such as the availability of an input video signal or lock of the PLL in the THS8083 to this

Figure 1. Implementing two independent I^2C buses on a standard PC parallel port



input signal. The main page also displays readouts from the THS8083 for the pixel clock frequency and the frequencies of HSync (line rate) and Vsync (frame rate). They are continuously updated through this polling function and thus can be used, e.g., for the detection of an input video format change.

Instead of programming the devices from this high level, an expert user can control each register setting on the Register Map page individually for both the CPLD (controller) and the THS8083 by changing individual register bytes in decimal or hexadecimal format, as shown in Figure 2.

Once a setting is changed, the Apply button becomes active. When it is pressed, the new settings are downloaded onto the EVM.**

White-balance calibration

Besides programming the device, the user software implements an offset and gain calibration algorithm for the R, G, and B channels to ensure white balance in the digital output. When the button at the top of the page in Figure 3 is pressed, the software will first create a full-screen almost-black (R=G=B=32) and afterwards a full-screen almost-white (R=G=B=240) image to establish two points of reference. The black image will be used to establish equal offset on all channels and to create an offset-correction factor expressed as a value in the 0 to 255 range (a value of 128 on all channels means no correction). Similarly, the white image will compensate for any gain error by means of a gain-correction factor. For this procedure to work, the same PC must be used both for controlling the EVM via its LPT1 port and for video input.

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Figure 2. THS8083EVM PC software Register Map page

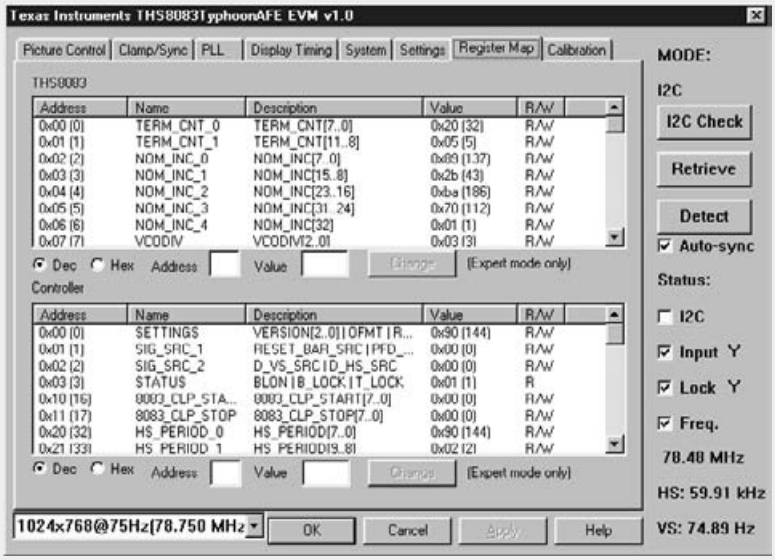
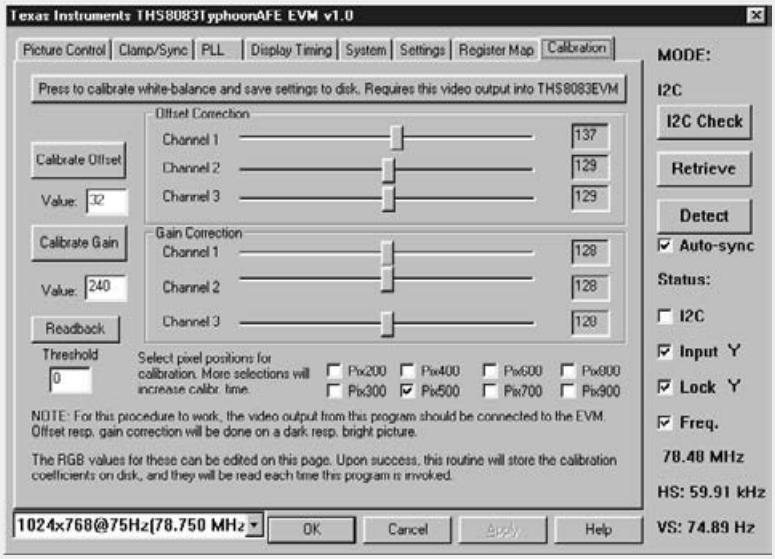


Figure 3. THS8083EVM PC software Calibration page



**Some selected settings, such as brightness/contrast control and the PLL phase setting, are updated as soon as they are changed in the software.

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Although the board does not have any provision for data capture as explained before, the THS8083 itself can read back the ADC output values on all three channels via dedicated I^2C registers. The user can program which horizontal location is used for readback. As shown in Figure 3, the default horizontal position for calibration is pixel 500 with respect to the Hsync, which will keep this position out of the horizontal blanking range for most video formats. More positions can be selected (pixel averages will be used) at the expense of a longer calibration time. Once calibration-correction factors are determined, they are taken into account automatically whenever the user changes brightness or contrast settings, so that white balance is preserved. The correction factors are also saved to disk and automatically loaded the next time the software is started, eliminating the need for re-calibration. More details, including the formula to determine corrected brightness/contrast settings, are given in Reference 1.

Conclusion

While this software control has been specifically designed for the THS8083EVM, its implementation of an I^2C interface from a standard PC parallel port is more widely applicable and can be of use for rapid prototyping in lab environments where there is no need for real-time host communication through a microcontroller. We have shown that a standard I^2C slave interface can be easily implemented in a CPLD, which opens up many possibilities for adding features to a prototype board via only software changes, by simply adding additional I^2C register map settings. For internal use, TI developed a derivative of this board—a board that routes the video data through a programmable device of larger density and pinout—and uses this to prototype image processing algorithms. We have also shown how one of the differentiated features of the THS8083—i.e., the ADC readback—can be used to implement a useful video algorithm.

References

1. THS8083EVM User Manual (furnished with THS8083 EVM kit).
2. "I^2C-bus specification (version 2.0)," Philips Semiconductors (December 1998).

Related Web sites

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