The SN65LVDS33/34 as an ECL-to-LVTTL converter

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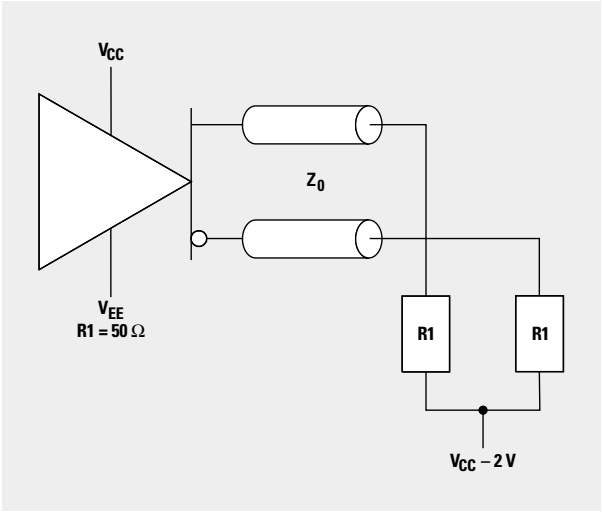
Introduction

Emitter-coupled logic (ECL) has often been the physical layer of choice for system designers to meet high-speed data transmission requirements. The fast edges (rise and fall times) of ECL have permitted higher speeds, but at the expense of increased PC board complexity, power consumption, and electromagnetic interference (EMI). Now, lower power and lower EMI technologies like LVDS provide designers with an alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to introduce LVDS receivers in ECL systems by implementing a resistor divider and capacitive coupling. These capacitors and resistors further add to the complexity and part count of a design. To alleviate the complexity of interfacing with ECL, TI has introduced the SN65LVDS33/34 receivers. This article describes a basic interface between an LVDS receiver and an ECL driver, and how the SN65LVDS33/34 receivers can be used to convert different types of ECL to LVTTL without a resistor divider or capacitive coupling. This article also demonstrates that, since no additional components are needed with wide common-mode receivers, these receivers can be used as a first step to replace an ECL physical layer with LVDS.

Figure 1. ECL characteristic load



PECL and LVPECL to standard LVDS

For ECL devices including negative ECL (NECL), positive ECL (PECL), and low-voltage, 3.3-V PECL (LVPECL), the load seen by the driver must be 50 Ω biased to 2 VDC below the device (driver's) V_{CC}. This characteristic load is depicted in Figure 1.

Often the bias voltage level for the characteristic load is not available and is attained through a Thevenin equivalent circuit (resistor divider). Figure 2 shows a Thevenin equivalent circuit intended to provide the characteristic load and the necessary voltage divider to translate the ECL output levels of node V_A and $\overline{V_A}$ to the LVDS level desired at node V_B and $\overline{V_B}$.

Equations 1–3 are used to calculate the resistor values in Figure 2.

$$50 = R1 \parallel (R2 + R3) \quad \textbf{(1)}$$

$$\frac{V_{CC} - 2 - V_{EE}}{V_{CC} - V_{EE}} = \frac{R2 + R3}{R1 + R2 + R3} \quad \textbf{(2)}$$

$$\text{Gain} = \frac{R3}{R2 + R3} \quad \textbf{(3)}$$

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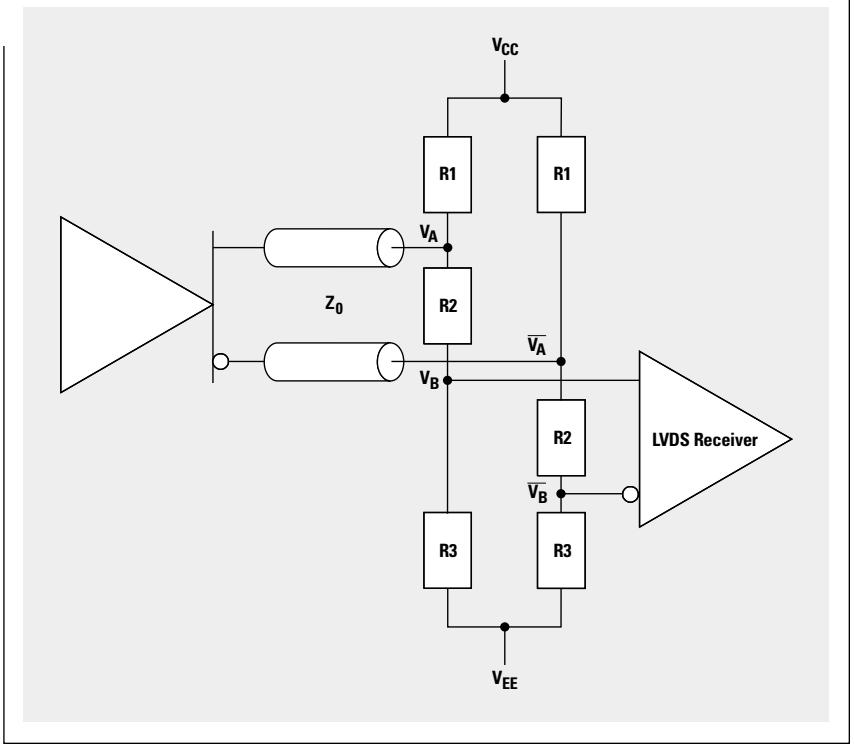
Figure 2. Differential ECL interface to standard LVDS equivalent circuit



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Equations 1 and 2 establish the necessary Thevenin equivalent termination and voltage as seen by the driver. The Thevenin equivalent termination is equal to the common-mode characteristic impedance of the transmission line, 50 Ω (100 Ω differential impedance). This equality satisfies Equation 4, the impedance matching of the load with the transmission line.

$$Z_0 = R1 \parallel (R2 + R3) \quad \textbf{(4)}$$

When Z_0 is not equal to 50 Ω, then Equations 1 and 4 are incompatible; and trade-offs need to be made with respect to driver flexibility and tolerance to reflections on the transmission line.

Equation 3 establishes the gain of the resistor network. The gain of the resistor network should provide the voltages within the valid input range of the receiver, given the range of the driver output. The minimum and maximum levels for the LVPECL, PECL, and NECL devices are given in Table 1.

Table 1. LVPECL, PECL, and NECL outputs

	LVPECL	PECL	ECL
V_{OH}max (V)	2.42	4.120	–0.880
V_{OH}min (V)	2.275	3.975	–1.025
V_{OL}max (V)	1.68	3.380	–1.620
V_{OL}min (V)	1.49	3.190	–1.810

The LVDS standard requires a differential voltage magnitude of 100 to 600 mV at the input to the receiver, and the valid input voltage range is 0 to 2.4 V. Table 2 shows the relationships between the gain and the varied input and output levels. The intent of Table 2 is to limit the gain selection to values that provide valid input voltage levels over the entire output range of the driver.

From Table 2 we find that the gain of LVPECL and PECL can be bound to the following values:

$$\text{LVPECL} \rightarrow 0.168 \leq \text{Gain} \leq 0.645$$

$$\text{PECL} \rightarrow 0.168 \leq \text{Gain} \leq 0.583$$

The gain is chosen to be 0.4 for both the LVPECL and PECL termination schemes. The resistor values are calculated in Table 3.

Table 2 shows that the NECL output levels are not compatible with standard LVDS, given the resistor network of Figure 2. Most LVDS receivers do not support the input range needed for a NECL interface and often require some type of capacitive coupling to adjust the common-mode voltage seen at the receiver inputs. The capacitors are usually placed on each of the differential lines before the termination network and before the receiver. Besides the obvious disadvantage of increased part count, capacitive coupling also introduces inter-symbol interference (ISI) when dealing with non-dc-balanced transmissions. An alternative to this coupling is the use of receivers that accept a wide range of common-mode inputs, eliminating ISI problems and minimizing the number of parts needed to interface various types of ECL to LVDS.

Table 2. Gain limits for standard LVDS interface

		OUTPUT DIFFERENTIAL		OUTPUT VALUE	
		min (V)	max (V)	min (V)	max (V)
LVPECL		2.275 – 1.68 = 0.595	2.42 – 1.49 = 0.93	1.49	2.42
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x 1.49 > 0.0	Gain x 2.42 < 2.4
PECL		3.975 – 3.38 = 0.595	4.12 – 3.19 = 0.93	3.19	4.12
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x 3.19 > 0.0	Gain x 4.12 < 2.4
ECL		(–1.025) – (–1.620) = 0.595	(–0.880) – (–1.810) = 0.93	–1.81	–0.880
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x –1.81 > 0.0	Gain x –0.88 < 2.4

Table 3. Standard resistor values and theoretical output voltages for LVDS translation

DRIVER	V_{CC} (V)	V_{EE} (V)	R1:R2:R3 (Ω)	V_A HIGH (V)	V_A LOW (V)	V_B HIGH (V)	V_B LOW (V)
LVPECL	3.3	GND	127: 49.9: 33.2	2.42	1.49	0.71	0.34
LVPECL	3.3	GND	127: 49.9: 33.2	2.28	1.68	0.64	0.40
LVPECL	3.3	GND	127: 49.9: 33.2	2.42	1.68	0.67	0.37
PECL	5.0	GND	82.5: 75: 50	4.12	3.19	1.65	1.27
PECL	5.0	GND	82.5: 75: 50	3.98	3.38	1.59	1.35
PECL	5.0	GND	82.5: 75: 50	4.12	3.38	1.65	1.35

Table 4. Gain limits for the SN65LVDS33/34 interface

		OUTPUT DIFFERENTIAL		OUTPUT VALUE	
		min (V)	max (V)	min (V)	max (V)
LVPECL		2.275 – 1.68 = 0.595	2.42 – 1.49 = 0.93	1.49	2.42
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x 1.49 > –4.0	Gain x 2.42 < 5.0
PECL		3.975 – 3.38 = 0.595	4.12 – 3.19 = 0.93	3.19	4.12
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x 3.19 > –4.0	Gain x 4.12 < 5.0
ECL		(–1.025) – (–1.620) = 0.595	(–0.880) – (–1.810) = 0.93	–1.81	–0.88
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x –1.81 > –4.0	Gain x –0.88 < 5.0

ECL to the SN65LVDS33/34

The SN65LVDS33/34 dual/quad receiver provides a wide common-mode capability and a maximum differential input voltage magnitude, both of which exceed the EIA-644 standard. The valid input range is increased to –4 to +5 V; and the differential inputs can vary from 100 mV to 3 V. These extended ranges provide wider bounds for the gain in Equation 3.

From Table 4 we see that the LVPECL-, PECL-, and ECL-to-SN65LVDS33/34 gain can be limited to the following values:

$$\text{LVPECL} \rightarrow 0.168 \le \text{Gain} \le 2.07$$

$$\text{PECL} \rightarrow 0.168 \le \text{Gain} \le 1.21$$

$$\text{ECL} \rightarrow 0.168 \le \text{Gain} \le 2.21$$

The SN65LVDS33/34 bounds for LVPECL, PECL, and NECL gain all include unit gain (Gain = 1). Choosing a unity gain value eliminates the need for the R2 resistors shown in Figure 2 and simplifies the circuit to the one shown in Figure 3.

The elimination of the R2 resistors also reduces the complexity of the equations used to calculate the resistor values in Figure 3.

$$50 = (R1 \parallel R3) \quad \textbf{(5)}$$

$$\frac{V_{CC} - 2 - V_{EE}}{V_{CC} - V_{EE}} = \frac{R3}{R1 + R3} \quad \textbf{(6)}$$

Equations 5 and 6 establish the necessary Thevenin equivalent termination and voltage as seen by the driver, and the third equation to establish gain is no longer needed. The calculated resistor values are shown in Table 5.

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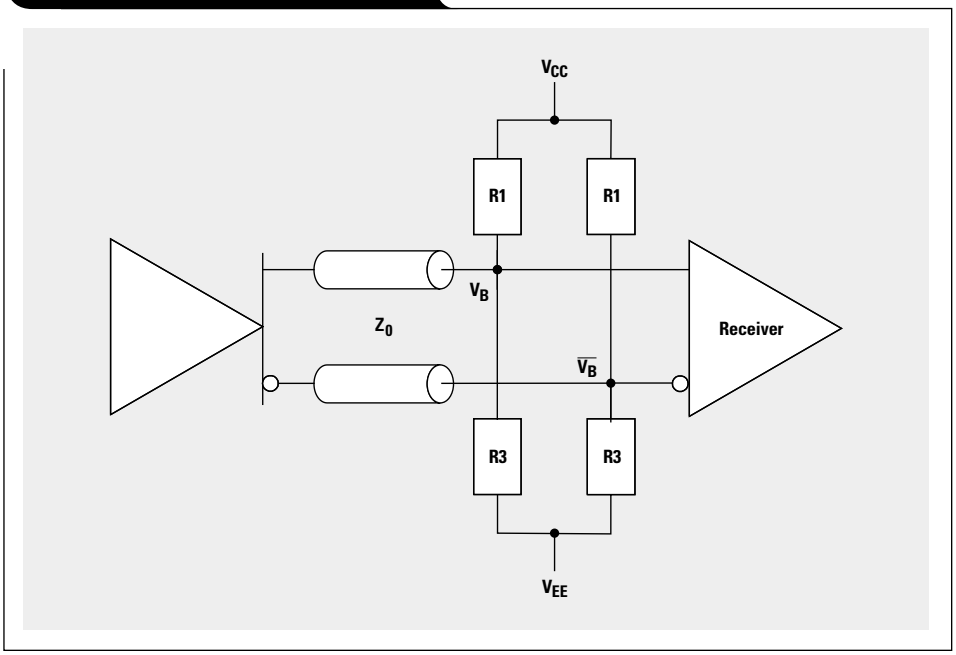
Table 5. Standard resistor values for PECL- and LVPECL-to-SN65LVDS33/34 translation

DRIVER	V_{CC} (V)	V_{EE} (V)	R1:R2 (Ω)
LVPECL	3.3	GND	126.9: 82.5
PECL	5.0	GND	83.3: 125.1
ECL	GND	–5.0	83.3: 125.1

Figure 3. ECL to SN65LVDS33/34



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The eye patterns of the SN65LVDS33/34 output with the LVPECL and NECL drivers are shown in Figures 4 and 5, respectively.

ECL receipt at a distance

Up to this point, for receiving ECL signals, the assumptions have been that the voltage supplies used by the driver are available for the termination network and that the only common-mode voltage is the ECL offset voltages. Another consideration is that the receiver is in a remote location and/or only the 3.3-V supply for the LVDS receiver is available.

A remote receiver creates two problems for the resistor networks previously discussed. First, the voltages are simply not available; only the 3.3 V required by the LVDS receiver is available. Second, in the case of LVPECL, where the V_{CC} is the same for both the driver and receiver, potential differences between grounds becomes a factor. With a ground potential difference between the receiver

Figure 4. LVPECL to SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

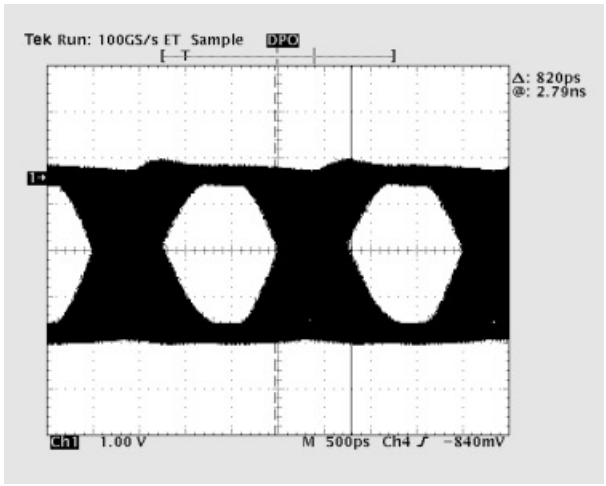


Figure 5. NECL to SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

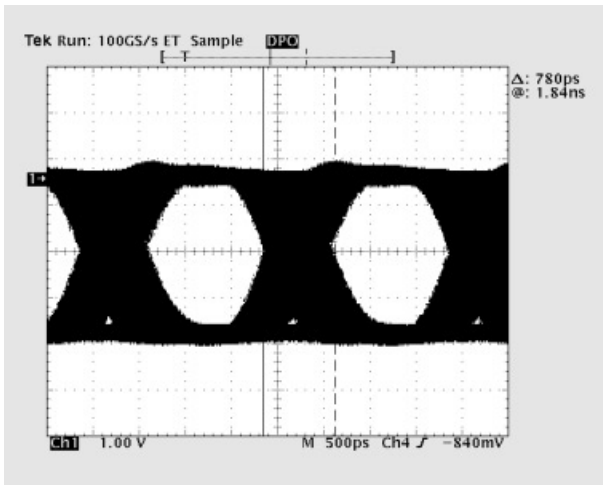


Figure 6. LVPECL and PECL to remote SN65LVDS33/34

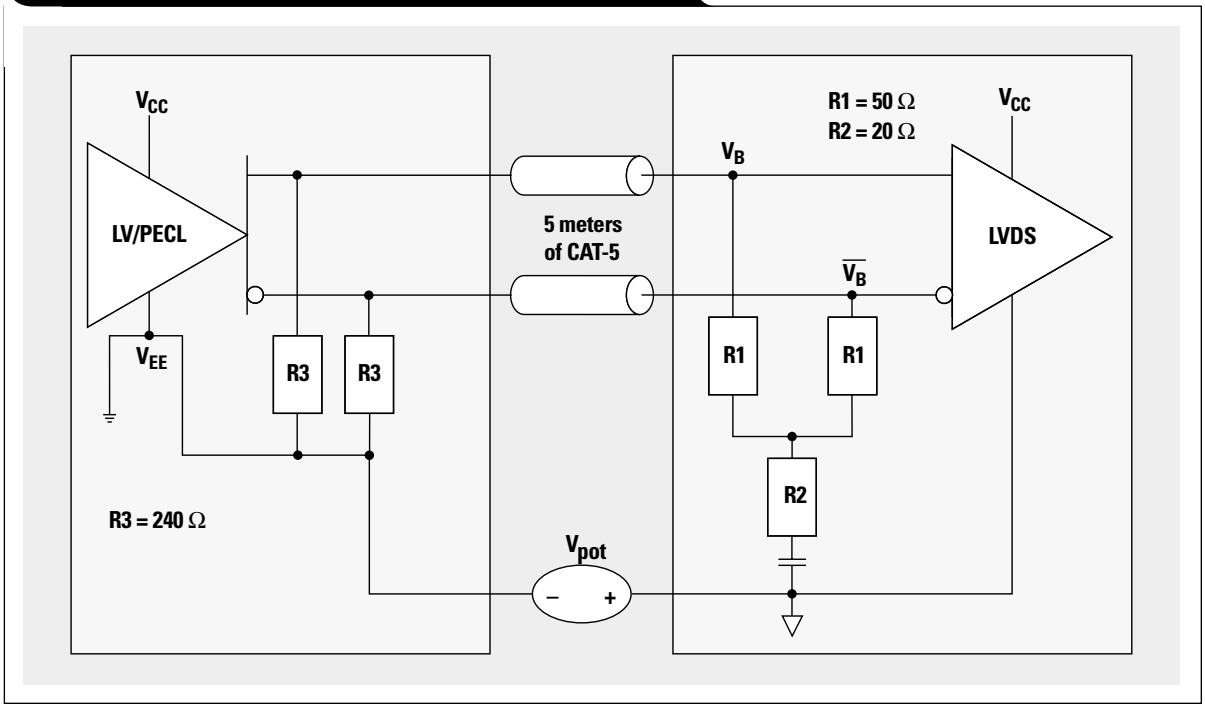
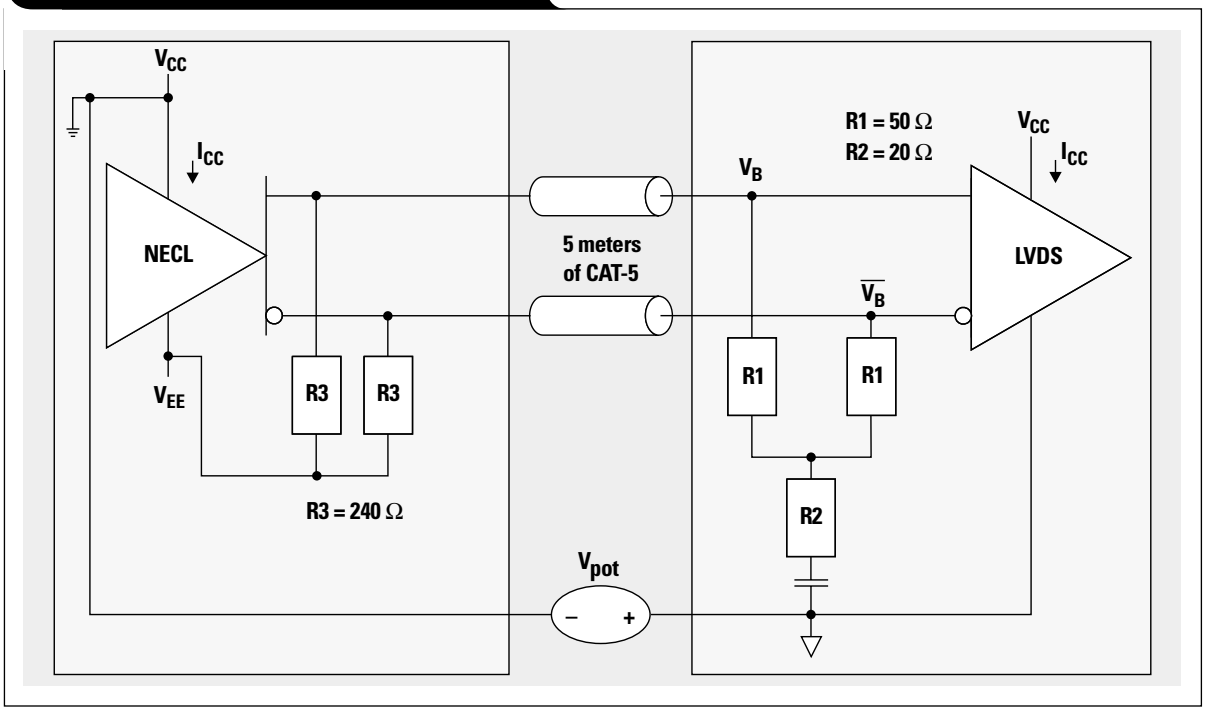


Figure 7. NECL to remote SN65LVDS33/34



and driver, the characteristic load voltage seen by the driver will not be the required $V_{CC} - 2$. The solution to the unavailability of voltages is ac termination. The ground noise problem is alleviated by the wide common-mode capabilities of the SN65LVDS33/34. Figures 6 and 7 depict the use of the SN65LVDS33/34 when the driver and receiver have different ground potentials and are separated by about 5 meters of CAT-5 cable. The eye pattern is shown in Figure 8. Table 6 shows that the SN65LVDS33/34 can tolerate a ground noise magnitude of 2.6 V for LVPECL, 1.1 V for PECL, and 2.3 V for NECL.

As mentioned earlier, the SN65LVDS33/34 receiver exceeds the EIA-644 requirement, and a resistor divider is not needed. With no resistor divider, R1 simply needs to match the characteristic transmission line impedance of 50 Ω. The value of R3 was chosen to provide a resistor path to ground for the ECL driver. When the designer uses a pre-existing source termination, the important parameter is the output voltages. If the voltage levels exceed the inputs of the receiver, then a resistor divider is required at the receiver. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

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Figure 8. NECL to remote SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

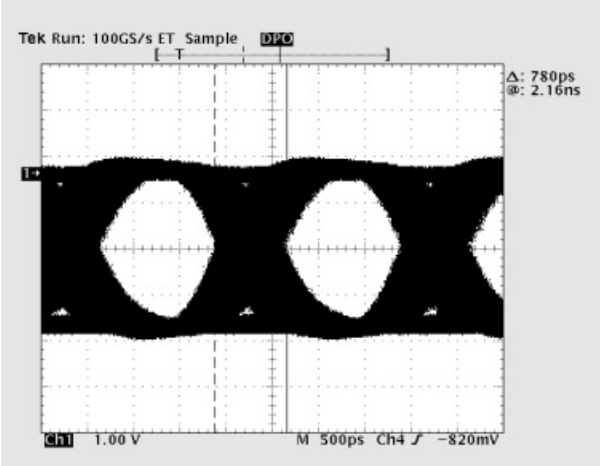

Table 6. LVDS inputs with respect to receiver ground

DEVICE DRIVER	DRIVER TO RECEIVER GROUND POTENTIAL (V_{pot})	V_B HIGH (V)	V_B LOW (V)
LVPECL	–2.64	5.0	4.24
LVPECL	0	2.36	1.60
LVPECL	5.60	–3.24	–4.00
PECL	–1.12	5.0	4.50
PECL	0	3.88	3.38
PECL	7.38	–3.50	–4.00
NECL	–5.87	5.0	4.17
NECL	0.0	–0.87	–1.70
NECL	2.30	–3.17	–4.00

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Conclusion

The SN65LVDS33/34 has the versatility and capability to be interchanged with ECL receivers without any component addition (beyond the bias resistor networks used in standard ECL transmission). In Figure 9, where the output structure of the optical device is PECL, the SN65LVDS33/34 can be installed just as easily as a PECL receiver. Also, the termination structures in Figure 9 provide equivalent differential impedances of 100 Ω, the recommended value for LVDS terminations. In the future, if the output structure of the optical device is changed from PECL to LVDS, then the circuit could be re-used as shown in Figure 10. (The connections between R1 and V_{CC} and the connections between R2 and GND would be removed, as shown in Figure 10.)

The idea of interfacing ECL to LVDS logic levels has been widely publicized, but the advantages of replacing ECL with LVDS are often not considered: +3.3-V operation, noise immunity, and low power consumption (which results in low EMI). Designers can now take into consideration the benefits of LVDS when upgrading legacy ECL systems, which no longer require the exclusive use of ECL receivers.

Figure 9. PECL-to-SN64LVDS33/34 application

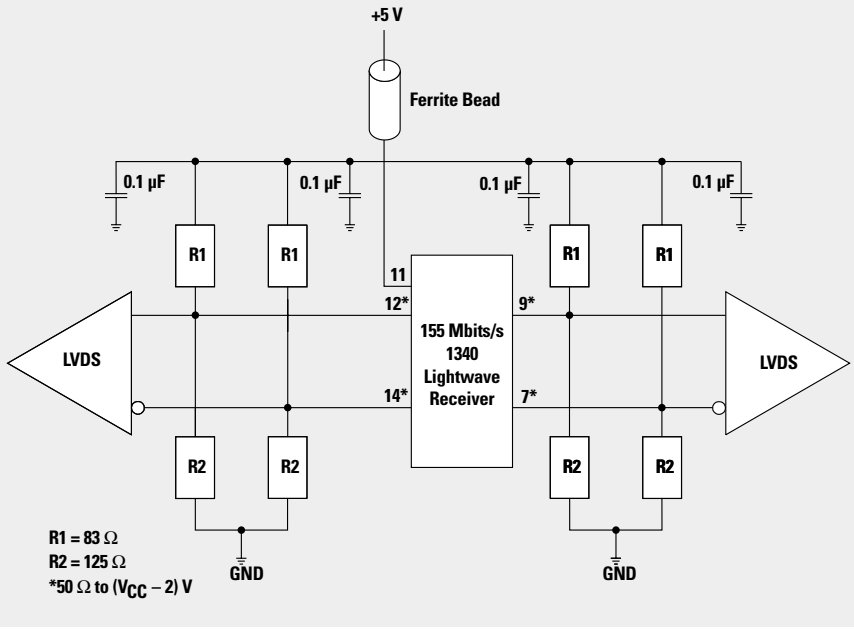

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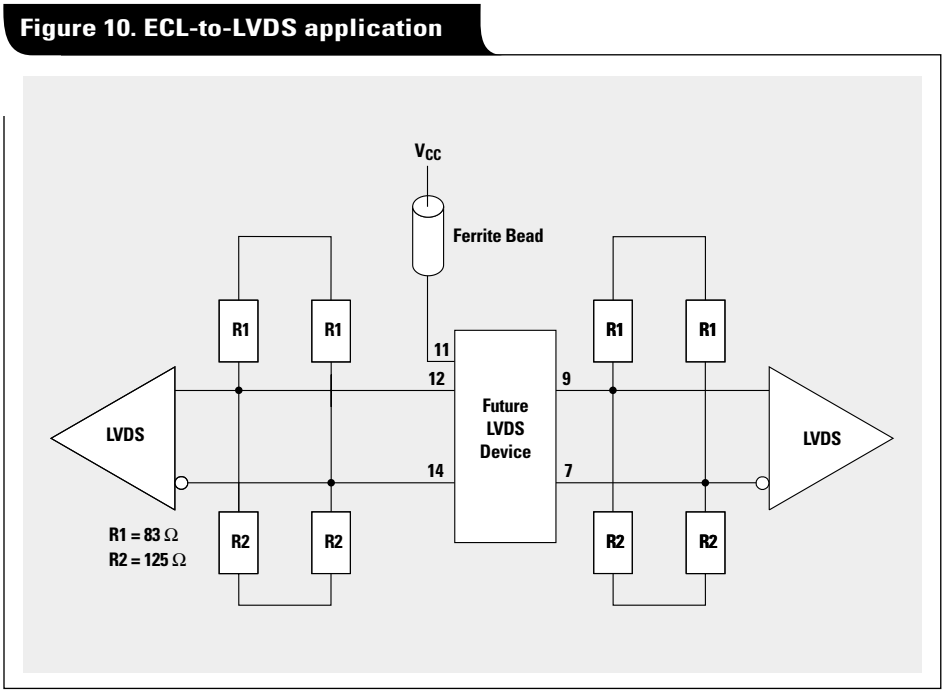
Figure 10. ECL-to-LVDS application



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