

# A/D and D/A conversion of PC graphics and component video signals, Part 1: Hardware

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## Introduction

This first part of a two-part article describes a design for the digitizing of component video signals, either sourced from a PC (PC graphics) or from a consumer video device (DVD, set-top box) that provides a component video output. First the characteristics of these signals are explained. Then we introduce the hardware of the THS8083 evaluation module (EVM) and a reference design for both A/D and D/A conversion. Finally, we explore some typical analog issues that affect the hardware, such as color spaces, video clamping, and its dependence on the color space used. We show an analog color space conversion circuit as a practical design example.

In the next issue of Analog Applications Journal, we will examine the functionality of the programmable logic device (PLD) on this board, the functionality of the PC configuration software, and its communication protocol with the board.

## Video signal characteristics

There are two possibilities for analog video representation: composite vs. component video. In composite video, as shown in Figure 1, the color information is phase modulated onto a subcarrier such that the complete color spectrum is represented by a 360-degree phase shift. The luminance of the video signal is amplitude-modulated, while the color information is added by phase modulation of a subcarrier.

This is the classical representation of NTSC/PAL or SECAM standard-definition TV. This video representation will not be discussed further here. PC graphics and high-definition TV (HDTV), on the other hand, use a component video format: the amplitude of three color component signals represents the relative intensities of three primary colors (Red/Green/Blue). This will be described later in this article.

A second characteristic of video signals is the way their timing is transferred—either as dedicated timing signals, signaling horizontal (Hsync) and vertical (Vsync) synchronization, or embedded within at least one of the color components. In the latter case, the sync information is composite; i.e., it contains both horizontal and vertical sync information. In order to synchronize the receiver, sync extraction is required of the composite sync from the color component (typically the Green or luminance

Figure 1. Composite video waveform

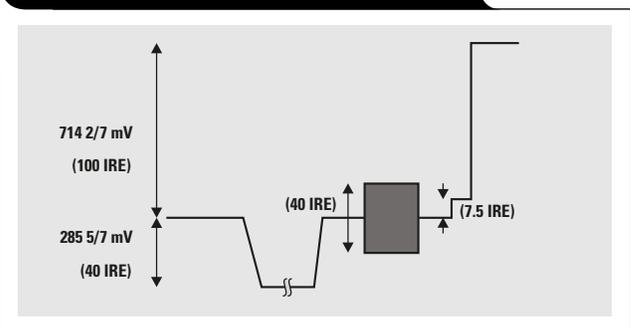
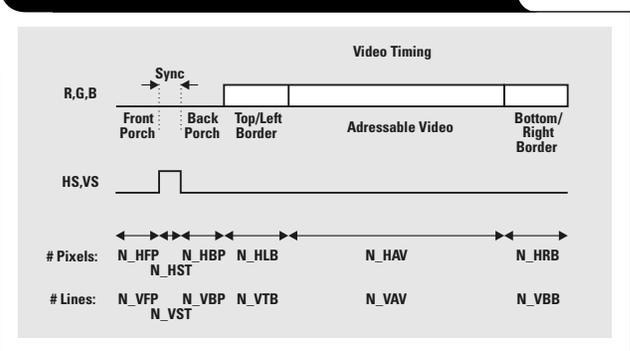


Figure 2. PC graphics timing definitions



channel) that embeds it. Subsequently this composite sync is separated into Hsync and Vsync.

Dedicated timing is used in PC graphics environments, while embedded composite sync is generally used for analog component video, including the analog representation of an HDTV signal.

Furthermore, in the case of PC graphics, Hsync and Vsync can differ in polarity. Figure 2 shows the nomenclature for defining typical timings for PC graphics signals. Each horizontal line is composed of FP, ST, BP, LB, AV, and RB, which denote, respectively: front porch (of sync), sync tip, back porch (of sync), left border, active video, and right border. Replace “left” and “right” with “top” and “bottom” for the vertical timing definitions. Tables 1 and 2

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Table 1. Frame rate/line rate/pixel clock, sync polarities and horizontal parameters for XGA (1024 x 768) PC graphics formats

RESOLUTION	F <sub>vert</sub> (Hz)	F <sub>hor</sub> (kHz)	F <sub>pixel</sub> (MHz)	HS POLARITY	VS POLARITY	H_FP (pixels)	H_ST (pixels)	H_BP (pixels)	H_AV (pixels)	H_TOT (pixels)
1024 x 768	60.004	48.363	65.000	neg	neg	24	136	160	1024	1344
1024 x 768	70.069	56.476	75.000	neg	neg	24	136	144	1024	1328
1024 x 768	75.029	60.023	78.750	pos	pos	16	96	176	1024	1312
1024 x 768	84.997	68.677	94.500	pos	pos	48	96	208	1024	1376

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**Table 2. Vertical parameters of XGA (1024 x 768) PC graphics formats**

RESOLUTION	V_FP (lines)	V_ST (lines)	V_BP (lines)	V_AV (lines)	V_TOT (lines)
1024 x 768	3	6	29	768	806
1024 x 768	3	6	29	768	806
1024 x 768	1	3	28	768	800
1024 x 768	1	3	36	768	808

define these parameters for the popular XGA (1024 x 768) PC formats (the border parameters are all 0 and therefore not listed). We can see that, depending on the vertical rate (frame rate, refresh rate), the total number of pixels per line (H\_TOT) or total number of lines per frame (V\_TOT) can be different and also that the sync polarities are different. Fvert, Fhor, and Fpixel show the vertical (frame) rate, horizontal (line) rate, and pixel clock of the video format.

**THS8083EVM features**

**Video input**

- Analog PC-type input from standard VGA connector or 5 BNC-type connectors (R or Pr, G or Y, B or Pb, Hsync, Vsync).

**Video output**

- Analog PC-type output to standard VGA connector or to 5 RCA-type connectors (R or Pr, G or Y, B or Pb, Hsync, Vsync).
- Video output carries separate sync signals (HS, VS) and Data Enable outputs, programmable in position, width, and polarity.
- Digital 3-V TTL/CMOS output to a flat-panel XGA-resolution display.
- Digital LVDS (Flatlink™) output to a flat-panel XGA- or SXGA-resolution display (not currently stuffed on board).

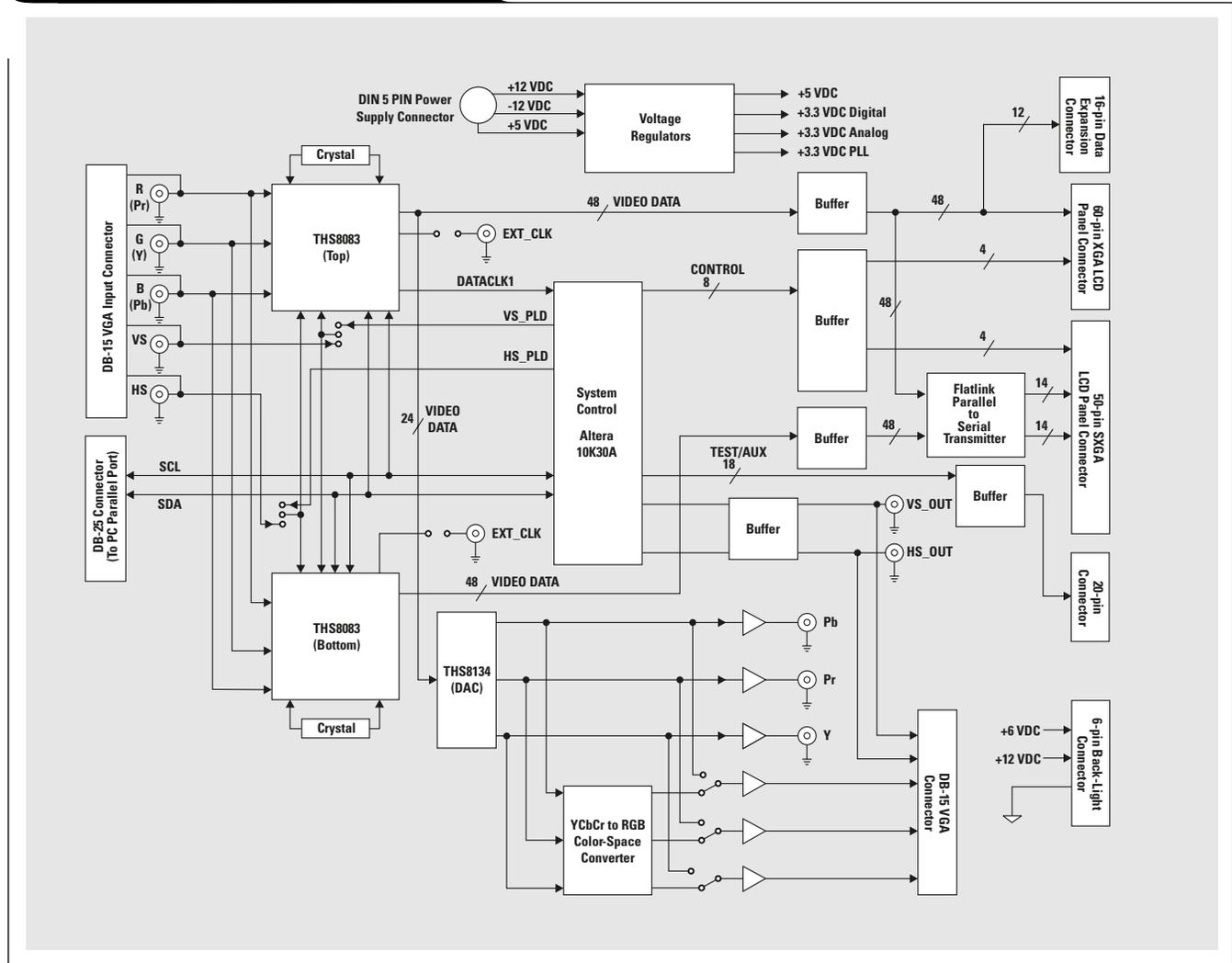
**Control**

- I<sup>2</sup>C control via interface to standard PC parallel port for configuration and control.

**Video processing**

- A/D of PC graphics and component video input. All image formats up to 4096 pixels/line are supported.
- Programmable digital timing generation to flat-panel display for image centering of the active video window.
- D/A conversion of digitized input video image for monitoring image quality on a regular display accepting analog signals.
- Optional YCbCr to RGB color space conversion on the analog output.

**Figure 3. THS88083EVM block diagram**



## THS8083EVM—a reference platform for component video and PC graphics A/D and D/A conversion

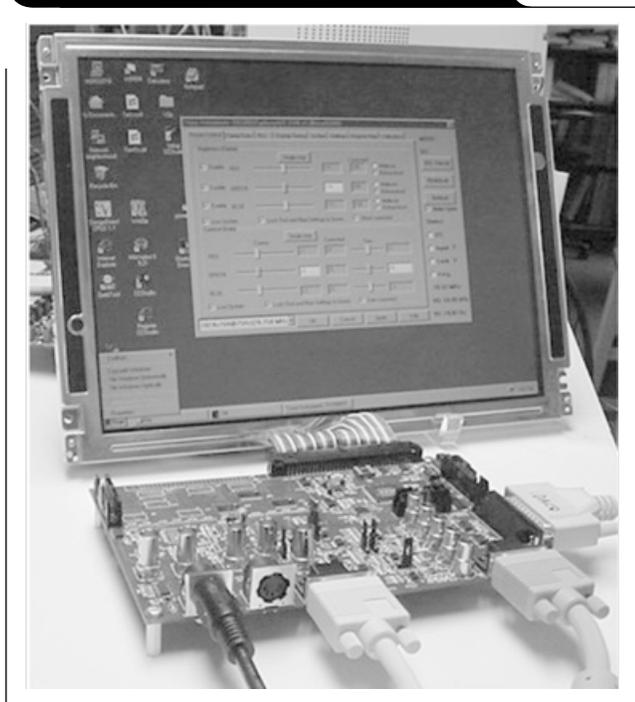
Figure 3 shows the block diagram of an evaluation module built around the THS8083, a triple 8-bit, 95-MSPS ADC for digitizing PC graphics or component video, and THS8134, a triple 8-bit video DAC.

The block diagram shows two ADCs, designated “Top” and “Bottom,” for a “ping-pong” approach in which each ADC takes up the digitization at half the pixel clock, essentially boosting supported input format pixel clocks to 2x the maximum speed of the ADC. While the EVM board is provided for this, currently only a single ADC is stuffed. The output data of the THS8083 is fed via damping series resistors to limit switching noise of the digital output drivers from coupling back into the analog input, which would otherwise cause reflections on the display. Buffers feed the digital output connector from the top part. The video data is also sent to the serializing LVDS transmitter that feeds a second digital output; therefore, this board can be hooked up to LCD panels accepting parallel data as well as panels accepting LVDS serial data (there is no single standard for LCD panel interfaces in practice\*).

An LCD panel also typically requires Hsync, Vsync, and Data Enable signals. Data Enable frames the active video window of the complete frame; i.e., only the viewed portion of the video frame is actually driven (unlike CRT tubes, there is no blanking time on LCD panels). These control signals are generated in the complex programmable logic device (CPLD) on the board. This design will be described in more detail later in this article.

\*The current EVM version available from TI is populated for XGA/HDTV resolution only, without LVDS output.

Figure 4. THS8083EVM with LCD panel



The data of the top ADC also feeds the THS8134 DAC. Note that 48 signal lines are provided from each ADC, since each ADC has three double-pixel-width buses (3 channels x 8 bits x 2). The DAC has only 3 x 8 input signals. For the DAC to work, the 24-bit output needs to be selected.

The DAC's output is either fed directly to the VGA output connector, in case the RGB input was converted, or sent through an analog color space conversion circuit. This circuit implements a conversion from the YPbPr to the RGB domain, and its design is discussed in more detail in the next paragraph. The intended use is for applications in which YPbPr analog video (as available from, for example, a DVD player or set-top box with component output), is sent to the board and an RGB output is desired.

While not shown in Figure 3, the THS8083 has built-in functionality for separating the embedded composite sync from the Y channel. Note that the ADC only extracts the sync. In video terminology, it “slices” the Y channel at a level below blanking to extract the sync; it does not separate the composite sync into Hsync and Vsync components. Since the extracted sync can be fed through the CPLD, and the CPLD can be used as a source for the Hsync/Vsync to THS8083, it is in principle possible to design this function into the CPLD. However, the current firmware does not implement this. Figure 4 shows a picture of this EVM hooked up to a flat-panel display.

### Video clamping and color space conversion

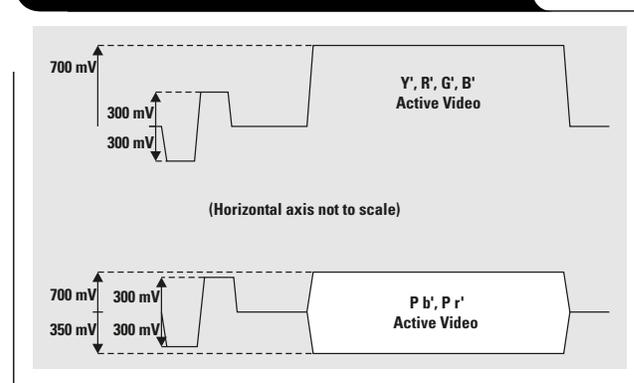
Video clamping and color space conversion are two video processing functions implemented on the analog video input by the THS8083EVM.

Clamping refers to a dc restoration of an ac-coupled signal. The circuit receiving the ac-coupled signal provides a dc bias to the signal in such a way that, during a period in which the amplitude of the signal is known, its dc level is fixed. In the case of video signals, the amplitude is known during the blanking period. Figure 5 shows the position of the blanking level during the back porch of the horizontal sync in the case of the R'G'B'Y' signals\*\* and in the case of the color difference signals Pb'Pr'. Since by definition the color differences can go higher or lower than the blanking level, a circuit that is designed to receive both color spaces (R'G'B' vs. Y'Pb'Pr') needs to have a configurable blanking level on at least two channels. THS8083 has an

\*\*The ' (prime) notation indicates that these signals are gamma-corrected.

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Figure 5. HDTV waveform (active video)



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internal clamping circuit for either bottom-level (R'G'B'Y') or mid-level (Pb'Pr') clamping, selectable via an I<sup>2</sup>C register. Therefore, on the THS8083EVM, R'G'B' or Y'Pb'Pr'-type input component video signals can be fed directly to the device's input channels by using coupling capacitors with no additional processing.

How do we convert between both color spaces? We will look at the case converting Y'Pb'Pr' HDTV signals to an R'G'B' format suitable for display on an LCD panel or CRT display.

The matrix to convert from Y'Pb'Pr' to R'G'B' is:

$$E'_R = E'_Y + 1.575 E'_{Pr}, \tag{1}$$

$$E'_G = E'_Y - 0.468 E'_{Pr} - .187 E'_{Pb}, \text{ and} \tag{2}$$

$$E'_B = E'_Y + 1.856 E'_{Pb}, \tag{3}$$

where E' denotes a gamma-corrected normalized intensity level between 0 and 1.

Using the following notes, the user can verify that the circuit implements this conversion.

**Red channel**

In Figure 6,  $X = Pr(1 + R2/R1)$ , and  $[(R - X)/R3] + [(R - 2Y)/R3] = 0$ . Therefore,  $R = Y + Pr/2(1 + R2/R1)$ . From comparison to Equation 1, we need  $R2/R1 = 2.15$ . If we let  $R2 = 1300$ ,  $R3 = 499$ , and  $R4 = 649$ , then  $R1 = 604$ .

**Blue channel**

Use the same circuit to arrive at  $B = Y + Pb/2(1 + R2/R1)$ . From comparison to Equation 3, we need  $R2/R1 = 2.71$ . If we let  $R2 = 1300$ ,  $R3 = 499$ , and  $R4 = 649$ , then  $R1 = 475$ .

**Green channel**

We derive Thevenin equivalents for both circuits in Figure 7, as shown. The top equivalent is straightforward. The bottom equivalent becomes

$$W2 = R9/(R8 + R9)W1 = -(R7 R9)/(R6(R8 + R9))Pb.$$

$$Z = (R8 \parallel R9) + R5. \text{ If we let } R3 \text{ and } Z = 1000, \text{ then } (G - W2)/1000 + [G + (R2/R1)Pr]/1000 + (G - 2Y)/499 = 0.$$

$$\text{Therefore, } G = Y - R2/(4R1)Pr - \{(R7 R9)/[4 R6(R8 + R9)]\}Pb.$$

By comparison to Equation 2, we have the equalities  $-0.468 = -R2/(4R1)$ ;  $-0.187 = -R7 R9/[4 R6(R8 + R9)]$ ; and  $Z = [(R8 R9)/(R8 + R9)] + R5 = 1000$  as previously assigned. Therefore, if we let  $R8 = 768$  and  $R9 = 1430$ , then  $R5 = 499$ . If  $R1 = 499$ , then  $R2 = 931$ ; and if  $R6 = 931$ , then  $R7 = 1430$ .

**Conclusion**

This article introduced a generic hardware platform for digitizing PC graphics and component video built around THS8083 and THS8134. It also described the hardware of the EVM and gave a design example of a color space conversion circuit implemented in the analog domain (obviously, the 3 x 3 matrixing could also be implemented in the digital domain prior to D/A conversion).

In the next issue of Analog Applications Journal, we will discuss the CPLD design, the communication protocol and PC software, and the software implementation of a white-balance control mechanism for accurate channel-to-channel gain and offset matching.

Figure 6. Color space conversion (red and blue)

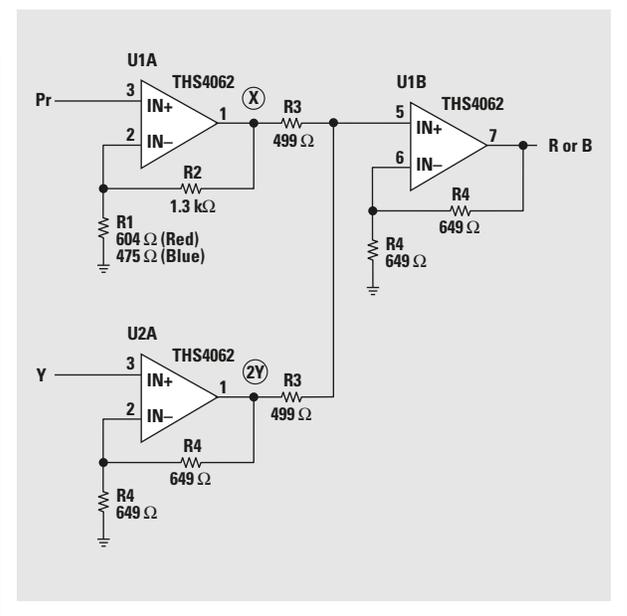
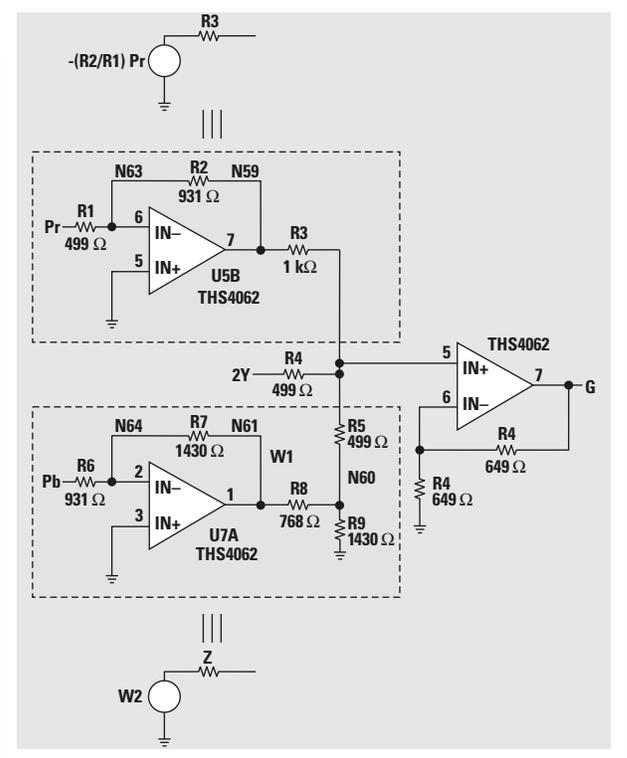


Figure 7. Color space conversion (green)



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