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This article describes a simple way to interface the ADS8341/3/4 (as well as the 12-bit counterparts ADS7841/4) to any TI DSP with at least one McBSP port. The simple interface uses the frame sync transmit (FSx) pin to initiate a conversion cycle. The ADC's BUSY pin can then be used as the source of the frame sync return (FSr) to simplify the transfer of conversion data to the DSP. This simple method of interfacing the ADS784x and ADS834x families of ADCs eliminates cumbersome data manipulation and provides an efficient method of connecting the device to the TMS320C5000™ and TMS320C6000™ DSP platforms with minimal software overhead.

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Miniature DC/DC converters with galvanic isolation offer very low output noise and high accuracy. This article covers a variety of off-the-shelf device configurations that use highly integrated packages and are suitable for a wide range of applications in space-constrained board designs. When compared to discrete designs, miniature DC/DC converters offer lower risk, much faster time to market, and development-cost savings.

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This article describes TI's improved board-mounted power module that is produced as a double-sided surface-mount (DSSMT) subassembly. This attachment method, designed to be more reliable than other surface-mount interconnects, translates into improved manufacturability for customers that employ high-volume, surface-mount production methods.

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The task of selecting the right op amp for an application can sometimes be time-consuming because, in addition to the wide variety of general-purpose op amps available, there are many specialty amps. This article provides an overview of several op amp configurations with performance trade-offs for current feedback versus voltage feedback and single-ended versus differential. Also included are circuit applications with considerations for frequency compensation and gain variations.

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Using resistive touch screens for human/machine interface

By Rick Downs (Email: downs_rick@ti.com)
Applications Engineering Manager, Data Acquisition Products

Introduction

Touch-screen interfaces are effective in many information appliances, in personal digital assistants (PDAs), and as generic pointing devices for instrumentation and control applications. Getting the information from a touch screen into a microprocessor can be challenging. This article introduces the basics of how resistive touch screens work and how to best convert these analog inputs into usable digital data. Issues such as settling time, noise filtering, and speed trade-offs are addressed.

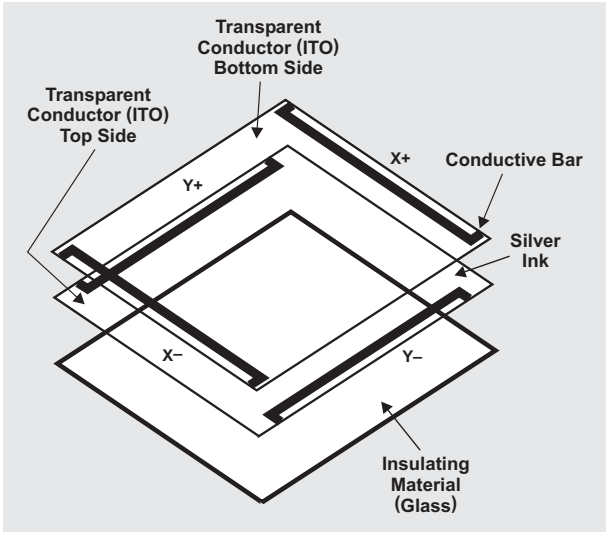
Resistive touch screens

Resistive touch screens consist of a glass or acrylic panel that is coated with electrically conductive and resistive layers made with indium tin oxide (ITO) (see Figure 1). The thin layers are separated by invisible spacers.

Resistive screens are generally the most affordable type of touch screen, which explains their success in high-use applications like PDAs and Internet appliances. Although clarity is not as good as with other touch-screen types, resistive screens are very durable. The only concern is that the resistive layers can be damaged by a very sharp object.

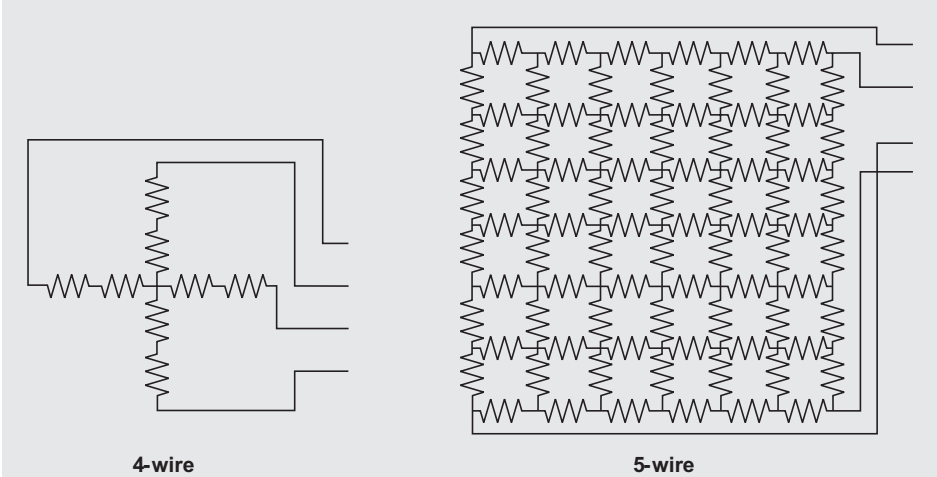
The two most popular resistive architectures use 4-wire or 5-wire configurations, as shown in Figure 2 (the 5-wire configuration uses the second layer as a wiper contact, not shown here). The circuits determine location in two coordinate-pair dimensions, although a third dimension can be added for measuring pressure in 4-wire configurations.

Figure 1. Resistive touch screen



Texas Instruments (TI) offers specialized analog-to-digital converters (ADCs) for interfacing to these two popular resistive touch screens. Since the majority of applications use 4-wire touch screens, the rest of this article concentrates on this architecture, although the same advice applies to the 5-wire screens and the ADS7845, TI's 5-wire touch-screen controller.

Figure 2. Touch-screen circuit configurations



Resistive touch-screen controllers

When a position is measured on a 4-wire touch screen, voltage is applied across the screen in the Y direction; and a touch presses the layers together, where a voltage can be read from one of the X electrodes. The contact made as a result of the touch creates a voltage divider at that point, so the Y coordinate can be determined; the process then repeats with the X direction being driven, and a reading is taken from one of the Y electrodes.

A touch-screen controller is simply an ADC that has built-in switches to control which electrodes are driven and which electrodes are used as the input to the ADC. The ADC can often be operated with different reference modes: single-ended or differential.

Single-ended configuration

In a single-ended configuration, the ADC reference is supplied between a reference input (V_{REF}) and ground. Very often, V_{REF} is actually the power supply voltage.

The ADC output is then a ratio of the input signal to the V_{REF} voltage. Since the touch screen is a voltage divider, this may seem sensible. However, there are several possible errors that may show up due to the driver switches, such as gain and offset errors from temperature, voltage drops in the switches, etc.

If the reference voltage is not the power supply, then power-supply variations could cause errors, since the power supply is the voltage placed across the screen; and, while it varies, the reference voltage will not.

Variations in touch-screen impedance can also cause gain or offset errors.

Differential configuration

In the differential configuration, the ADC's voltage reference is taken directly across the touch screen, eliminating driver variations, power-supply changes, and even changes in the touch-screen impedance. The output of the ADC is still the ratio of the input to V_{REF}. V_{REF} is now the voltage across the screen, and the output is a true reflection of the position of the touch on the screen.

Using a differential or ratiometric measurement technique like this provides much more accurate results, particularly in systems with noisy power supplies or where the touch screen is located a significant distance away from the controller.

Touch-screen settling time

When the touch panel is pressed or touched, there are two mechanisms that will affect the voltage level at the contact point. These two mechanisms will cause the voltage across the touch panel to "ring" and then to settle (decay) down slowly to a stable dc value.

The two mechanisms are:

1. Mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed.
2. The charging of the parasitic capacitance between the top and bottom layer sheets of the touch panel and at the input of the ADC that occurs when the drivers turn on, and inductive effects from the leads connecting the panel to the drivers in the controller.

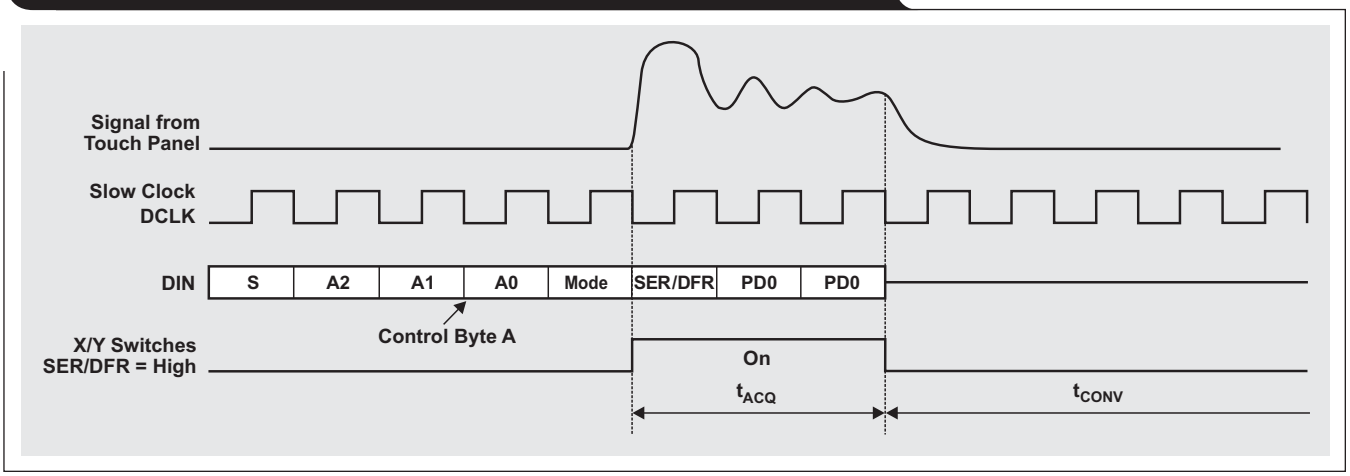
Difference between single-ended and differential modes

In both single-ended and differential modes, the ADC acquires (samples) the input analog voltage from the touch panel for some time, t_{ACQ} (see Figure 3). The input voltage has to settle within t_{ACQ} in order for the ADC to capture the correct voltage.

Turning the drivers on causes the touch panel's voltage to rise rapidly and then settle to the final value, as shown in Figure 3. To acquire the correct value for conversion, the acquisition must be complete when the touch panel has completely settled. There are two ways of accomplishing this.

One method (shown in Figure 3) uses the ADC in single-ended mode and a relatively slow clock. A slow clock extends the acquisition time, since it extends the clock periods used for acquisition. The drivers turn on at the beginning of the first of three clock periods (for simple controllers like the ADS7843, ADS7846, TSC2003, and TSC2046). The panel must then settle completely during

Figure 3. Timing diagram of single-ended-mode operation for TSC2046



the following two clock cycles, so that at the end of the third clock cycle, the acquired voltage is accurate.

The second method (shown in Figure 4) uses the differential mode and a much faster clock rate. Control byte B turns the drivers on and, as before, the touch panel's voltage rises rapidly and begins to settle. In this case, a conversion is done, and then a second conversion is begun, by sending control byte C. If control bytes B and C are the same, the internal X/Y switch of the ADC will not turn off after completing a conversion for control byte B. Thus, the touch panel voltage will be settled by the time the conversion from control byte C begins, and this conversion will be accurate. This method requires that the conversion result from control byte B be discarded, as it will not be accurate since its acquisition period occurred when the touch panel voltage was still ringing.

An advantage to using the second method is the potential for power savings. After the end of conversion for control byte C, the controller can go into power-down mode and wait for the next sampling period. In the slow-clock case, the next sample period may have to come immediately after the current conversion, leaving no time for power down.

Using a fast clock in single-ended mode (Figure 5) would not be of any help, because the drivers turn off between conversions. This results in the touch panel's voltage rising at the beginning of each conversion, which never gives the touch panel a chance to settle.

Figure 4. Using a fast clock in differential mode for TSC2046

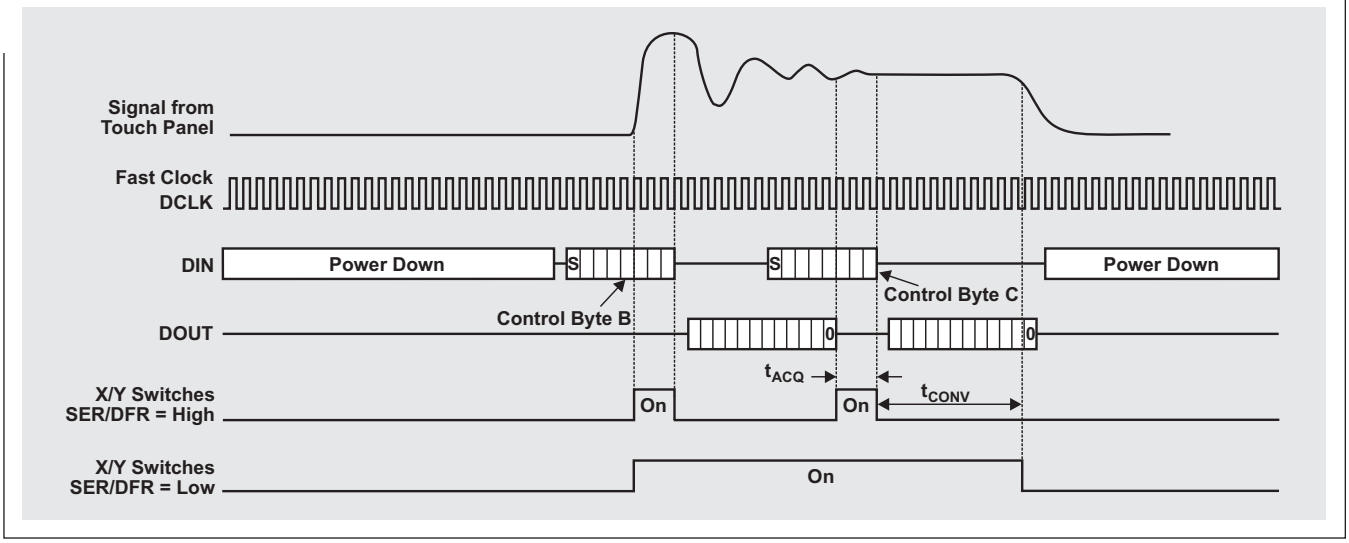
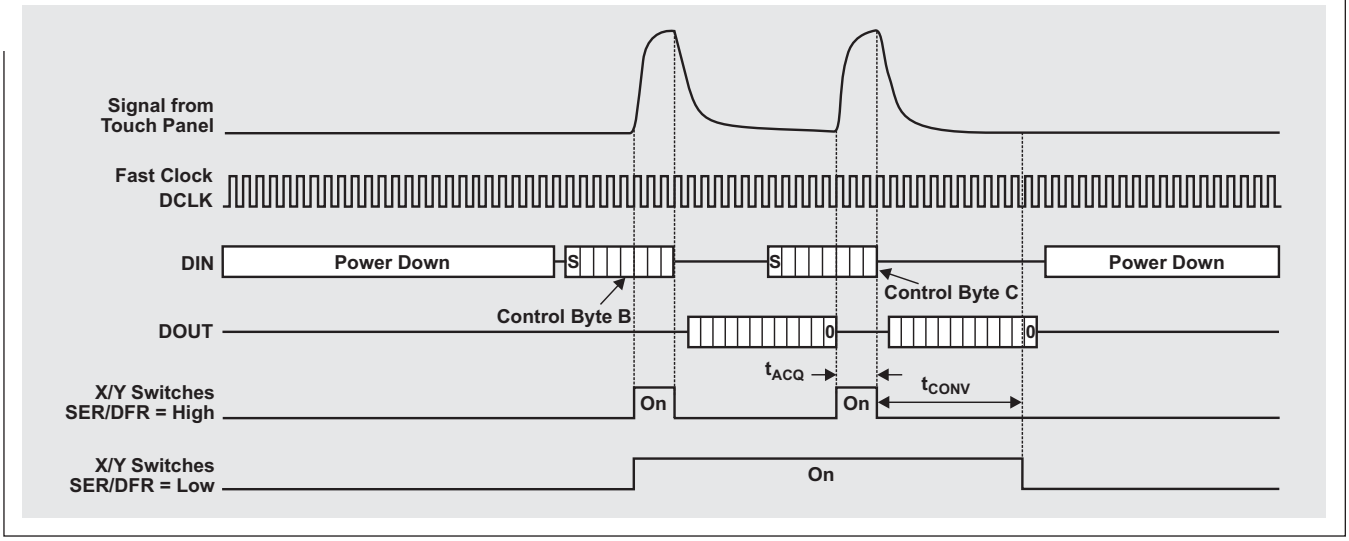


Figure 5. Using a fast clock in single-ended mode



Making the ADC results usable for a human interface

Since several measurements for one coordinate pair are being taken, the designer has the opportunity to do some processing on this data, like averaging. This will help prevent spurious readings that may make dealing with the human interface difficult.

Touch-screen acquisition flowchart

Figure 6 shows a typical flowchart for a touch screen. In its idle state, the touch-screen controller's pen interrupt (PENIRQ) line is held high. When a touch occurs on the screen, the PENIRQ line is driven low, signaling the host processor that it needs to start taking coordinate readings.

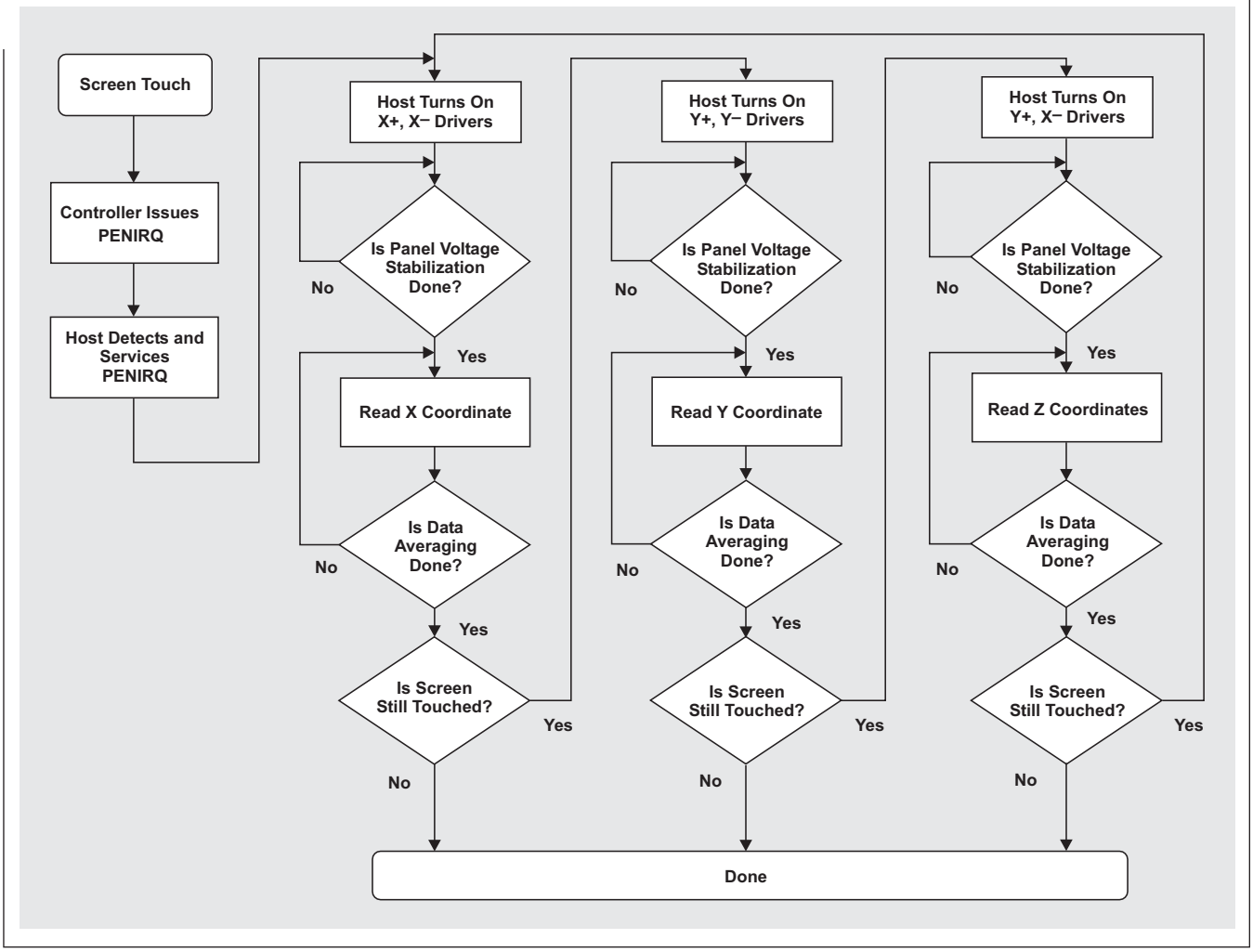
The host will then turn on the X drivers, wait for settling to occur, and then take several readings of the X coordinate. The host will then turn off the X drivers and turn on the Y drivers. After waiting again for the screen to settle, the host will take several readings of the Y coordinate. The same process can be used for taking Z-coordinate readings if touch pressure is also to be measured.

The Z-axis measurement for touch pressure is used in applications such as signature capture, where the pressure information is important for recognizing the authenticity of a signature. However, even in conventional X-Y applications, using the Z-axis measurement can be helpful in determining whether a touch data point is valid. Using this measurement can help prevent spurious readings that may occur due to the mechanical bouncing of the touch screen plates, simply because readings where the pressure is too light are not accepted. A complete description of the Z-axis measurement process can be found in the datasheets for touch-screen controllers with this capability.

Data-averaging algorithm

The averaging algorithm reduces noise resulting from contact bounce during use of the touch screen. Successive X and Y samples are tested to determine if their values

Figure 6. Touch-screen acquisition flowchart



differ by no more than a certain range. If one or more samples falls outside this range, the samples are discarded and the process is restarted. This is continued until successive X samples (then Y samples) fall within the range. The average of these values is used as the X and Y coordinates, respectively.

Once independent X and Y samples are obtained, coordinate pairs are sampled to eliminate the effects of noise. If a sample does not fall within an internal range, all X and Y coordinate pairs are discarded and the independent X and Y sequence is restarted. Once acceptable coordinate pairs have been obtained, an average coordinate pair is determined.

The entire process just described can be done by the processor or by some of the newer, intelligent controllers like TI's TSC2200, TSC2301, or TSC2101. These devices take care of the settling-time issues and other touchscreen interface problems previously described; they also relieve the host CPU from the tasks of reading and writing over the serial interface so often. These intelligent devices can be programmed to respond to a touch, take a complete set of coordinate readings, average several readings, and then—only when this entire process is complete—interrupt the host processor. The host then does only one reading of all coordinates and need not do any further averaging or noise reduction.

These highly integrated devices come paired with keypad controllers (TSC2200) or audio codecs (TSC2301, TSC2101) to provide complete human/machine interface controllers in a single package.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Skip Osgood, CK Ong, and Rick Downs, "Touch Screen Controller Tips," Application Report	sbaa036

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Simple DSP interface for ADS784x/834x ADCs

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Applications Engineer, Data Acquisition Products

Introduction

The 12-bit ADS7841 and 16-bit ADS8341/3 are pin-compatible, 4-channel analog-to-digital converters (ADCs) with a synchronous serial interface. Typical power dissipation is 2 mW at a 200-kHz throughput rate on the ADS7841 and 8 mW at 100 kHz on the ADS8341/3. The 12-bit ADS7844 and 16-bit ADS8344 are pin-compatible, 8-channel ADCs with the same typical power requirements as their 4-channel cousins.

The low power, high speed, and onboard multiplexer of these devices make them ideal for battery-operated systems such as personal digital assistants, portable multichannel data loggers, and measurement equipment.

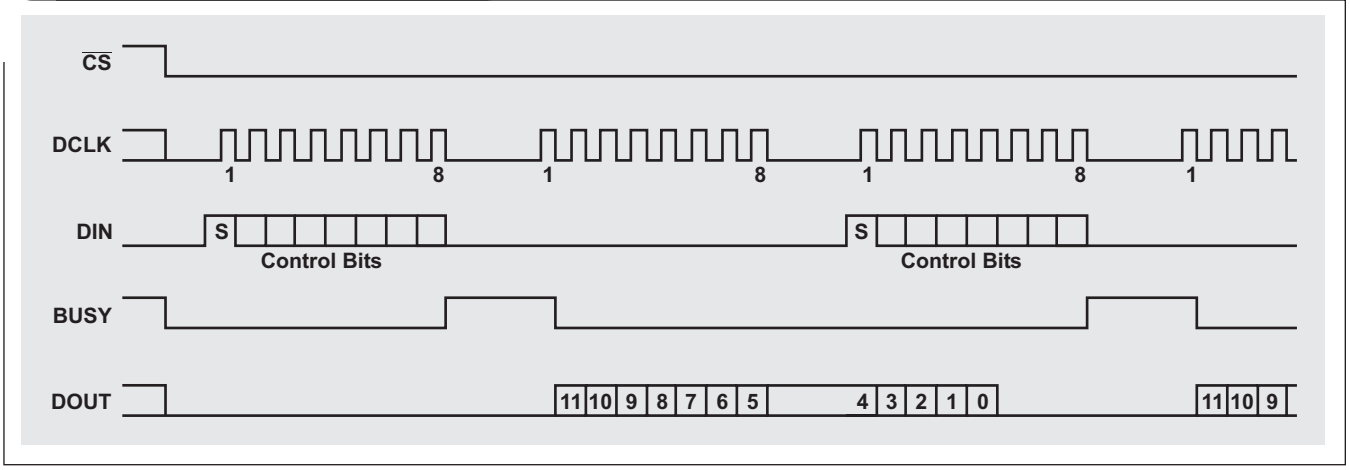
The datasheets for these devices show various ways to interface the parts to microcontrollers with a serial peripheral interface (SPI), but they do not mention how to use these parts with high-performance digital signal processors (DSPs). This article provides an easy way to connect these parts with any Texas Instruments (TI) DSP that contains at least one multichannel buffered serial port (McBSP). The information here pertains to the TMS320F2812 and all devices in the TMS320C5000™ and TMS320C6000™ DSP platforms.

Digital interface for microcontrollers

The digital interface section of the datasheet for all five of these devices shows a typical SPI with burst clock mode of operation based on 8 or 16 clock cycles. While an SPI interface is certainly not difficult to implement, there can be a bit of difficulty associated with getting the received data into a format that the processor can actually use. Figure 1 shows a typical 8-bit SPI interface.

The difficulty many users run into with this interface is in formatting return data with minimal software overhead. At first glance, it is not always obvious to new users of these parts that the most significant bit (MSB) is presented on the 9th clock cycle. With a microcontroller like the MSP430 series of devices and the SPI interface shown in Figure 1, the 7 MSBs of data are stored in an 8-bit register, with the 5 least significant bits (LSBs) stored in a second 8-bit register. In order to store the converted data in a meaningful fashion, both the upper and lower bytes would need to be shifted (left or right) and then concatenated before being stored into a data array for future processing. In applications such as motor control, the software latency of these data manipulations proves too costly.

Figure 1. Typical 8-bit SPI interface



The process can be simplified a little if the microcontroller is capable of running with a 16-bit SPI interface, such as the TMS470 series of devices from TI. For the 12-bit parts, all returned data can be captured in a single 16-cycle transmission. To accomplish this, simply shift the command byte to the left by 7 bits as shown in Figure 2. The SPISCS line shown in Figure 2 could be tied to the chip select line of the ADC if multiple devices share the SPI bus.

The modified 16-clock SPI interface of Figure 2 sends the BUSY signal high on the falling edge of the 15th clock. In some applications, this approach might still require a data shift. The 12-bit data is MSB-aligned and the MSB is provided twice. The software overhead becomes less of an issue in this case since the shift can be done during the actual data reception in the SPI routine.

There are two drawbacks to this approach—first, the LSB is lost. The LSB is cut short during the switch from sample to hold mode and the host processor will always read it as a "one." The second issue is latency. These converters enter their acquisition phase after the A0 bit is read into the part. The data shown in Figure 2 would be the conversion results from the previous cycle, which adds latency to the system.

When the 16-bit parts are used, the problem is aggravated even further. An 8- or 16-bit SPI device like the MSP430 or TMS470 would need to issue at least 24 SCLKs to complete a 15-bit transfer. If the entire 16 bits of data are needed, a total of 32 clocks would be required. Data manipulation would still need to be done, adding software overhead.

Digital interface for TI DSPs

Using the high speed and flexible capabilities of the McBSP ports found on the TMS320F2812 or the C5000™ and C6000™ DSP platforms can virtually eliminate the software overhead associated with the microcontroller and the SPI interface.

The McBSP ports have independent transmitter and receiver functions. Since transmit and receive sections are independent, transmit and receive frame sync (FS) signals are also independent. If the chip select (/CS) signal is tied low, the BUSY signal can be used as the frame sync return (FSr) to indicate that a serial stream is on its way into the receiver. The data transfer to the DSP is done without any further need for manipulation. Setting the data transfer length in the DSP to 16 bits allows exactly the same software routine to be used with the 12-bit ADS7841 or the 16-bit ADS834x devices.

Figure 2. Modified 16-clock SPI interface

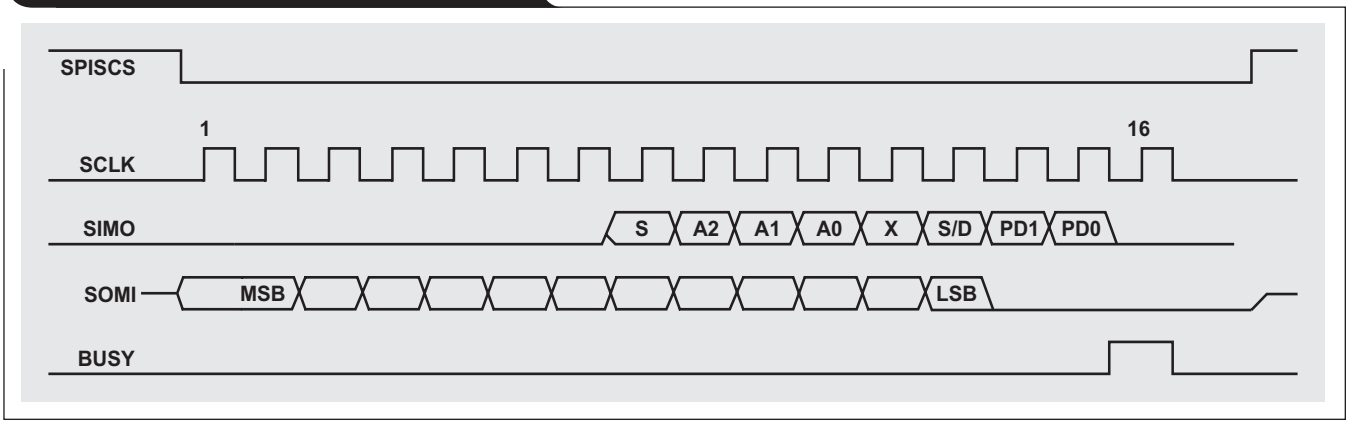
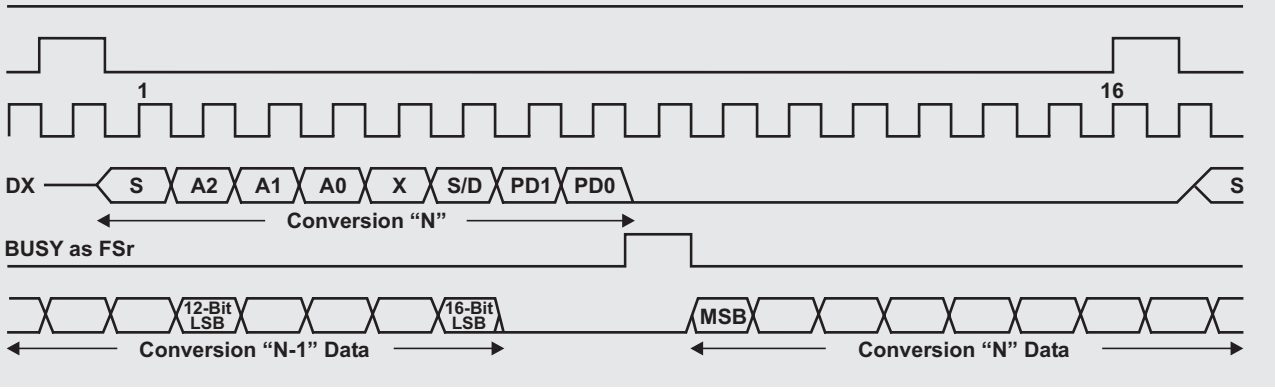


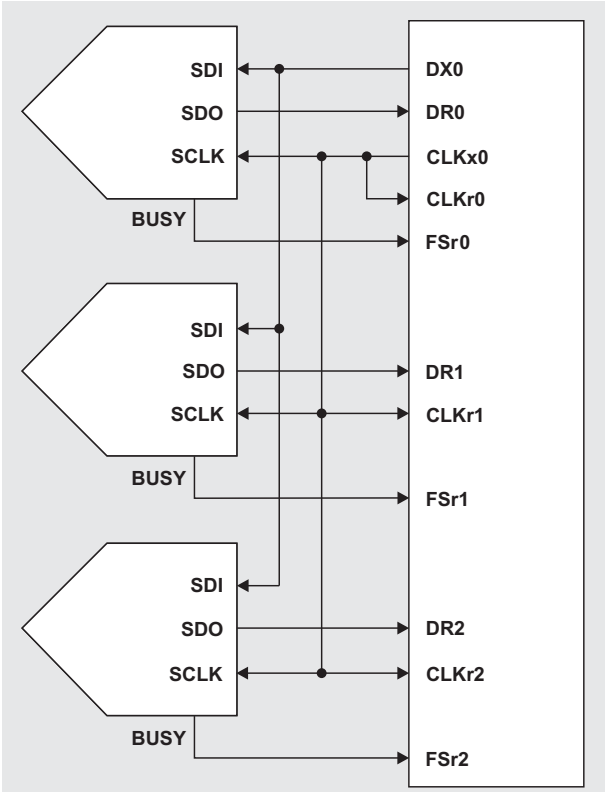
Figure 3. DSP transfer with 16 clock cycles



As shown in Figure 3, the output data is actually wrapped between conversion start commands so that there is minimal latency between conversion cycles. Data is presented to the DSP MSB first from both the 12-bit and 16-bit devices. If LSB alignment is required, a 4-bit shift could be implemented to the received data as it is sampled.

Another added advantage of using the DSP is the possibility to realize simultaneous sampling on up to three devices on a DSP with multiple serial ports. This would be done by using a single "master" transmitter tied to all three ADCs and returning the master clock to all three "slave" receiver ports. The BUSY signal from each of the three ADCs would again act as the FSr to each receiver. Figure 4 shows a potential method for implementing multiple ADCs in a simultaneous sampling application.

Figure 4. Multiple ADC configuration



Conclusion

The ADS784x/ADS834x data converters are truly versatile with their simple serial interface, low power, high-speed operation, and ease of use. They are ideal for portable and handheld applications that require excellent performance capability and upgrade flexibility. For additional information on the devices mentioned in this article, please contact your local distributor, the TI Product Information Center listed on the last page of this document, or the Data Converter Applications team at dataconvapps@list.ti.com

Related Web sites

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microcontroller.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS7841, ADS7844, ADS8341, ADS8343, ADS8344, or TMS320F2812

Miniature solutions for voltage isolation

By Geoff Jones (Email: gjones@ti.com)
Marketing Manager

The hot growth in distributed-power architecture has fueled the development of miniature low-power (<2-W) DC/DC converters. As their name implies, these devices minimize the impact of the converter onboard space. They provide point-of-use isolated power conversion for analog circuitry in industrial applications and safety-critical applications such as telecommunications and medical equipment. Additionally, miniature DC/DC converters benefit designers who need galvanically isolated output power or noise reduction in analog circuitry.

In most modern noise-sensitive circuitry, system designers often have a small number of components that require total isolation from their input power supply. It is necessary to isolate the load and noise presented to the local power-supply rails from the main-supply rails of the entire system. Mixed-signal integrated circuit (IC) design, for example, frequently leads to nonfunctional devices because of noise problems. Large amounts of digital noise combined with sensitive analog circuitry often results in interference noise.[1]

Miniature DC/DC converters with galvanic isolation offer very low output noise and high accuracy. Galvanic isolation helps to reduce system noise by providing a floating ground on the secondary side of the converter.[2] The input-to-output isolation can then be used to provide a simple, isolated-output power source; or, it could be used to generate different voltage rails, dual-polarity rails, and/or nonstandard voltages. Also, as a noise reduction technique in analog circuitry, the isolation barrier prevents noise from the digital ground bus from affecting the sensitive analog circuits.

The standard brick-type converter is not well suited for this requirement. In addition to its higher cost, the brick's output power is overkill for applications requiring <2 W. What's more, the installed size of a brick is often prohibitive. Designers require miniaturization to save valuable board real estate. Because they are significantly smaller than even the new sixteenth-brick format (0.29 in^2 vs. 1.17 in^2), miniature DC/DC converters are particularly suited to generating onboard voltages in space-constrained designs.

So why not "roll your own" DC/DC power supply? Discrete component onboard converter designs are a low-cost alternative to bricks and off-the-shelf miniature DC/DC converters. However, fewer designers are developing discrete designs because of their disadvantages. Extra functionality, such as device protection and module-to-module synchronization, are difficult to implement; reliability is often poor; and achieving a small-sized power supply is difficult. In addition, many designers of higher-level products—of which the DC/DC converters are only one component—lack the time to become expert enough in converter design to build their own devices. As a result of these challenges, more and more designers are specifying miniature DC/DC converters for their applications. The converters offer significantly lower risk, much faster time to market, and development-cost savings.

Besides their advantages over bricks and discrete designs, miniature DC/DC converters also provide a compact-sized power solution for point-of-load (POL) power conversion. POL converters enable designers to overcome the challenges caused by the high peak-current demands and low-noise margins of the latest high-performance semiconductor devices. The converters can be placed close to their loads. This minimizes losses caused by voltage drops, helps overcome noise sensitivity and EMI emission issues, and ensures tight regulation under dynamic load conditions.

What's available?

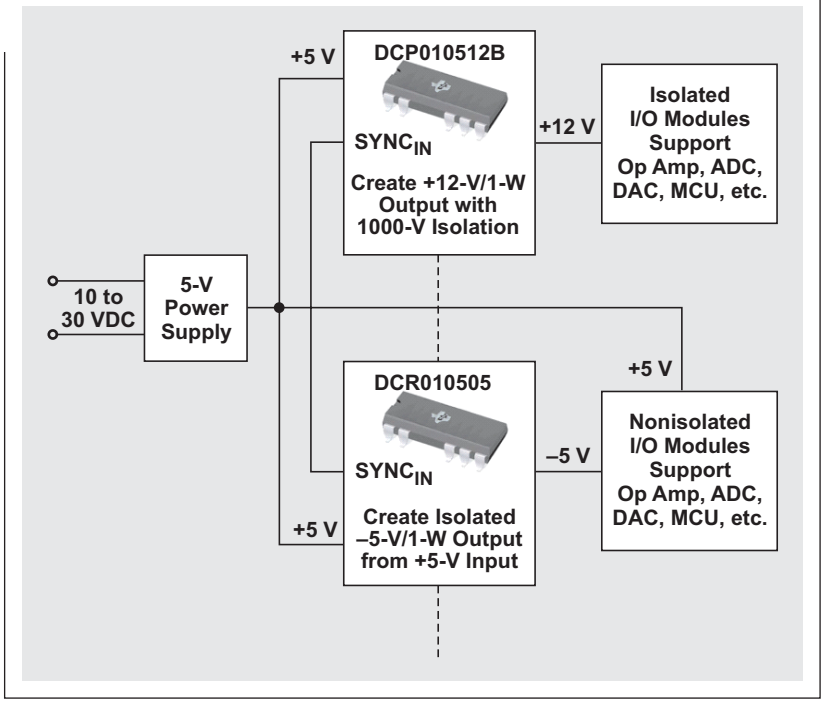
Miniature DC/DC converters offered by C&D Technologies, Texas Instruments, Wall Industries, and others benefit designers who require isolation and output current in the 20- to 500-mA range. The converters are available with 5-, 12-, 15-, or 24-V inputs. Single-output converters are available with voltages from 3.3 to 24 VDC. Dual-output converters with voltages from ±3.3 to ±24 VDC are also available.

Miniature DC/DC converters offer regulated or unregulated outputs with input-to-output isolation ratings of 1000, 1500, or 3000 VDC. Operating temperature extends from –40°C to +100°C. Due to their high switching frequencies (up to 400 MHz), the converters deliver efficiencies of up to 85%.

Built-in features

For system designers seeking to implement miniature DC/DC converters, the devices offer various built-in features that ease system integration and simplify design. Many of the available products incorporate thermal and short-circuit protection and internal filtering. Some of the more advanced converters allow device-to-device synchronization. If an application uses more than one converter on a PC board,

Figure 1. Self-synchronizing DC/DC converters in distributed-power application



beat frequencies and other electrical interference can be generated. DCP010512B and DCR010505 converters (Figure 1) overcome this problem with a built-in synchronization control that allows multiple converters to be synchronized to one another. The feature makes it easy for designers to synchronize up to eight devices by connecting the $SYNC_{IN}$ pins together. This eliminates electrical interference caused by variations in switching frequencies.

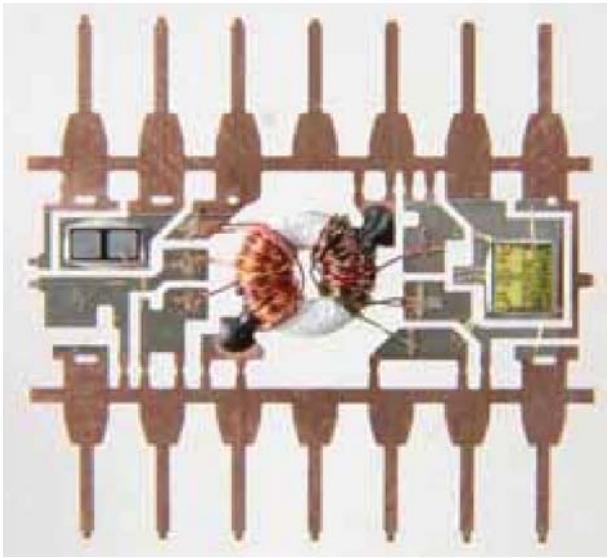
Construction

Today's DC/DC converter technologies continue to focus on higher densities and efficiencies as well as on smaller packages. One of the more innovative converters is manufactured with the same technology as standard IC packages, including dual-in-line (DIL) and small-outline (SO) styles (Figure 2). They use an IC lead-frame as the medium to interconnect silicon devices and magnetic components within the IC package (Figure 3). The result is an isolated DC/DC converter that provides high reliability, excellent thermal management, small size, and compatibility with standard board-assembly processes. The standard IC format also allows tape-and-reel assembly, which helps reduce manufacturing costs.

Figure 2. Miniature isolated DC/DC converter in standard IC package



Figure 3. IC lead-frame



Different configurations

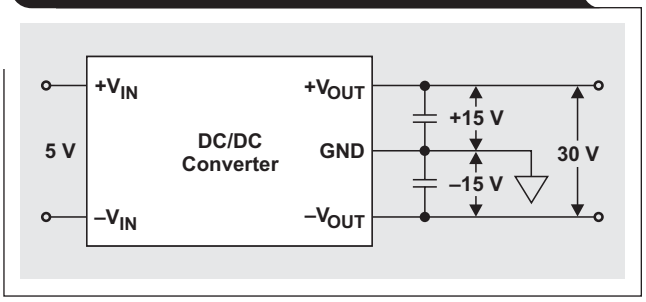
The galvanic isolation of the output from a miniature DC/DC converter allows nonstandard voltage rails to be generated by connecting multiple converters in series. This is accomplished by simply connecting the positive output of one converter to the negative output of another. This configuration allows a wide variety of voltage variations to be produced. The outputs on some dual-output converters can also be connected in series to provide two times the magnitude of output voltage. Figure 4 shows a dual ±15-V converter connected to provide a 30-V rail.[3]

Multiple converters connected in parallel often provide a suitable solution for cases where a single converter is unable to deliver the required output power. When parallel connection is used, it is always a good design practice to use parallel converters of the same type. Figure 5 shows two converters connected in parallel.[2]

Addressing voltage isolation in low-power applications

Miniature DC/DC converters that provide input-to-output isolation and low output power offer innovative solutions for high-density power-supply designs in a variety of applications. Some typical examples include industrial process control, DC motor drive, test and measurement, power transmission, medical equipment, and data acquisition.

Figure 4. Connecting dual-output converters in series



Figures 6-8 show examples of DC/DC converters and operational amplifiers (op amps) used in common power-supply designs.

Positive-to-negative voltage conversion

Positive-to-negative voltage conversion is a popular application for miniature DC/DC converters. Precision op amps are optimized for higher-speed applications. The devices offer very low offset voltage and drift and are commonly found in data acquisition, telecom equipment, professional audio equipment, and portable applications requiring high precision. Some op amps require complementary power-supply

Figure 5. Connecting multiple DC/DC converters in parallel

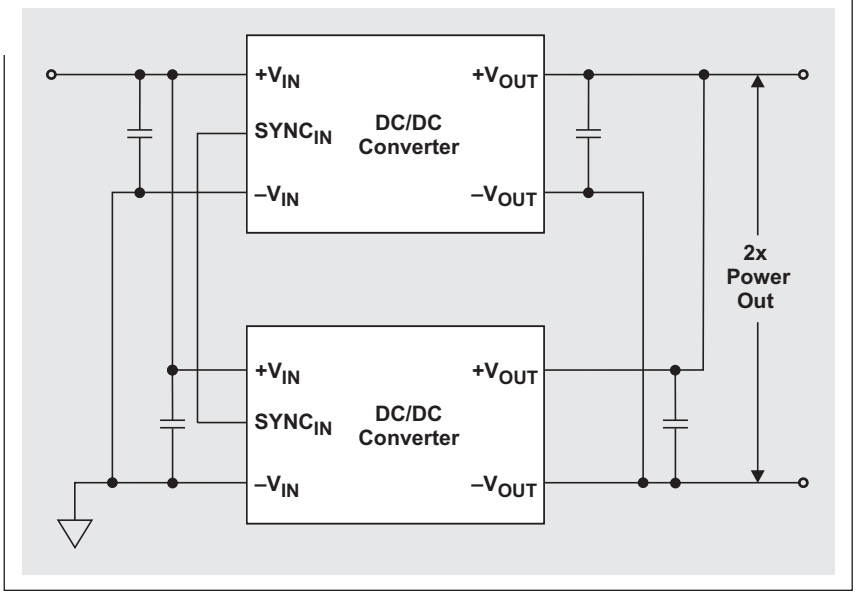


Figure 6. Positive-to-negative voltage from single supply

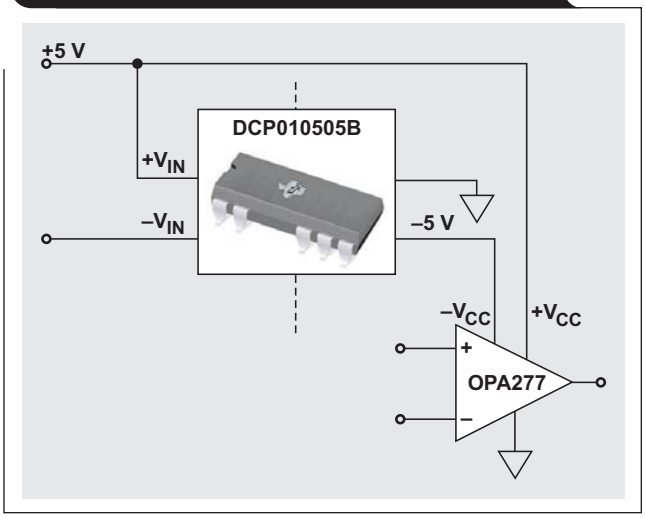
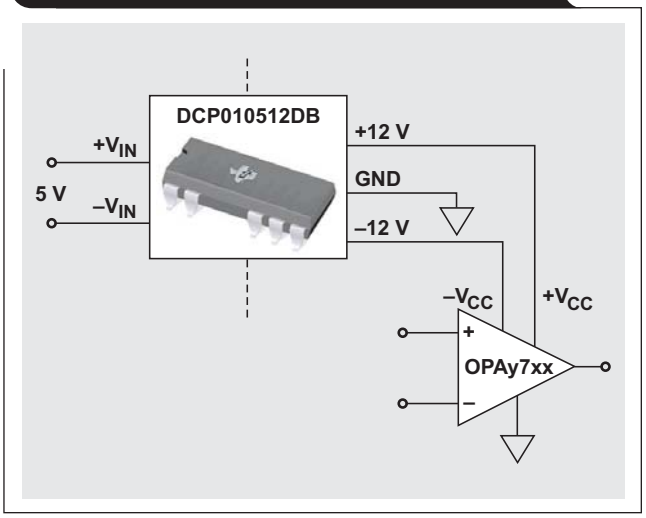


Figure 7. Positive and negative voltage from single supply



rails. The isolated output of the converter in Figure 6 is used to generate a negative supply voltage. The isolated negative output is referenced to the op amp's positive input.

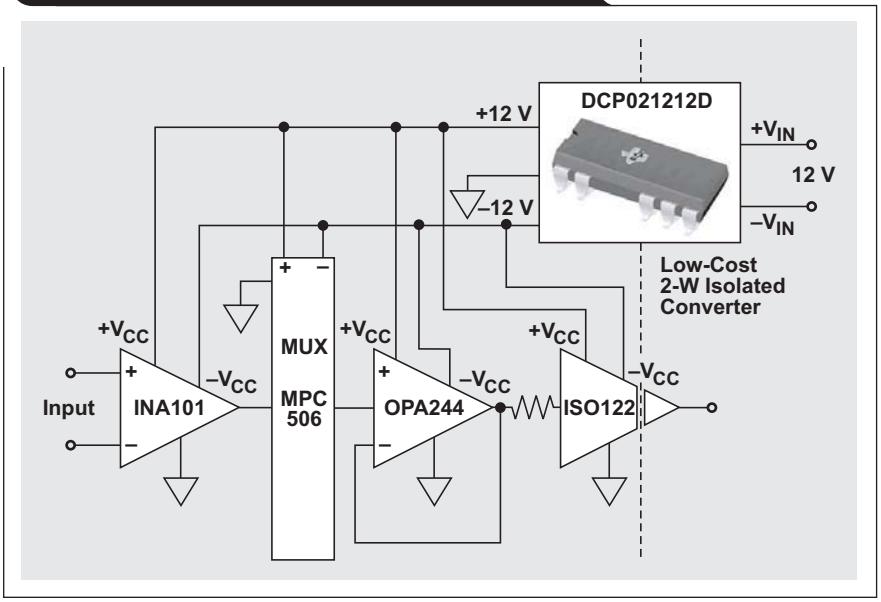
Positive and negative voltage from a single supply

Miniature DC/DC converters in standard IC packaging reduce the board space required to create positive and negative output voltages to an op amp. Figure 7 shows the ability of a single isolated converter to create positive-to-negative output voltages efficiently for a signal conditioning circuit with differential input. The dual-output converter is used to create unregulated output voltages with a magnitude higher than its +5-V input. Operating from an input voltage range of 4.5 to 5.5 V, the converter performs a boost function that creates a +12-V output and a buck-boost function with a –12-V output.

Power-supply isolation for AC or DC instrumentation amplifier

The challenge for system designers working with signal conditioning circuits in AC or DC instrumentation amplifiers is to eliminate ground loops that can affect measurement accuracy. Miniature isolated DC/DC converters achieve this goal. The circuit in Figure 8 uses a dual-output DC/DC converter to produce an isolated voltage. The converter is used in conjunction with a precision isolation amplifier to

Figure 8. Power-supply isolation for AC or DC instrumentation amplifier



fully isolate the instrumentation from noise generated by other parts of the circuit. The isolation barrier characteristics do not affect the signal integrity, resulting in excellent reliability and good high-frequency immunity across the barrier.

Summary

In most modern noise-sensitive circuitry, system designers often have a small number of components that require total isolation from their input power supply. Miniature DC/DC converters effectively isolate the load and noise presented to the local power-supply rails from the main-supply rails of the entire system.

The off-the-shelf devices use a highly integrated package design that makes them suitable for a wide range of applications in space-constrained board designs. They are smaller and lower-priced than the standard brick-type converters. When compared to discrete designs, miniature DC/DC converters offer lower risk, much faster time to market, and development-cost savings.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Noise Reduction is Crucial to Mixed-Signal ASIC Design Success," *Electronic Design* (October 30, 2000).	—
2. "Packaged DC-DC Converters Solve Distributed Power Dilemmas," *Electronic Design* (June 12, 2000).	—
3. "Miniature, 2W Isolated Unregulated DC/DC Converters," DCP02 Series Datasheet	sbvs011

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New power modules improve surface-mount manufacturability

By Chris Thornton (Email: cthornton@ti.com)
Plug-in Power Products

Introduction

The latest generation of Texas Instruments (TI) board-mounted power modules utilizes a pin interconnect technology that improves surface-mount manufacturability. These modules are produced as a double-sided surface-mount (DSSMT) subassembly, yielding a case-less construction with subcomponents located on both sides of the printed circuit board (PCB). Products produced in the DSSMT outline use the latest high-efficiency topologies and magnetic-component packaging. This provides customers with a high-efficiency, ready-to-use switching power module in a compact, space-saving package. Both nonisolated point-of-load (POL) switching regulators and the isolated dc/dc converter modules are being produced in the DSSMT outline.

TI's plug-in power product line offers power modules in both through-hole and surface-mount packages. The surface-mount modules produced in the DSSMT outline use a solid copper interconnect with an integral solder ball for their attachment to a host PCB. This attachment method is designed to be more reliable than other surface-mount interconnects, which translates to improved manufacturability for customers that employ high-volume, surface-mount manufacturing methods.

Component coplanarity

In the electronics industry, the term "coplanarity" means the maximum distance that the physical contact points of a surface-mount device (SMD) can be from its seating plane. When placed on a flat surface, an SMD will rest on its three lowest points. This defines the seating plane of the device. The number given for coplanarity defines the maximum gap that can exist from the underside of any pin to the PCB to which it is being soldered. This measurement is unilateral.

The traditional requirement for a reliable solder joint is that each pin of an SMD make contact with the solder paste covering its respective solder pad. Solder paste is deposited on the host PCB with a solder stencil and squeegee. The thickness of the solder stencil determines the thickness of the solder deposited. The thicker the solder paste, the more likely it is that the SMD pin will make contact with the solder. During reflow, the surface tension properties of liquid solder cause the solder to wet between the pin and pad. The solder bridges any physical gap between them to form a fillet. Figure 1 shows a cross section of an acceptable solder joint.[1] If the measured coplanarity of the pins is too great for the amount of solder deposited, some pins may not make contact with the solder paste. In this situation the liquid solder simply forms a pool on the PCB pad. It does not wet to bridge the gap between the pin and pad, resulting in an electrical open circuit. Figure 2 shows how an excessive gap between the component lead and solder pad prevents the formation of a solder fillet. In this case the finished assembly must be either reworked or rejected, with a corresponding impact to manufacturing yield and cost. A thicker solder stencil can be used to deposit more solder. This will accommodate parts with a higher coplanarity variance but will cause problems with smaller components that have fine lead pitches. Excessive solder on the pads of small parts can result in adjacent pins being bridged and shorted. The additional volume of solder also increases the risk of solder debris being formed during reflow.

One commonly used thickness for a solder stencil is 0.006 in. (0,015 mm). This thickness generally provides a sufficient amount of solder to ensure that the pins of the components make contact with the PCB solder paste. This dimension is consistent with the coplanarity of SMD packages that limit the maximum distance of any pin from the

Figure 1. Acceptable SMT solder joint

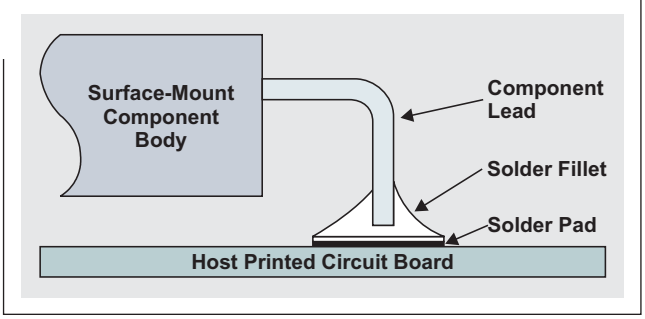


Figure 2. Excessive gap prevents fillet formation

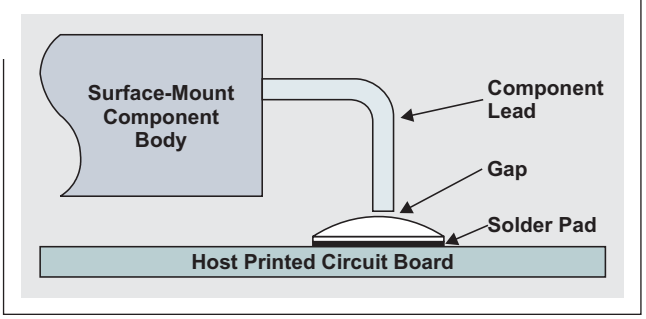
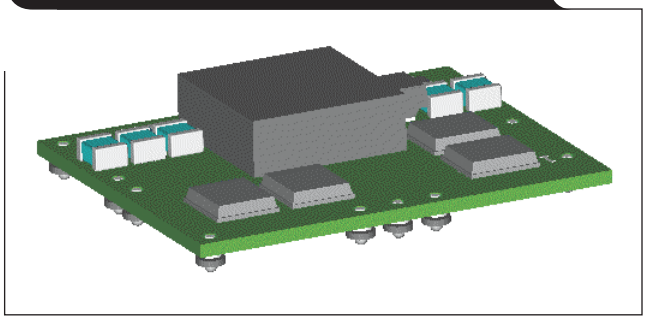


Figure 3. DSSMT power-module assembly



seating plane to no more than 0.004 in. (0,01 mm). For large, complex components such as power semiconductors, magnetic components, and power modules, the package coplanarity is often higher. These parts require a larger solder pad and a thicker layer of solder paste to ensure that they are soldered.

While it is always possible to dispense more solder paste to a select few pads on the host PCB, it complicates the soldering process. A thicker solder stencil can be used, but steps must then be made to reduce the amount of solder deposited onto pads that do not require it. The stencil thickness can be "stepped down" or the apertures (openings) reduced. There are issues with both approaches. The disadvantage with step-down stencils is that they are more expensive and are impractical to implement on a few pads of a densely populated PCB. The reduced-aperture option has to be applied to a large number of solder pads and often requires trial and error to determine a workable aperture pattern. Because of the issues associated with these techniques, original-equipment and contract manufacturers are reluctant to employ them. The expectation is that all components should comply with coplanarity limits that are compatible with a 0.006-in. (0,015-mm) solder stencil thickness. From the industry's standpoint, this simplifies the design of the solder stencil and minimizes the cost.

Power-module construction

Due to their size and construction, the surface-mount packages of power modules are challenged to meet the same coplanarity as smaller surface-mount components. Power components tend to have larger PCB footprints with thicker, longer pins, located on a wider pitch. These characteristics make it more difficult to manufacture power components to the same coplanarity tolerances as small semiconductor ICs. It is not unusual for power-module packages to specify a maximum pin distance from the seating plane of 0.006 in. (0,015 mm) or greater.

Power modules are usually constructed from a subassembly PCB. The leads or pins can be either part of a leadframe or independently attached to the PCB. Depending on the construction, the module may include a plastic or metal case or may even be covered by an exterior molding. The pins can be either solid (rolled or stamped) or flat. The pins elevate the module, giving clearance underneath the body, and provide a foot that can be soldered onto a pad of the host PCB.

As the industry pushes toward higher levels of integration, power modules produced in the DSSMT outline are being well received. The case-less construction allows components to be placed on both sides of the module's PCB (see Figure 3). This results in a more compact module with a correspondingly higher power density. The DSSMT modules use solid pins mounted directly beneath the module. This provides mechanical support as well as an electrical connection to the host PCB.

Factors affecting DSSMT module coplanarity

The three principal factors that affect the coplanarity of DSSMT power modules are dimensional variations in pin length, warping of the module PCB, and soldering variations.

Compared to flat pins, which must be cropped and formed, solid pins are relatively thick and short. This makes them more robust and less susceptible to misalignment through handling. They are manufactured to a predefined length with modern machine tools, a process that results in a consistent product with tight tolerance limits.

The DSSMT package outline places the module PCB in control of the mechanical integrity of the package. This includes the physical alignment of its pins, both lateral and axial. The PCB material is a laminate and subject to manufacturing variations, including warping. Over the dimensions of a semiconductor IC or even a large discrete component, the effects of warping are minimal compared to those of a power module, which can measure up to 3 in. (75 mm) along one side.

Pins with integral solder ball

The solid pins used on TI's DSSMT power modules incorporate a solder ball on the end that interfaces with the host PCB. The solder ball can comprise regular tin/lead (63 Sn/37 Pb) solder or high-temperature tin/silver/copper solder. DSSMT modules manufactured with these interconnects have improved solder-reflow capability. Most significant is their ability to automatically compensate for coplanarity differences between the module and the host PCB.

Figure 4. Detailed view of a Solderball Pin

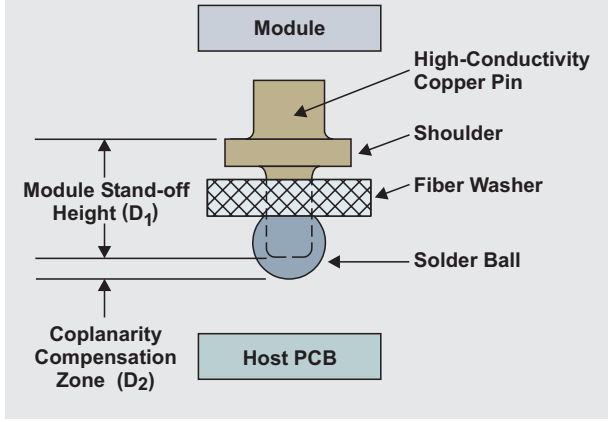


Figure 4 shows a detailed view of a single Solderball Pin™. The high-conductivity solid copper pin incorporates an integral contact or shoulder. The top of the pin is formed into a barrel, which locates within a plated through hole on the module PCB. The shoulder provides a contact area for the copper landing pad on the underside of the module. The lower part of the pin extends through a small fiber washer into a ball of solder. When the module is placed on the host PCB, the solder-ball end of the pins is placed into the same thickness of solder paste as other components. The module is then processed in a normal reflow operation. The main purpose of the fiber washer is to prevent liquid solder from wicking up the pin. The washer retains the solder around the butt joint formed between the pin and the pad on the host PCB. This ensures that there is sufficient solder to form a solder fillet when standard paste levels are used.

Coplanarity compensation

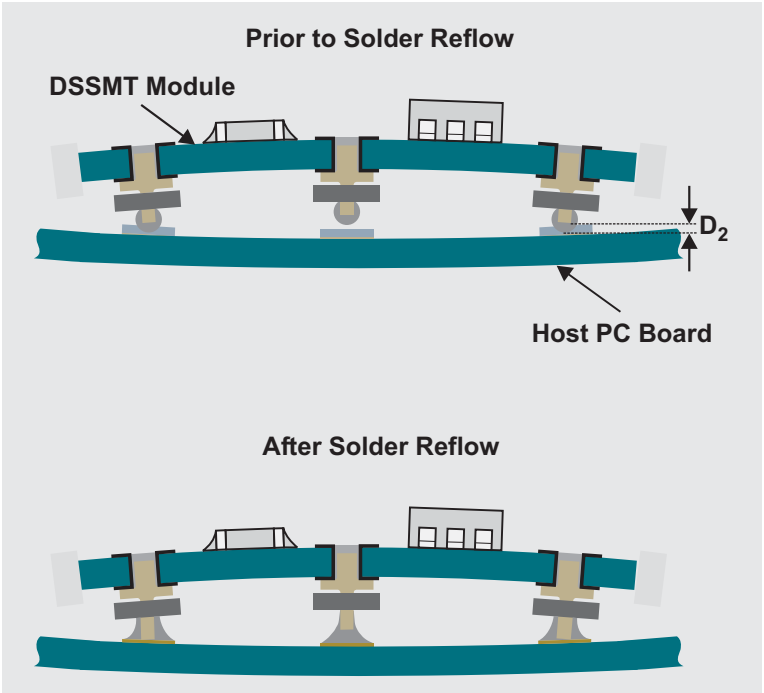
When a standard solder-paste stencil is used, the solder ball adds two important attributes that allow a higher coplanarity variance to exist between the module and host PCB. First, it provides an additional source of solder; and second, it allows the subassembly to drop slightly when the solder becomes liquid during reflow. This drop occurs when the weight of the module overcomes the buoyancy of the molten solder. The amount of drop is equal to the distance that the solder ball extends beyond the end of the pin (within the ball). This is the dimension D_2 in Figure 4, known as the coplanarity compensation zone.[2]

The dimension D_2 corresponds to the additional amount of coplanarity adjustment. The extent of this adjustment is such that the solder ball end of the pin does not have to make physical contact with the solder paste prior to reflow. The seating plane of the module need only bring each solder ball to within a distance of less than D_2 of the solder paste. Figure 5 demonstrates how the coplanarity compensation zone works when a DSSMT module is passed through a standard solder-reflow process. For the purposes of this illustration, the coplanarity variance between the module and the host PCB has been exaggerated.

Prior to reflow, the solder balls of only the two outer pins are shown making contact with the solder paste on the host PCB. The solder ball of the center pin is raised above the paste due to the warping of the boards. The gap created by the raised pin is not a problem as long as it is less than the distance D_2. This is the distance that the lowest pins are raised above the host PCB pads by the solder balls. During reflow, the solder balls become liquid, allowing the module to drop by this distance. The solder ball of the center pin is then able to make contact with the solder paste. Once contact is made, the solder from the ball and paste coalesce to form a fillet. A typical module may have a dozen or more discrete connections, several of which could be raised off the host PCB pads. The joints of these connections would all be brought into compliance as a result of the module sinking toward the host PCB during the solder-reflow process.

The dimension D_2 is a key parameter. The pin manufacturer characterizes this dimension as 0.0127 in. (0,32 mm) nominal, with a standard deviation of 0.0013 in. (0,033 mm). This suggests that the manufacturer's process can easily meet a minimum of 0.008 in. (0,2 mm).

Figure 5. Behavior of DSSMT module during reflow



The amount of coplanarity compensation offered by the dimension D_2 adds to that provided by the thickness of the solder paste on the host PCB. The sum total of these dimensions represents the maximum gap that can exist between the end of a pin and its PCB pad to form a fillet. If the minimum dimension for D_2 is 0.008 in. (0,2 mm), and the recommended solder paste thickness is 0.006 in. (0,15 mm), then the combination can accommodate for a minimum of 0.014 in. (0,36 mm).

DSSMT module coplanarity variance

Generally the coplanarity variance of an SMD can be evaluated by measuring the distance of each contact point from its seating plane. With a solder ball covering the pin ends, the contact point cannot be directly inspected. It is only during reflow that the module settles onto its seating plane. Applying heat to remove the solder to permit inspection is impractical. This would disturb the pin and affect the measurement. For this reason the coplanarity is best assessed by a review of the manufacturing process, along with empirical measurements on manufactured parts.

The three principal factors that affect the DSSMT module coplanarity are: the dimensional tolerance of the copper pin length, warp in the module PCB during solder reflow, and soldering variations of the pin/module joint. Each of these factors can be assessed for its impact on the module's coplanarity variance.

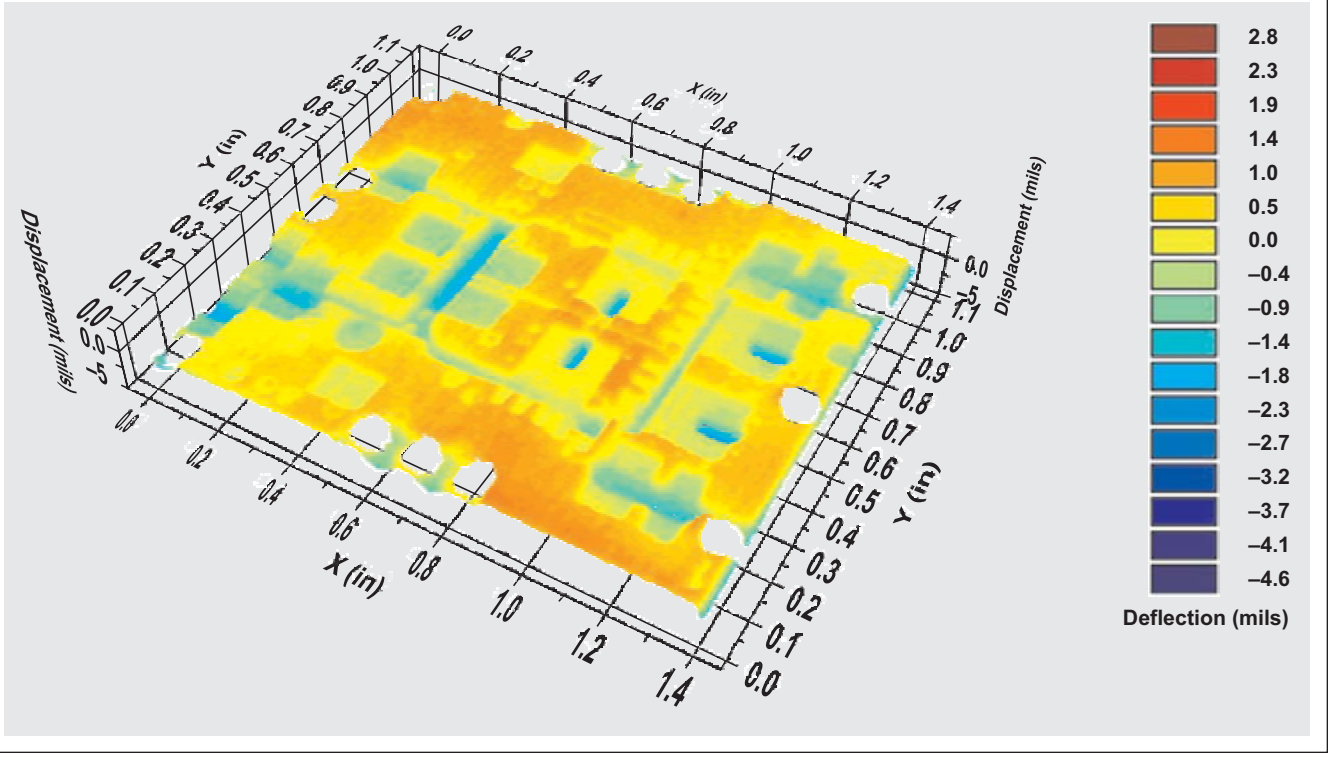
The first factor, variation in pin length, has a direct effect on coplanarity. The pin length is dimension D_1 in Figure 4, the distance from the top of the shoulder to the pin end (within the solder ball). Statistical process control (SPC) obtained from the pin manufacturer gives this dimension as 0.065 in. (1,65 mm). The standard deviation is σ = 0.00056 in. (0,014 mm). If 3σ is used, the variance of the pin will be ±0.0017 in. (±0,043 mm).

To evaluate the second factor, PCB warp, a shadow moiré test system was used to study samples of the module's PCB under reflow temperature conditions. This test is an optical technique that gives a precise measurement of out-of-plane displacements. It was conducted on PCB samples of TI's larger DSSMT modules, the PTH12030WAS. This product measures 1.37 in. × 1.12 in. (34,8 mm × 28,45 mm). The deflection of the PCB was mapped with color 3D plots at various temperatures, from 25°C up to 260°C ambient.

Figure 6 shows the plot from one of the samples at 260°C. The vertical displacement is given in mils (0.001 in.). The results of this testing[3] revealed that none of the PCB samples saw a deflection greater than 0.003 in. (0,1 mm) at reflow temperature. This maximum deflection was recorded in the areas around the pin landing pads, at the opposite corners of the PCB. PCB deflection was also reduced as the ambient temperature was raised from 25°C, and was lowest at reflow temperatures. This is notable, as it is during reflow that the module establishes its seating plane.

The third factor that can affect coplanarity, soldering variances of the pin/module joint, is primarily caused by the pin's tendency to float on its landing pad. This is known as axial float. It can cause the pin to drop slightly

Figure 6. Shadow moiré 3D plot at 260°C



due to its shoulder not being completely flush with the underside of the PCB. Figure 7 is a cross section of a DSSMT module, taken through the pin/module joint. It shows the shoulders of the pins to be almost flush with the module's PCB surface, indicating that pin float is well controlled during the manufacturing process. This variance is considered negligible compared to the other parameters examined; and it promises to be even less significant if the module is exposed to a high-temperature, lead-free reflow process. The pin is attached to the module with high-temperature tin/silver (96.5 Sn/3.5 Ag) solder. At high-temperature reflow, this joint will also reflow, and any pins standing proud (due to axial float) will be reseated by the weight of the module. However, for the purposes of this assessment, we'll assume a token variance of 0.001 in. (0,025 mm) for this parameter.

Of the three principal factors that affect module coplanarity, pin length is the largest contributor. This is because it has a twofold (2×) effect on the gap that can exist beneath a pin and the module's seating plane. Consider that the seating plane of the module might be established by three pins close to their maximum variance in length. A gap of 2× this variance will then exist beneath each pin that is close to its minimum variance.

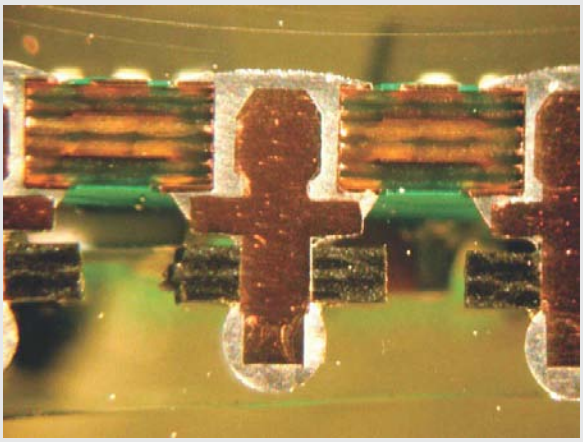
Table 1 summarizes the three major factors that affect module coplanarity. The results suggest that the module could contribute as much as 0.0074 in. (0,188 mm) in coplanarity variance with respect to its seating plane.

Table 1. Module coplanarity variance to seating plane

DESCRIPTION	VARIANCE (in.)	MULTIPLIER	CONTRIBUTION (in.)
Pin length	0.0017	x2	0.0034
PCB warp	0.003	x1	0.003
Pin float	0.001	x1	0.001
		Total:	**0.0074**

To add confidence to this assessment, physical measurements were also made on sample lots of PTH12030WAS production parts before their assembly to a host PCB. In each case the amount of gap beneath the solder ball that was most elevated from the component's seating plane was measured. The results revealed that the maximum lift of a module pin averages 0.004 in. (0,1 mm), with a standard deviation of σ = 0.0018 in. (0,0457 mm). This suggests that the maximum process limit is 0.0094 in. (0,24 mm), assuming normal distribution. This compares to the calculated variance of 0.0074 in. (0,188 mm) for the pin ends. While the physical measurements give some insight into the assessed variances, they include the solder ball. The solder ball covers the pin ends, and its thickness also varies.* Therefore the spread of the physical measurement is expected to be higher.

Figure 7. Cross section of pin/module solder joint



Irrespective of whether the calculated or measured value represents the module's true coplanarity variance, the pin design provides up to 0.014 in. (0,36 mm) of coplanarity compensation. This is sufficient to ensure that all the module's interconnects form a satisfactory solder joint with the host PCB.

Qualification to IPC-9701

The reliability of the host board solder joints was evaluated with the procedure set forth in Reference 4. Thermal cycling qualification was carried out on 42 test modules designed to simulate the PTH12030WAS product. This is the full production sample size per IPC-9701. An additional 10 samples were used to verify the integrity of the joints after rework.

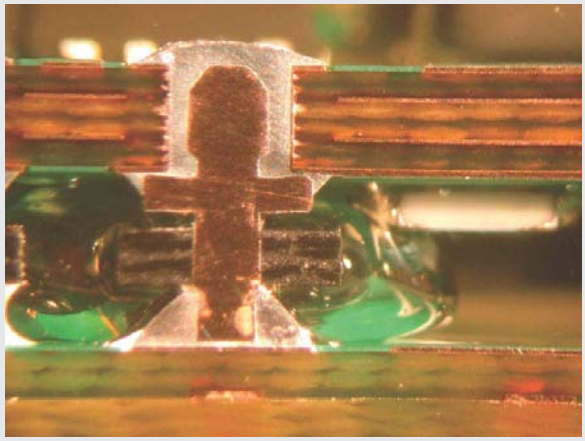
The PTH12030WAS is one of the larger DSSMT modules incorporating pin interconnects with an integral solder ball, specifically the regular tin/lead (63 Sn/37 Pb) version. The test modules were fabricated with the same manufacturing methods used to build the functional PTH12030WAS module. They were then attached to 7 larger host PCBs (6 per host PCB) with 0.006-in. (0,15-mm) tin/lead solder paste and 235°C maximum reflow temperature—the same solder/reflow limits recommended to customers. Both the test modules and the host PCBs were designed to allow the solder interconnects to be continuously monitored for electrical continuity.

With the prescribed test and monitoring methods, the 42 module PCBs were subjected to a total of 3500 thermal cycles over a temperature range of 0°C to 100°C. The results revealed zero failures.[5] Additional analysis was conducted on cross sections of parts that had been freshly soldered to a host PCB. These cross sections allowed the macro-inspection of the solder joints around the interconnect

*The solder ball thickness over the pin end has been characterized by the pin manufacturer as having a standard deviation of σ = 0.0013 in. (0,033 mm).

pins. There were no apparent defects. Figure 8 is an example of a cross section. It shows that the pin has established a generous solder fillet with the host PCB landing pad.

Figure 8. Cross section after reflow to host PCB



Conclusion

The latest power modules from TI are produced in a compact DSSMT package outline. The surface-mount-compatible versions of these packages use a solid cylindrical copper interconnect for their electrical connection with the customer's host PCB. These interconnects incorporate a solder ball at the end of the pin. The solder ball compensates for the coplanarity of a large module, allowing it to be assembled to the host board via a standard solder-paste stencil and a surface-mount solder-reflow process.

The amount of coplanarity compensation provided by these interconnects was compared against the variance that may be introduced by a large DSSMT module. The evaluation revealed a minimum compensation capability of 0.014 in. (0,356 mm) versus a potential total variance of 0.074 in. (0,188 mm). The analysis concluded that interconnects that incorporate a solder ball provide sufficient solder to compensate for the module's coplanarity variance. The integrity of the solder joints between the module and the host PCB were qualified to IPC-9701. The qualification tests that were performed showed good component-to-PCB solder-joint integrity. This translates to improved manufacturing yields and component reliability.

References

1. IPC standard IPC-A-610, Rev. C., "Acceptability of Electronic Assemblies," January 2000.
2. "Solderball Pin™ Interconnects," Application Note, Autosplice, Inc. Available upon request from connect@autosplice.com
3. 081-45028, "PCB Flatness Testing," Texas Instruments internal document. Available upon request from Brett Barry, TI Plug-In Power, jbbarry@ti.com
4. IPC standard IPC-9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," January 2002.
5. 081-45026, Rev. 1A, "IPC 9701 Test Report PTH/PTB Series," Texas Instruments internal document. Available upon request from Joe Pudlo, TI Plug-In Power Products, jpudlo@ti.com

Related Web sites

power.ti.com
www.ti.com/sc/device/PTH12030W

So many amplifiers to choose from: Matching amplifiers to applications

By Ron Mancini (Email: rmancini@ti.com)
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Introduction

Amplifier selection is confusing because there are many different amplifier types to choose from and many of the amplifiers seem to do identical jobs. Various amplifier types include op amps, instrumentation amps, audio amps, differential amps, current feedback amps, high-frequency amps, buffers, and several kinds of power amps. Selecting amplifiers by name is complicated because an amplifier name often stems from the initial rather than present application. "Op amp" is an abbreviation for operational amplifier, an application where the op amp performed mathematical functions in an analog computer.

One sure thing about a semiconductor amplifier (the only kind discussed here) is that it involves either internal or external feedback. The basic building blocks of amplifiers are transistors, and the characteristics of transistors are that their base-emitter voltage and current gain vary with manufacturing tolerances, temperature, stress, and time. Without feedback, the amplifier gain becomes uncontrollable, often varying by a factor of 10 or more.

The best method to control gain variations is with feedback, but there is no free lunch because along with feedback comes the possibility of overshoot, ringing, and eventual oscillation.[1] Internal feedback, or internal compensation (a more popular name), compensates for the amplifier's tendency to overshoot, ring, or oscillate. Internal compensation is transparent to the user, and the amplifier is stable in the recommended application and conditions; but any amplifier with gains greater than one can oscillate under certain conditions. You must supply external compensation components for amplifiers requiring external feedback (externally compensated amplifiers) or they will oscillate or saturate. Always investigate the compensation situation when selecting an amplifier, because it is exasperating to complete a design only to discover that you have built an oscillator rather than an amplifier.

Operational amplifiers (op amps)

Op amps are versatile and within their limitations can replace any other amplifier. The key to good design is to find the op amp limits and then know where to go when you reach these limits. Often the limits are not the op amp; rather the external components impose the limits. Figure 1 shows a generalized schematic for the op amp circuit. Table 1 shows some of the many options available for the circuit performance as a function of the external components. Notice that replacing impedances with capacitors yields functions that are frequency-dependent, and that the placement of the input signal changes the transfer function. There are many specialty amplifiers that replace op amps because general-purpose op amps have limitations, but the separating line has become so gray that in many cases the designer has a choice between an op amp or a specialty amp because both will do the job. This discussion moves on to the types of specialty amps, but it always refers back to the op amp because some deficiency in the op amp has resulted in a specialty amp being designed for a specific purpose.

Figure 1. This op amp configuration produces many different circuits

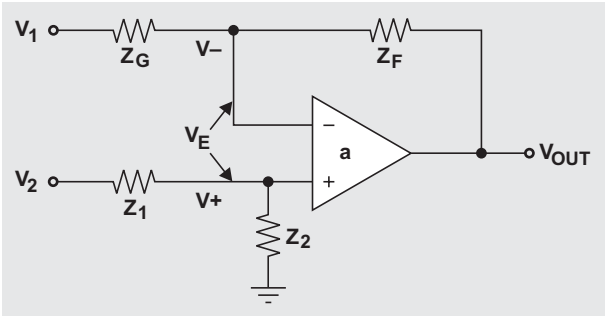


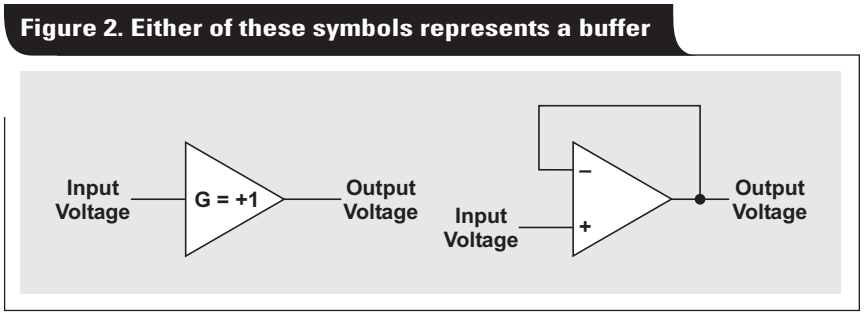
Table 1. Changing component values yields many op amp circuits

CIRCUIT TYPE	V_1	V_2	Z_G	Z_F	Z_1	Z_2
Inverting amp	Input signal	Ground	Determined by gain	Determined by gain	Open	$Z_G \parallel Z_F$
Noninverting amp	Ground	Input signal	Determined by gain	Determined by gain	$Z_G \parallel Z_F$	Open
Inverting integrator	Input signal	Ground	R_G	C_G	Open	$Z_G \parallel Z_F$
Buffer	Ground	Input signal	Open	Short	Short	Open
Subtractor	Input signal –	Input signal +	R_G	R_F	R_G	R_F

Buffer amplifiers

This discussion is limited to voltage buffer amps (see Figure 2) because we enclose current buffer amps inside feedback loops. Voltage buffers have a gain of one, exceptionally high input impedance, and very low output impedance. In an op amp, the input voltage sees an impedance load composed of the input components and the op amp input impedance. In the buffer circuit, the impedance load is due solely to the op amp. This is the first limitation of the op amp; the external components always load the input signal, and this situation is detrimental to good performance when the signal source has significant resistance. The key to solving the input impedance problem is to use buffer amplifiers or possibly instrumentation amplifiers.

Figure 2. Either of these symbols represents a buffer



Op amps exhibit output impedance characteristics like all other amplifiers, but the op amp output impedance is a complex function because feedback modifies the output impedance. The first component of output impedance is the resistance of the output stage. The output stage is usually an emitter-follower type configuration that has low inherent output impedance, usually $r_{ib} + R_B/\beta$ on the order of 25 Ω. The emitter-follower output impedance increases as frequency increases, causing moving poles (poles are points where the frequency response changes sharply) and errors at high frequencies. Worse yet, the output stage of a rail-to-rail op amp is common-collector; and the total impedance depends on the load and can be quite large, often in the kilohm range. The saving grace is the circuit loop gain that divides into the output stage impedance, lowering the overall output impedance dramatically.

The final result is that at low frequencies op amps generally have very low output impedances (fractional ohm values) at dc or low frequencies. Their output impedance rises as frequency increases because the op amp gain decreases as frequency increases. High output impedance causes two problems: dc errors caused by load currents, and stability problems caused by output capacitors creating poles. The best solution for high load currents is to buy an op amp designed to drive the output load in question. A few years ago, a buffer was required to drive several hundred milliamps into a back-terminated cable, but now there are op amps specifically designed to drive these cables without incurring any errors. The buffer always has an advantage over the op amp when it comes to low output impedance because its loop gain is always maximum and the output stage is designed for low impedance.

Some op amps become unstable when they drive capacitive loads, and some op amps drive any capacitive load with no problem. Those op amps designed to drive large capacitive loads have very low resistance output stages, but they sacrifice some speed because of the large structures the output transistors require. In summary, output impedance may cause you to migrate to a buffer, select a very application-specific op amp, or select a power amp.

Subtractor or difference amplifiers

Building an op amp circuit requires external resistors and capacitors. We see from Table 1 that when all the external impedances are resistive and equal, the circuit is a subtractor. Equation 1 is the general subtractor equation.

$$V_{OUT} = V_2 \frac{R_2}{R_1 + R_2}\left(\frac{R_F + R_G}{R_G}\right) - V_1 \frac{R_F}{R_G} \quad (1)$$

When $R_2 = R_F$ and $R_1 = R_G$, Equation 1 reduces to Equation 2.

$$V_{OUT} = (V_2 - V_1)\frac{R_F}{R_G} \quad (2)$$

If the designer is after common-mode voltage rejection—i.e., where $V_2 = V_{2Signal} + V_{CM}$ and $V_1 = V_{1Signal} + V_{CM}$—the conditions to get to Equation 2 demand excellent matching between the resistors. The designer implements Equation 2 with op amps and discrete resistors or with an integrated circuit (IC). The op amp approach is more general because there are ICs with multiple op amps in the package, op amps are inexpensive, and the discrete resistor values are easy to change for gain changes. The down side of the op amp discrete resistor approach is that the resistors don't match well. A designer using 1% tolerance resistors hopes for a 40-dB common-mode rejection, but the discrete circuit yields a worst-case common-mode rejection of 24.17 dB.[2]

Integrated circuit subtractors obtain common-mode rejection ratios greater than 100 dB. The IC subtractors tune the front-end transistors to enable optimal matched performance. Then they use film resistors deposited on the IC substrate to match the resistors. Although thin-film matched resistors are accurate, they still need some help to achieve 100-dB+ performance, so the thin-film resistors are laser trimmed to the final accuracy.

Subtractors have resistors; thus they don't present the highest possible impedance to the load. Many measurements like strain-gage bridge measurements need high common-mode rejection to eliminate common-mode noise, but bridge circuits have appreciable output resistance that interacts with the subtractor input resistance. These applications need a high-input-impedance circuit that eliminates common-mode noise.

Instrumentation amplifiers (IAs)

An instrumentation amplifier has high input impedance coupled with high common-mode rejection, so it is the circuit of choice for many instrumentation and industrial applications (see Figure 3).

Notice that each circuit input of the three-op-amp instrumentation amp is the noninverting input to an op amp; this configuration yields the highest input impedance without resorting to fancy feedback tricks. The subtractor is comprised of R_3 through R_6 and A3. The subtractor still provides the excellent common-mode rejection capability, but A1 and A2 buffer the subtractor, keeping the input impedance high. This circuit can amplify the bridge signal voltage and strip off the common-mode voltage with very little error. Another advantage of the instrumentation amplifier is that a single, nonmatched resistor determines the gain, so the resistor matching problem goes away. The down side of the instrumentation amplifier is increased cost, extra signal delay, and a reduced common-mode voltage range.

The two-op-amp instrumentation amplifier also contains a subtractor to obtain high common-mode rejection capability (see Figure 4). It also has two noninverting op amp inputs acting as the circuit inputs, thus it has the high input impedance of the three-op-amp instrumentation amplifier. This instrumentation amplifier has the added advantage of having a wider common-mode voltage range because it only has two op amps stacked instead of three. The disadvantage of the two-op-amp instrumentation amplifier is unequal stage delays for the input signals. The inverting input has two stage delays while the noninverting input has one stage delay. Unequal stage delays introduce distortion at any frequency above dc, and the distortion increases as the input signal frequency increases. The distortion is present but minimal at frequencies within the IA's operating range.

Current feedback amplifiers (CFAs)

Current feedback amplifiers exist because they have high bandwidth. All of the previous amplifiers discussed were voltage feedback amplifiers (VFAs). VFAs have an open-loop gain that starts decreasing at very low frequencies (often at 10 Hz) with a rate of decrease of –20 dB/decade of frequency. This gain decrease causes poor accuracy at high frequencies. Referring to Figure 5, it is obvious that the voltage feedback amplifier loses gain at high frequencies while the current feedback amplifier retains its high gain on into very high frequencies. VFAs must

Figure 3. This instrumentation amplifier uses three op amps

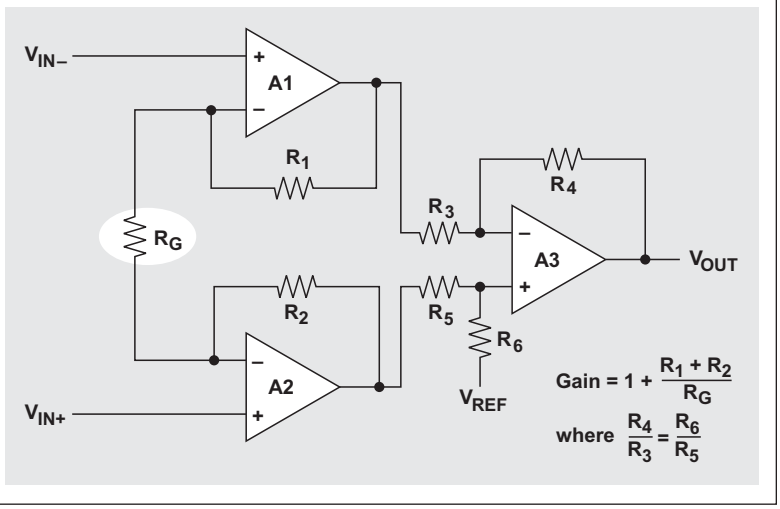


Figure 4. This instrumentation amplifier does the job with fewer parts

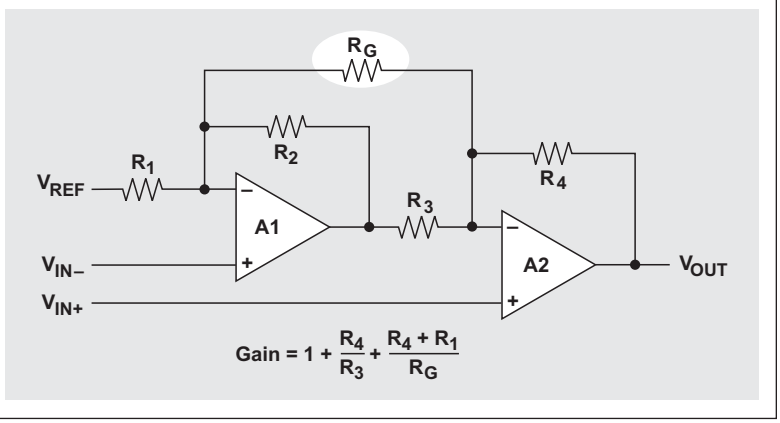
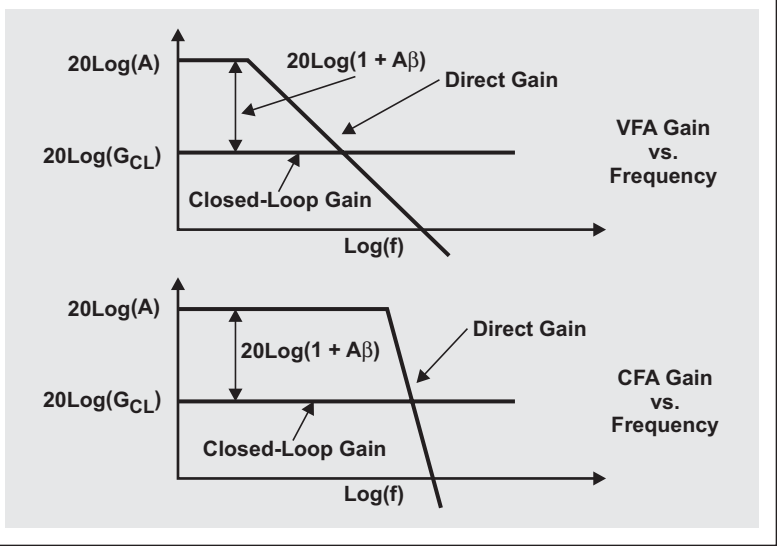


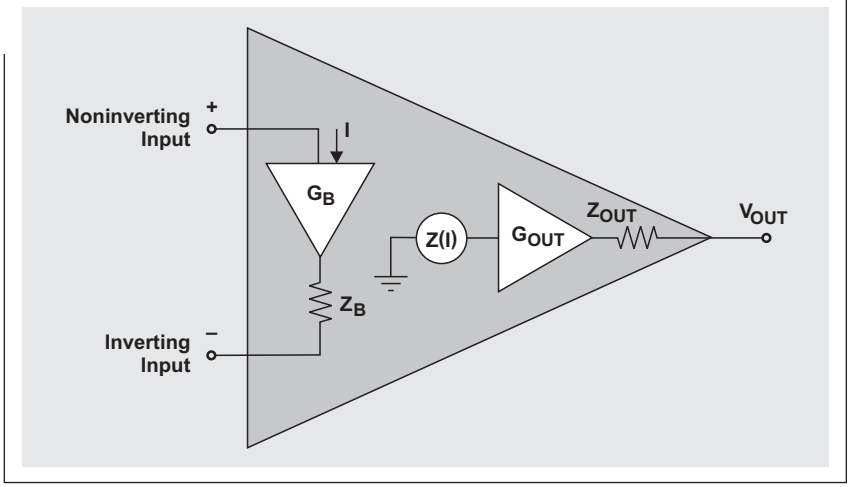
Figure 5. Frequency responses of VFAs and CFAs



operate in the frequency spectrum where the gain is decreasing because their open-loop gain begins to fall off so quickly. CFAs don't work under this constraint, so they offer better distortion performance. The rate of gain decrease is equal for both amplifiers; it looks worse for a CFA because the frequency scale is compacted.

The model in Figure 6 shows that the CFA uses transimpedance rather than gain. The input current is mirrored to the output stage and buffered by the output buffer. This configuration offers the highest bandwidth circuit possible with a given process. CFAs are usually limited to bipolar transistors because the applications they serve, communications and video, don't require high input impedance or rail-to-rail output voltage swing. Notice that the inverting input lead looks into the output of a buffer; so it has low input impedance, usually the output impedance of an emitter-follower stage.

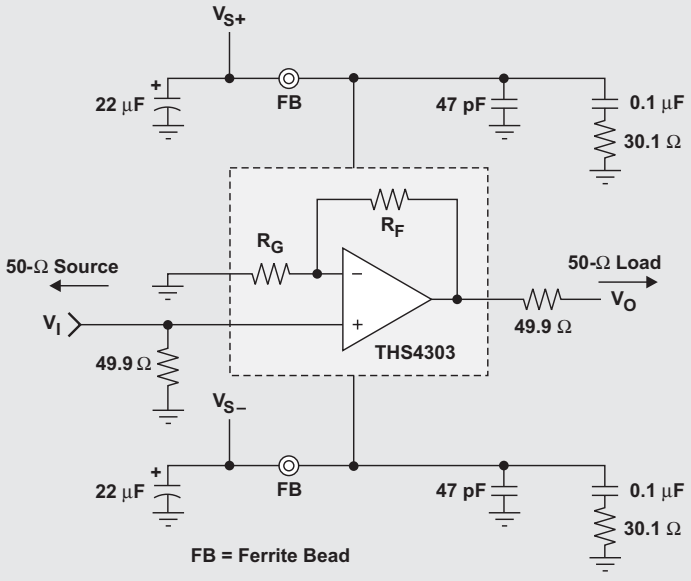
Figure 6. Simplified model of a CFA

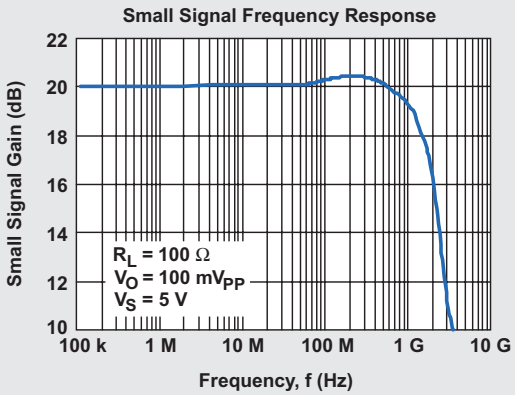


The noninverting lead looks into a buffer input, so it is a high-impedance input. The inputs of a voltage feedback amplifier look into the base-emitter junctions of a long-tailed pair (differential amplifier fed by a current source). Accurately matching the long-tailed pair minimizes the input offset voltages and currents, and this is where the voltage feedback amplifier derives its accuracy. It is impossible to match the input and output stages of a buffer, so the CFA is not a high-precision circuit. We design the CFA for speed, and while the VFA usually tops out at about 400-MHz GBW, the CFA often reaches a GBW of several gigahertz. Later we discuss an exception to this rule, a special class of VFAs called wideband fixed-gain amplifiers (WFGAs). The CFA covers the frequency range from approximately 25 MHz to the low gigahertz area quite well.

A caution about using CFAs is mandatory. Many designers unconsciously depend on the decreasing gain versus frequency attribute of the VFA for stability because a circuit with a gain less than one is unconditionally stable. This CFA keeps its gain as frequency increases, thus it doesn't have a hidden stability advantage. Circuits that were stable with VFAs can become unstable when implemented with CFAs. Furthermore, the input lead and feedback resistor of a CFA is sensitive to stray capacitance, so the designer must be much more aware of the layout. Vendor evaluation boards are usually free, and they should be used for testing and as a layout example.

Figure 7. Notice the special decoupling used in a WFGA application





High-frequency amplifiers

High-frequency amplifiers are usually fixed-gain amplifiers. Most amplifiers in the low to tens of gigahertz range are hybrid amplifiers; i.e., the circuit is constructed from discrete transistors and passive components mounted on a substrate. This type of construction is costly; the cost reflects in the final selling price. Most hardware developers are willing to spend the extra money for a hybrid amp because the technology required to develop such an amplifier is expensive and hard to obtain.

WFGAs are a new IC product, and their secrets are not yet general knowledge. They use a special high-frequency process to obtain the high GBW required to make a circuit that functions in the gigahertz region. They also use nonstandard internal compensation techniques to obtain stability. These op amps are available in fixed circuit configurations with fixed gains, but their GBW goes up to 10 GHz, a dramatic increase in performance.

Any type of high-frequency amp needs a lot of tender loving care before it performs as advertised in the datasheet. The cautions given for CFAs apply here, along with the added advice to adhere strictly to the datasheet applications information.

Fully differential amplifiers (FDAs)

FDAs create and use fully differential signals. Many ADCs require a differential input signal to achieve maximum performance, and the FDA can easily convert a single-ended signal to a differential signal. Before the advent of the FDA, single-ended signals were converted to differential signals with the aid of the circuit shown in Figure 8.

A discrete single-ended to differential signal converter requires two op amps and a handful of matched resistors. This ends up being a difficult design job that is not cost-effective. An FDA simplifies the signal conversion job, and it offers other advantages like fewer components (see Figure 9).

Besides simplicity and low cost, the FDA provides for a common ground point determined by the ADC. Signals transmitted differentially force the noise coupled into the signals to be common to both inputs, thus the coupled noise is common-mode noise. The ADC or receiver rejects common-mode noise through its built-in common-mode rejection capability.

Figure 8. Traditional single-ended to differential converter circuit

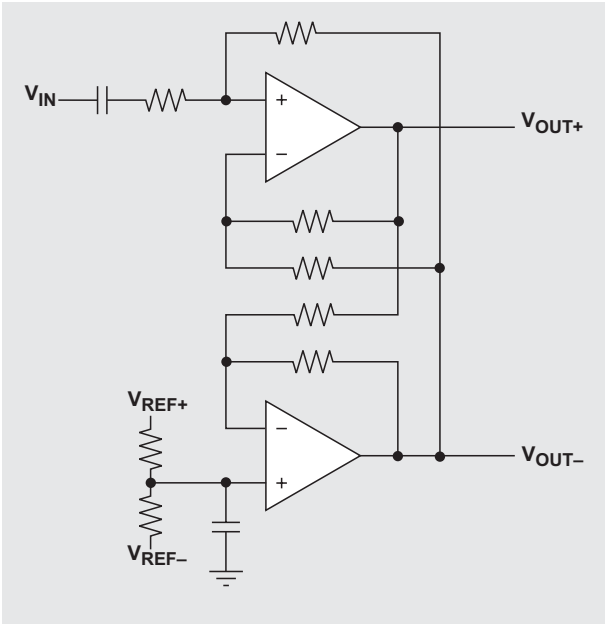
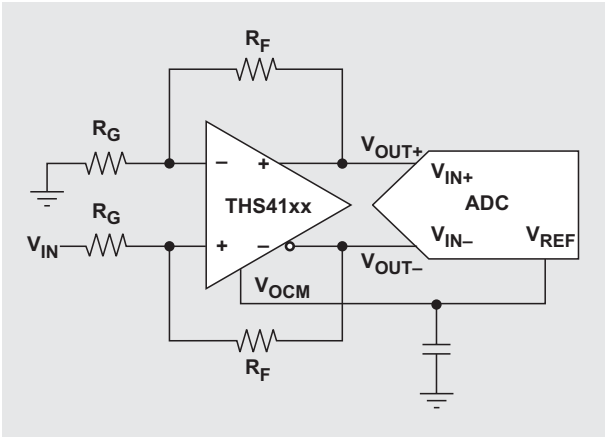


Figure 9. The FDA converts a single-ended signal to differential



Power amplifiers (PAs)

When an op amp has to deliver more than a few hundred milliamps at several volts, it is time to think of using a PA because PAs can handle large currents and voltages. PAs are not switching-type amplifiers; rather, they are linear amplifiers that are capable of handling large amounts of power. Making a power amp is not attaching the biggest heat sink possible to an op amp with the lowest thermal resistance. Heat sinks and thermal resistance are critical in PAs, but other functions like current sense, overload shutdown, and hooks for paralleling devices are very important (see Figure 10).

The new PA can handle considerable current for a precision op amp, but it has peripheral functions like current limit set, current monitor, parallel connections, enable, a current limit flag, and a thermal limit flag. Of course, there are PAs that can handle much more current at higher voltages, but the similar characteristics of the new devices are the bells and whistles.

Audio amplifiers

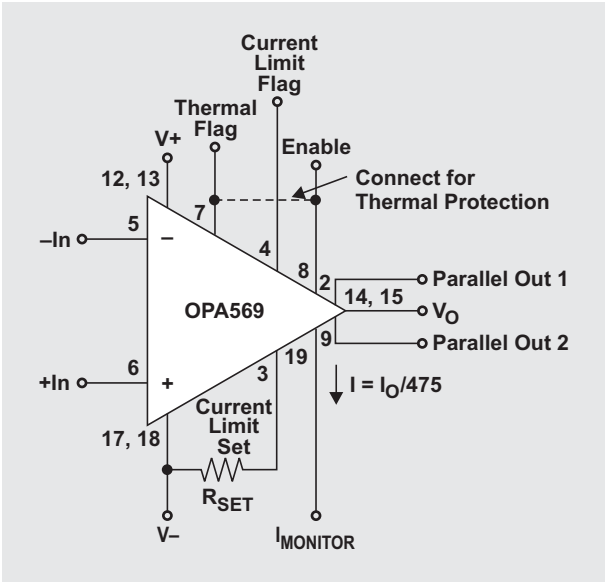
The volume of audio amplifiers is so high that there has been a special category for them since the 1950s. Most semiconductor manufacturers offer a line of audio amplifiers that ranges from simple op amps to involved switching power amps. Seek, and you shall find.

The next step

This discussion should get you into the specialty area that deals in the type of amplifiers you need to solve a problem. Naturally, you ask, "Where do I go from here?" The answer is to the Web. Any IC manufacturer worth doing business with has a Web site, and you can visit all the pertinent sites in a few hours. When you are on a site, look at the interesting ICs for problem solutions, but don't neglect the applications information.

Some IC manufacturers flood the engineer with applications information while others offer little or no applications information. This information often determines how quickly and completely you can do your job. If you don't know about decoupling capacitors or thermal runaway, the hardware mistakes you make will teach you; but if you read about these phenomena in the applications section, you can avoid designing them into the hardware. The choice of manufacturer is yours and shouldn't be influenced by applications information unless the choice is even or you don't want to stray too far from the source of knowledge.

Figure 10. The new breed of power amplifier does more than handle power



References

1. Ron Mancini, *Op Amps for Everyone* (Newnes Publishers, 2003). An earlier 2002 edition is available at www-s.ti.com/sc/techlit/slod006
2. Ron Mancini, "Worst-case circuit design includes component tolerances," *EDN* (April 15, 2004), pp. 61–64. Also available online at www.edn.com/article/CA408380.html

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/OPA569
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