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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Operating multiple oversampling data converters

By Joe Purvis (Email: j-purvis1@ti.com)
Data Acquisition Products

The secret is in the timing

Frequently it's important to arrange or predict a series of events in order to achieve a successful result. A nontrivial example is that of a pedestrian safely crossing a busy road. In this case the pedestrian may have to perform a number of estimated measurements in parallel. The speed and direction of any cars, for example, should be monitored throughout the process until the pedestrian safely reaches the other side of the road. The technique in this case is essentially to ensure that the pedestrian's x, y, and t coordinates do not correspond to any vehicle's x, y, and t coordinates. If all three coordinates were the same, then the pedestrian would have a problem.

Similarly, in many control situations it is often essential to know the value of more than one property of an event at a specific instant in time. When various values of a property need to be known concurrently, this is typically referred to as "simultaneous sampling."

For example, in seismic applications, the vibrations from controlled explosions can be sensed and measured. Vibrations in the x, y, and z planes should be recorded at the same time for more precise measurements and simpler data analysis.

Elsewhere, it may be important to monitor the same physical variable simultaneously. For example, in automobile braking systems it's important to measure the torque for each wheel to enable the car's onboard computer to decide if the car is skidding and what appropriate action to take.

A final example where simultaneous sampling is useful is in spacecraft sensors. The Galileo spacecraft, for instance, launched a probe into the Jovian atmosphere in September 2003. The probe had around 60 minutes to make its measurements and transmit data before the extreme atmospheric pressures crushed it. As the spacecraft descended, it was important to know the depth to which it had descended and at the same time the pressure being exerted upon it, the outside temperature, and perhaps the magnetic field strength.

Oversampling trap

Oversampling data converters generally have better ac and dc specifications than those based on a successive approximation register (SAR). But SAR converters do have one fundamental advantage; namely, on command from the host, they can complete and deliver one measurement.

By comparison, oversampling architectures rely upon averaging repeated coarse measurements before arriving at a final value. The architecture details are beyond the scope of this article, but it's essential to appreciate this point to successfully use oversampling converters.

Seeing double

The Oxford English Dictionary's definition of "simultaneous" is given as "occurring, existing or operating at the same time." However, this definition is unsatisfactory in real applications. Typically, in the real world, the user may want to measure two, three, or more properties of an event within the same space of time. Doing this, as with any time-domain data conversion, quantizes the continuous analog value into a series of discrete data values. However, it also quantizes the measurements to specific instants of time. This is the "space of time" that the user determines is adequate for the purpose of the measurements to be made. In oversampling systems, time quantization is determined by the MCLK used. Later in the conversion process, through various averaging processes, the data rate is essentially slowed down.

Data transfer principles

The preliminary details in support of this article are contained in Reference 1. It is recommended that the reader should first read this application report to gain an understanding of the device's operation.

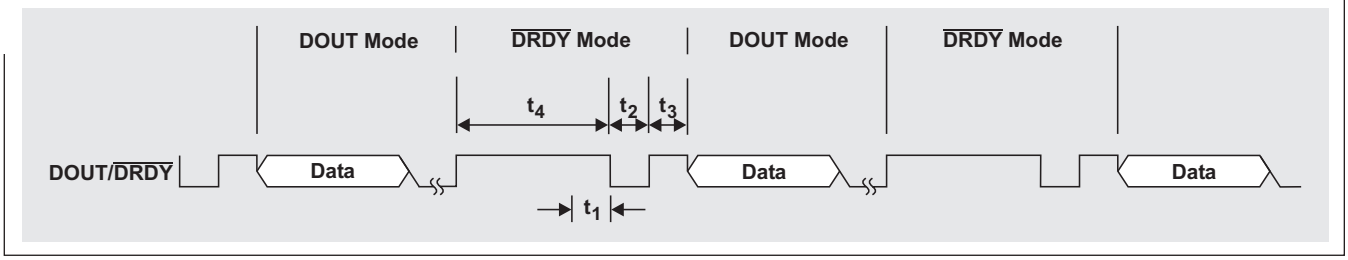
Modulator clock (MCLK)

The MCLK applied to the ADS1252 ADC is the principal driver used to set the characteristics of the ADC. The two properties that MCLK provide are the frequency response of the ADC and the frequency at which the ADC indicates that new data is available.

The MCLK period (τ_{MCLK}) is defined as

$$\tau_{MCLK} = \frac{1}{MCLK}. \quad (1)$$

Figure 1. $\overline{\text{DRDY}}$ and DOUT phases of MCLK cycle



Digital interface

To briefly recap the operation of the digital interface from the datasheet, there is only one data output pin. The function of this pin is multiplexed between DOUT and $\overline{\text{DRDY}}$. A complete conversion consumes 384 MCLK cycles. The cycle is divided into two phases (Figure 1).

The first phase of the cycle is known as $\overline{\text{DRDY}}$ mode. Following the t_{DOUT} time, the rising edge of the DOUT/$\overline{\text{DRDY}}$ signal indicates that new data will be available in 36 MCLK cycles. During this time the data output register is updated. This signal is connected to an interrupt pin on the host system.

The second phase of the cycle is known as DOUT mode. During this time the user can safely read the converted data at a clock rate determined by the shift clock (SCLK).

Discussion of a 5-ADC system

Let's consider a system that requires 5 variables to be measured simultaneously. We can summarize what this situation would look like over 2 complete cycles, as shown in Table 1.

The operation can be described as follows:

1. $\overline{\text{DRDY}}$ mode—The first rising edge of DOUT/$\overline{\text{DRDY}}$ indicates that new data will be available in 36 MCLK cycles.
2. DOUT mode—Since there are 5 ADCs in this example, the data from each of these devices must be read sequentially.
   - The data stored within ADC1 is clocked out of the device with a dedicated SCLK signal, SCLK1. During this time SCLK2, SCLK3, SCLK4, and SCLK5 should remain LOW (inactive).
   - The data stored within ADC2 is clocked out of the device with a dedicated SCLK signal, SCLK2. During this time SCLK1, SCLK3, SCLK4, and SCLK5 should remain LOW (inactive).
   - The data stored within ADC3 is clocked out of the device with a dedicated SCLK signal, SCLK3. During this time SCLK1, SCLK2, SCLK4, and SCLK5 should remain LOW (inactive).
   - The data stored within ADC4 is clocked out of the device with a dedicated SCLK signal, SCLK4. During this time SCLK1, SCLK2, SCLK3, and SCLK5 should remain LOW (inactive).
   - The data stored within ADC5 is clocked out of the device with a dedicated SCLK signal, SCLK5. During this time SCLK1, SCLK2, SCLK3, and SCLK4 should remain LOW (inactive).

To provide a coherent basis within which the measurements are made, all the ADCs share the same MCLK. This provides two important advantages:

- It requires that the measurements from all ADCs be made within the same duration of time (simultaneously sampled).
- It provides the user with confidence in knowing exactly when data from any ADC is available. In a multiple-ADC system this is significant, since we can be certain that when data is signaled as available for any ADC it will be available for all ADCs. The consequence of this is that the system and software can be simplified by connecting only one interrupt pin and writing only one interrupt service routine to read data from 5 converters.

Table 1. Measuring 5 variables simultaneously

2 CONVERSION CYCLES											
1 CONVERSION CYCLE						1 CONVERSION CYCLE					
MODE						MODE					
$\overline{\text{DRDY}}$	DOUT					$\overline{\text{DRDY}}$	DOUT				
36 MCLKs	348 MCLKs					36 MCLKs	348 MCLKs				
$\overline{\text{DRDY}}$	ADC1					$\overline{\text{DRDY}}$	ADC1				
		ADC2						ADC2			
			ADC3						ADC3		
				ADC4						ADC4	
					ADC5						ADC5

An additional benefit of this architecture is that, since all ADCs complete a conversion at the same time, the host system can choose to read the data in any particular order. In some cases it might read data sequentially, starting with ADC1 data and ending with ADC5 data. In some cases it might read data in reverse order; and perhaps in some other situations it might always read data from ADC1, ADC2, and ADC3 data but read ADC4 and ADC5 data only under special circumstances.

A tale of 2 clocks

Regardless of the number of ADCs, the same principle of DOUT/$\overline{\text{DRDY}}$ time must still be adhered to for the ADS1252.

In general, for n data converters, the time allocated for DOUT mode can be expressed in seconds as

$$t_{DOUT(n)} = \frac{348 \times \tau_{MCLK}}{n}. \quad (2)$$

The maximum MCLK for the ADS1252 is specified as 16 MHz. Therefore τ_{MCLK} is 62.5 ns, and t_{DOUT} can be rewritten in seconds as

$$t_{DOUT(n)} = \frac{21.75 \times 10^{-6}}{n}. \quad (3)$$

As the number of ADCs sharing the same MCLK increases while the $\overline{\text{DRDY}}$ period stays the same, the data from each ADC must be accessed faster.

Table 2 indicates how fast SCLK must be to keep pace with the DOUT/$\overline{\text{DRDY}}$ cycle.

Table 2. SCLK speed required to keep pace with DOUT/$\overline{\text{DRDY}}$ cycle

NUMBER OF ADCs	t_{DOUT} (µs)	SCLK (MHz)
1	21.750	1.1
2	10.875	2.2
3	7.2500	3.3
4	5.4375	4.4
5	4.3500	5.5

To receive the complete 24 bits from each ADC requires 3 × 8-bit accesses, or 24 SCLKs in total. Therefore, to be able to access the data from 5 ADCs requires a time of 5 × 24 SCLKs. It is the user's responsibility to ensure that all accesses are complete before the next $\overline{\text{DRDY}}$ time begins.

An alternative approach would be to verify the maximum speed offered by the host system for SCLK (for example, 2 MHz) and then determine how long it would take to transfer 24 bits of data at that clock speed. This would determine the maximum MCLK frequency that could be used. In a multiple ADC system, if the MCLK is faster than the calculated maximum, there will not be enough time for the host to read the data before the ADC switches from DOUT mode to $\overline{\text{DRDY}}$ mode.

For example, if τ_{SCLK} = 500 ns, then 24 × τ_{SCLK} = 12 µs, for 24 bits of data. This indicates that it will take at least 12 µs to clock the data out of any ADC (this sets t_{DOUT}). Consequently, if there are 5 ADCs sampling data synchronously, it will take at least 5 × 12 µs (60 µs) until the system can read the first ADC again.

Therefore, according to Equation 2, the maximum MCLK will be 5.8 MHz.

This reasoning can sometimes become clearer if we consider the contrary position. For instance, in the preceding example, if the MCLK is faster than 5.8 MHz—say, 10 MHz—this means that t_{DOUT} is 34.8 µs (348 × 100 ns). If, during this time, 5 ADCs are expected to send data to a host system, each ADC can send data for only 6.96 µs. So each ADC has 6.96 µs to transfer 24 bits of data. If one bit of data is transmitted on successive SCLK edges, then τ_{SCLK} = 6.96 µs/24 = 290 ns; therefore, SCLK is $1/\tau_{SCLK}$ = 3.45 MHz. Since the SCLK frequency sourced by the SPI ports of many microprocessors is limited to around 2 MHz, it is an important parameter to check in the host system's specification during the design phase.

The ADS1252 can support SCLK rates of up to 16 MHz.

Slowing things down

Considering the case when MCLK is 32.768 kHz, we can determine t_{DOUT} and SCLK as given in Table 3, since τ_{MCLK} is now 30.5 µs.

The software example given in this article is for a 2-ADC system using a 32.768-kHz modulator.

Table 3. Determination of t_{DOUT} and SCLK when MCLK is 32.768 kHz

NUMBER OF ADCs	t_{DOUT} (ms)	SCLK (µs)
1	10.61	442.1
2	5.31	221.3
3	3.53	147.1
4	2.65	110.4
5	2.12	88.3

HPA449

The HPA449 development card is available directly from Softbaugh (www.softbaugh.com). This MSP430 evaluation board allows you to experiment with TI data acquisition products using the MSP430F449.

The MSP430F449 possesses two SPI ports. Both these ports are mapped and available for use on the HPA449. This structure makes it easy to demonstrate the principles of using oversampling converters to design a 2-ADC system. However, the principles can be scaled to more than 2 ADCs as previously discussed.

Figure 2 shows the block diagram of the system. Notice that only one interrupt pin is required regardless of the number of ADCs connected in parallel. Since all ADCs share the same MCLK, they will all provide the same characteristic DOUT/$\overline{\text{DRDY}}$ signal at the same time. All the HPA449 requires is an indication of when the data is available; it's then up to the MSP430 and the software to schedule when to read the data.

Figure 3 is a composite of two adjacent screen captures showing CLKX_A, DR_A, CLKX_B, and DR_B.

Summary

This article has discussed some of the important factors to consider when oversampling data converters are used to design a simultaneously sampling system.

For this type of design to be successful, the MCLK for each ADC must be shared. This assures that each converter is truly sampling the inputs concurrently. It also has the added benefits of simplifying the digital interface, since only one interrupt pin is required regardless of the number of ADCs in the system.

However, a significant limitation is that there is a fixed amount of time available—348 MCLK periods—to read the converted data. After this fixed time, the data output register is updated with a new data word regardless of whether or not the data has been read.

The converted data is read from the device with an SCLK generated via the host system. There is no direct relationship between MCLK and SCLK, but the user should be aware that if the data is not shifted out of the ADC quickly enough, t_{DOUT} time will expire and the data read back will be a meaningless mixture of old and new data. This should be carefully considered, particularly where multiple ADCs are concerned.

Finally, a simple 2-ADC example using the MSP430 was presented, showing that the DOUT/$\overline{\text{DRDY}}$ modes for both ADCs are identical when the same MCLK is used. Simply ensuring that only one SCLK signal at a time is active arbitrates for which ADC sends data back to the microcontroller.

Figure 2. Block diagram of 2-ADC system using MSP430F449

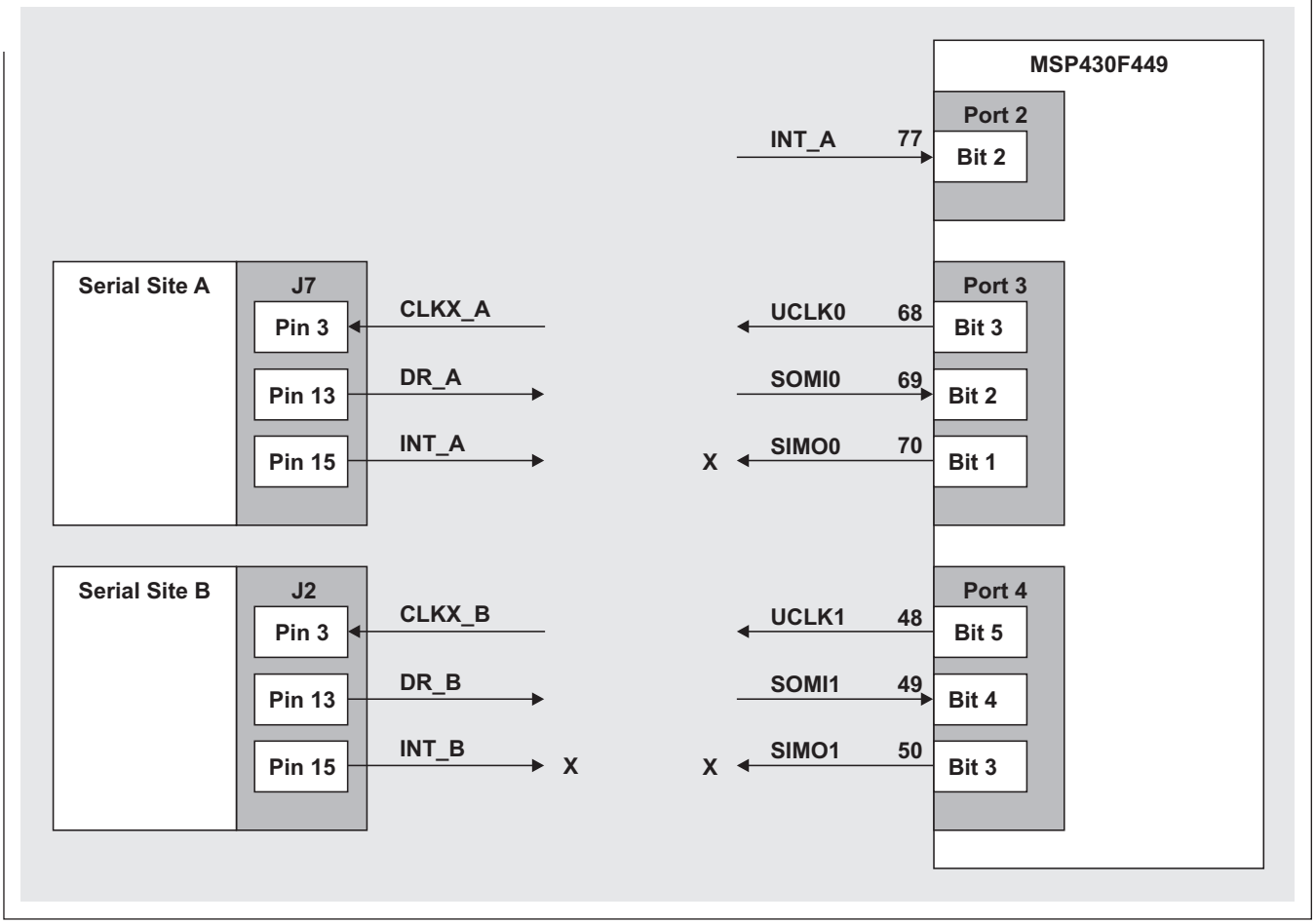
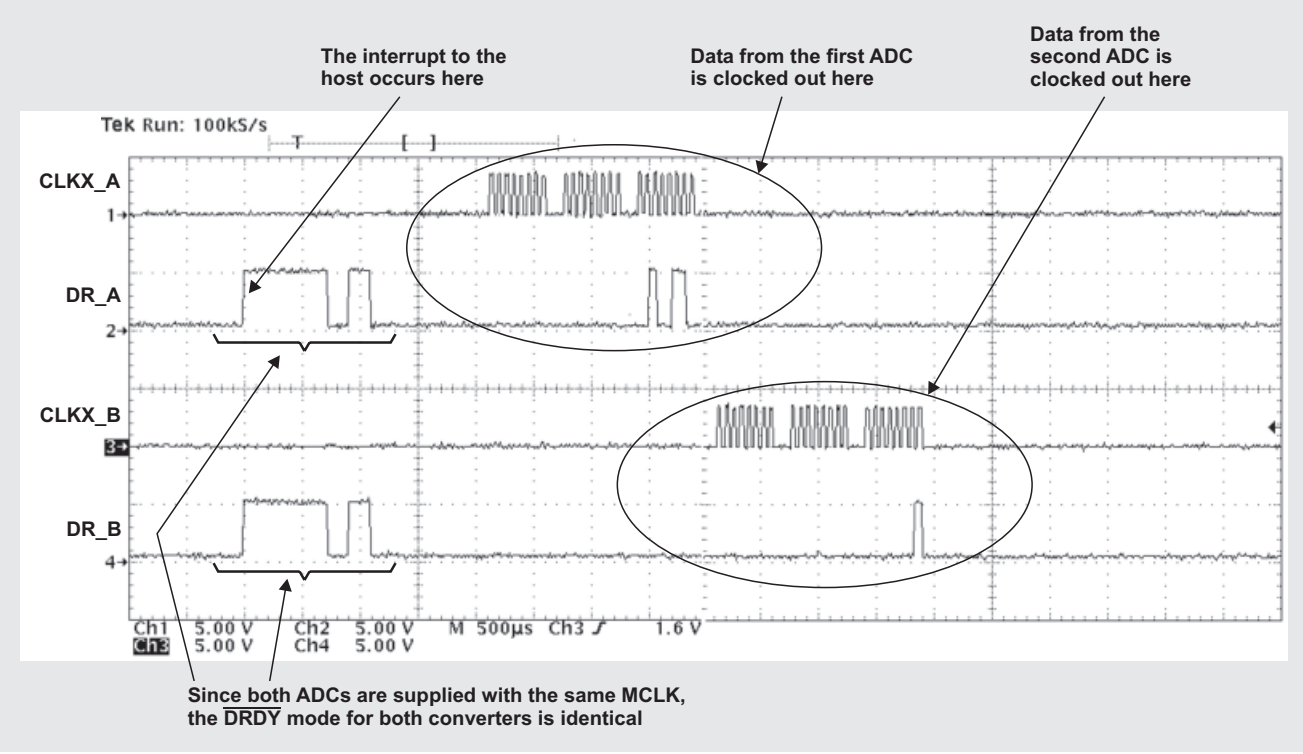


Figure 3. Composite of two adjacent screen captures showing identical $\overline{\text{DRDY}}$ modes for ADCs using the same MCLK



Reference

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Document Title **TI Lit. #**

1. "Interfacing the ADS1251/52 to the MSP430F449," Application Report slaa242

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Low-power, high-intercept interface to the ADS5424 14-bit, 105-MSPS converter for undersampling applications

By Michael Steffes, *Market Development Manager, High Speed Signal Conditioning* (Email: steffes_michael@ti.com), **and Xavier Ramus,** *Applications Engineer, High Speed Signal Conditioning* (Email: x-ramus2@ti.com)

With the advent of very highly linear ADC input stages, parts like the ADS5424 can deliver >75-dBc spurious-free dynamic range (SFDR) for two-tones at 170 MHz. The last-stage interface to this converter then needs to be better than 80-dBc two-tone SFDR to take full advantage of this exceptional performance in the converter itself. Until recently, the only amplifier solutions that have met this demanding performance level have been very high-power RF amplifiers, typically using >1.5 W to reach >80-dBc SFDR levels. A much lower-power alternative has recently emerged using the THS4509. This wideband fully differential amplifier, along with a number of external design tricks, can support this last-stage interface requirement using <200 mW of total power. This article steps through the design, measurement techniques, and resulting performance levels required to provide >80-dB SFDR at up to 170 MHz in support of the ADS5424.

Converter two-tone undersampling performance

Numerous applications are asking high-speed ADCs to deliver very high SFDR for narrowband applications at the various intermediate frequencies (IFs) used in communications. These include applications at 44 MHz, 70 MHz, 140 MHz, and 170 MHz. Recent converter introductions (such as the ADS5424) have done a very good job of meeting >80-dBc SFDR at the lower IFs and even >75-dBc SFDR at 170 MHz. Figure 1 shows a plot from the datasheet (Reference 1) of a two-tone SFDR for the ADS5424 at 170-MHz center frequency.

In this test, the converter is sampling at 92.16 MHz on a two-tone input at 169.6 MHz and 170.4 MHz. The input frequencies are falling in the fourth Nyquist zone and are folded to the difference between 4fs/2 and 170 MHz, giving the 14-MHz fast Fourier transform (FFT) output shown in Figure 1. Each tone here is at –7 dBFS so that the combined two-tone envelope sums to a –1-dBFS maximum. The full-scale input voltage for the ADS5424 is a 2.2-V_{PP} differential, giving a –1-dBFS level of 1.96 V_{PP} with each tone then at 0.98 V_{PP}. The converter plot report shows IMD3 = –82 dBFS, where this is the absolute level below 0 dB in Figure 1. The difference between each carrier level and the third-order intermodulation spurious signal level is more commonly used for amplifiers. To translate the converter specification to something that is comparable to amplifier specifications, subtract 7 dB from |IMD3|, just given, resulting in a 75-dBc third-order SFDR for the converter. This exceptional performance is the difference between the carrier level and the average spurious signal level at a 170-MHz center frequency. The converter is also generating another cluster of spurs near 42 MHz, but it is the close-in third-order intermodulation terms that are of interest in developing an amplifier interface compatible with this level of ADC performance.

Figure 1. Two-tone SFDR for the ADS5424 at 170-MHz ±400-kHz input frequencies

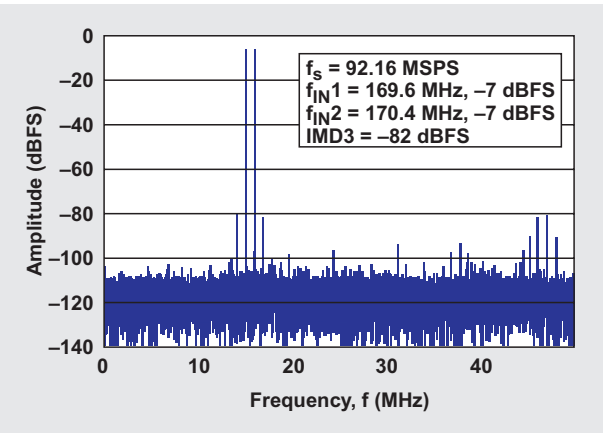
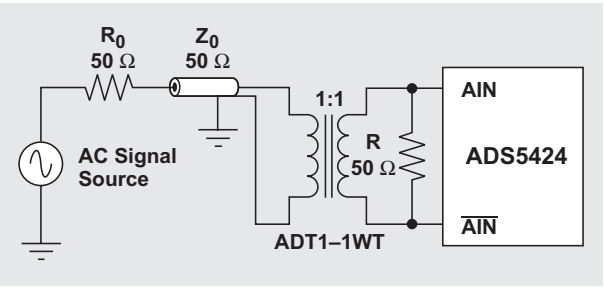


Figure 2. Simple characterization circuit for the ADS5424

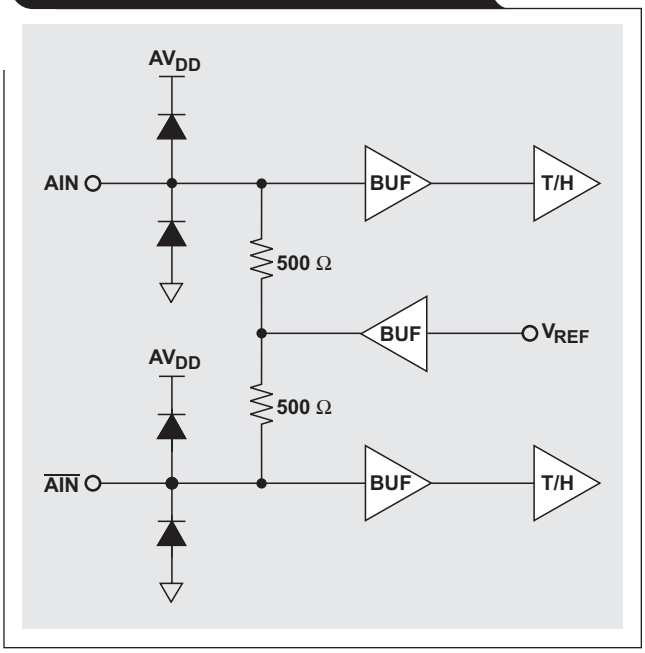


The test interface to get this plot for the converter is quite specific and depends on very high-quality sources (from a phase-noise standpoint) with moderate linearity. Each source is heavily filtered before the power combiner then drives the signal into a 1:1 transformer to get the differential converter input signal. This simple interface is shown in Figure 2 (from Reference 1), where the real magic is in getting the element called "AC Signal Source."

The input signal during the converter test is so heavily filtered that it is considered spurious-free.

One of the really nice features of the ADS5424 is that the differential input provides its own common-mode reference voltage and resistive termination, which then drive on-chip buffers prior to the sampling element. Figure 3 shows the analog input stage for the ADS5424. V_{REF} is sitting at 2.4 V when the power supply is +5 V on the analog portion of the ADS5424.

Figure 3. Differential analog input for the ADS5424



Target distortion levels for the last-stage interface to the ADS5424

Now we must estimate a target SFDR for the signal coming into the converter to hit some level of system performance. Imagine a two-tone input signal that has its own set of close-in spurious tones being presented to the converter input. The converter will process the fundamental tones to generate the converter spurious power levels shown in Figure 1. The spurious tones presented at the input are also processed by the converter as a signal and passed on to the FFT output combined with the converter-generated spurious signals at the same frequency. A worst-case assumption, which actually has been shown to hold true at lower frequencies, is that these spurious tones add in phase. For instance, the –82-dBFS close-in spurs of Figure 1 imply a spurious signal of 2.2 $V_{PP} \times 10^{-82/20}$ = 175 μV_{PP}. If the input signal also has this same level of third-order spurious tones (which would be falling at 170 MHz ± 3 × 400 kHz), the final FFT output would have 2 × 175 μV_{PP} = 350 μV_{PP} in the FFT, or –76-dBFS worst-case. So, providing an input signal with the same two-tone SFDR as the converter results in a combined 6 dB worse than the converter alone. This is normally not acceptable, suggesting that the SFDR for the signal coming into the converter must be much higher than that of the converter itself to minimize degradation in system performance. While this may be a worst-case assumption, it will set a target for the amplifier performance. Equation 1 shows the combined SFDR calculation when the spurious signal levels are adding in phase.

$$SFDR_{System} = -20\log\left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}}\right) \quad (1)$$

SFDR, a positive number, is the difference in dBc between the carrier and the close-in spurs.

In Equation 1 we must enter the SFDR defined in the same way. For instance, from Figure 1, the ADC has a 75-dBc SFDR. If the signal to the converter has an $SFDR_{Amp}$ of 82 dBc, then the combined $SFDR_{System}$ will be 71.8 dBc. This approximate 3-dB degradation requires an input signal with an SFDR at least 7 dB better than that of the converter. Equation 1 can also be solved for the required $SFDR_{Amp}$ to hit a target $SFDR_{System}$:

$$SFDR_{Amp} = SFDR_{ADC} - 20\log\left(10^{\frac{\Delta}{20}} - 1\right), \quad (2)$$

where Δ is the desired drop in SFDR. With Δ defined as a positive number, Equation 2 will add to the $SFDR_{ADC}$ to get the amplifier target. Note that this calculation is independent of the starting level for $SFDR_{ADC}$. For instance, a 1-dB drop requires the amplifier to be 18.3 dB better than the converter regardless of the starting point for the converter. An exact 3-dB drop would require the input signal to have an SFDR 7.7 dB better than that of the converter itself.

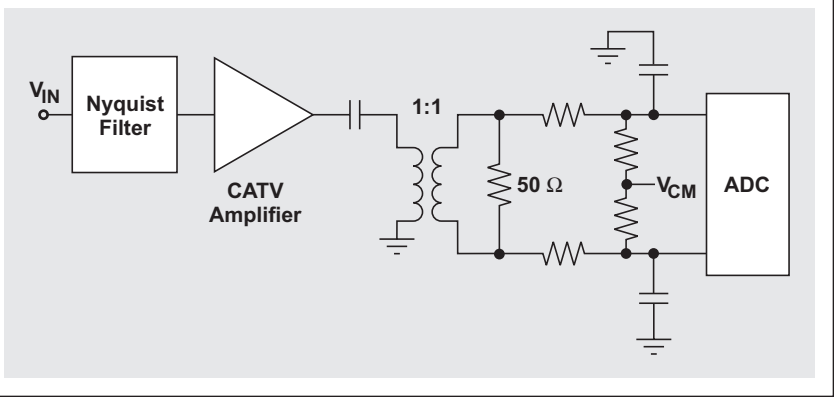
Typical amplifier solutions

Since most designs are converting to differential in the last stage, a typical design would use a very low-distortion RF amplifier driving a transformer. This has worked reasonably well in the past but typically requires in excess of 1.5 W in the amplifier to suppress its spurious signals to the levels

calculated earlier. A typical interface, shown in Figure 4, bears a marked resemblance to the converter test circuit.

This design is encumbered by two issues that require very high-power dissipation in the amplifier to achieve the desired linearity. The first issue is that the full-scale converter input is required at the amplifier output, since there is no further gain to the converter input. Some step-up in the transformer can be used to reduce this swing, but high turns ratios run into a band-limiting problem in the transformer. The second issue is that the single-ended output of the amplifier is not taking advantage of the even-order suppression available in a differential design. It is much tougher to get even-order suppression single-ended, again leading to very high-power dissipation in the amplifier. While the discussion thus far has focused on third-order intermodulation, the second-order and higher harmonics have to be dealt with at some point. Taking a single-ended signal path to differential at low-power level, then providing the final gain stage in a very balanced differential design, will go far towards removing the even-order terms as a limit to dynamic range. With the cost of one more transformer, all these problems go away and a much lower-power, very high-SFDR design can be delivered with the THS4509.

Figure 4. Single-ended amplifier driving a last-stage transformer

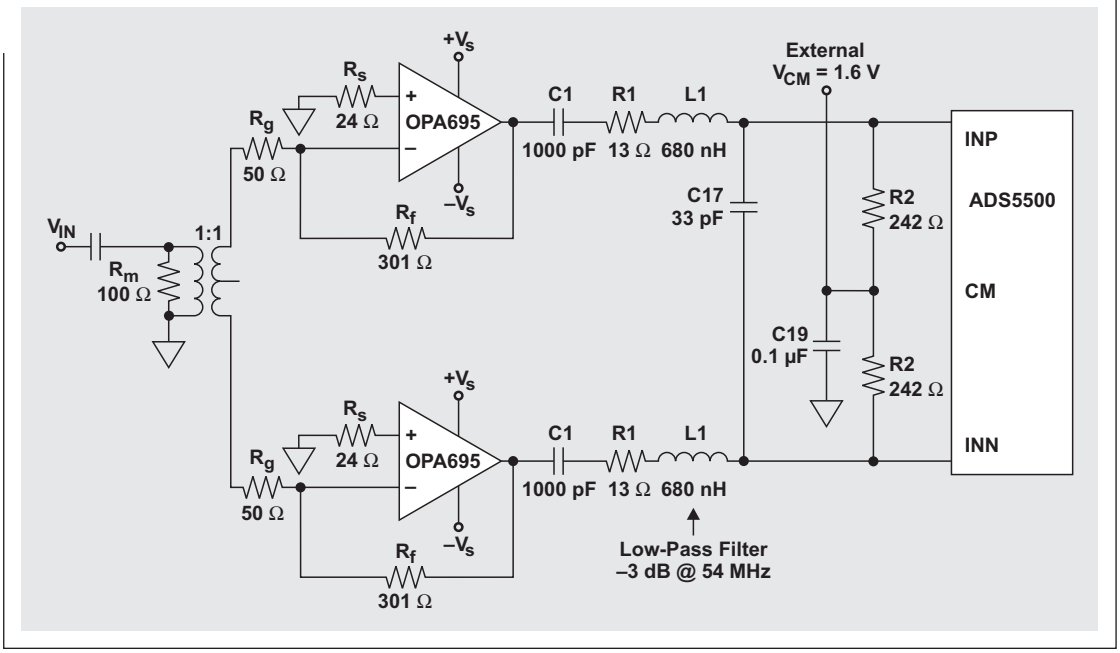


Low-power ADC interface with exceptional SFDR

Moving the transformer to the input of a balanced differential interface allows the final single-ended amplifier driving that transformer to operate at a much lower power level. Normally, every dB of reduction in fundamental power level will reduce the even-order harmonics by 2× and the third-order harmonics by 3×. For instance, if an arbitrary single-ended amplifier is driving the full 2 V_{PP} at its output (10 dBm) and delivering –70-dBc second-order and –80-dBc third-order harmonics, dropping its output level by 20 dB to –10 dBm will drop the second-order harmonic down to –90 dBc and the third-order to –120 dBc. This is why moving the single-to-differential conversion upstream in the signal path can move the SFDR limit to the final stage, where running differentially has numerous advantages.

Figure 5 shows some earlier work in this topology where a very wideband current feedback amplifier, the OPA695, was used. This example was intended for the first Nyquist zone and included a second-order low-pass filter at the output to limit the noise-power bandwidth (see Reference 2).

Figure 5. Example input transformer-based circuit using the OPA695



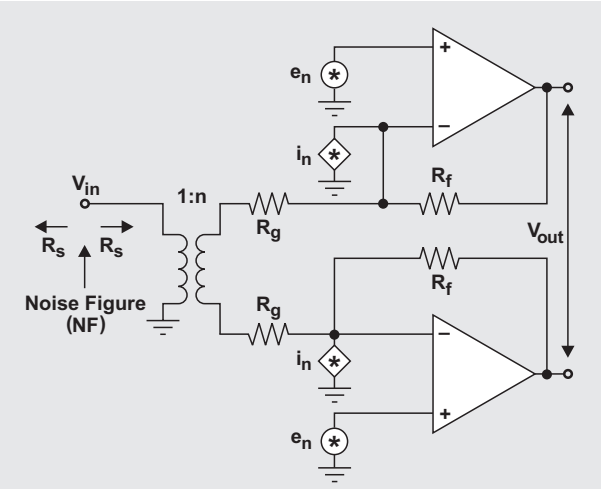
Adding a transformer to the input can improve dynamic range (reduce noise and distortion at the converter input) in at least three different ways.

1. The transformer provides a noiseless and distortionless signal conversion from single-ended to differential. This is very useful for ac-coupled signal requirements.
2. The signal gain from the transformer secondary is greater than the gain for the amplifier's voltage noise. This has the effect of reducing the contribution at the output for the amplifier's input voltage noise, or, equivalently, attenuating the amplifier input voltage noise contribution to the total noise when it is input-referred to the signal input at the transformer primary.
3. Similarly, if the amplifier is a voltage feedback device (like the THS4509, but not the OPA695), this reduced noise gain versus achieved signal gain also increases the loop gain for the amplifier. Increased loop gain will, all other things being equal, reduce harmonic distortion at the output.

The transformer interface of Figure 5 used a 1:1 transformer where a 50-Ω input match was desired. This was achieved with 100 Ω on the input side and two 50-Ω resistors on the secondary, where those reflect back to the input side as their sum—again, 100 Ω. A more general low-noise development (shown in Figure 6) would let the turns ratio be adjustable, eliminate the 100 Ω on the input side, and simply set $2R_g$ to get the required input impedance. The impedance looking out of the transformer secondary is the sum of the two R_g resistors, since the inverting amplifier inputs are assumed to be low-impedance points.

Then, with R_g set, R_f would be selected as needed to get the desired gain. Figure 6 shows the simplified circuit used to develop the noise figure (NF) equation (Equation 3) for this inverting-input, transformer-coupled design.

Figure 6. Noise figure analysis circuit

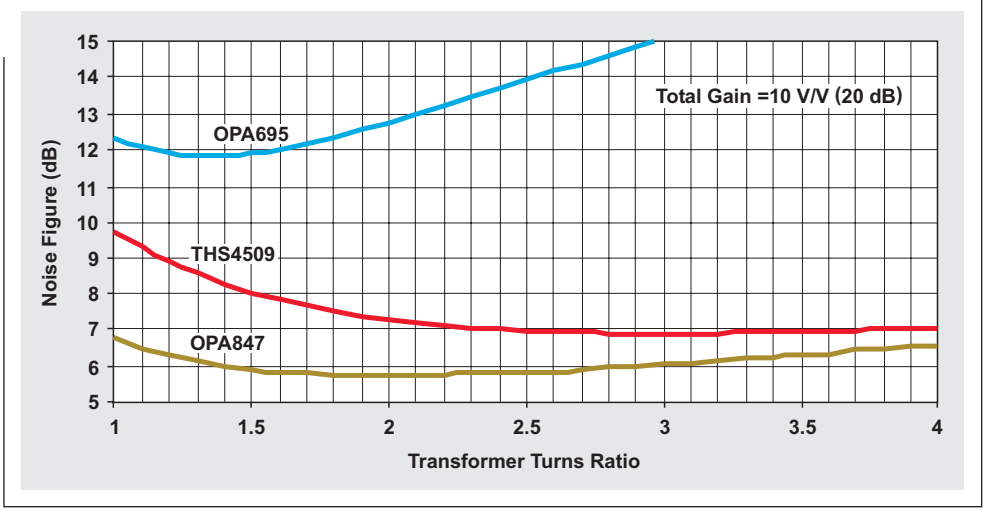


To get an input match, define $\alpha = R_f/R_g$ and set $R_g = \frac{1}{2}n^2R_s$, where n is the turns ratio and n^2 is the impedance ratio. Then $V_{out}/V_{in} = n\alpha \equiv A_v$, and R_f will be $(A_v/2)nR_s$.

While not shown in Figure 6, all the resistor noise terms are included in this analysis. Since R_g and R_f are so constrained by the input impedance and target gain requirements, they drop out explicitly from the total NF expression of Equation 3 but are effectively picked up by the 2+4/α term:

$$NF = 10\log\left(2+\frac{4}{\alpha}+2\left\{\left[\frac{e_n\left(\frac{1}{2}+\frac{1}{\alpha}\right)}{n}\right]^2+\frac{1}{2}\left(i_b nR_s\right)^2\right\}\div kTR_s\right). \quad \textbf{(3)}$$

Figure 7. Input noise figure vs. turns ratio with fixed total gain for the circuit in Figure 6



It is interesting to sweep the turns ratio and recompute the noise figure while holding a fixed target gain. Figure 7 does this for the OPA695, the THS4509, and the lowest-noise Texas Instruments op amp, the OPA847. While the THS4509 is a fully differential amplifier and not strictly an op amp, the analysis model in Figure 6 shows two equal voltage-noise sources (e_n) at the input that are equal to the THS4509 specified voltage noise divided by $\sqrt{2}$.

All of these devices show a shallow minimum where going from a 1:1 turns ratio to some higher input turns ratio will improve NF. The OPA695 gets worse at higher turns ratios due to the dominant output noise term coming from its relatively large inverting current noise. That term becomes dominant at low amplifier gains—which is what happens in this analysis as the turns ratio increases for a fixed target total gain.

Table 1 summarizes the noise terms used in Equation 3 to generate Figure 7 (with R_s = 50 Ω and kT = 4×10^{-21} J). Recall that the THS4509 input noise used here is the actual specification divided by 1.41 to share that single input noise voltage in the two inputs used in the analysis model of Figure 6.

Table 1. Noise terms used in Equation 3 to generate Figure 7*

DEVICE	e_n (nV)	i_n (pA)
OPA847	0.8	2.5
OPA695	1.8	22
THS4509	1.4	2.2

*R_s = 50 Ω and kT = 4×10^{-21} J

While this is an interesting mathematical exercise, it is important to consider other constraints that come into play over this turns ratio sweep. Specifically, as n>3 is used, the transformer will start to limit the bandwidth for high-IF applications. Also, letting R_f be completely driven from the target gain and required R_g value will quickly move it beyond its useful range. For the OPA695, letting R_f get too large will limit the bandwidth of the design. For the THS4509, letting R_f get too low will load the output, increasing distortion.

Tested design with the THS4509

Numerous efforts were made to find a working solution at 170 MHz that would not drop the ADS5424 two-tone performance of 75 dBc more than 3 dB. This gave an 82.7-dBc target for the amplifier SFDR with the analysis detailed earlier. Figure 8 shows the final configuration for just the amplifier portion of the circuit that has given the best results. A total gain of 10 V/V, or 20 dB, was targeted in these tests. Therefore, a –1-dBFS input to the converter requires a maximum input swing at V_{IN} of 200 mV_{PP}.

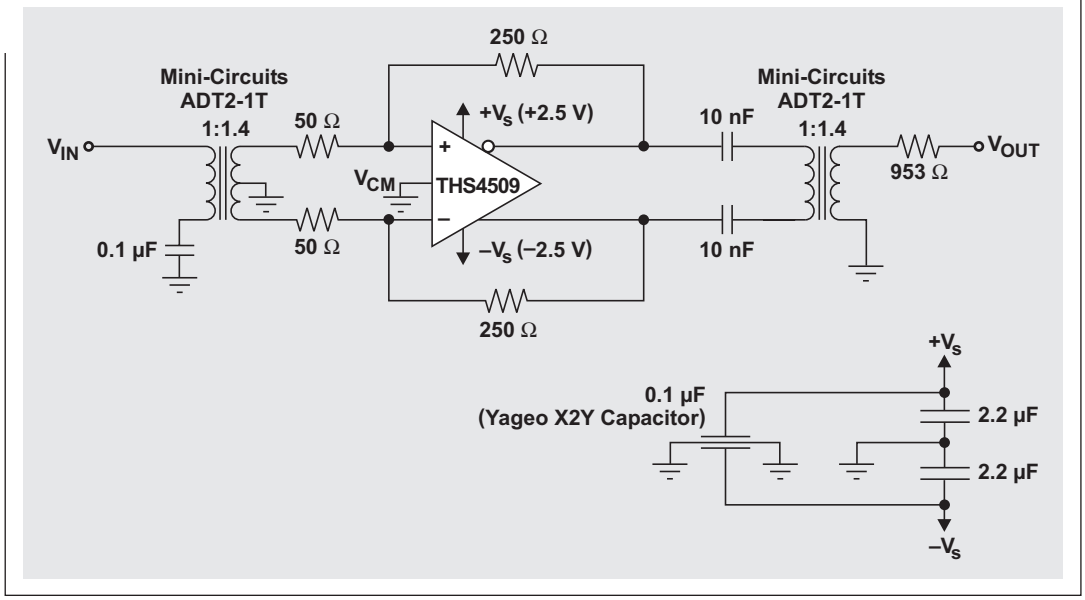
Early tests with just the input transformer did not meet the distortion targets. Reducing the amplifier gain by 1.4 and adding a 1:1.4 turns ratio output transformer helped both to improve the loop gain and to lighten the output swing requirement for the THS4509 so it can now meet the target.

The output transformer does not run doubly terminated, while the input transformer does provide a match to the source. It was assumed that the source needs to see a matched load for proper operation, while the output can (thus far) drive into the converter input impedance with no consideration of source matching. The output transformer provides 1.4-V/V gain that is removed from the THS4509 gain setting to still hit the target gain of 10 V/V.

We intended to test only the THS4509 with this test circuit to see if we could extend the performance to meet the SFDR target by using several design tricks:

1. This circuit runs completely differentially around ground. It does not use the internal common-mode loop (in an ac sense) in an effort to improve high-frequency linearity. The common-mode loop still controls the output common-mode voltage, but minimal dc, and hopefully no ac, current signal is required to do this for the implementation chosen.

Figure 8. Tested THS4509 circuit



2. Testing and design are simplified with ±2.5-V supplies. Putting both the input transformer centertap and the V_{CM} pin at ground should eliminate common-mode currents and signals.
3. The signal path is ac-coupled at both the input primary and the outputs of the THS4509, eliminating dc currents.
4. While the THS4509 provides a gain of 5 for each side of the differential input signal, its noise gain is somewhat lower. Reflecting the 50-Ω source through to the secondary as 50 Ω on each side [50 × $(\sqrt{2})^2$] and computing the equivalent noninverting gain, we get 1 + 250/100 = 3.5 V/V. This is high enough to ensure stability in the THS4509 but lower than the signal gain delivered, which should improve loop gain and hence distortion by a factor of 20log(5/3.5) = 3.1 dB over a simple noninverting stage gain of 5.
5. The final output drives out through a 953-Ω resistor to a 50-Ω spectrum analyzer. This is intended to emulate the 1-kΩ input impedance of the ADS5424. Reflecting that load through to the THS4509 outputs, we see what looks like a 500-Ω load across the outputs. Each output then sees half of this in parallel with the feedback element as a total load, or 125 Ω in Figure 8.
6. To get 2 V_{PP} at the transformer secondary (the required –1 dBFS for the ADS5424), $2/\sqrt{2}$ must be driven differentially at the THS4509 outputs. Dividing the result by 4 gives ±0.355 V on each output, which then drives 2.84 mA peak in each direction into the total equivalent load of 125 Ω.

The two-tone, third-order intermodulation test configuration is shown in Figure 9.

Two very low-phase-noise synthesized signal sources are used. One acts as the primary source and the other, along with the spectrum analyzer, is phase-locked to the primary. This allows very narrow frequency spans of where the spur should be. Notice that no filters are used here. The spectrum coming out of the mixer has numerous harmonics we don't care about—but nothing where the third-order intermodulation spurs should be. This test performed on a converter would always use filters for the signal sources, as the converter will fold the higher-order harmonics into the Nyquist zone—possibly falling on top of the spurious signal of interest.

Figure 9. Test configuration for two-tone, third-order intermodulation testing

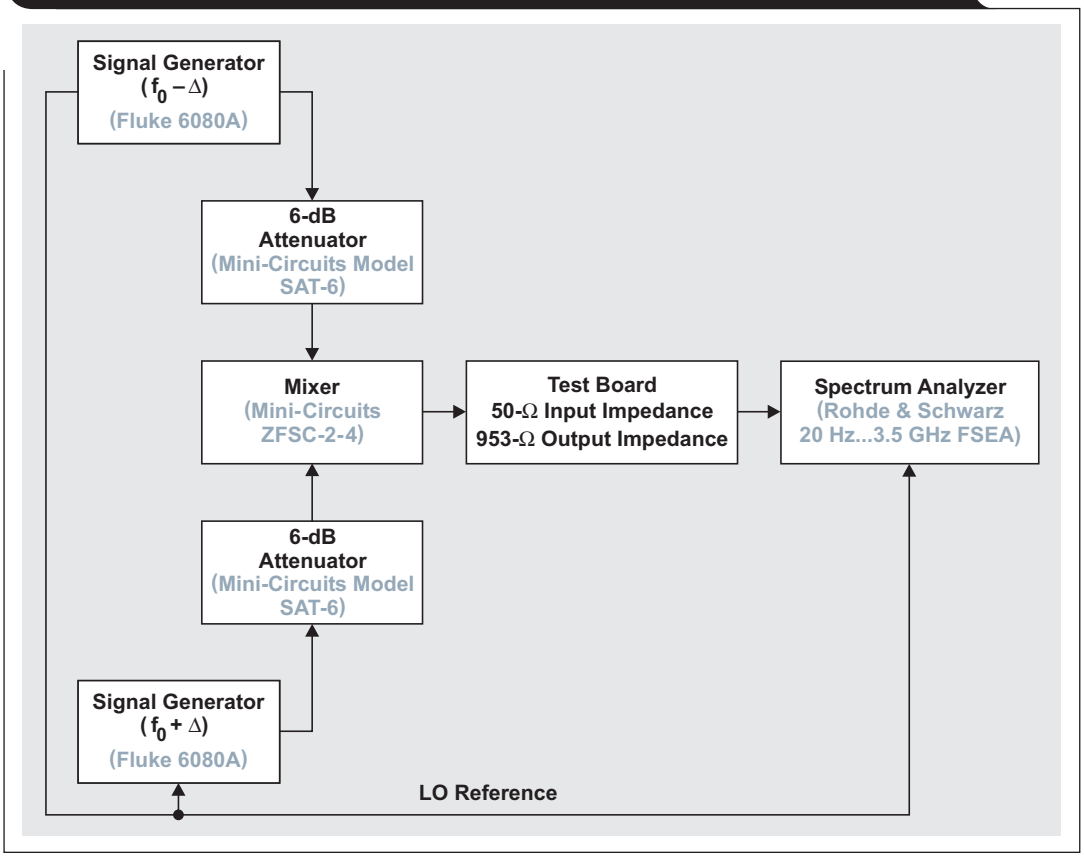


Figure 10. Measured third-order intermodulation spurious signal level

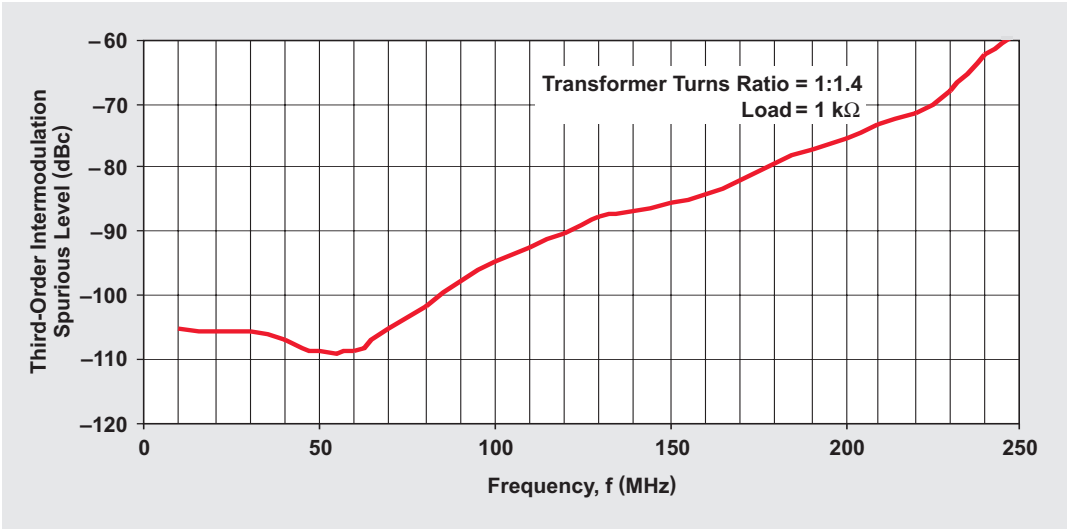
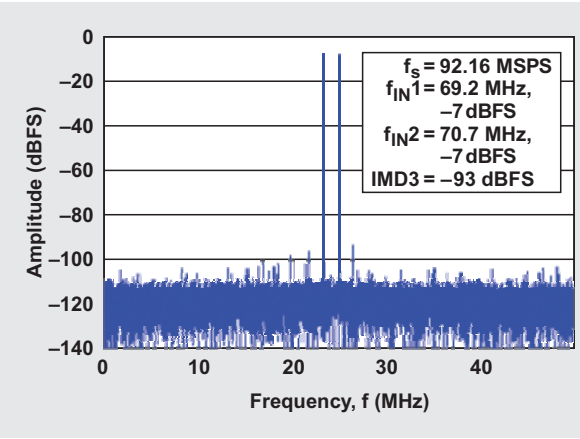


Figure 10 sweeps the center frequency (f_0) and reports the measured level of the close-in third-order intermodulation spurious signal. The SFDR is the negative of the numbers plotted.

This data not only shows the main target of –83 dBc at 170 MHz but also exceptional performance at lower frequencies. To make these lower-frequency measurements, a 4-V_{PP} output test was used, and the spurious level was projected at 2 V_{PP} with an intercept model. Figure 11 shows that at 70 MHz the ADS5424 has a two-tone SFDR of approximately 86 dBc. Again, to get SFDR in dBc, the reported –93 dBFS is adjusted as |SFDR| – 7 dB.

If the –105-dBc SFDR for the THS4509 interface (from Figure 10 at 70 MHz) were combined with the ADS5424 SFDR, the system performance would drop from 86-dBc to 85-dBc SFDR—extremely good performance, particularly when the low 190-mW total power dissipation in the THS4509 is considered (38 mA across a 5-V total supply).

Figure 11. Two-tone SFDR of the ADS5424 at 70 MHz



Layout issues

To achieve this very low harmonic distortion, considerable attention to layout symmetry is required. Every effort is made to keep the signal current out of the ground plane and purely differential (see Reference 3). Figures 12 through 15 show the four layers for the test board we developed that resulted in the performance data reported here.

Top layer

To limit trace length around the THS4509 QFN-16 package, 0402-size resistors and capacitors were used (see Figure 12). R2A/B and R3A/B are the gain and feedback resistors. R4A/B are component placeholders that can be either resistors or capacitors. In this case, these placeholders have been populated with 10-nF capacitors as shown in Figure 8. T1 and T2 are transformers. To accommodate different transformer pinouts, pin 2 and pin 5 of T1 are connected together. Note that the transformers tested have a centertap on the secondary winding and no centertap on the primary. The transformers this board can accommodate used either pin 2 as the centertap with pin 5 as a no-connect, or pin 5 as the centertap with pin 2 as a no-connect.

First inner layer (ground plane)

In the ground plane (Figure 13), note the window opening around the device pins as well as the signal trace to the transformers. This window minimizes parasitic capacitance effects that could push the THS4509 into instability.

Used immediately underneath the top layer, this ground plane can help shield traces from other layers. It can also be used to create controlled-impedance traces.

Second inner layer (power plane)

The power planes (Figure 14) were set to avoid crossing any top-layer signal trace and thus to limit parasitic capacitance. Each power plane is connected to the large bypass capacitors C1 and C2 from the top layer. C1 and C2 can also be used as elements of a low-pass filter formed by the combinations L1-C1 and L2-C2. The L1 and L2 components are optional and intended to be lossy ferrite beads. They were not used for the tests taken here and were replaced with a short. Note in Figure 12 that C1 and C2 are connected together and then connected to the ground plane. This limits the return path traces and maximizes the self-resonant frequency of each capacitor.

Figure 12. Top layer, where most components are loaded

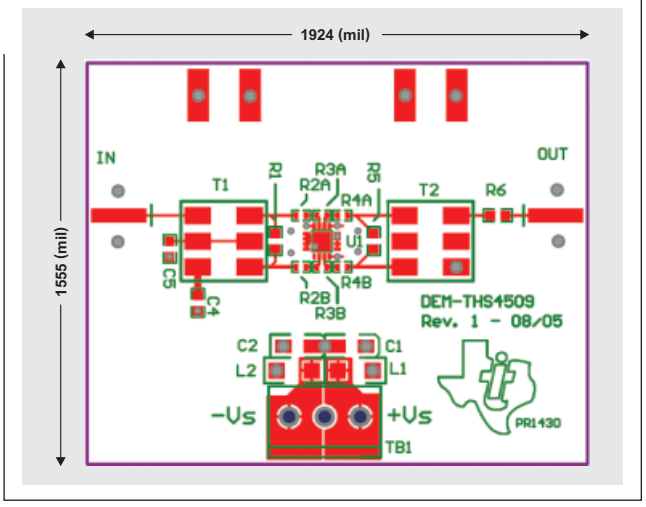


Figure 13. First inner layer (ground plane)

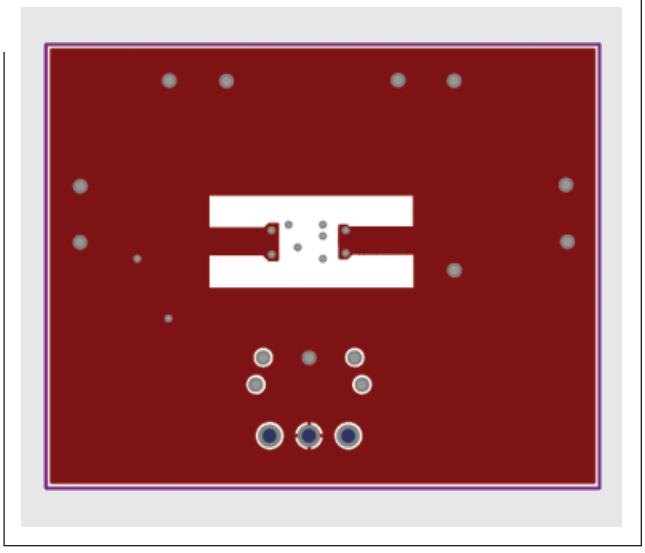
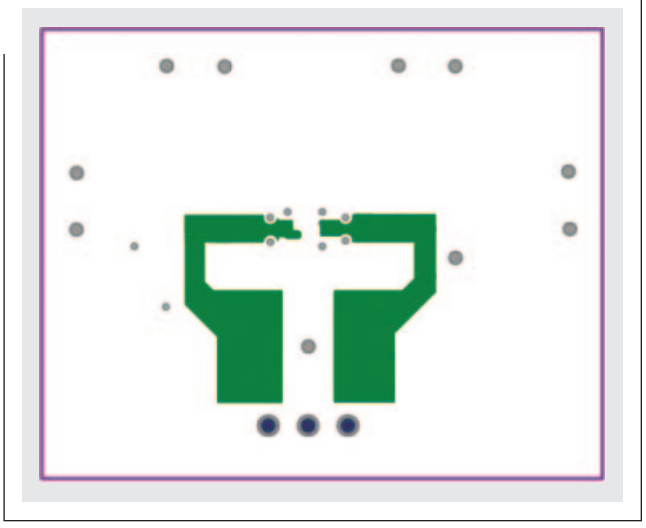


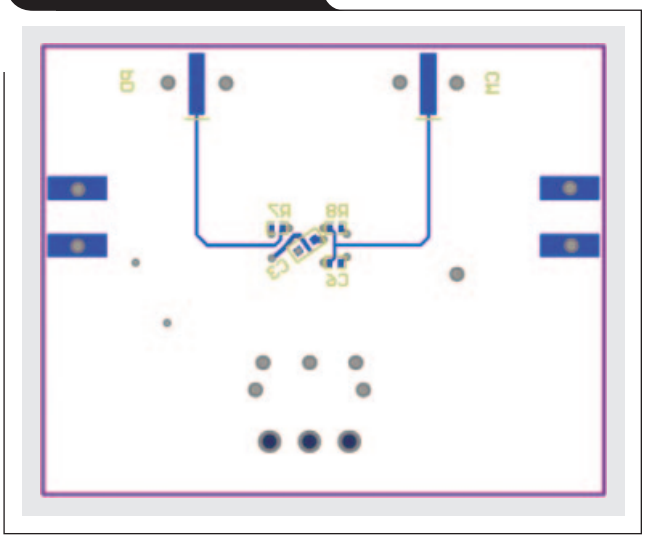
Figure 14. Second inner layer with power connections



Bottom layer

The key element on this layer (Figure 15) is C3, a very high-quality, four-terminal capacitor from supply to supply. This capacitor replaces three regular capacitors in this circuit—two capacitors from each supply to ground and one capacitor across the supplies—simplifying layout and improving bypassing. For more information on this type of capacitor, go to www.x2y.com

Figure 15. Bottom layer



Adapting the THS4509 test circuit to an IF ADS5424 interface

The circuit and testing discussed here have shown that the THS4509 has the intrinsic capability to support the SFDR requirements of the ADS5424 over a wide range of IF frequencies. Actual implementations must also consider the out-of-band distortion terms, single-supply operation, and noise-power bandwidth issues. Most implementations will need to add at least a simple bandpass filter between the amplifier and the converter to limit the noise-power bandwidth and to attenuate the out-of-band distortion terms generated by the THS4509. Figure 16 shows an example implementation.

This circuit ac couples in a few more places and adds a passive bandpass filter at the input of the converter. This will add some insertion loss to the channel that may require a slightly higher gain in the amplifier to achieve 20-dB total gain in the interface.

Summary

The THS4509 has been shown to provide adequate two-tone, third-order intermodulation levels to support the reported specifications for high-performance, 14-bit ADCs such as the ADS5424. While other approaches have also proven effective, the THS4509 is particularly attractive for its low 190-mW total power dissipation. For specific IF interface applications, an LC filter should be introduced prior to the converter to limit the signal-to-noise ratio and the SFDR degradation due to the broadband noise and distortion at the THS4509 output.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "14-Bit, 105 MSPS Analog-to-Digital Converter," ADS5424 Datasheet	slws157
2. Michael Steffes, "RLC Filter Design for ADC Interface Applications," Application Report	sbaa108
3. Xavier Ramus, "PCB Layout for Low Distortion High-Speed ADC Drivers," Application Report	sbaa113

Related Web sites

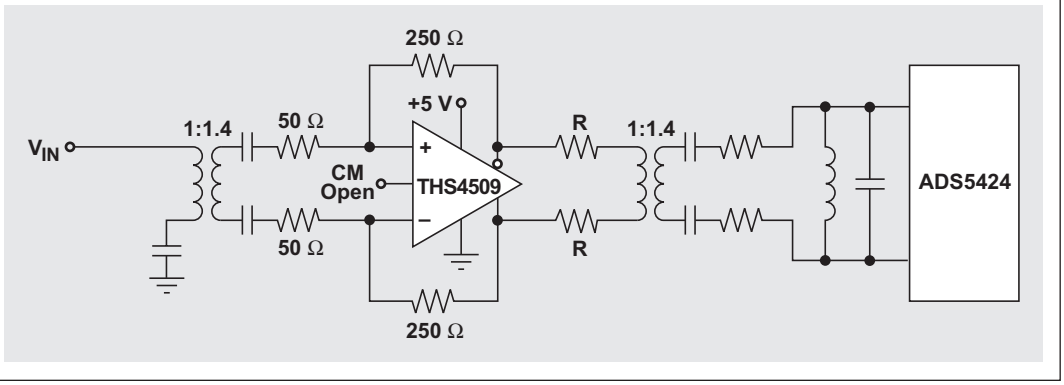
dataconverter.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with ADS5424, ADS5500, OPA695, OPA847, or THS4509

www.x2y.com

Figure 16. Single-supply implementation with bandpass filtering



Li-ion switching charger integrates power FETs

By Anne Huang (Email: sh@ti.com)
Product Manager

Introduction

Linear battery chargers suffer from excessive power dissipation when the input-to-output overhead voltage and/or charging current are high. Take the example of a typical portable DVD player configuration that incorporates a 2-cell Li-ion battery pack, a car adapter at 12 V, and a charge rate of 1.2 A. The power dissipation of a linear charger is above 5 W on average. A simple solution to the overheating is the bq241xx series switching charger. The internal power FETs are capable of supplying up to 2 A of charging current. The synchronous PWM controller operates at 1.1 MHz from an input voltage of up to 18 V, making it ideal for use in systems powered by 1-, 2-, or 3-cell battery packs. The high-voltage, high-current, and high-efficiency features together with integrated reverse leakage protection and internal loop compensation are nicely housed in a small 3.5-mm × 4.5-mm QFN package that saves board space and reduces system design time.

Design example (see Figure 1)

Adapter voltage: 12 V
Battery pack: 2 S Li-ion, 1800 mAH
Battery regulation voltage: 4.2 V/cell
Battery cutoff voltage: 3 V/cell
Fast-charge current: 1.2 A
Precharge and termination current: 120 mA
Safety timer: 5 hours

Determine the inductor, L

Given 30% ripple current, the inductance is given by

$$L1 = \left(\frac{V_{IN} - V_{BAT}}{\Delta I_L}\right)\left(\frac{V_{BAT}}{V_{IN}}\right)\left(\frac{1}{f_S}\right) = \left(\frac{12-8.4}{30\% \times 1.2}\right)\left(\frac{8.4}{12}\right)\left(\frac{1}{1.1\times 10^6}\right) = 6.364\ \mu H, \quad (1)$$

where L = 8.2 µH.

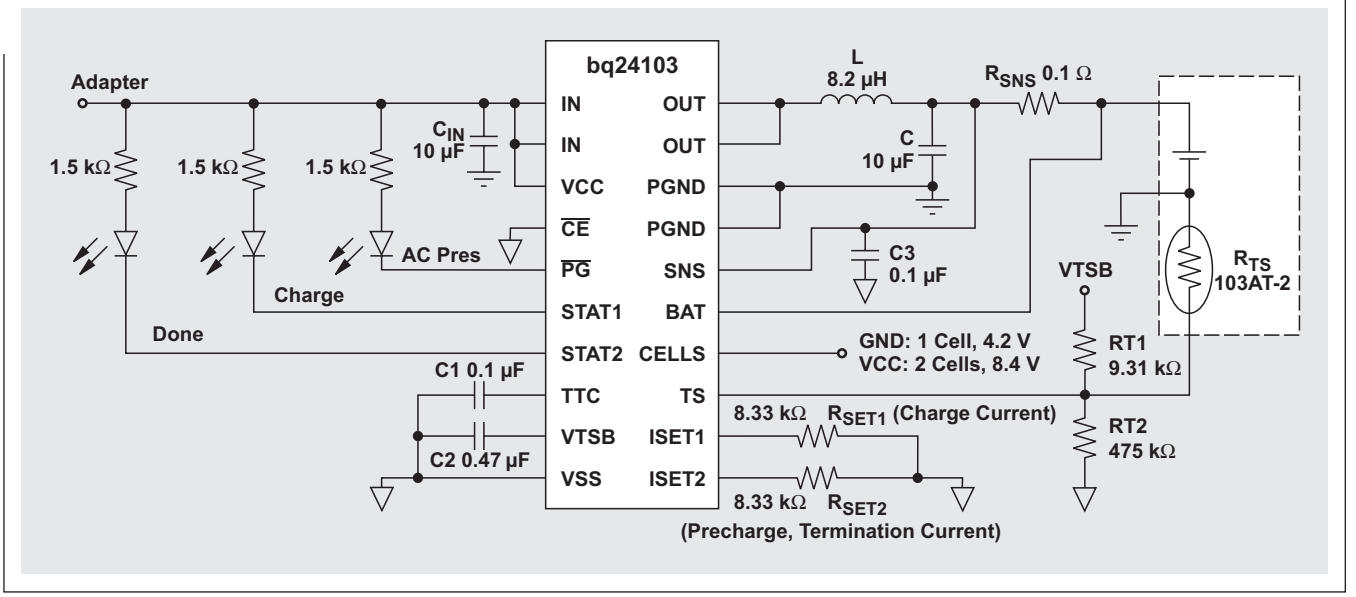
The inductor saturation current should be larger than the peak current to prevent inductor saturation.

$$\Delta I_{L\_max} = \left(\frac{V_{IN} - V_{BAT}}{L}\right)\left(\frac{V_{BAT}}{V_{IN}}\right)\left(\frac{1}{f_S}\right) = \left(\frac{12-6}{6.8\times 10^{-6}}\right)\left(\frac{6}{12}\right)\left(\frac{1}{1.1\times 10^6}\right) = 0.40\ A \quad (2)$$

$$I_{pk} = I + \frac{\Delta I_{L\_max}}{2} = 1.2 + \frac{0.40}{2} = 1.4\ A \quad (3)$$

Select an 8.2-µH, 1.6-A, 39-mΩ Sumida CDRH5D28 inductor.

Figure 1. bq24103 application circuit



Determine the output capacitor, C

The resonant frequency, f_o, of the internal loop compensation is approximately 16 kHz. To achieve optimum loop stability,

$$C = \frac{1}{(2\pi f_o)^2 L} = \frac{1}{(2\pi \times 16 \times 10^3)^2 \times (8.2 \times 10^{-6})} = 12 \times 10^{-6} \text{ farads.} \quad (4)$$

Select a 10-µF, 25-V X7R 1206 ceramic capacitor.

Determine the sense resistor, R_{SNS}

$V_{R_{SNS}}$ = 100 mV to 200 mV. To get a standard resistance value, select $V_{R_{SNS}}$ = 120 mV:

$$R_{SNS} = \frac{V_{R_{SNS}}}{I_{BAT}} = \frac{120 \text{ mV}}{1.20 \text{ A}} = 0.1 \ \Omega$$

$$P_{R_{SNS}} = I_{BAT}^2 R_{SNS} = 144 \text{ mW} \quad (5)$$

Select a 1%, 100-mΩ, 0.25-W resistor.

Determine R_{SET1} and R_{SET2}

$V_{I_{SET1}}$ = 1.0 V, $V_{I_{SET2}}$ = 0.1 V, and K_{SET1} = K_{SET2} = 1000 V/A.

$$R_{SET1} = \frac{V_{I_{SET1}} K_{SET1}}{I_{Fast\text{-}charge} R_{SNS}} = 8.33 \text{ k}\Omega \quad (6)$$

$$R_{SET2} = \frac{V_{I_{SET2}} K_{SET2}}{I_{Precharge} R_{SNS}} = 8.33 \text{ k}\Omega \quad (7)$$

Select 1%, 8.33-kΩ resistors.

Determine C1

C1 is used to program the fast-charge timer.

$$C1 = \frac{300 \text{ min}}{2.6 \text{ min/nF}} = 0.115 \ \mu\text{F} \quad (8)$$

Select a 0.12-µF or 0.1-µF X5R or X7R ceramic capacitor for good temperature performance.

Determine R_{T1} and R_{T2}

R_{TS}, the resistance of the thermistor, normally drops with temperature. Using a 103AT-2 thermistor, assume that the resistance at cold temperature is R_{TS_Cold} = 27306 Ω (0°C) and at hot temperature is R_{TS_Hot} = 4935 Ω (45°C).

The voltage threshold at cold temperature, V_{LTF}, equals 73.5% × VTSB. The voltage threshold at hot temperature, V_{HTF}, equals 34.4% × VTSB. Therefore,

$$\frac{R_{T2} // R_{TS\_Cold}}{R_{T1} + R_{T2} // R_{TS\_Cold}} = 73.5\% \text{ and} \quad (9)$$

$$\frac{R_{T2} // R_{TS\_Hot}}{R_{T1} + R_{T2} // R_{TS\_Hot}} = 34.4\%. \quad (10)$$

These equations yield R_{T1} = 9.31 kΩ and R_{T2} = 475 kΩ.

PCB layout considerations

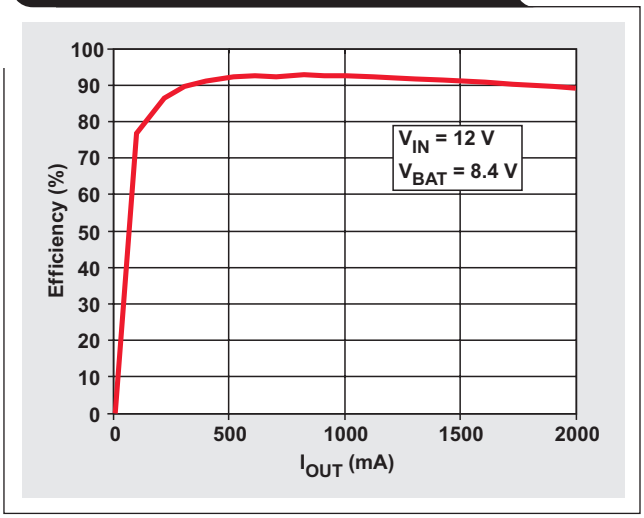
The results of measuring the efficiency with the bq24103 EVM are shown in Figure 2. Following are some layout guidelines to maximize efficiency:

- Make the connections of the power stage as wide and short as possible.
- The ground planes of the power stage and the control stage should run separately and be connected together at a single point.
- Place the decoupling capacitors close to the pins.
- Minimize the current-sensing feedback loop.
- Place the inductor close to the OUT pin.

Related Web sites

power.ti.com
www.ti.com/sc/device/bq24103

Figure 2. Efficiency vs. I_{OUT} (V_{IN} = 12 V, V_{BAT} = 8.4 V)



TLC5940 dot correction compensates for variations in LED brightness

By Michael Day, *Applications Manager, Portable Power Products* (Email: m-day@ti.com),
and Tarek Saab, *Product Marketing Engineer, Portable Power Products* (Email: tareksaab@ti.com)

The abundance of light-emitting diodes (LEDs) in various types of end equipment has surpassed even the most aggressive expectations. The reduction in LED prices, coupled with increased LED efficiency (lumens per watt), has fueled the redesign of many common devices. LEDs are entering new markets such as architectural lighting, LCD TV backlighting, car headlamps, and traffic lights. At the same time, they continue to dominate other markets such as high-quality, large form-factor video displays and alphanumeric displays. As the efficiency and brightness of LEDs improve and the cost decreases, it is anticipated that LED usage will eventually replace conventional lighting methods in consumer applications. Some of these markets, such as LCD TV backlighting and large form-factor video displays, require a much higher degree of LED brightness uniformity than is possible from the LEDs alone. This article shows how the dot correction function in the Texas Instruments (TI) TLC5940 and in other similar LED drivers generates uniform LED brightness across thousands of pixels in these displays.

Figure 1. Large form-factor video display

A stadium or advertising display like that shown in Figure 1 integrates dozens of display panels and thousands of LEDs. The individual LEDs inside each array vary significantly in brightness, with the delta in lumens between the brightest and dimmest LED regularly approaching 15 to 20%, if not more. The design engineer must ensure that each LED is calibrated to provide the same amount of brightness so that when the entire screen is turned on, it appears uniform. Without this calibration, the screen will have a blotchy, uneven look. Even after the display is properly calibrated and deployed to the field, variations in LED aging will generate changes in brightness. As a result, companies must continually solve difficult quality and maintenance issues. To compensate for variations in LED brightness and aging, manufacturers often employ two techniques: First, they purchase matched LEDs from a supplier (also known as "binning"); and second, they utilize a high-quality LED driver with dot correction functionality.

LED suppliers offer the benefit of matched LEDs for an incremental increase in price. They measure and bundle these red, green, and blue (RGB) diodes together with LEDs that generate similar lumens at a specified current. Using this method can provide the desired uniformity with minimal design considerations for low-end lighting systems. However, the variance in decay rate, or degradation in brightness, per pixel over time makes this method a short-lived solution. In other words, in a year or two the picture will become blotchy. Furthermore, should a defective panel need replacement, the lumenal output of the new panel will be visually dissimilar to the others.

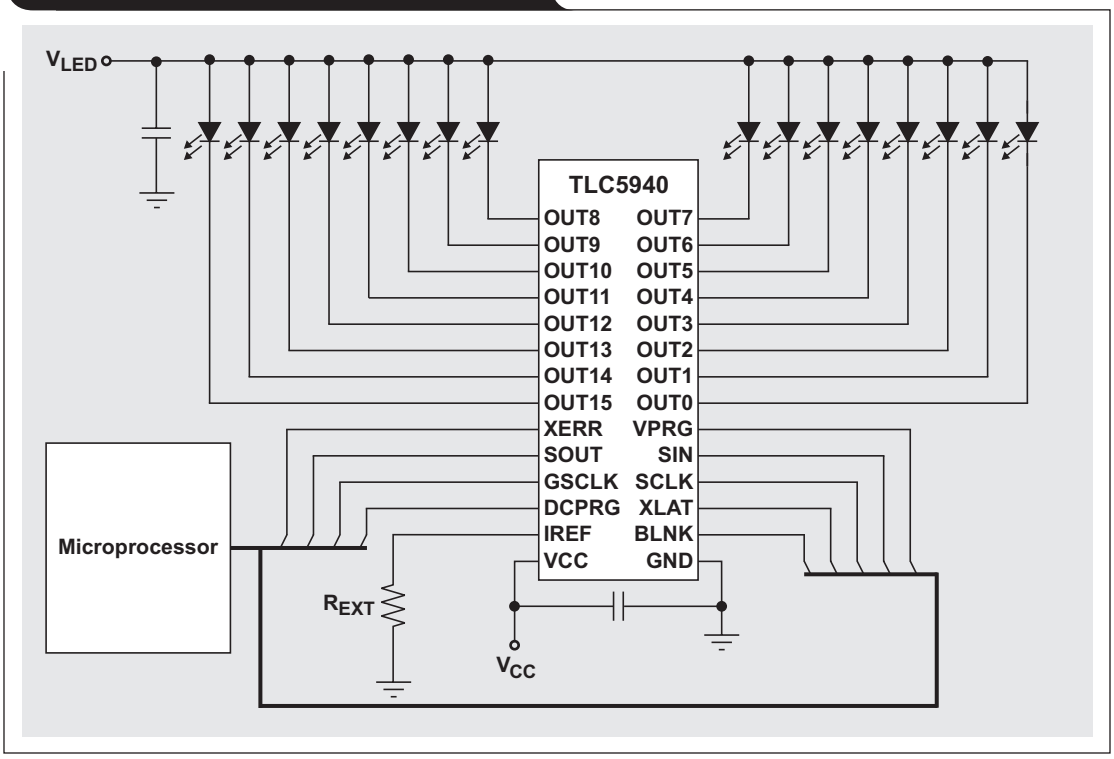
High-end display systems require brightness-matching levels that are unattainable by simply binning the LEDs. To achieve pixel and panel uniformity over the *life span* of a display unit, manufacturers use advanced LED drivers with dot correction capability. Dot correction is a method for managing pixel brightness by adjusting the current supplied through each individual LED in the array. The dot correction feature enables the processor to control full current to a panel of LEDs while the LED driver scales the current to each LED and creates uniform brightness. This frees the processor for other functions, since it no longer has to check a look-up table or perform complex multiplication tasks for each LED in every refresh cycle.

To implement dot correction, manufacturers measure the brightness of individual LEDs through photo capture. The dimmest LED in the system is designated as the "base" LED to which every other pixel is matched. To accomplish this calibration, the current supplied to each pixel is multiplied by a fractional value proportional to the LED's lumenal output. In a device like TI's TLC5940, the dot correction value for each LED can be dynamically changed every refresh cycle or stored inside an integrated EEPROM. This dual dot correction method offers the flexibility to update overall panel brightness as external lighting conditions change, and provides long-term, nonvolatile dot correction information that ensures panel uniformity. The EEPROM data can be rewritten as lumenal measurements vary over time or as panels fail, requiring correction or replacement, respectively. The following example shows how dot correction is used to match LED brightness at production.

A typical display panel has anywhere from dozens to thousands of LED drivers and from hundreds to hundreds of thousands of individual LEDs. For simplicity, this example considers only the 16 LEDs connected to a single driver. Figure 2 shows the typical schematic of a single driver. An external power supply, V_{LED}, provides the power to the LEDs. R_{EXT} sets the absolute maximum current through any LED. An external processor programs the TLC5940 to turn on or off each individual LED and to set its current to a percentage of the maximum programmed current.

The first step in calibrating a panel's brightness is to set the maxium current. This example requires a green LED to have a luminous intensity of 80 millicandela (mcd). The LED (Osram LP E675) is available in 4 different luminosity bins: 45–56, 56–71, 71–90, and 90–112 mcd, each measured at a normalized current of 50 mA. Selecting the highest bin guarantees at least 80 mcd per LED. R_{EXT} must set the current high enough to allow even the dimmest LED to produce 80 mcd. According to the datasheet for the LP E675, setting the LED current to 43 mA guarantees

Figure 2. Typical TLC5940 implementation



80 mcd. At production, the brightness of all LEDs is measured at full current (43 mA). This might produce an LED histogram of luminous intensity resembling Figure 3. As shown, the brightness variation measured between each LED in the panel may vary as much as ±10% without dot correction. A brightness deviation this large is unacceptable in higher-end displays. The TLC5940 dot correction feature can now be used to calibrate the LED brightness. When programmed to full brightness, the IC must dot correct the luminous intensity of LED1 from 83 mcd to 80 mcd. The TLC5940 has 6-bit dot correction (64 steps), which corresponds to a full-scale resolution of 1.56% per step.

The following formula calculates the correct dot correction level for each LED:

$$DC_{Production} = \frac{L_{Baseline}}{L_{Initial}} \times 64 = 61.7,$$

where $DC_{Production}$ is the required dot correction value at production, $L_{Baseline}$ is the desired brightness level, and $L_{Initial}$ is the measured brightness at maximum current.

By rounding the calculated dot correction value to the closest fractional number and then multiplying the original luminosity by the new dot correction ratio, one can produce the updated LED brightness.

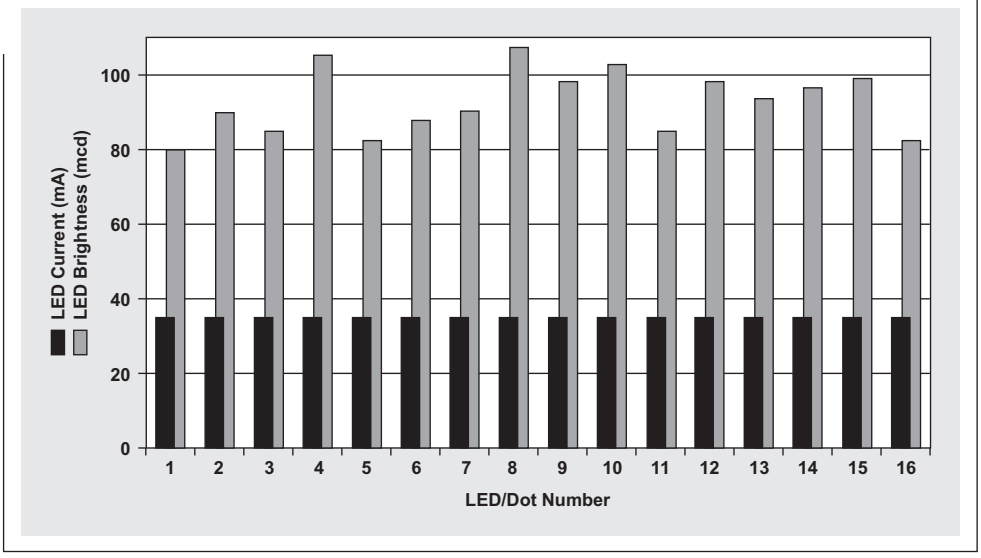
$$L_{Production} = \frac{DC_{Production}}{64} \times L_{Initial} = 80.4 \text{ mcd}$$

After the dot correction values are calculated and stored, the TLC5940 is capable of automatically generating a uniform brightness in all LEDs. When the processor programs the TLC5940 to drive full current, the TLC5940 automatically adjusts the actual current in each channel to properly calibrate the LED brightness. The current in LED1 is calculated as

$$I_{LED1} = \frac{DC_{LED1}}{64} \times I_{max} = 41.66 \text{ mA},$$

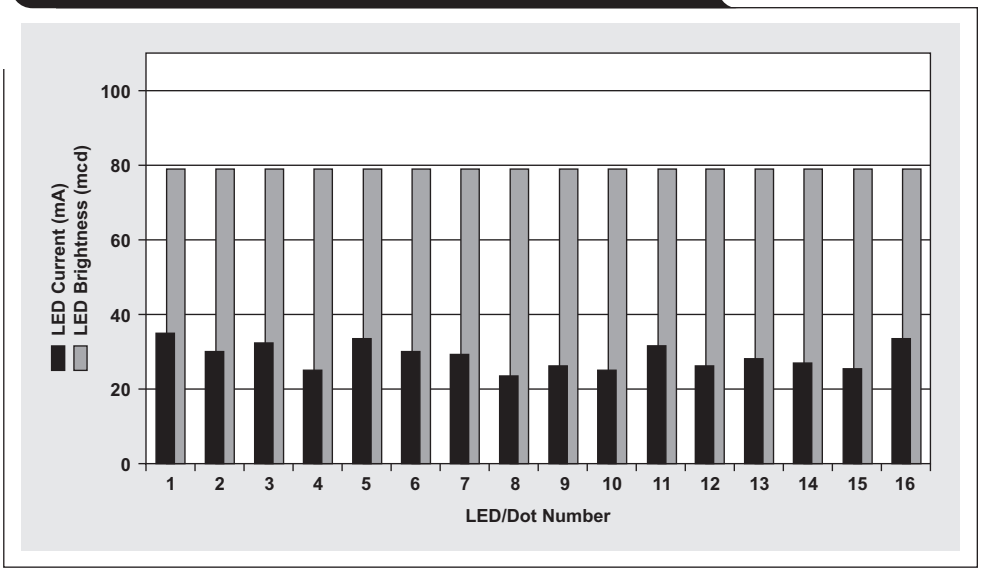
where I_{LED1} is the actual LED1 current, DC_{LED1} is the dot correction value for LED1 (62), and I_{max} is the maximum LED current programmed by R_{EXT} (43 mA). Applying these

Figure 3. LED brightness and forward current histogram before dot correction



formulas to the remaining LEDs produces the histogram in Figure 4. If programmed into the TLC5940's nonvolatile EEPROM, the dot correction data is available each time the panel is turned on and remains constant until the next time the panel is recalibrated.

Figure 4. LED brightness and forward current histogram after dot correction



For indoor/outdoor industrial applications such as billboards and large form-factor video displays, "static" adjustment (calibration that remains fixed until manually adjusted) is sufficient. dot correction values don't change until the next routine maintenance cycle. The newer market applications such as LCD TV backlighting require a dynamic dot correction scheme. Products such as the Sony 40″ Qualia 005 and the Samsung 46″ LNR460D have each introduced LCD TVs that incorporate LED-based backlighting. Contrary to popular belief, the diodes in these TV displays are not white. RGB LEDs are controlled and mixed to create "tunable" white light.

The advantages of LED backlighting over conventional lamps are numerous: enhanced power efficiency, reduced motion artifacts, broader color spectrum (>105% NTSC in some cases), longer life span, tunable color temperature, etc. The picture quality is incomparable. However, LCD TV engineers encounter not only the same lumenal variance challenges as conventional panel makers but also temperature concerns. TV backlighting applications are sensitive to changes in LED brightness as a function of temperature. In addition, a TV set achieves optimum display quality only when its backlighting properties are adjusted to meet the constantly changing ambient lighting conditions for each consumer's living room. These considerations, coupled with the fact that this is a consumer application, create a need for dynamic brightness adjustment.

To create this dynamic control loop, internal sensors that measure LED temperature and brightness fluctuations, as well as external sensors that measure ambient-light conditions, are required. The control loop, in its most basic form, begins with the sensors gathering data and feeding these measurements into a processor. The processor evaluates this data and provides the "intelligence" to an LED driver such as the TLC5940. The processor combines the original factory-calibrated dot correction data with the new, dynamic data and generates updated dot correction values.

In the previous example, if the ambient-light meter detects low ambient-light conditions that require only 70% of full brightness, or 56 mcd, the processor calculates a new ambient-light dot correction value of 44.8. If, simultaneously, the LED light output drops 10% due to an increase in temperature, the processor calculates a temperature dot correction value of 71.1. Combining all three dot correction values generates the new dot correction data, compensating for all three brightness variations.

$$DC_{Ambient} = \frac{80 \times 0.7}{80} \times 64 = 44.8$$

$$DC_{Temp} = \frac{80}{80 \times 0.9} \times 64 = 71.1$$

$$DC_{Total} = \left(\frac{DC_{Ambient}}{64}\right)\left(\frac{DC_{Temp}}{64}\right)\left(\frac{DC_{Production}}{64}\right)64 = 48.0$$

As shown in the following equation, the combined dot correction value of 48 yields the desired brightness of 56 mcd. Note that the initial current in this calculation is set to 90% of the initial production current due to the brightness drop caused by the temperature.

$$L_{Final} = \left(\frac{DC_{Total}}{64}\right)(83 \times 0.9) = \frac{48}{64} \times 74.7 = 56 \text{ mcd}$$

Advanced LED drivers such as the TLC5940 are capable of providing a dynamic dot correction value to optimize the lighting solution for a consumer's specific viewing conditions.

Related Web sites

power.ti.com
www.ti.com/sc/device/TLC5940

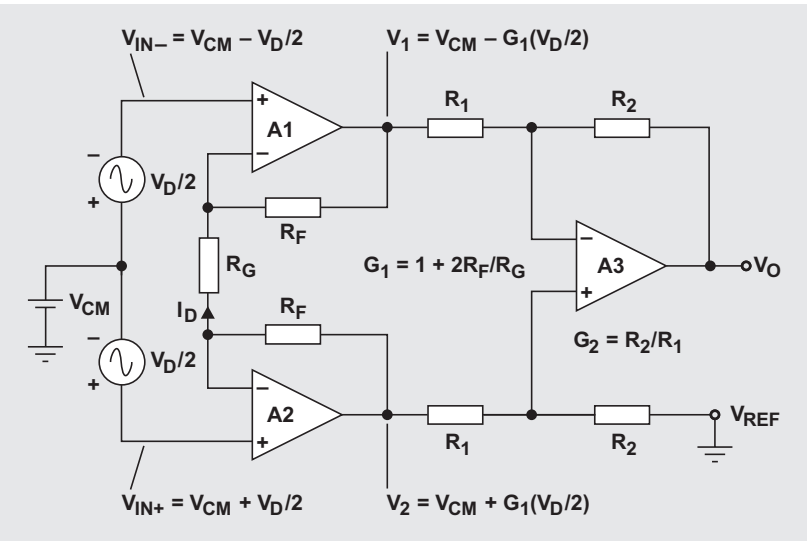
Getting the most out of your instrumentation amplifier design

By Thomas Kugelstadt (Email: tk@ti.com)
Senior Systems Engineer, Industrial Systems

Many industrial and medical applications use instrumentation amplifiers (INAs) to condition small signals in the presence of large common-mode voltages and DC potentials. Standard INAs using a unity-gain difference amplifier in the output stage, however, can limit the input common-mode range significantly. Thus, common-mode signals induced by adjacent equipment, as well as large differential DC potentials from differently located signal sources, can increase the input voltage of the INA, causing its input stage to saturate. Saturation causes the INA output voltage, although of wrong value, to appear normal to the following processing circuitry. This could lead to disastrous effects with unpredictable consequences.

This article reviews some principles of the classic three-op-amp INA and provides design hints that extend the input common-mode range to avoid saturation while preserving overall gain at maximum value. The article also discusses the removal of large differential DC voltages through active filtering, avoiding passive RC filters at the INA input that otherwise would lower its common-mode rejection ratio (CMRR).

Figure 1. Classic three-op-amp INA and its voltage nodes



INA principles

Figure 1 shows the block diagram of the classic three-op-amp INA. The inputs, V_{IN+} and V_{IN-}, are defined through the input polarities of the difference amplifier, A3.

By definition, the INA's input signals are subdivided into a common-mode voltage, V_{CM}, and a differential voltage, V_D. While V_{CM}, the voltage common to both inputs, is defined as the average of the sum of V_{IN+} and V_{IN-}, V_D represents the net difference between the two.

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \text{ and } V_D = V_{IN+} - V_{IN-}. \quad (1)$$

Solving both equations for V_{IN+} or V_{IN-} and equating the received terms results in a new set of equations, which, when solved for either input voltage, yields

$$V_{IN+} = V_{CM} + \frac{V_D}{2} \text{ and } V_{IN-} = V_{CM} - \frac{V_D}{2}. \quad (2)$$

In the nonsaturated mode, the op amp action of A1 and A2 applies the differential voltage V_D across the gain resistor, R_G, generating the input current, I_D:

$$I_D = \frac{V_{IN+} + V_{IN-}}{R_G} = \frac{V_D}{R_G}. \quad (3)$$

The output voltages of A1 and A2 are therefore

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D R_F \text{ and } V_2 = V_{CM} + \frac{V_D}{2} + I_D R_F.$$

Replacing current I_D with Equation 3 yields

$$V_1 = V_{CM} - \frac{V_D}{2} G_1 \text{ and } V_2 = V_{CM} + \frac{V_D}{2} G_1, \quad (4)$$

where $G_1 = 1 + 2\frac{R_F}{R_G}$.

Equation 4 shows that only the differential component, $V_D/2$, is amplified by the input gain, G_1, while the common-mode voltage, V_{CM}, passes the input stage with unity gain.

The difference amplifier, A3, subtracts V_1 from V_2 and amplifies the difference with the gain G_2:

$$V_O = (V_2 - V_1)G_2, \text{ where } G_2 = \frac{R_2}{R_1}. \quad (5)$$

Inserting Equation 4 into Equation 5 and solving for V_O/V_D provides the transfer function of the INA:

$$\frac{V_O}{V_D} = G_1 G_2 = G_{TOT}. \quad \textbf{(6)}$$

Extending the input common-mode voltage range

Note that V_1 and V_2 in Equation 4 do not represent absolute voltages. Because V_{CM} and V_D can change their polarities, the maximum voltage either output can assume before reaching saturation is

$$\pm\left|V_{1,2}\right| = \pm\left(\left|V_{CM}\right| + \left|\frac{V_D}{2}\right|\right) \le \pm\left|V_{SAT}\right|.$$

For clarification, the following description simply ignores signal polarities, and the variables refer only to magnitude values. Assuming that $V_{1,2}$ and $V_D/2$ are constant, the only way to increase the input common-mode voltage from V_{CM} to V_{CM}' is to reduce the input gain from G_1 to G_1' so that

$$V_{1,2} = \text{constant} = V_{CM} + \frac{V_D}{2} G_1 = V_{CM}' + \frac{V_D}{2} G_1'.$$

Solving for V_{CM}' yields

$$V_{CM}' = V_{CM} + \frac{V_D}{2}\left(G_1 - G_1'\right).$$

Reducing G_1 reduces the range of the amplified differential component, $G_1'(V_D/2)$, thus providing an expansion range for V_{CM}. Standard INAs, using unity-gain difference amplifiers, have $R_2 = R_1$ and $G_2 = 1$.

The total INA gain is then placed into the input stage, making $G_1 = G_{TOT}$. Equation 6 shows that reducing G_1 from G_{TOT} to G_1', while preserving G_{TOT}, requires an increase in difference amplifier gain from $G_2 = 1$ to $G_2' = G_{TOT}/G_1'$.

Replacing G_1 with G_{TOT} and G_1' with G_{TOT}/G_2' results in the extended common-mode range:

$$V_{CM}' = V_{CM} + \frac{V_D}{2} G_{TOT}\left(1 - \frac{1}{G_2'}\right) = V_{CM} + \frac{V_D}{2} G_1'\left(G_2' - 1\right). \quad \textbf{(7)}$$

This improved common-mode range at the amplifier output is now passed on 1:1 to the input. Applying gain to the difference amplifier requires access to the feedback resistor of A3 in Figure 2. A common solution uses a stand-alone difference amplifier, which provides access to the feedback resistor via a V_{SENSE} pin. The input stage is then realized by a dual low-noise amplifier, with external resistors R_F and R_G being used to set the input gain.

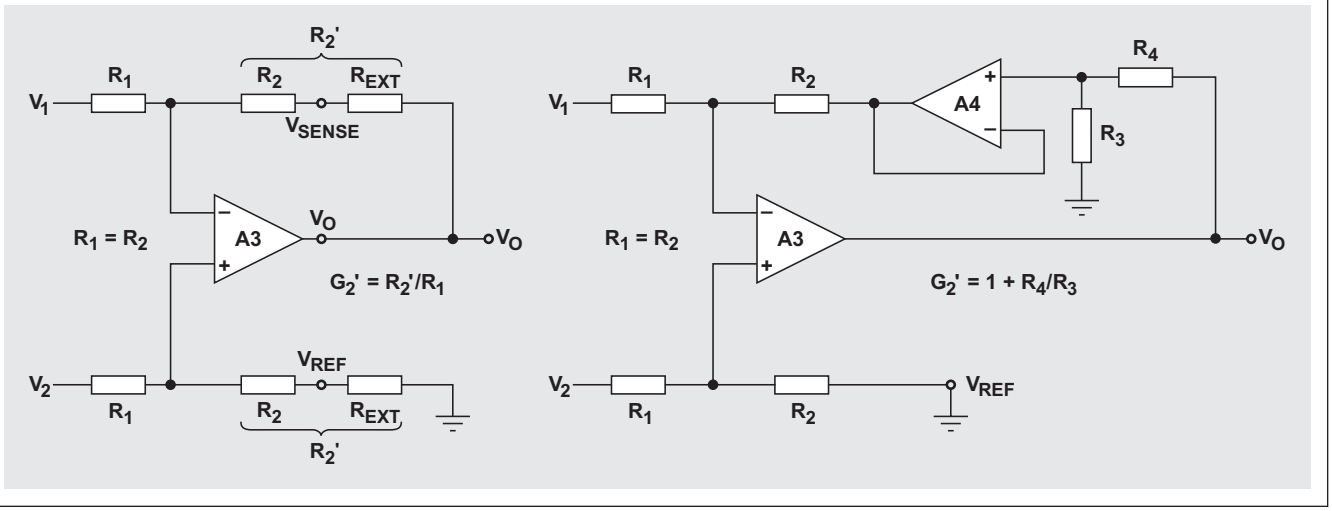
To raise the gain of a unity-gain amplifier, external resistors can be switched in series to R_2. However, the internal resistor values must be measured, as they can deviate by ±30% from their nominal values given in the datasheet. This approach works well for moderate gain. For large gain, however, the external resistors can reach prohibitive values, increasing noise to an undesirable level. A buffered voltage divider in the feedback path of A3 is then required.

Resistors R_3 and R_4 allow a wide range of gain settings with moderate resistor values. Voltage follower A4 provides low output impedance, which preserves the high CMRR of the difference amplifier.

Removing large differential DC potentials

The signal conditioning in analog front ends of medical equipment, such as electrocardiographs (ECGs), presents the additional design challenge of detecting small AC signals in the presence of large differential DC potentials.

Figure 2. Increasing difference amplifier gain via R_{EXT} or buffered voltage divider



Signal composition

Contraction of the heart wall spreads electrical currents from the heart throughout the body. The currents create different potentials at different parts of the body, which are sensed by electrodes on the skin surface via biological transducers made of metals and salt.

A typical electric potential is a 0.5- to 1.5-mV AC signal with a bandwidth of 0.05 to 100 Hz and sometimes up to 1 kHz. This signal is superimposed by a large electrode DC offset potential of ±500 mV and a large common-mode voltage of up to 1.5 V. The common-mode voltage comprises two parts: 50- to 60-Hz interference and DC electrode offset potential.

To determine the input signal of the INA in the ECG front end, the electrode attached to a patient's right arm has a DC offset of 450 mV and an AC signal of 0.5 mV_{PP}, while the one on the left arm has a 50-mV_{PP} offset and 1.5-mV_{PP} AC. The differential input is therefore

$$\begin{aligned} V_D &= V_{D\_DC} + V_{D\_AC} \\ &= \left(V_{DC\_R} - V_{DC\_L}\right) + \left(V_{AC(PP)\_R} - V_{AC\,(PP)\_L}\right) \\ &= 400\ \text{mV} + 1\ \text{mV}. \end{aligned}$$

Thus, the differential DC is 400 times larger than the AC signal of interest and, if untreated, will receive amplification through the entire INA, causing its amplifiers to saturate.

At the same time, to convert the 1-mV AC into a representative signal that is of use to a following signal processing system, a total gain of 1000 or more is required.

The solution to this problem is performed in three steps:

(1) Limit the input gain, G1, to avoid saturation of A1 and A2;
(2) implement low-pass filtering in the output stage to remove the differential DC, VD_DC; and
(3) apply high gain in the output stage, boosting the AC signal of interest, VD_AC.

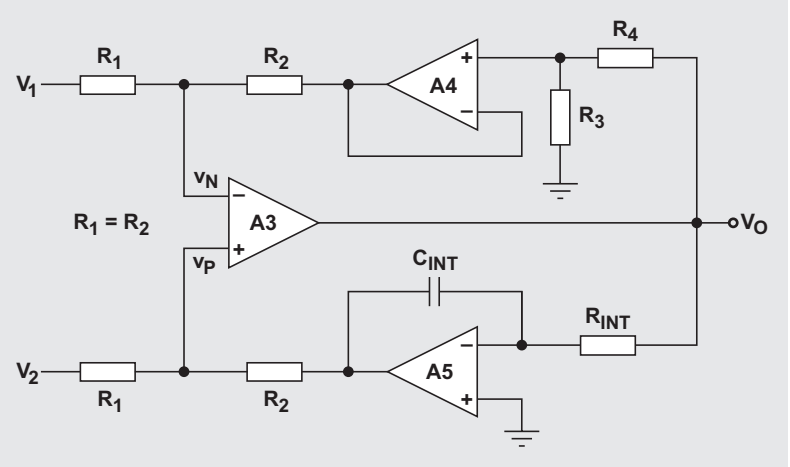
To determine G_1, the INA is assumed to operate from a typical ±5-V supply. For simplification, A1 to A3 have rail-to-rail inputs and outputs, and the common-mode potential is at a maximum of V_{CM} = 1.5 V.

Neglecting the small AC component of V_D, rewriting Equation 4 for G_1 gives a maximum input gain of

$$G_1 = 2\left(\frac{V_{2\_SAT} - V_{CM}}{V_{D\_DC}}\right) = 2\left(\frac{5\ \text{V} - 1.5\ \text{V}}{400\ \text{mV}}\right) = 17.5.$$

For convenience, we choose a conservative value of G_1 = 10; thus, the differential input signal of A3 consists of a 4-V DC component and a 10-mV AC component. To remove the DC part, an active low-pass filter is implemented, providing negative feedback from the output to the noninverting input of A3. At the same time, output gain, G_2, is increased by the buffered voltage divider, R_3,R_4.

Figure 3. Difference amplifier with low-pass filter and gain stage



To determine G_2, we calculate the total gain for maximum dynamic output range,

$$G_{TOT} = \frac{V_{SAT}}{V_{D\_AC}} = \frac{5\ \text{V}}{1\ \text{mV}} = 5000,$$

and divide it by the applied input gain,

$$G_2 = \frac{G_{TOT}}{G_1} = \frac{5000}{10} = 500.$$

With the low-pass filter in the feedback loop of A3, the transfer function of the difference amplifier assumes high-pass characteristics. One would now assume that the filter's –3-dB frequency occurs at

$$f_0 = \frac{1}{2\pi R_{INT} C_{INT}}.$$

However, establishing the transfer function reveals that f_0 has been increased by the gain factor G_2 to $f_0' = f_0 G_2$.

Mathematical proof:

By op amp action, the input terminals of A3 (Figure 3) have identical potentials: $v_N = v_P$. Thus, for $R_1 = R_2$:

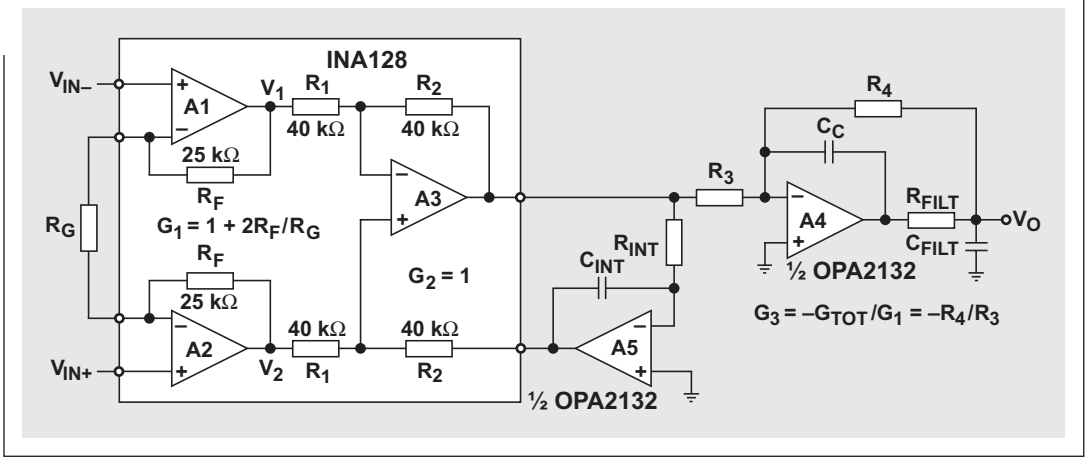
$$v_N = \frac{V_1}{2} + \frac{V_O}{2G_2} \text{ and } v_P = \frac{V_2}{2} - \left(\frac{V_O}{2}\right)\left(\frac{1}{jf/f_0}\right),$$

$$\text{where } G_2 = 1 + \frac{R_4}{R_3} \text{ and } f_0 = \frac{1}{j\omega R_{INT} C_{INT}}.$$

Equating both expressions and solving for $V_O/(V_2–V_1)$ yields the transfer function of the output stage:

$$\frac{V_O}{V_2 - V_1} = G_2\left(\frac{j\frac{f}{f_0 G_2}}{1 + j\frac{f}{f_0 G_2}}\right) = G_2\left(\frac{j\frac{f}{f_0'}}{1 + j\frac{f}{f_0'}}\right).$$

Figure 4. INA128 with OPA2132 providing low-pass filter and external gain stage



To return to the specified f_0 of 0.05 Hz requires the increase of the time constant by the factor G_2, thus quickly leading to prohibitive values for R_{INT} and C_{INT}.

There are two alternatives to design around this problem. Either (1) change the gain settings of G_1, G_2, and G_{TOT} until moderate values for R_{INT} and C_{INT} can be found, or (2) make $G_2 = 1$ and perform the final signal boost via a separate gain stage (Figure 4).

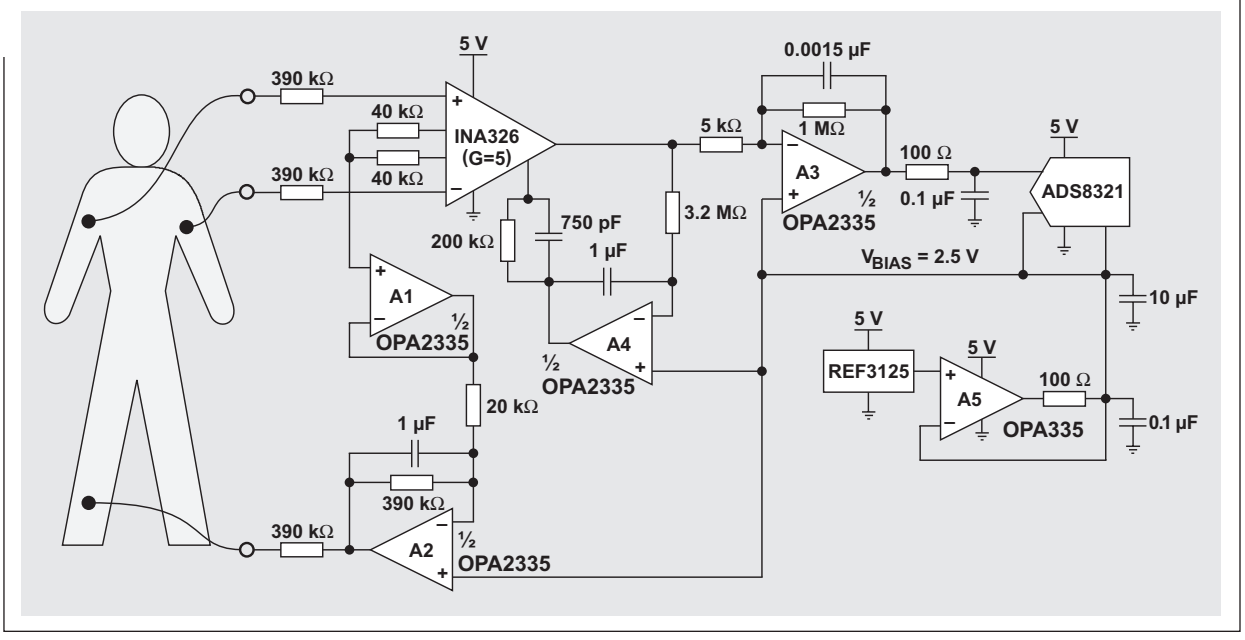
The latter approach, which is the easier one, provides the following benefits:

- Standard INAs with unity-gain output stages, such as INA128 or INA118, can be used. Both devices allow for input gains from 1 to 10000, providing a maximum non-linearity of 0.002%.
- Gain-booster A4 and integrator A5 can be designed with the dual low-noise amplifier OPA2132 with an input-referred noise of 8 nV/√Hz.
- The adjustment of G_1 is independent from G_2 and f_0, allowing the input gain to be set for maximum input common-mode range.
- The RC values defining the integrator time constant now reflect the real lower-bandwidth limit, f_0.
- The final gain stage A4 allows independent adjustment of any desired gain value and performs low-pass filtering of high-frequency noise.

Single-supply applications

Portable ECG equipment requiring single-supply operation can use the high-precision analog front end in Figure 5.

Figure 5. High-precision analog front end of a portable ECG application



Both types of amplifiers, the instrumentation amplifier INA326 and the dual precision amplifier OPA2335, operate from a single 5-V supply and apply autozeroing techniques, keeping the initial offset and offset drift over temperature and time near zero.

The input gain of the INA326 is set to 5 via $G_1 = 2R_2/R_G = 2(200\ k\Omega/80\ k\Omega)$. The 750-pF capacitor parallel to R_2 cancels resistor noise. The 3-dB frequency of the integrator A4 is set to 0.05 Hz, while the output stage around A3 provides a gain of $G_2 = 1\ M\Omega/5\ k\Omega = 200$. The precision voltage reference, REF3125, provides low-noise biasing of the 2.5-V bias voltage to the amplifiers and the 16-bit, 100-kSPS, SAR-ADC ADS8321.

To further reject 50/60-Hz noise, the input common-mode voltage is fed back via the amplifiers A1 and A2 to the right leg of the patient. This approach requires only a few microamps of current to significantly improve the common-mode rejection and to ensure compliance with the UL544 standard.

Summary

This article has described extension of the input common-mode range and filtering of large DC potentials in high-gain signal conditioners with three-op-amp INAs.

Further application information, in particular about high-precision, single-supply INAs, is available at www.ti.com, keyword "instrumentation amplifier."

Related Web sites

amplifier.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with ADS8321, INA118, INA128, INA326, OPA335, OPA2132, OPA2227, OPA2335, or REF3125

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