Designing DC/DC converters based on ZETA topology

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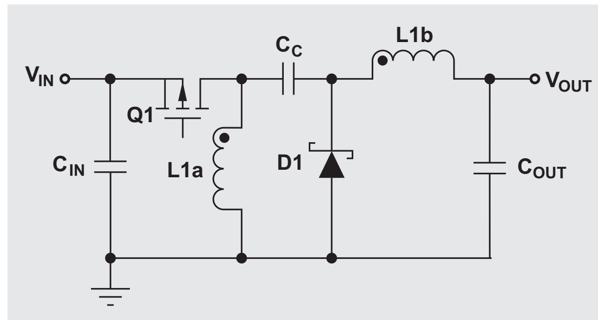
Introduction

Similar to the SEPIC DC/DC converter topology, the ZETA converter topology provides a positive output voltage from an input voltage that varies above and below the output voltage. The ZETA converter also needs two inductors and a series capacitor, sometimes called a flying capacitor. Unlike the SEPIC converter, which is configured with a standard boost converter, the ZETA converter is configured from a buck controller that drives a high-side PMOS FET. The ZETA converter is another option for regulating an unregulated input-power supply, like a low-cost wall wart. To minimize board space, a coupled inductor can be used. This article explains how to design a ZETA converter running in continuous-conduction mode (CCM) with a coupled inductor.

Figure 1. Simple circuit diagram of ZETA converter



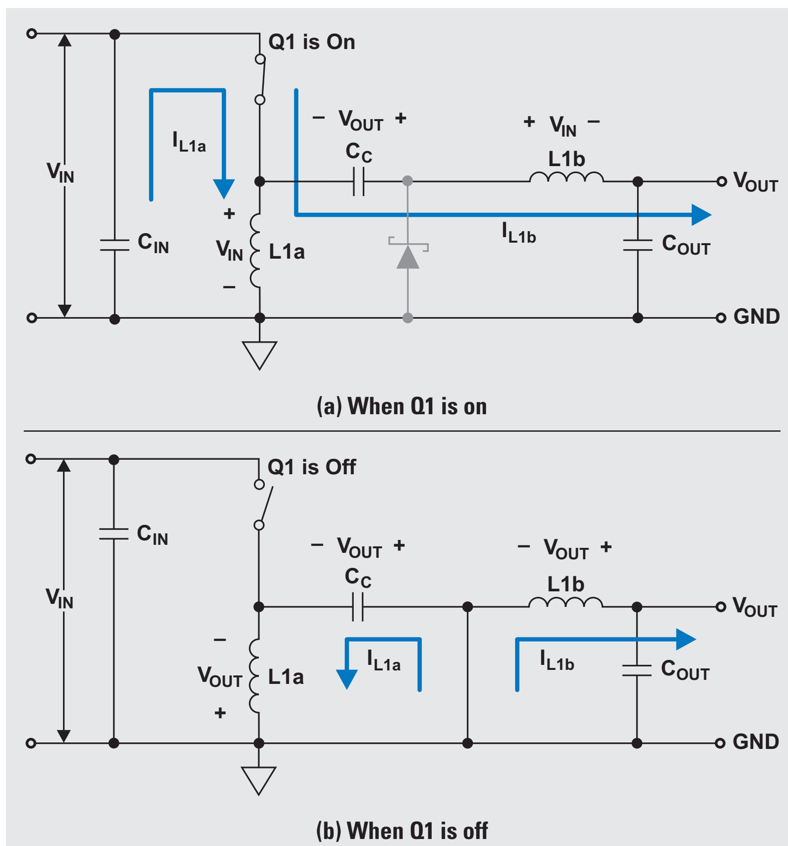
Basic operation

Figure 1 shows a simple circuit diagram of a ZETA converter, consisting of an input capacitor, C_{IN}; an output capacitor, C_{OUT}; coupled inductors L1a and L1b; an AC coupling capacitor, C_C; a power PMOS FET, Q1; and a diode, D1. Figure 2 shows the ZETA converter operating in CCM when Q1 is on and when Q1 is off.

To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when both switches are off and not switching. Capacitor C_C will be in parallel with C_{OUT}, so C_C is charged to the output voltage, V_{OUT}, during steady-state CCM. Figure 2 shows the voltages across L1a and L1b during CCM operation.

When Q1 is off, the voltage across L1b must be V_{OUT} since it is in parallel with C_{OUT}. Since C_{OUT} is charged to V_{OUT}, the voltage across Q1 when Q1 is off is $V_{IN} + V_{OUT}$; therefore the voltage across L1a is $–V_{OUT}$ relative to the drain of Q1. When Q1 is on, capacitor C_C, charged to V_{OUT}, is connected in series with L1b; so the voltage across L1b is $+V_{IN}$, and diode D1 sees $V_{IN} + V_{OUT}$.

Figure 2. ZETA converter during CCM operation



The currents flowing through various circuit components are shown in Figure 3. When Q1 is on, energy from the input supply is being stored in L1a, L1b, and C_C. L1b also provides I_{OUT}. When Q1 turns off, L1a's current continues to flow from current provided by C_C, and L1b again provides I_{OUT}.

Duty cycle

Assuming 100% efficiency, the duty cycle, D, for a ZETA converter operating in CCM is given by

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}. \quad (1)$$

This can be rewritten as

$$\frac{D}{1-D} = \frac{I_{IN}}{I_{OUT}} = \frac{V_{OUT}}{V_{IN}}. \quad (2)$$

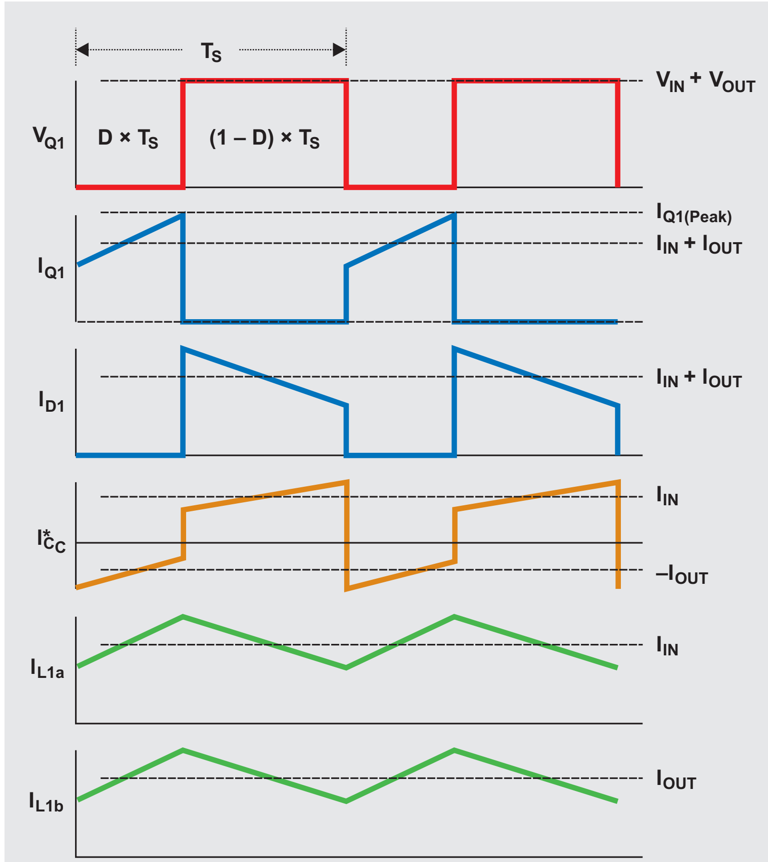
D_{max} occurs at $V_{IN(min)}$, and D_{min} occurs at $V_{IN(max)}$.

Selecting passive components

One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current, $\Delta I_{L(PP)}$, to allow. Too much increases EMI, while too little may result in unstable PWM operation. A rule of thumb is to assign a value for K between 0.2 and 0.4 of the average input current. A desired ripple current can be calculated as follows:

$$\text{Desired } \Delta I_{L(PP)} = K \times I_{IN} = K \times I_{OUT} \times \frac{D}{1-D}. \quad (3)$$

Figure 3. ZETA converter's component currents during CCM



*Measured flowing into C_C from Q1's drain.

In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the coupling forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, the inductors do not have equal inductance and the ripple currents will not be exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what would be needed if there were two separate inductors, as shown in Equation 4:

$$L1a_{min} = L1b_{min} = \frac{1}{2} \times \frac{V_{IN} \times D}{\Delta I_{L(PP)} \times f_{SW(min)}} \quad (4)$$

To account for load transients, the coupled inductor's saturation current rating needs to be at least 1.2 times the steady-state peak current in the high-side inductor, as computed in Equation 5:

$$I_{L1a(PK)} = I_{OUT} \times \frac{D}{1-D} + \frac{\Delta I_L}{2} \quad (5)$$

Note that $I_{L1b(PK)} = I_{OUT} + \Delta I_L/2$, which is less than $I_{L1a(PK)}$.

Like a buck converter, the output of a ZETA converter has very low ripple. Equation 6 computes the component of the output ripple voltage that is due solely to the capacitance value:

$$\Delta V_{C_{OUT}(PP)} = \frac{\Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}]}{8 \times C_{OUT} \times f_{SW(min)}}, \quad (6)$$

where $f_{SW(min)}$ is the minimum switching frequency. Equation 7 computes the component of the output ripple voltage that is due solely to the output capacitor's ESR:

$$\Delta V_{ESR\_C_{OUT}(PP)} = \Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}] \times ESR_{C_{OUT}} \quad (7)$$

Note that these two ripple-voltage components are phase-shifted and do not directly add together. For low-ESR (e.g., ceramic) capacitors, the ESR component can be ignored. A minimum capacitance limit may be necessary to meet the application's load-transient requirement.

The output capacitor must have an RMS current rating greater than the capacitor's RMS current, as computed in Equation 8:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}]}{\sqrt{3}} \quad (8)$$

The input capacitor and the coupling capacitor source and sink the same current levels, but on opposite switching cycles. Similar to a buck converter, the input capacitor and the coupling capacitor need the RMS current rating,

$$I_{C_{IN}(RMS)} = I_{C_C(RMS)} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN(min)}}}. \quad (9)$$

Equations 10a and 10b compute the component of the output ripple voltage that is due solely to the capacitance value of the respective capacitors:

$$\Delta V_{C_{IN}(PP)} = \frac{D_{max} \times I_{OUT}}{C_{IN} \times f_{SW(min)}} \quad (10a)$$

$$\Delta V_{C_C(PP)} = \frac{D_{max} \times I_{OUT}}{C_C \times f_{SW(min)}} \quad (10b)$$

Equations 11a and 11b compute the component of the output ripple voltage that is due solely to the ESR value of the respective capacitors:

$$\Delta V_{ESR\_C_{IN}(PP)} = (I_{IN(max)} + I_{OUT}) \times ESR_{C_{IN}} = \frac{I_{OUT}}{1 - D_{max}} \times ESR_{C_{IN}} \quad (11a)$$

$$\Delta V_{ESR\_C_C(PP)} = (I_{IN(max)} + I_{OUT}) \times ESR_{C_C} = \frac{I_{OUT}}{1 - D_{max}} \times ESR_{C_C} \quad (11b)$$

Again, the two ripple-voltage components are phase-shifted and do not directly add together; and, for low-ESR capacitors, the ESR component can again be ignored. A typical ripple value is less than 0.05 times the input voltage for the input capacitor and less than 0.02 times the output voltage for the coupling capacitor.

Selecting active components

The power MOSFET, Q1, must be carefully selected so that it can handle the peak voltage and currents while minimizing power-dissipation losses. The power FET's current rating will determine the ZETA converter's maximum output current.

As shown in Figure 3, Q1 sees a maximum voltage of $V_{IN(max)} + V_{OUT}$. Q1 must have a peak-current rating of

$$I_{Q1(PK)} = I_{L1a(PK)} + I_{L1b(PK)} = I_{IN} + I_{OUT} + \Delta I_L. \quad (12)$$

At the ambient temperature of interest, the FET's power-dissipation rating must be greater than the sum of the conductive losses (a function of the FET's $r_{DS(on)}$) and the switching losses (a function of the FET's gate charge) as given in Equation 13:

$$\begin{aligned} P_{D\_Q1} &= P_{r_{DS(on)}} + P_{SWG} + P_{Gate} \\ &= I^2_{Q1(RMS)} \times r_{DS(on)} \\ &+ (V_{IN(max)} + V_{OUT}) \times I_{Q1(PK)} \times Q_{GD} / I_{Gate} \times f_{SW(max)} \\ &+ V_{Gate} \times Q_G \times f_{SW(max)}, \end{aligned} \quad (13)$$

where Q_{GD} is the gate-to-drain charge, Q_G is the total gate charge of the FET, I_{Gate} is the maximum drive current, and V_{Gate} is the maximum gate drive from the controller. Q1's RMS current is

$$I_{Q1(RMS)} = (I_{IN(max)} + I_{OUT}) \times \sqrt{D_{max}} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(min)} \times \sqrt{D_{max}}}. \quad (14)$$

The output diode must be able to handle the same peak current as Q1, $I_{Q1(PK)}$. The diode must also be able to withstand a reverse voltage greater than Q1's maximum voltage ($V_{IN(max)} + V_{OUT}$) to account for transients and ringing. Since the average diode current is the output current, the diode's package must be capable of dissipating up to $I_{OUT} \times V_{FWD}$, where V_{FWD} is the Schottky diode's forward voltage at I_{OUT}.

Loop design

The ZETA converter is a fourth-order converter with multiple real and complex poles and zeroes. Unlike the SEPIC converter, the ZETA converter does not have a right-half-plane zero and can be more easily compensated to achieve a wider loop bandwidth and better load-transient results with smaller output-capacitance values. Reference 1 provides a good mathematical model based on state-space averaging. The model excludes inductor DC resistance (DCR) but includes capacitor ESR. Even though the converter in Reference 1 uses ceramic capacitors, for the following design example, the inductor DCR was substituted for the capacitor ESR so that the model would more closely match measured values. The open-loop gain bandwidth (i.e., the frequency where the gain crosses zero with an acceptable phase margin of typically 45°), should be greater than the resonant frequency of L1b and C_C so that the feedback loop can dampen the nonsinusoidal ripple on the output with fundamental frequency at that resonant frequency.

Design example

For this example, the requirements are for a 12-V, 1-W supply with η = 0.9 peak efficiency. The load is steady-state, so few load transients are expected. The 2-A input supply is 9 to 15 V. A nonsynchronous voltage-mode controller, the Texas Instruments TPS40200, was selected, running with a switching frequency between 340 and 460 kHz. The maximum allowed ripple at the input and flying capacitor is respectively 1% of the maximum voltage across each. The maximum output ripple is 25 mV, and the maximum ambient temperature is 55ºC. Because EMI is not a concern, an inductor with a lower inductance value was selected by using the minimum input voltage. Table 1 on the next page summarizes the design calculations given earlier. Equations 7 through 9 and Equation 11 were ignored because low-ESR ceramic capacitors with high RMS current ratings were used.

Table 1. Computations for example ZETA-converter design

BASED ON DESIGN EQUATION	COMPUTATION (ASSUMING η = 1)	ADJUSTED FOR η = 0.9	SELECTED COMPONENT/RATING
Passive Components			
(1)	$D_{max} = \frac{12\text{ V}}{12\text{ V}+9\text{ V}} = 0.57$	N/A	N/A
(1)	$D_{min} = \frac{12\text{ V}}{12\text{ V}+15\text{ V}} = 0.44$	N/A	N/A
(2)	$I_{IN(max)} = 1\text{ A}\times\frac{0.57}{1-0.57} = 1.33\text{ A}$	$\frac{1.33\text{ A}}{0.9} = 1.48\text{ A}$	N/A
(3)	Desired $\Delta I_{L(PP)}$ [at $V_{IN(min)}$] $= 0.3\times1.33\text{ A} = 0.4\text{ A}$	$\frac{0.4\text{ A}}{0.9} = 0.44\text{ A}$	N/A
(4) using $V_{IN(min)}$	$L1a = L1b = \frac{1}{2}\times\frac{9\text{ V}\times0.57}{0.40\text{ A}\times340\text{ kHz}} = 18.9\ \mu\text{H}$	$18.9\ \mu\text{H}\times0.9 = 17.0\ \mu\text{F}$	Coilcraft MSD1260: 22 µH – I_{RMS} = 1.76 A in each winding simultaneously, I_{SAT} = 5 A
(4) at $V_{IN(min)}$	Actual $\Delta I_{L(PP)} = \frac{1}{2}\times\frac{9\text{ V}\times0.57}{22\ \mu\text{H}\times340\text{ kHz}} = 0.34\text{ A}$	N/A	
(5)	$I_{L1a(PK)} = 1.33\text{ A}+\frac{0.34\text{ A}}{2} = 1.50\text{ A}$	$1.48\text{ A}+\frac{0.34\text{ A}}{2} = 1.65\text{ A}$	
(4) at $V_{IN(max)}$	Actual $\Delta I_{L(PP)} = \frac{1}{2}\times\frac{15\text{ V}\times0.44}{22\ \mu\text{H}\times340\text{ kHz}} = 0.45\text{ A}$	N/A	N/A
(6)	$C_{OUT(min)} = \frac{0.44\text{ A}}{8\times0.025\text{ V}\times340\text{ kHz}} = 6.5\ \mu\text{F}$	N/A	Two 10-µF, 25-V X5R ceramics and one 4.7-µF, 25-V X5R ceramic to provide good load-transient response and to accommodate ceramic capacitor derating
(10a) for C_{IN}	$C_{IN(min)} = \frac{0.57\times1\text{ A}}{0.01\times15\text{ V}\times340\text{ kHz}} = 11.2\ \mu\text{F}$	$\frac{11.2\ \mu\text{F}}{0.9} = 12.4\ \mu\text{F}$	Two 10-µF, 25-V X5R ceramics and one 4.7-µF, 25-V X5R ceramic to accommodate ceramic capacitor derating
(10b) for C_C	$C_{C(min)} = \frac{0.57\times1\text{ A}}{0.01\times12\text{ V}\times340\text{ kHz}} = 14\ \mu\text{F}$	$\frac{14\ \mu\text{F}}{0.9} = 15.6\ \mu\text{F}$	Three 10-µF, 25-V X5R ceramics to accommodate ceramic capacitor derating
Active Components			
(12)	$I_{Q1(PK)} = 1.33\text{ A}+1\text{ A}+0.34\text{ A} = 2.67\text{ A}$	$1.48\text{ A}+1\text{ A}+0.34\text{ A} = 2.82\text{ A}$	N/A
(14)	$I_{Q1(RMS)} = \frac{1\text{ A}\times12\text{ V}}{9\text{ V}\times\sqrt{0.57}} = 1.77\text{ A}$	$\frac{1.77\text{ A}}{0.9} = 1.96\text{ A}$	Fairchild FDC365P: –35-V, –4.3-A, 55-mΩ PFET
(13)	$P_{D\_Q1} = (1.96\text{ A})^2\times55\text{ m}\Omega + (15\text{ V}+12\text{ V})\times2.82\text{ A}\times2.2\text{ nC}/0.3\text{ A}\times460\text{ kHz} + 8\text{ V}\times15\text{ nC}\times460\text{ kHz} = 0.54\text{ W}$	Included	
—	$P_{D\_D1} = 1\text{ A}\times0.5\text{ V} = 0.5\text{ W}$	N/A	MBRS340: 40 V, 3 A, SMC

Figure 4. ZETA-converter design with 9- to 15-V V_{IN} and 12-V V_{OUT} at 1 A

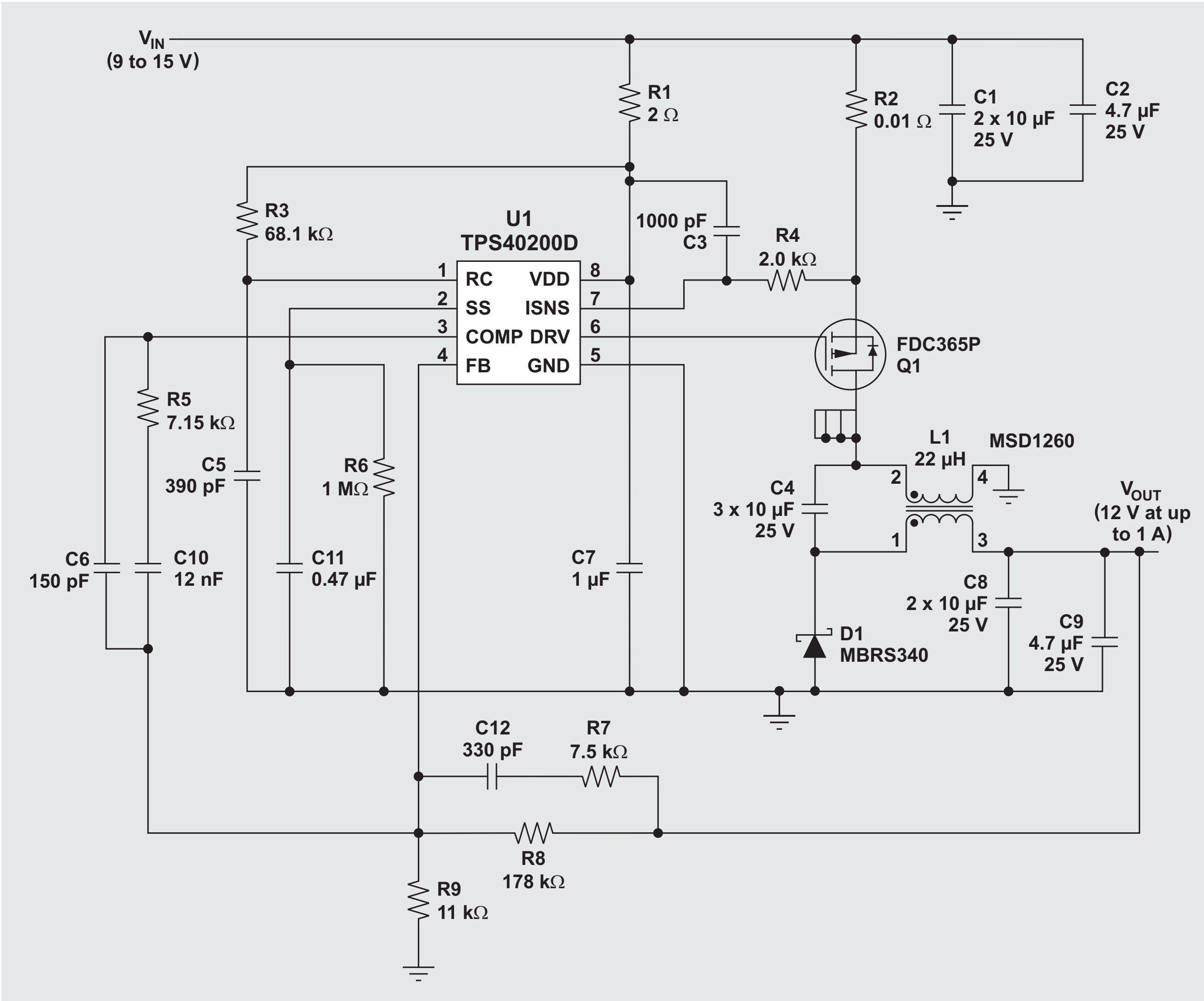
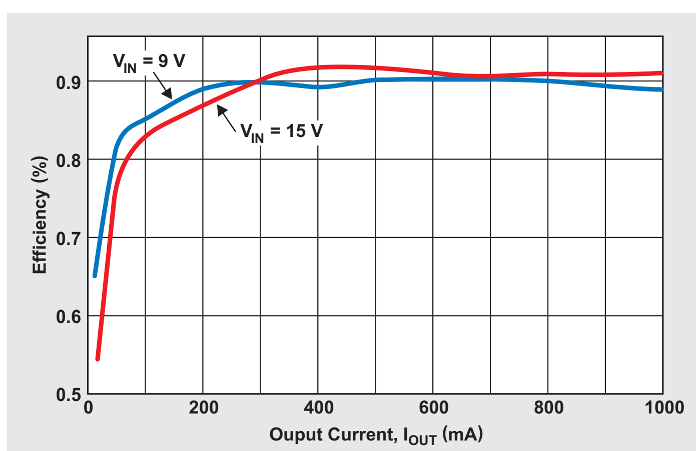


Figure 4 shows the schematic and Figure 5 the efficiency of the ZETA converter. On the next page, Figure 6 shows the converter's operation in deep CCM, and Figure 7 shows the loop response.

Conclusion

Like the SEPIC converter, the ZETA converter is another converter topology to provide a regulated output voltage from an input voltage that varies above and below the output voltage. The benefits of the ZETA converter over the SEPIC converter include lower output-voltage ripple and easier compensation. The drawbacks are the requirements for a higher input-voltage ripple, a much larger flying capacitor, and a buck controller (like the TPS40200) capable of driving a high-side PMOS.

Figure 5. Efficiency of example ZETA-converter design



Reference

1. Eng Vuthchhay and Chanin Bunlaksananusorn, "Dynamic modeling of a zeta converter with state-space averaging technique," *Proc. 5th Int. Conf. Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON) 2008,* Vol. 2, pp. 969–972.

Related Web sites

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Figure 6. Operation at V_{IN} = 9 V and I_{OUT} = 1 A

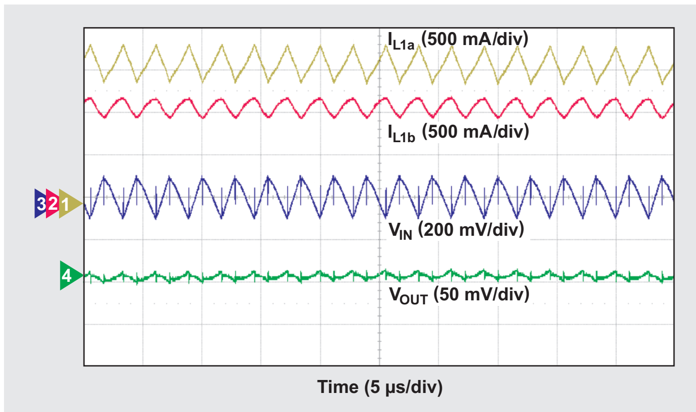
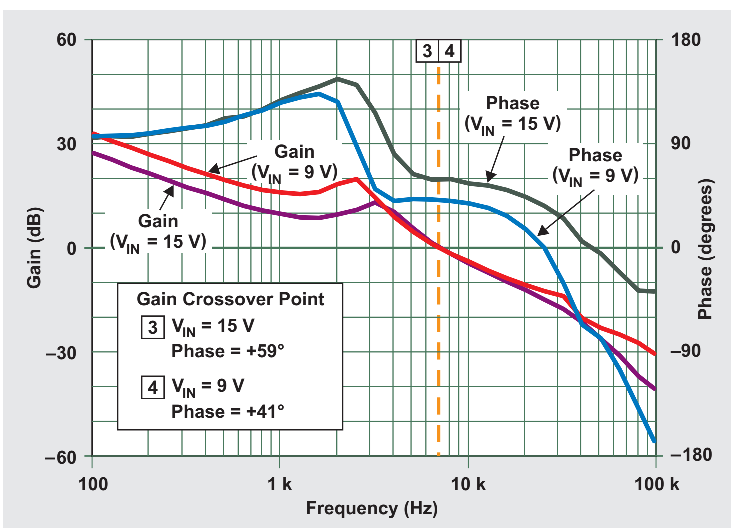


Figure 7. Loop response at V_{IN} = 9 V and 15 V, and I_{OUT} = 1 A



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