Add a digitally controlled PGA with noise filter to an ADC

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Introduction

In some applications, a signal with high dynamic range needs to be digitized. A common method of digitization is to add an external programmable gain amplifier (PGA) in front of the analog-to-digital converter (ADC). Only a few microcontrollers have internal PGAs. However, nowadays PGAs are available in a single chip with one or multiple input channels. Such PGAs add additional costs to the system and usually consume more power as a fixed-gain solution.

This article describes how to implement a PGA by using just a single resettable integrator, with the following benefits:

- The solution is economical and easy to design.
- Gain can be digitally controlled and calibrated.

Figure 1. Basic block diagram of the PGA
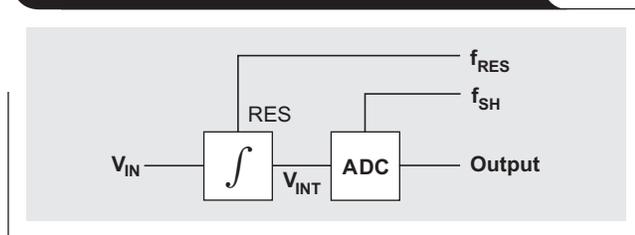
- Signal noise is reduced with a low-pass filter, which is especially useful in noisy microcontroller environments and for small analog signals. The cutoff frequency automatically adjusts with the chosen sample rate.
- The zero-level voltage reference can be controlled externally, which makes it handy for single-supply circuits where the zero level usually is set to $V_{REF}/2$.

The basic circuit

Figure 1 shows the basic circuit, where an integrator is added in front of the ADC. The integrator can be reset with the signal f_{RES} (1 = integrator is reset). The ADC is controlled with the signal f_{SH}, which connects to the ADC's sample-and-hold (SH) unit (1 = sample, 0 = hold). A falling edge starts the analog-to-digital conversion cycle.

Figure 2 shows a single analog-to-digital (A/D) conversion cycle with the circuit from Figure 1. The cycle is split into four periods:

1. *Integrator reset period:* Resets the integrator to "0."
2. *Integration period:* The integrator reset signal is released and the integrator starts to integrate.
3. *Sample period:* The ADC's sample-and-hold unit samples the integrator output, V_{INT}.
4. *A/D conversion period:* The sample-and-hold unit holds the voltage, and the ADC starts to convert.

Figure 2. Single A/D cycle with gain = 1
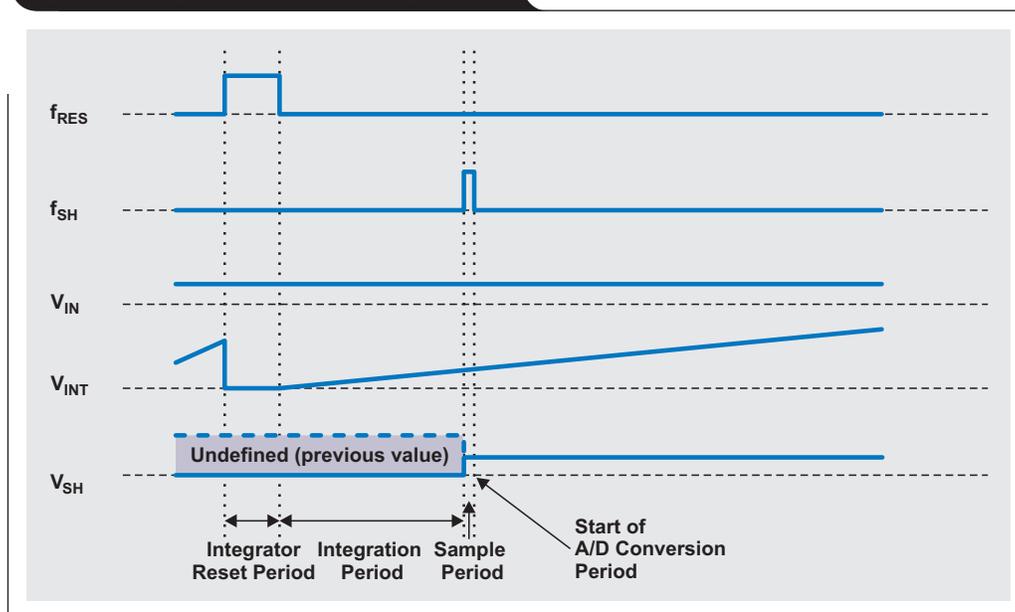
Figure 3. Single A/D cycle with PGA gain = 2
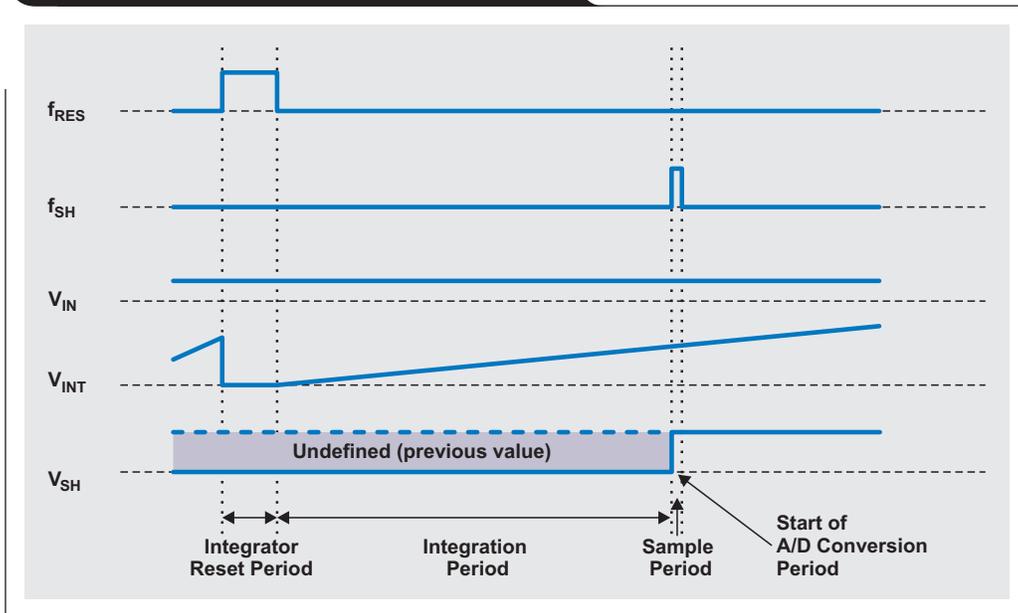
The duration of the integration period defines the PGA's gain, as the voltage on its input influences the slope linearly: A doubling of the integration time doubles the gain. Figure 3 demonstrates this influence. The integration period is doubled and the voltages V_{SH} are increased by a factor of two.

A nice benefit from this integration scheme is that the input signal is averaged during the integration period, which reduces out-of-band noise from the input signal, V_{IN}. The filter's impulse response is of finite duration and is comparable to the behavior of a digital FIR filter rather than to that of a standard low-pass filter.

Practical configuration of a PGA

An inverting amplifier can be built with a single operational amplifier (Figure 4). The integrator can be reset by short-circuiting the capacitor, C, with the switch element, S. The components R and C influence the integrator's gain.

The signal V_{COM} defines the integrator's zero-level voltage and can be set, for example, to $V_{REF}/2$, where V_{REF} is the ADC's reference voltage. The integrator is reset to this voltage when the capacitor is discharged. Usually a V_{COM} signal is present in the system anyway. Often it is used as a virtual ground or bias voltage for single-supply analog signal chains.

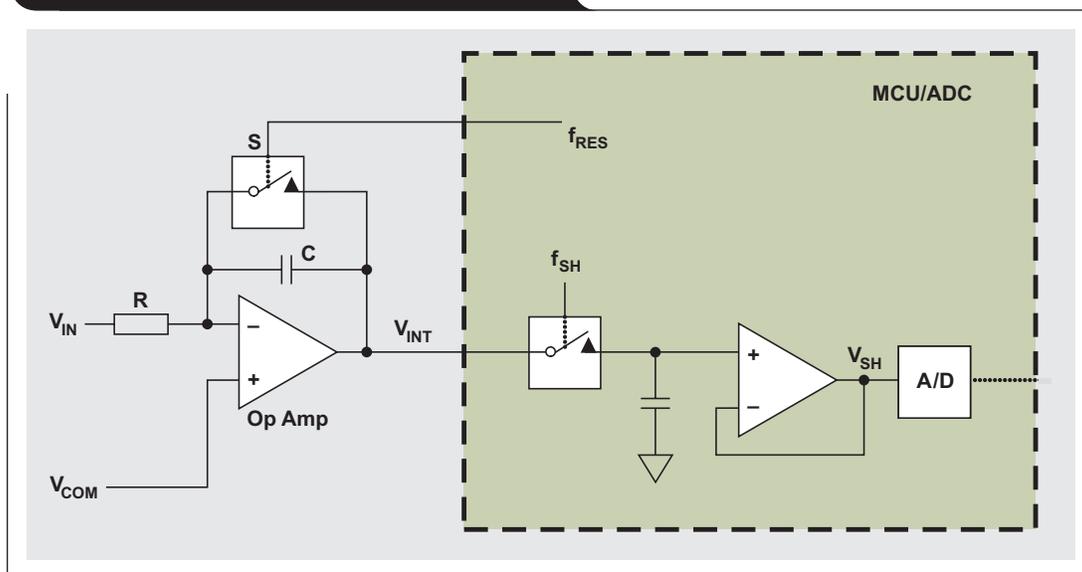**Figure 4. Practical configuration of the PGA**

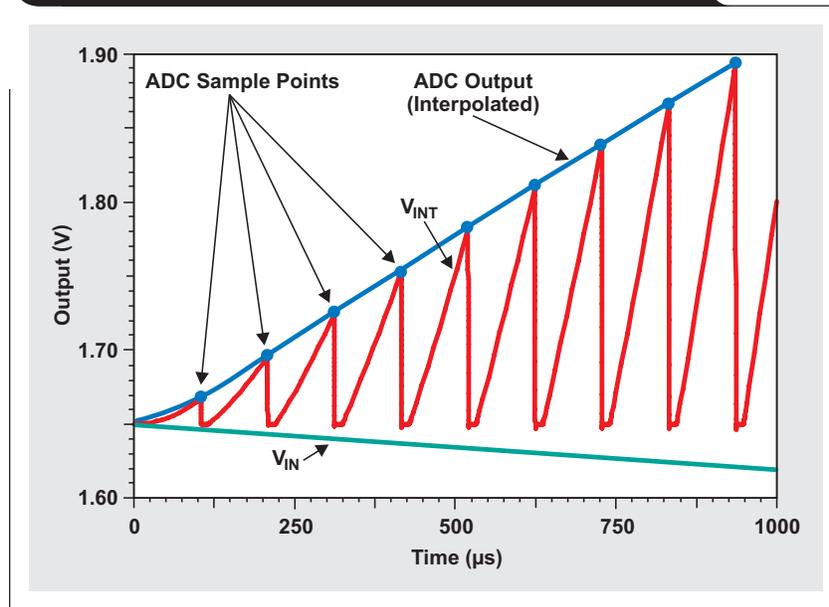Figure 5. SPICE-simulation results of circuit in Figure 4

Figure 5 shows SPICE-simulation results of the circuit in Figure 4. The blue dots mark the sample moments of the ADC. As shown, the signal V_{IN} is amplified by a factor of about –8. The red signal is inverted to the green due to the integrator's inverting behavior.

How it works

The sample rate, the maximum desired gain, and the A/D conversion time influence the selection of the integration constant defined by the components R and C. As shown in Figures 2 and 3, the integrator needs enough time to reach the gain, G, within the duration of the integration period, t. The dependency of G and t can be calculated as

$$G = \frac{-t}{R \times C}.$$

The close time (integrator reset period) of the switch (S) depends on the impedance of the switch and the value of the capacitor (C).

Calibration

Tolerances of R and C lead to modification of the gain factor. The capacitor should have a very small piezo effect to get a very linear integration. Capacitors can have an especially large tolerance--for example, 20%. This is just the initial tolerance, which can be calibrated once. Tolerances due to aging effects are very small (less than 1% per year).

The gain and offset can be calibrated in the same way as with a standard ADC by applying known voltages to the input and calculating correction values for offset and gain based on expected and actual values. The calibration can be done for each gain factor used in the application.

Circuit variations

Using the PGA as a low-pass filter only (gain = 1)

In case input-signal amplification is not wanted, it is possible to use the PGA circuit only as a noise filter. The integrator constant can be set to a value that leads to a fixed

gain of 1. In this case the integration phase can start immediately after the sample, and the hold stage can be set to hold mode (Figure 6).

Non-inverting integration

The circuit in Figure 4 uses an inverting integrator. When this inversion is not acceptable, it is possible to use a non-inverting integrator by adding a single-supply inverting buffer in front of the integrator.

Conclusion

This article has presented a cost-effective and simple way to implement PGA functionality in cost- and power-driven applications. Its filtering properties also reduce costs by eliminating the need for an external filter, which is often

present in front of ADCs. Nevertheless, this method cannot replace a PGA in all cases; for example, high sample rates or very large gain variations make such a solution difficult to realize.

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Figure 6. PGA circuit used as a filter only (gain = 1)
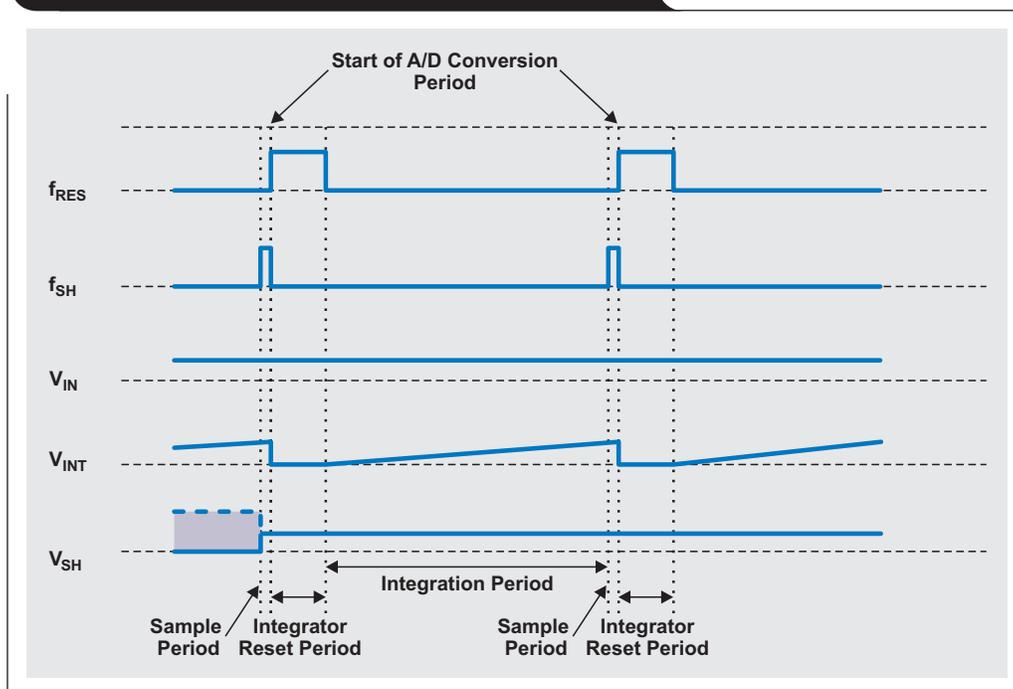
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