How to use power scaling to maximize power savings in a SAR ADC system

By Cynthia Sosa
Applications Engineer, Precision ADC - SAR ADC

Introduction

Designs for low-power analog-to-digital converters (ADCs) need to minimize power consumption while maintaining high performance. By modifying the digital timing and power-supply voltages of a successive-approximation register (SAR) ADC, the ADC's power-scaling capabilities can be used to achieve the design goals.

This article describes different elements in an ADC system that consume power, provides methods for calculating total power consumption, and discusses the design of a front-end driving circuit to maximize overall power savings.

ADC power consumption

The SAR ADC architecture allows its operational characteristics to be modified to scale down power consumption. Before describing the modifications, first consider the two basic phases to the internal operation of a SAR ADC: acquisition and conversion. During the acquisition phase, shown at left in Figure 1, switch 2 opens, disconnecting the internal ADC comparator from the sample and hold circuit. The conversion phase begins when the sample-and-hold circuit disconnects from the external circuitry and connects to the ADC comparator.

The average power consumed by the converter (the power per cycle) is the sum of the power consumed during both the acquisition and conversion phases divided by the cycle time. During the acquisition phase, the power consumed is solely from the quiescent current because the internal circuitry is not operating; this is the zero-power phase. The majority of power consumption occurs during the conversion phase because the internal circuitry for the capacitive digital-to-analog converter (CDAC) generates the binary-weighted voltages and the internal comparator performs the bit decisions. Digital communication usually occurs during the conversion phase and Figure 2 illustrates an example of SPI digital communications of a conversion cycle.

It is possible to reduce the ADC's power consumption by decreasing the sampling rate. A lower sampling rate increases the acquisition phase, which increases the time the ADC is in the zero-power range. Reducing the sampling rate will also result in a longer cycle time, which also decreases the average power consumption.

Figure 1. The two phases of a SAR ADC: acquisition and conversion

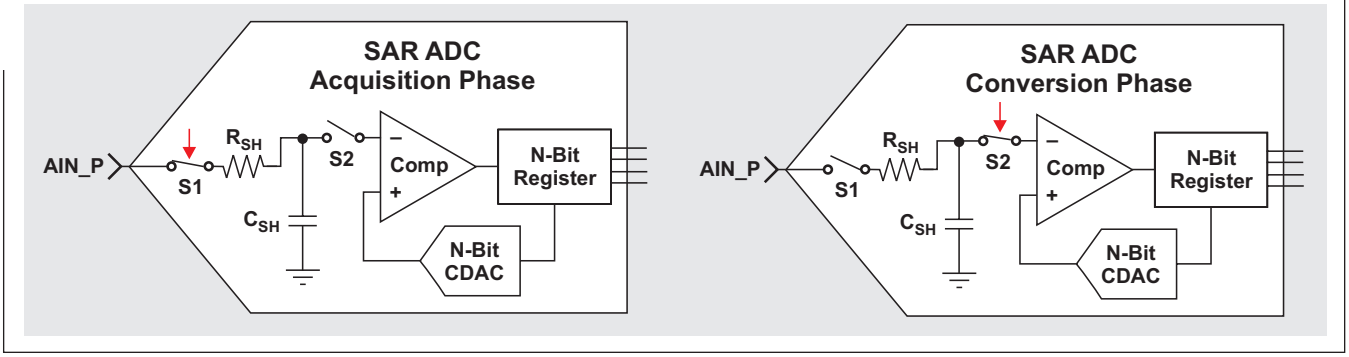
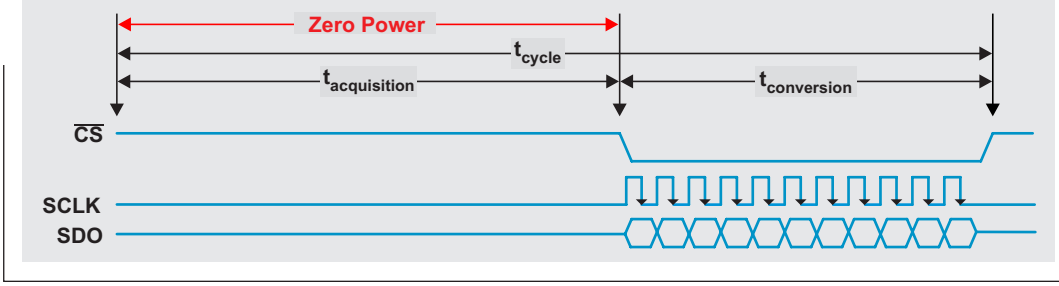


Figure 2. Example SPI digital communications of conversion cycle



Different data converters will require different approaches to adjust the timing. The most common device type has an internal clock that sets the conversion time. Regardless of cycle time, the conversion phase will always remain the same length of time. Increasing the acquisition time in these device types requires a decrease in the operating sampling rate. A constant conversion phase will result in a longer cycle time dominated by the acquisition phase.

Another device type uses an external clock and relies on the frequency of the clock input to increase the acquisition phase. The clock frequency is inversely correlated with the length of the conversion phase; thus, increasing the clock-input frequency decreases the conversion time. Increasing the clock frequency without changing the sampling rate will result in an increase in the acquisition phase, while the cycle time remains the same. Decreasing the sampling rate further adds to the power savings by elongating the cycle time.

There are other uncommon timing requirements not covered. It is best to read the device datasheet to confirm its operation.

Power consumption of the ADC power supplies

A SAR ADC will usually consist of two separate power supplies: analog and digital. Each can scale down its respective power consumption by modifying the device's operation and reducing supply voltages. Some devices have a single power supply but the following general methods still apply.

The analog voltage supply (AVDD) powers the device's internal conversion circuitry; thus, each conversion contributes to the power consumed by the supply. The more conversions per unit time, the more power the device dissipates. The conversion frequency (in other words, the sampling rate) is directly proportional to the power consumed.

Equation 1 calculates the power consumption of the analog power supply (P_{AVDD}), which shows how decreasing the analog voltage reduces power. The AVDD may determine the input range on certain devices; thus, it's best to use the lowest AVDD the system can support. The current drawn from AVDD (I_{AVDD}) is usually found in the device data sheet based on the sampling rate (f_S).

$$P_{AVDD} = AVCC \quad I_{AVDD} \tag{1}$$

If I_{AVDD} is not available, Equation 2 can be used to calculate I_{AVDD} using the analog current drawn at 1 MHz ($I_{AVDD@1\ MHz}$), a very common parameter:

$$I_{AVDD} = \left(I_{AVDD@1\ MHz}\right) \quad \frac{f_S}{1\ MHz} \tag{2}$$

The digital voltage supply (DVDD) is used for the device's digital communications. The most common digital-communication protocols are serial-peripheral interface (SPI) and inter-integrated circuit (I^2C). For a device that supports SPI, the line for serial-data output (SDO) determines the ADC power consumption, since it is the only signal controlled by the device. The microcontroller supplies the power consumed by the other digital lines—including serial-data input (SDI), clock (CLK), and chip select (CS)—as it drives these bus lines.

The average digital-power consumption (P_{DVDD}) is a function of DVDD and DVDD current (I_{DVDD}), as shown in Equation 3. The digital supply consumption is directly related to DVDD; thus, use the lowest digital supply voltage that the system can support.

$$P_{DVDD} = DVDD \quad I_{DVDD} \tag{3}$$

The DVDD current shown in Equation 4 comprises DVDD, the frequency of state changes to the digital output signal ($f_{digital\_output}$), and the load capacitance of the digital output line ($C_{digital\_output}$). The current is drawn from charging and discharging the capacitance on the digital-output line when the digital signal transitions to a different logic level. If the digital communications function at a higher frequency, the charging and discharging of the bus capacitance occurs more frequently per unit time; thereby increasing the digital current.

$$I_{DVDD} = f_{digital\_output} \quad DVDD \quad C_{digital\_output} \tag{4}$$

The frequency of state changes is determined by the number of output bits (usually the resolution of the device) divided by the sampling rate. The TI Analog Engineer's Calculator[1] can help determine the capacitance of the printed circuit board, but also add in any external capacitance (including the pin's capacitance) to the total load capacitance. In lower-power applications, SPI is popular because it only dissipates power when the digital signal transitions logic states.

When using I^2C, the power consumption is determined by the pullup resistors applied to the data lines and the communication's frequency. Using the largest-value pullup resistors the system can support will minimize power dissipation when driving the open-drain output low.

When the device's communication operates continuously, the output is frequently pulled low causing significant power consumption. On the other hand, when the I^2C bus is idle, it will not consume power. Designers will employ I^2C in low-power applications that use polling and the device communicates infrequently.

In summary, one method to decrease the average power consumption is to use the lowest possible power-supply voltages and another approach is to decrease the sampling rate of the device. These changes will help reduce both digital and analog power consumption. The overall ADC power-supply consumption is the addition of the two averages' of supply-power consumption: $P_{total} = P_{AVDD} + P_{DVDD}$.

Power consumption of the ADC front-end driver circuit

A typical input-driving circuit for a SAR ADC consists of an amplifier, usually an operational amplifier (op amp), which must also be considered. An amplifier's power consumption is directly related to its bandwidth, which is a determining parameter in SAR ADC system performance. The sampling rate of the ADC determines the amplifier's bandwidth requirement. The amplifier should be able to charge the ADC sample-and-hold circuit to 0.5 least significant bits (LSB) within the allotted acquisition time to show good settling.

For a high sampling rate, the acquisition time is short and a high-bandwidth amplifier is required for good settling of the internal sample-and-hold capacitor. For a lower sampling rate, the acquisition time is longer; therefore, a low-bandwidth amplifier is sufficient for good settling. Reducing the sampling rate also reduces the amplifier's bandwidth requirement while still achieving good performance and enables the use of low-power, low-bandwidth amplifiers. When designing the front- end driving circuit consider TI Precision Labs – ADC: Front-End Component Selection,[2] as it explains how to select an amplifier with the proper bandwidth and the external resistor-capacitor (RC) charge-bucket circuit for an application. Keep in mind that a lower-power amplifier will have trade-offs, such as worse noise and slew-rate performance.

Amplifier bandwidth is directly related to its quiescent current and hence to its power consumption. Equation 5 calculates the average power consumed by an amplifier by multiplying the total supply voltage by the quiescent current.

$$P_{amp} = (V_+ - V_-) \times I_Q \quad (5)$$

The power supplies should also be at the lowest voltage the amplifier can support while still maintaining correct operation and performance. Figure 3 demonstrates the relationship between quiescent current and bandwidth for multiple amplifiers.

Applications that don't require an input driving amplifier would experience a large decrease in power consumption because of the eliminated amplifier circuit. This operation pertains to low-sampling-rate applications where a low-frequency voltage input connects directly to the input of a SAR ADC. There are trade-offs when using this topology, such as a decrease in effective number of bits (ENOB).

Measured results

Table 1 demonstrates the total system power using the ADS7042 ultra-low-power SAR ADC with AVDD = 3.3 V, DVDD = 3.3 V and the op-amp power supply at 4.5 V. These three measurements use different amplifiers in the front-end circuit to highlight the effects on total system power. A combination of a high sampling rate and the high-performing OPA320 op amp resulted in a total system power consumption of 7696.4 µW, which is magnitudes greater than a lower ADC sampling rate and the nanopower LPV811 amplifier, which resulted in a total of only 3.5 µW. At lower sampling rates, performance is still high, as the bandwidth requirement is lower.

Figure 3. Quiescent current versus bandwidth of multiple amplifiers

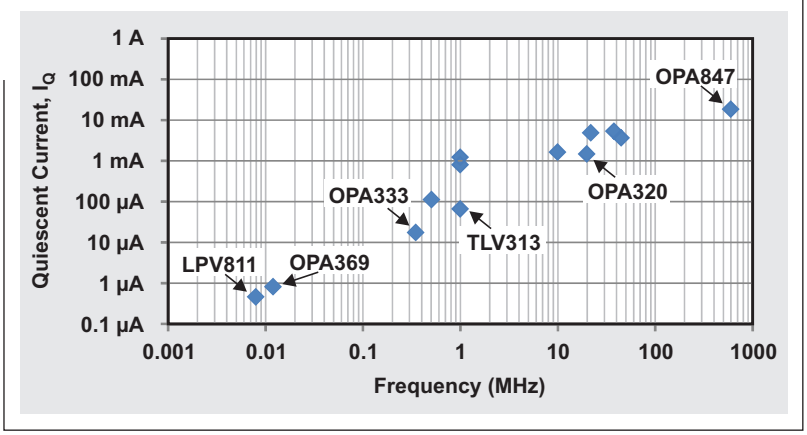


Table 1. Total system power consumption of the ADS7042

Amplifier	ADC Sampling Rate	Measured Amplifier Power	Measured ADC Analog Power	Measured ADC Digital Power	Total System Power
LPV811	1 kSPS	1.8 µW	0.737 µW	0.988 µW	3.5 µW
TLV313	100 kSPS	192.7 µW	73.1 µW	135.8 µW	464.3 µW
OPA320	1 MSPS	6386 µW	708.3 µW	655.2 µW	7696.4 µW

Other sources of power consumption

Reducing the sampling rate will also scale down other sources of power consumption within an ADC system, such as the reference voltage of the device. Devices often have an external reference voltage input used by the CDAC. The reference power consumption will decrease with lower sampling rates because the current consumption drawn by the CDAC occurs less frequently.

High-precision devices need an external reference whose noise and drift-error contributions must be kept small to avoid degrading the performance of the data-acquisition system. For devices such as the ADS7042, Table 1 results are based on using the analog power supply as a reference. The consumption of the external reference is included in the analog power and scales accordingly.

Conclusion

Reducing the sampling rate of a SAR ADC will reduce the consumption of an ADC system by minimizing the ADC digital, analog, and reference power consumption. A decreased sampling rate also permits for a decrease in the power consumption of the input driving amplifier; as the lower sampling rate lowers the bandwidth requirement. Reducing the supply voltages also minimizes power consumption. For maximum power savings while still maintaining high performance, use the lowest supported sampling rate and an amplifier with the lowest bandwidth that still meets performance requirements.

References

1. TI Design tool, “Analog Engineer’s Calculator,” (ANALOG-ENGINEER-CALC)
2. Peggy Liska, “TI Precision Labs – ADCs: Introduction to SAR ADC Front-End Component Selection,” TI training video (TIPL4401).
3. Rajan Arora, “I^2C Bus Pullup Resistor Calculation,” TI Application Report (SLVA689), February 2015.
4. Abhijeet Godbole, “Driving a SAR ADC Directly Without a Front-End Buffer Circuit,” TI Analog Engineer’s Circuit (SBAA256), January 2018.
5. Amit Kumbasi, Rafael Ordonez, and Harsha Munikoti, “18 bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power <1 mW,” TI Precision Designs (SLAU514), June 2013.

Related Web sites

Product information:

ADS7042, OPA320, LPV811

TI Precision Labs – ADCs

TI Precision Labs – Op Amps

TI Worldwide Technical Support

TI Support

Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

China: http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp

Japan: http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp

Technical support forums

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

e2e.ti.com

China: http://www.deyisupport.com/

Japan: http://e2e.ti.com/group/jp/

TI Training

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

China: http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968

Japan: https://training.ti.com/jp

A011617

SLYT754

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265