Fundamentals of Analog Electronics Design

Yang Yan、Fu Qiang

Fundamentals of TINA-TI™ Simulation Software Application

No matter how carefully it is designed, an analog circuit experimenter board can only be used to experiment with a limited number of circuit concepts. Students majoring in electronics and information technology are fortunate to have access to a wide range of mature, specialized circuit simulation software, which can significantly enhance their learning efficiency and engagement. It would be a great pity if we didn't use circuit simulation software to study and design analog circuits.

However, among the vast array of circuit simulation software, there are few free options suitable for beginners. Among them, TINA-TI™ is a free analog circuit simulation software jointly developed by Texas Instruments (TI), a manufacturer of analog devices, and DesignSoft. It can be considered a streamlined version of TINA, the full-featured paid simulation software. While it may not have the most comprehensive set of features, TINA-TI offers the optimal support for circuit simulations of TI's devices. Furthermore, TINA-TI is SPICE-based simulation software, which is essentially consistent with other simulation software. Learning to use TINA-TI will also make it easier to get started with other simulation software.

General information about TINA-TI, such as how to download, how to install, and improvements across versions, can be found on the Texas Instruments website. This chapter primarily illustrates how to use TINA-TI through 7 examples:

1. Op amp buffer circuit analysis.
2. Fourier analysis.
3. DC parameter sweeping.
4. Mathematical analysis tools.
5. Programmable power supply.
6. Time switch and switching power supply circuit.
7. Adding component models.

- Op Amp Buffer Circuit Analysis
- Fourier Analysis
- DC Parameter Sweeping
- Mathematical Analysis Tools
- Programmable Power Supply
- Time Switch and Switching Power Supply Circuit

Op Amp Buffer Circuit Analysis

In this section, we will simulate an op amp buffer circuit with a capacitive load. Through this circuit simulation, we will learn about circuit component construction, electrical rule checking, DC characterization, AC characterization, transient analysis, and the optimized design of this buffer circuit.

Circuit Construction

First, we construct an op amp buffer circuit as shown in **Figure 1**, with the load set to a 1µF capacitor.

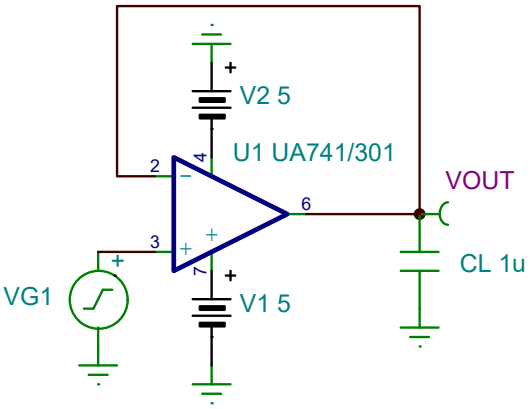


Figure 1. *Buffer Circuit*

The circuit is constructed from the op amp µA741, the signal generator VG1 (the simulation software defaults to naming voltage generators "VG"), power supplies V1 and V2, load capacitor CL, and voltage probe VOUT. All component names and attributes may be modified by double-clicking the respective element.

1. The µA741 is a highly classical op amp in analog circuits. Where feasible, we always select actual op amp models rather than idealized ones for circuit simulation. In TINA-TI, click on “Spice Macros” to select a Class 11 device model from Texas Instruments (TI) and National Semiconductor (NS, acquired by Texas Instruments), as shown in **Figure 2**. From left to right, there is op amp, differential (input) amplifier, fully differential (output) amplifier, instrumentation amplifier, comparator, reference source, buffer, current sense amplifier, switching power supplies, data converter, and other components. The µA741 belongs to the component in the "op amp" subcategory.

Figure 2. *Device Model Category*

2. As shown in **Figure 3**, for signal generator VG_1, the type of waveform that needs to be programmed for the signal generator is “Square wave”, while setting amplitude to be 100mV, frequency to be 1kHz, with 1ns rise/fall times by default.

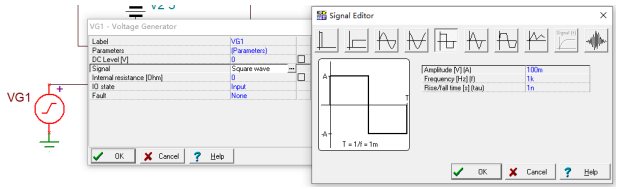


Figure 3. *Signal Generator Parameter Settings*

3. Power supplies V_1 and V_2 may use the default 5V. To modify parameters, double-click the battery symbol for adjustment.
4. The load capacitor CL is selected from the "Basic" component library. Using the ideal capacitor model is sufficient; even when considering the capacitor's equivalent series resistance (ESR) later, it is preferable to directly series-connect an external resistor for greater clarity.
5. The voltage probe V_{OUT} is selected from the "Meter" filed. This will serve as an observable node during future circuit simulation analyses.

DC Characterization

In the simulation software, the parameters of any node and branch are already determined and can be displayed or not, depending on the user's requirements.

Click “Analysis” > “DC Analysis” in the TINA-TI menu bar to display four options: "Calculate Node Voltage", "DC Results Table", "DC Transfer Characteristics", and "Temperature Analysis".

1. In the calculation of the node voltage, the value of the DC voltage at the voltage probe location can be displayed. As shown in Figure 4, V_{OUT} should be an AC signal, so its DC voltage value is only 11.18μV.

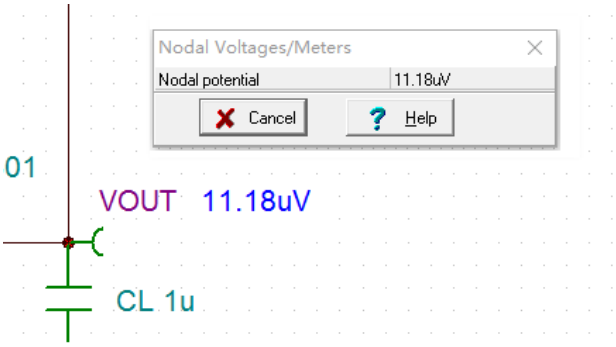


Figure 4. *Calculating Node Voltage*

2. The DC results table shows all DC parameters of the circuit, including DC voltage and DC current. As shown in **Figure 5**, the software automatically labels all loop and node names. As shown in **Figure 5**, there are only five nodes (0/1/2/3/V_{OUT}) with unequal voltages in the circuit. The simulation software displays all DC parameters in a list, based on the component names and node numbers generated by connections. The list is comprehensive, including, for example, some internal current and voltage parameters of the chip. These can be ignored, as we generally only need to focus on the parameters of interest to us.

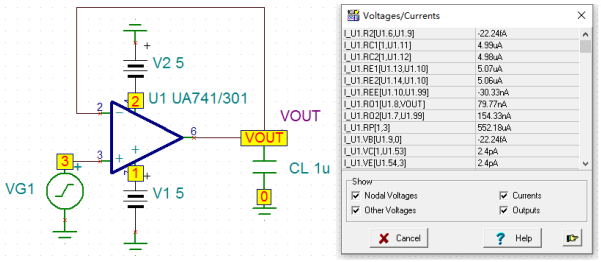


Figure 5. *DC Results Table*

3. DC transfer characterization is a very useful feature for studying how output DC parameters change as input DC parameters vary. This feature is not used in this example but will be covered in detail in subsequent examples.
4. Temperature analysis studies the effects of temperature on semiconductor devices, and this feature will not be discussed in this book.

AC Characterization

In the menu bar of TINA-TI, click “Analysis” > “AC Analysis” to access four options, such as "Calculate Node Voltage", "AC Results Table", and "AC Transfer Characteristics". "Calculate Node Voltage" and "AC Results Table" are similar to those for DC characterization, so we will not cover them here, but provide a detailed introduction to "AC Transfer Characteristics".

1. The so-called "AC transfer characteristics" focus on the circuit's output variations as the frequency of the signal generator varies, which is equivalent to providing a swept-frequency signal generator. This falls within the scope of spectrum analysis.
2. Select the "AC Transfer Characteristics"option, and the settings window shown in **Figure 6** will appear. We need to configure the signal generator's start/stop frequencies, sample number, linear/logarithmic sweep, and the parameters to be observed.

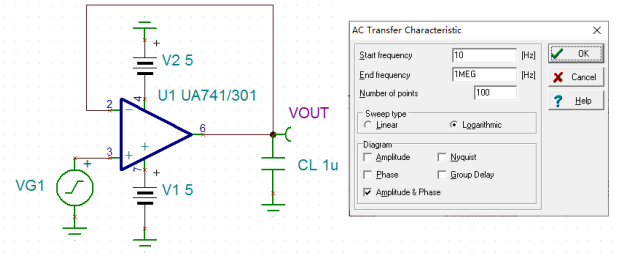


Figure 6. *AC Transfer Characteristics Settings Window*

3. The start/stop frequencies should be set based on the actual bandwidth of the circuit. If the start/stop frequency range is too narrow, the changes in the AC transfer characteristics will not be noticeable. In other words, the characteristics will show no significant change within that frequency band. If it is too wide, information at important frequency points may not be clearly displayed. In this example, the default frequency range is 10Hz-1MHz, exceeding the actual bandwidth of the μA741 op amp by several times.
4. Set the sample number properly. The more points are sampled, the longer the simulation calculation will take. The waveform obtained from the default 100 sampling points is sufficient for observation.

5. In terms of sweep type, we generally choose a logarithmic sweep for amplifier applications to ensure "significant changes" are displayed.
6. In the graph options, we can choose to observe how parameters such as amplitude, phase, and group delay vary with the signal frequency, i.e., a graph with frequency as the horizontal axis and these parameters as the vertical axis. In this example, we choose to display both the amplitude and phase, i.e., to plot both amplitude-frequency and phase-frequency characteristic curves.
7. After all parameters are set, click “OK” to generate the amplitude-frequency and phase-frequency characteristic curves shown in **Figure 7**. Double-clicking the horizontal or vertical axis of the curve allows you to modify the displayed scale.

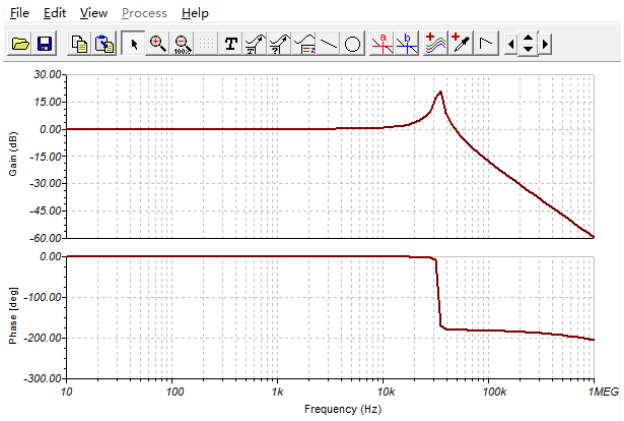


Figure 7. *Amplitude-Frequency and Phase-Frequency Characteristic Curves*

Transient Analysis

The so-called transient refers to the time-domain waveform, which depicts how circuit parameters vary over time. An oscilloscope is a tool used for observing time-domain waveforms. Circuit simulation software can obtain all time-domain data through calculation and display it directly as a graph.

1. Click “Analysis” > “AC Analysis” > “Transient Analysis” to open the transient analysis settings window, as shown in **Figure 8**.

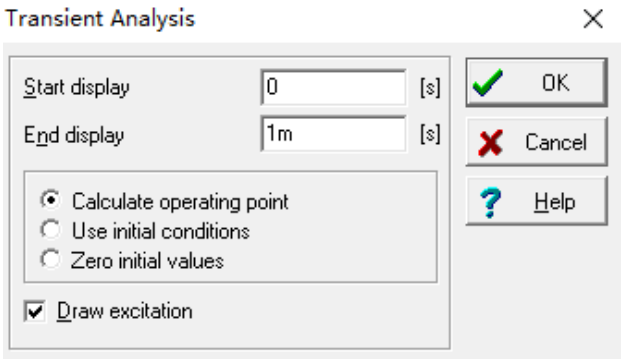


Figure 8. *Transient Analysis Settings*

2. For transient analysis, we primarily set the start and stop times. These parameters should be set in a way that ensures a complete cycle can be captured for periodic signals, and that the settling process can be appropriately

examined for unstable signals - for example, "observation" starts after the signal settles (the "Start Display" is not set to 0).

3. In this example, the signal generator frequency is set to 1kHz, so a time duration of 2ms allows for the observation of two complete cycles, and the start time can be set to 0. **Figure 9** shows the transient analysis graph.

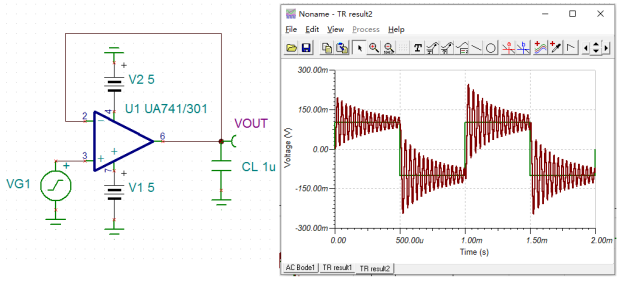


Figure 9. *Transient Analysis of Buffer Circuit*

4. The signal waveform and output waveform shown in **Figure 9** share a coordinate system, which in some cases causes inconvenience to observation. We can click “View” > “Separate curves” to separate the input and output curves. Then, change the vertical axis range for both waveforms to –300mV~300mV by double-clicking the axes, thereby producing the waveforms shown in **Figure 10**.

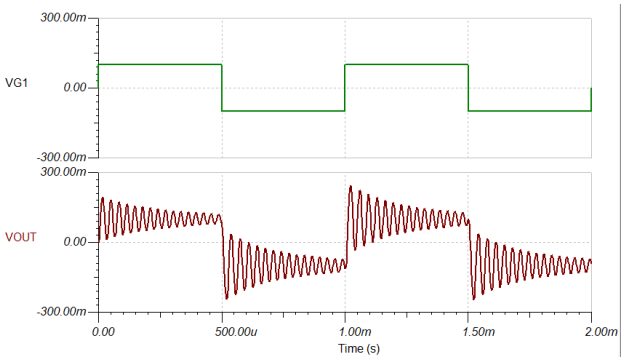


Figure 10. *Separation of the Input and Output Waveforms*

5. From **Figure 10**, we find that the output waveform of the buffer should ideally be consistent with the input waveform. However, the actual output waveform exhibits strong oscillation (commonly known as ringing), which is caused by the pure capacitive load of 1μF. The specific causes of oscillation can be found in Appendix A, and this section only covers the common simulation features of TINA-TI.

Buffer Circuits for Stable Output

Based on the analysis shown in the previous section, a pure capacitive load inevitably causes ringing. A method for eliminating ringing is to add a series resistor to the load to change the "pure capacitive" property of the load. This section will not specifically explain the principles behind ringing elimination, but primarily illustrates that circuit simulation software can indeed significantly help with our circuit design.

1. As shown in **Figure 11**, the load capacitor CL is connected in series with a load resistor R_L. To avoid significantly changing the load characteristics, we first set the value of R_L to 1Ω.

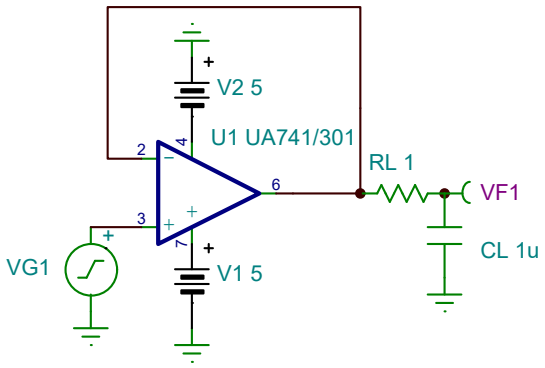


Figure 11. *Series Resistor Load*

2. Click “Analysis” > “Transient Analysis”, and configure the parameters with the same settings as those specified in the previous subsection, thus producing the waveforms shown in **Figure 12**. Ringing is mitigated after a 1Ω resistor is connected in series.

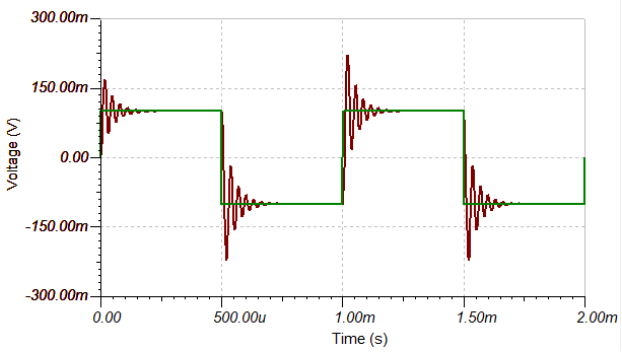


Figure 12. *Ringing under Resistor Load*

3. Modify the value of R_L to 3Ω and plot the "transient" waveforms again. As shown in **Figure 13**, although further mitigated, ringing is still present.

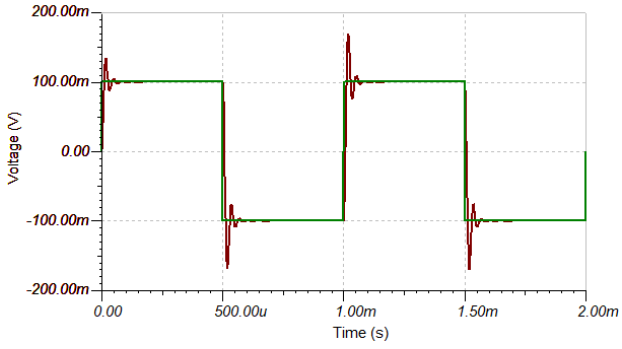


Figure 13. *Ringing under Resistor Load*

4. Modify the value of R_L to 8Ω and plot the "transient" waveforms again. Click “View” > “Separate curves” to modify the axis scale range (–200mV to 200mV), thus producing the waveforms shown in **Figure 14**. Ringing almost disappears, and a stable buffer circuit is constructed.

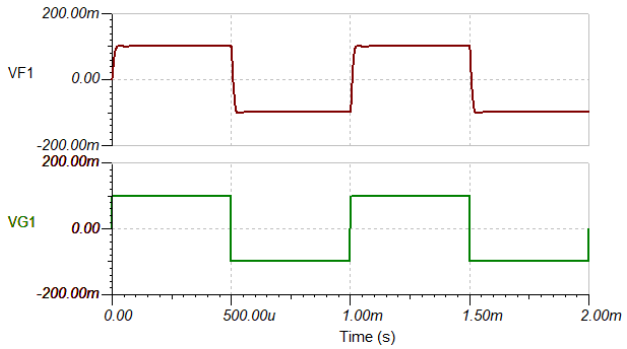


Figure 14. *Time-Domain Waveforms of Stable Buffer*

Summary

This section illustrated the features of circuit simulation software through an op amp buffer circuit. Unlike solely relying on textbooks to study circuits, simulation software offers the following advantages:

1. The quantitative parameter calculation for a circuit is quick and accurate.
2. It can not only analyze and study the ideal conditions of a circuit, but also significantly reflect the properties of a real circuit through component models.
3. It is convenient to modify circuit parameters, which can help in correcting them.
4. It is cost-effective, with no risk of causing device damage and personal injury.

Fourier Analysis

Through the study of the previous section, we have mastered the basic usage of TINA-TI. In this section, we will introduce some other useful features of it.

Fourier analysis is mainly used for frequency-domain analysis. If you have only used an oscilloscope and not a spectrum analyzer, the brief explanation below can help you understand what time-domain analysis and frequency-domain analysis are.

1. As shown in **Figure 15**, if the three axes of a spatial coordinate system represent time, frequency, and amplitude (power), respectively, plotting time against amplitude yields a time-domain waveform (as seen on an oscilloscope). and plotting frequency against amplitude yields a frequency-domain waveform (as seen on a spectrum analyzer).

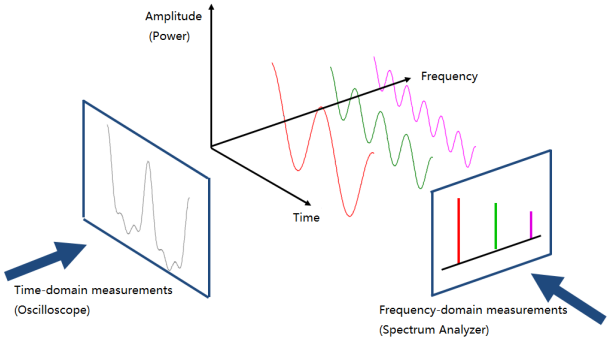


Figure 15. *Differences Between Time Domain and Frequency Domain*

2. Both time-domain and frequency-domain waveforms can be used to describe the same signal, but they emphasize different aspects. For example, the oscilloscope, which we are most familiar with, allows us to observe many useful characteristics of signals. When we require a filter to remove unwanted components of a signal, however, it is obviously more meaningful to know the spectral components of the signal, as this allows us to choose a filter with the right cutoff frequency.

For simulation software, we do not need to further discuss the differences in the principles of oscilloscopes and spectrum analyzers; we only need to learn how to use TINA-TI's Fourier analysis features. Next, we will construct a mixed frequency signal using TINA-TI and then decompose the signal into its spectral components by performing Fourier analysis.

1. **Equation 1** represents the Fourier decomposition formula for sawtooth waves.

$$x\left(t\right) = \frac{2V_{peak}}{\pi}\left(\sin\omega_0 t - \frac{1}{2}\sin 2\omega_0 t + \frac{1}{3}\sin 3\omega_0 t - \frac{1}{4}\sin 4\omega_0 t + \ldots\right) \quad (1)$$

2. A sawtooth wave, as shown in **Figure 16**, can be constructed based on **Equation 1**. Using an op amp non-inverting summing circuit, we can combine four signals. The frequency, amplitude, and phase parameters for the signal generators VG_1 to VG_4 are set according to the provided specifications. Based on the characteristics of the op amp circuit and the calculations using the superposition principle, the signals from VG_1 to VG_4 shown in **Figure 16** can be considered as attenuating to one-fifth of their original amplitudes before superposition. The superposition principle for circuit calculations is very useful. Please take the initiative to learn about it.

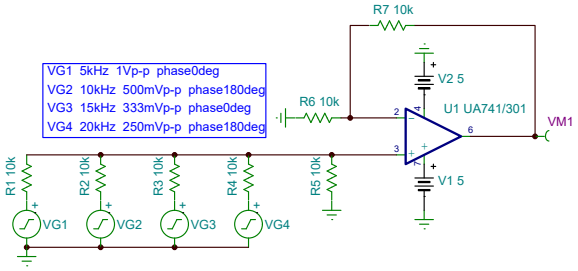


Figure 16. *Synthesizing a Sawtooth Waveform*

3. After generating a transient waveform, separate the curve and modify the vertical axes to ±1V, yielding the waveforms shown in **Figure 17**. The amplitudes decrease sequentially from $1V_{PP}$ for VG_1 to $0.25V_{PP}$ for VG_4. Besides, the phases of VG_1 and VG_3 are 0°, and the phases of VG_2 and VG_4 are 180°. The combination of these 4 waveforms will produce an approximate sawtooth wave VM_1.

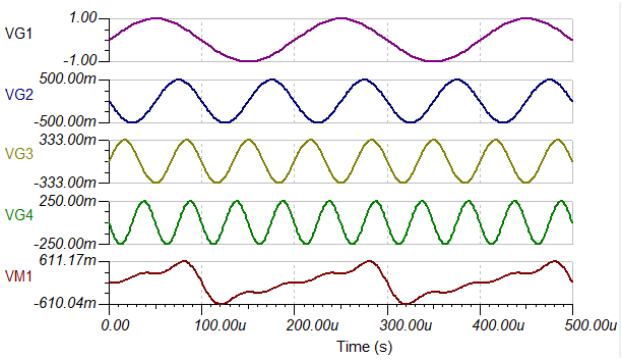


Figure 17. *Synthesized Sawtooth Wave and the Time-Domain Waveforms of its Sinusoidal Components*

On the menu bar, click “Analysis” > “Fourier Analysis” > “Fourier Series” to open the Fourier series settings window, as shown in **Figure 18**. It is necessary to configure parameters such as "Fundamental", "Sample Number", "Harmonic Number", "Output", etc.

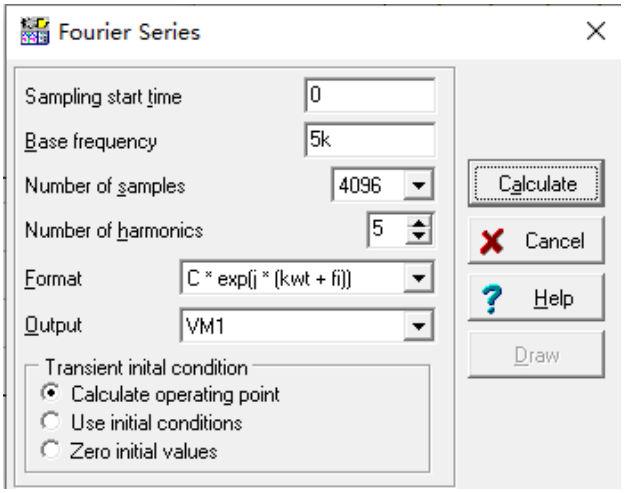


Figure 18. *Fourier Series Settings*

1. The fundamental for the sawtooth wave we constructed is 5kHz.
2. The sample number can be set to the default value, which is related to the simulation calculation speed.
3. As the maximum harmonic frequency is 20kHz in this example, 4 times the 5kHz fundamental, the maximum harmonic number can be set to 4. For a visually appealing representation in the future graph, we can set it to display the 5th harmonic (the amplitude of the 5th harmonic and higher harmonics in the Fourier decomposition should be nearly 0).
4. To set the output is to select the signal to be Fourier decomposed. In this case, only the signal VM_1 is available for selection.
5. Click “Calculate”, and the Fourier coefficients will be displayed, as shown in **Figure 19**. The amplitudes of the 0th and 5th harmonics are approximately 0; the phases of the fundamental wave and the 3rd harmonic are virtually the same; and the phases of the 2nd and 4th harmonics are virtually the same. Odd and even harmonics are out of phase by 180°.

Fourier coefficients

k	Amplitude (C)	Phase (?
0.	502.85u	0
1.	199.97m	-90.53
2.	99.94m	88.93
3.	66.51m	-91.6
4.	49.88m	87.85
5.	1.99u	134.51

Harmonic distortion : 65.008%

Figure 19. *Fourier Decomposition Coefficients*

6. Continue to click “Draw” to plot a frequency-domain curve, as shown in **Figure 20**. **Figure 20** The upper waveforms reflect the harmonic amplitudes of components with different frequencies in the synthesized sawtooth wave, which are reduced to one-fifth compared to the original signals VG_1~VG_4 shown in **Figure 17**. This is consistent with the theoretical values for op amp circuits. The lower waveforms show the phase of each harmonic and are also consistent with the actual situation.

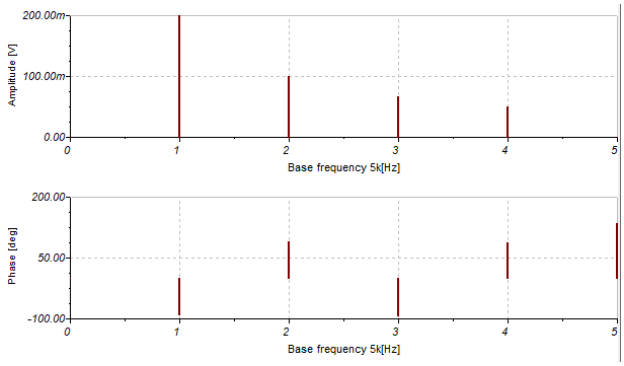


Figure 20. *Frequency-Domain Curves of the Synthesized Sawtooth Wave*

DC Parameter Sweeping

In TINA-TI, the option "DC Transfer Characterization" under the "DC Analysis" feature can be used to sweep DC parameters, which is equivalent to the "Sweep Frequency" for AC transfer characterization. For example, in the detection of a comparator circuit, it is necessary to alter the input DC voltage to observe the changes in the output. Altering the DC voltage automatically is referred to as DC parameter sweeping. **Figure 21** shows a window comparator circuit.

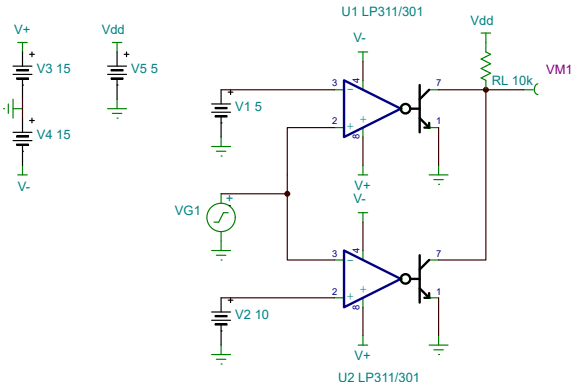


Figure 21. *Window Comparator Circuit*

1. Select the "Comparator" category under "Manufacturer Model", and then select the LP331 comparator, which is a comparator with an open-collector (abbreviated as OC gate) output. From **Figure 21**, it is clear that one characteristic of the OC gate is that an external pull-up resistor (R_L) can be connected to implement a wired-AND logic configuration. For more information about wired-AND logic, you may independently refer to additional relevant resources.
2. For the comparator circuit shown in **Figure 21**, the output VM_1 is high when VG_1 is above 5V and below 10V, and both bipolar junction transistors are cut off. If VG_1 is below 5V, the upper transistor conducts, and the output VM_1 is low. If VG_1 is above 10V, the lower transistor conducts, and the output VM_1 is low. Thus, a window comparator is formed.
3. When detecting the window comparator circuit, it is necessary to sweep the voltage across VG_1 to observe the output VM_1. We can use the "DC Transfer Characteristics" feature to implement it. Click “Analysis” > “DC Analysis” > “DC Transfer Characteristics” to open the settings window shown in **Figure 22**. The start and stop values represent the amplitude "sweeping" range of the input signal. In this example, 0 to 15V is selected, which is consistent with the positive supply voltage for the comparator. More samples lead to slower simulation calculations, while fewer samples result in a "coarse" waveform. Therefore, the default sample number can be used. The input signal is selected as VG_1, indicating that the DC parameter we intend to alter is the voltage input to the comparator.

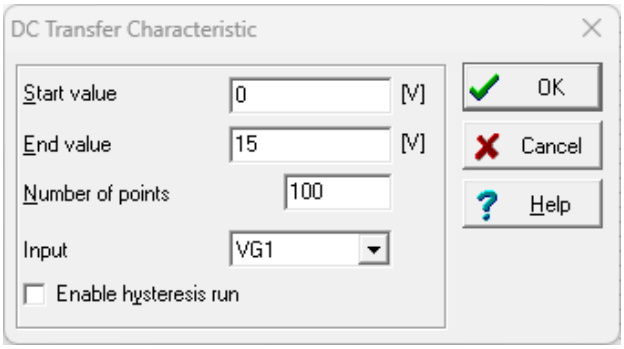


Figure 22. *DC Transfer Characteristic Settings*

4. Click “OK”, and a DC transfer characteristic curve is obtained, as shown in **Figure 23**. If the input voltage varies from 0V to 15V, the output is high only when the input voltage is between 5V and 10V. This is consistent with the characteristics of the window comparator.

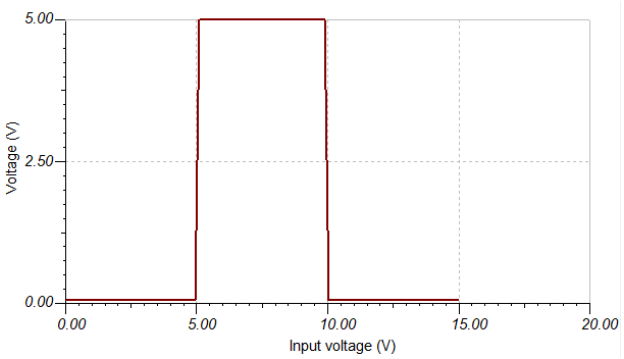


Figure 23. *DC Transfer Characteristic Curve of the Window Comparator*

Mathematical Analysis Tools

Circuit simulation software inherently relies on mathematical calculations to simulate circuits, making mathematical analysis an inherent feature of TINA-TI.

For an active filter circuit, changing the values of an op –amp's resistor and capacitor not only alters the filter's cutoff frequency but also brings about other characteristic changes. This gives rise to various filter (response) types, such as Bessel, Butterworth, and Chebyshev.

Two filters are constructed as shown in **Figure 24** to process the same signal, with one configured to Butterworth and the other to Chebyshev.

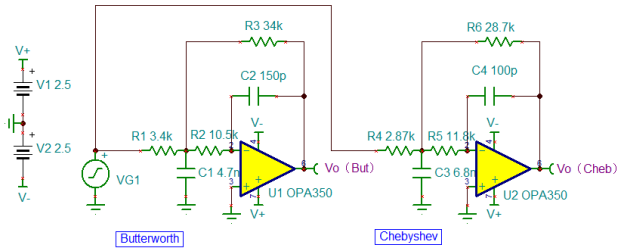


Figure 24. *Active Filter*

1. Observe the amplitude-frequency characteristic curves for both filters. Click “Analysis” > “AC Analysis” > “AC Transfer Characteristics” to open the AC transfer characteristics configuration screen, as shown in **Figure 25**.

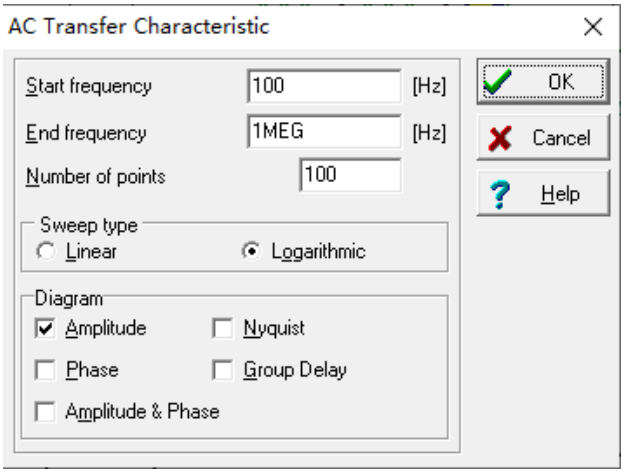
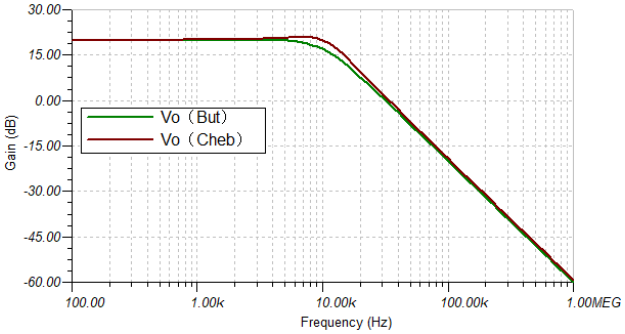


Figure 25. *AC Transfer Characteristics Configuration Table*

2. Set the frequency range for the analysis to 100Hz-1MHz, select "Logarithmic" as the sweep type, and then check "Amplitude" to produce the gain characteristic curves shown in **Figure 26**. Click



("Legend") in the curve toolbar to display annotations for the two curve colors.

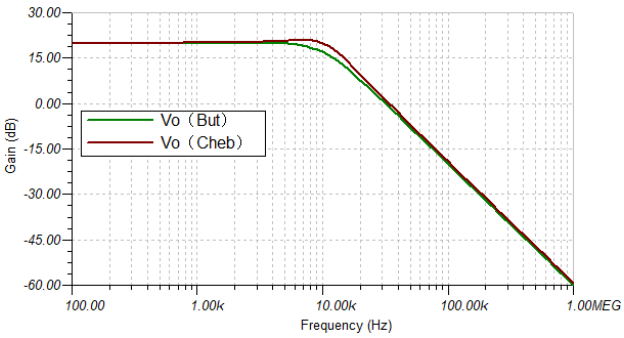


Figure 26. *Amplitude-Frequency Characteristic Curves of Both Filters*

3. Perform mathematical "Post-Processing" on the amplitude-frequency characteristic curves. To more intuitively understand the difference between the two curves shown in **Figure 26**, we can use the mathematical tool "Post-Processing"  . As shown in **Figure 27**, perform mouse operations on options 1 through 8 sequentially to plot a new curve: Differential="Vo(But)(s)"/"Vo(Cheb)(s)".

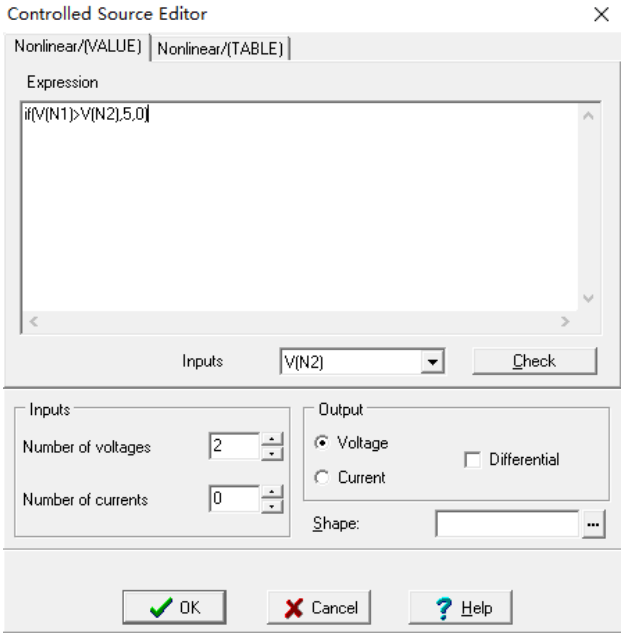


Figure 27. *Curve Post-Processing Settings Window*

4. After you click option 8 “Create”, a curve named "Difference" will appear in the “Curves to insert” field. Then, click “OK” to generate the difference curve, as shown in **Figure 28**. The illustration intuitively reveals in which frequency band the gain characteristics of the Butterworth and Chebyshev filters differ.

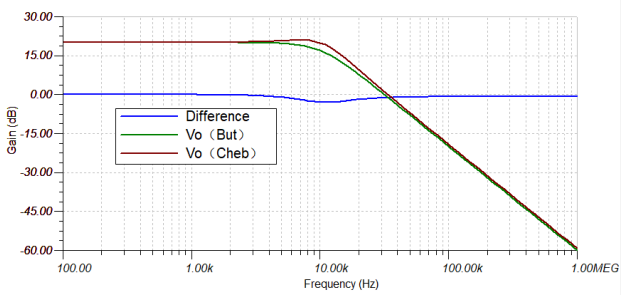


Figure 28. *Difference Curves of the Butterworth and Chebyshev Filters*

Programmable Power Supply

The power supply is one of the three essential pieces of equipment in an electronics laboratory (the other two being the signal generator and the oscilloscope). The completeness of its performance and functions directly determines the results of circuit debugging.

In a circuit, four types of power supplies can be obtained by combining current sources and voltage sources in different configurations, all of which have practical circuit prototypes. One example is the voltage-controlled voltage source (VCVS). Transformers in AC circuits can be considered as VCVSs. Another example is the current-controlled current source (CCCS). A bipolar junction transistor can be considered as a CCCS where the collector current is controlled by the base current. Similarly, a field-effect transistor (FET) can be regarded as a voltage-controlled current source (VCCS) where the drain current is controlled by the gate-source voltage.

The inherent advantages of circuit simulation software enable us to obtain any desired power supply with no additional cost. In this section, we will discuss how to utilize TINA to obtain "arbitrarily controlled" power supplies.

1. Click the source in the window toolbar, select  (Controlled Source), and then click the last option "Controlled Source Wizard" to open the Controlled Source Editor shown in **Figure 29**.

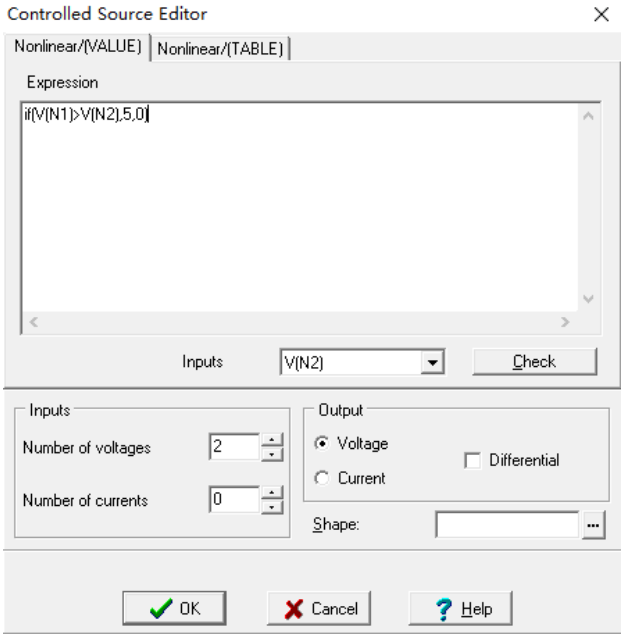


Figure 29. *Controlled Source Editor*

2. As shown in **Figure 29**, the voltage number is set to 2 in the input field, which indicates that the controlled power supply is a voltage-controlled source. In other word, the output is determined by two input voltages.
3. As shown in **Figure 29**, voltage is selected in the output field, indicating that the controlled source is a voltage-controlled voltage source (VCVS).
4. As shown in **Figure 29**, the voltage-controlled relationship for this VCVS is specified in the expression filed. It should be noted that not only linear relationships define a VCVS. As long as the output voltage is determined by the input voltage, regardless of the functional relationship between them, the source is defined as a VCVS. The expression shown in the figure means that the output voltage of the controlled voltage source is 5V when the control voltage V (N_1) is higher than the control voltage V(N_2); in all other cases, it is 0V.
5. After clicking “OK”, you will get a controlled power supply label, as shown in **Figure 30**.

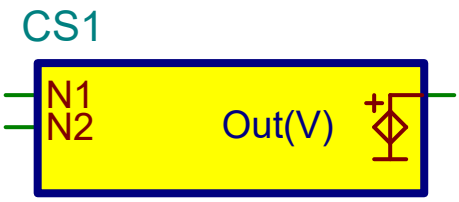


Figure 30. *Controlled Power Supply Label*

6. The controlled power supply label shown in **Figure 30** is comprehensive. CS_1 stands for controlled source 1; N_1 and N_2 represent the input control voltages $V(N_1)$ and $V(N_2)$ mentioned in the expression shown in **Figure 29**; Out(V) and the voltage source symbol indicate that this is a voltage source.
7. Apply control voltages to the controlled source, as shown in **Figure 31**, with VG_1 configured as a $1V_{PP}$/1kHz triangle wave and VG_2 configured as a $1V_{PP}$/50Hz sine wave.

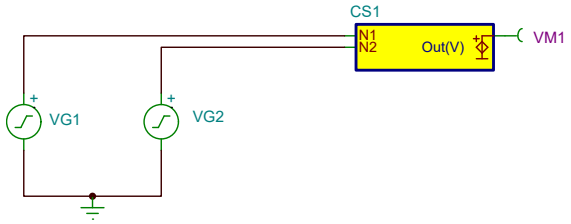


Figure 31. *Applying Excitation Voltage to Controlled Source*

8. In the window bar, click “Analysis” > “Steady State”. Set the simulation start/stop period to 0-20ms, thereby producing the input and output waveforms of the controlled source, as shown in **Figure 32**. The controlled voltage source output represented by VM_1 actually exhibits a crucial SPWM (Sinusoidal Pulse Width Modulation) waveform. As it shows, the programmable power supply feature of simulation software allows us to obtain a variety of "signal generators" that are very useful in real-world circuits but difficult to obtain.

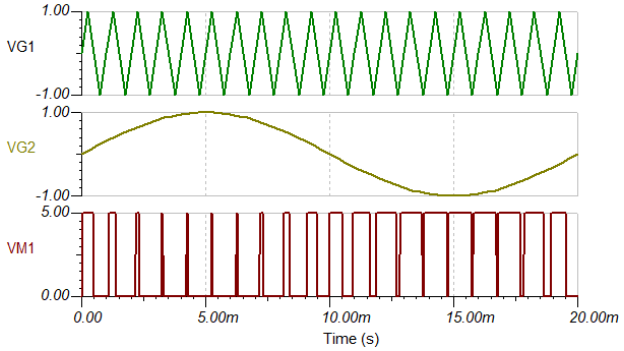


Figure 32. *Input and Output Waveforms of the Tested Controlled Source*

Time Switch and Switching Power Supply Circuit

In the analysis of a switching power supply circuit, using a time switch is a very convenient way to emulate the PWM "switch" effect. As shown in **Figure 33**, switch SW1 in the Buck chopper circuit is in a "floating ground" state. If a real switch were used, the driver circuit would be quite complex. Since our focus is on examining the characteristics of the Buck circuit itself, using a time switch instead of a real semiconductor switch allows for a very convenient analysis of the main circuit's characteristics.

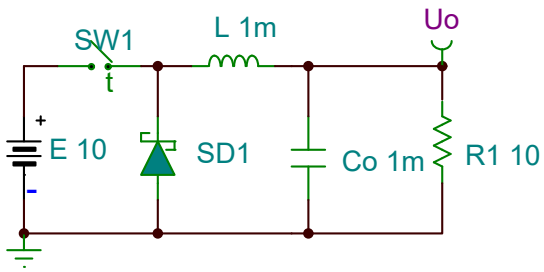


Figure 33. *Buck Chopper Circuit Using Time Switch*

1. The time switch can be used as a PWM switch. According to **Figure 34**,“Periodic” is set to “Yes”; “Period” is set to 10µ; "t On" is set to 0; and "t Off" is set to 6µ. These settings result in a PWM frequency of 100kHz and a duty cycle of 60%.

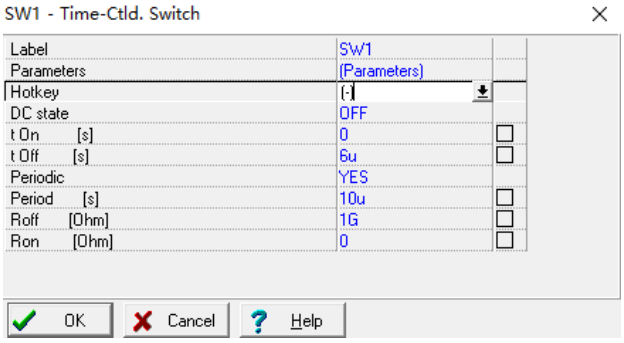


Figure 34. *Parameter Settings of the Time Switch*

2. **Figure 35** shows the output voltage waveforms of the Buck circuit (using a time switch) with duty cycles of 60% and 40%.

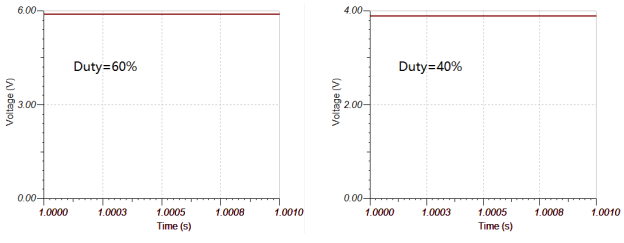


Figure 35. *Simulated Transient Waveforms of the Chopper Circuit*

Fundamentals of Analog Circuits

This chapter will focus on some extremely important yet often overlooked or misunderstood topics in the study of analog circuits, including the following 11 subsections:

1. Voltage source and current source.
2. Nature of electronic devices.
3. Impedance and filter.
4. Equivalent models of resistors and capacitors.
5. Bode plot and zeros/poles.
6. Input impedance and output impedance.
7. Bandwidth of circuit.
8. Temperature characteristics of electronic components.
9. Thermal resistance and thermal dissipation.
10. Impedance matching.
11. Power factor.

- Voltage Source and Current Source
- Supercharger
- Nature of Electronic Devices
- Impedance and Filter
- Bode Plot and Zeros/Poles
- Practical Equivalent Models of Resistor and Capacitor
- Input Impedance and Output Impedance
- Bandwidth of Circuit
- Temperature Characteristics of Electronic Components
- Thermal Resistance and Thermal Dissipation
- Impedance matching
- Power factor

Voltage Source and Current Source

What is a power supply? It seems to be an easy question. Mains power is a 220V AC supply, a lithium battery is a 4.2V DC supply, and a dry cell is a 1.5V DC supply. However, is any circuit that can output a voltage called a power supply? In addition, these examples we encounter in our daily lives are actually just the "voltage sources", and we know very little about the other type of power supply - the "current source".

Let's begin our study of voltage sources and current sources with an interesting story. One day, a student ran to me and asked if his device would be burnt out if he used a 5V/2A power supply since he had lost his 5V/1A power supply. While I was stunned, I realized it was necessary to explain what voltage and current are.

Nature of Voltage Source

Figure 36 shows a potentiometer circuit, where the input voltage V_1 is 5V, the resistance of the potentiometer P_1 is 5kΩ, and the adjustable wiper of the potentiometer is at its midpoint. As a result, the voltmeter reads 2.5V for the output of U_O. Now, can we consider U_O as a 2.5V voltage source?

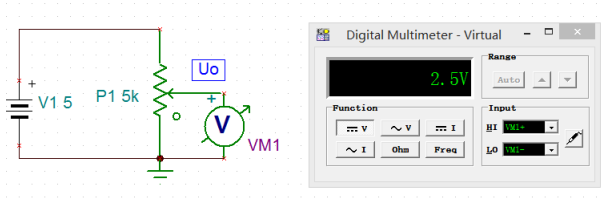


Figure 36. *Potentiometer Divider Circuit*

It is obvious that UO cannot act as a 2.5V voltage source. As shown in **Figure 37**, adding a 2.5kΩ load R1 to the UO output will cause the voltage across UO to drop to 1.67V. It is easy to obtain this calculation using the resistance division relationship.

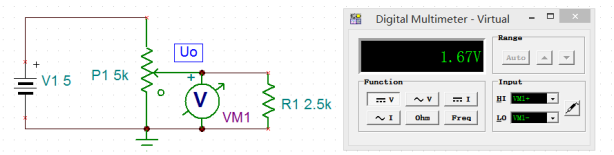


Figure 37. *Potentiometer Divider Circuit with Load*

What kind of circuit can be called a voltage source? A voltage source must be a circuit whose output voltage remains constant regardless of the load. Then, how can we maintain a constant output voltage regardless of the load? Will it work to chant a mantra like "NO CHANGE IN VOLTAGE"? Here, we will introduce a new perspective on the relationship between voltage and current:

1. To maintain a constant output voltage in a circuit, it is critical to provide the circuit with a robust output current capability - chanting a mantra helps nothing.
2. As shown in **Figure 38**, under a light load of 2.5kΩ, the 5V voltage source V_1 can be regarded as a 5V DC voltage source as long as it provides 2mA of current.
3. In the heavy-load circuit shown in **Figure 39**, where the 5V voltage source is connected to a heavy load of 1mΩ, the voltage source V_1 must provide 5000A of current to be a 5V DC voltage source, which is undoubtedly costly.

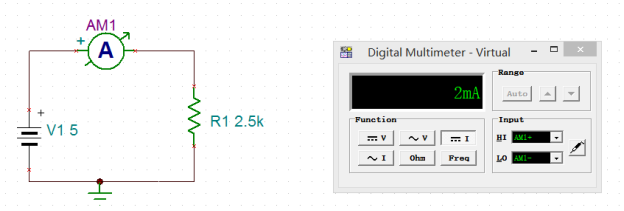


Figure 38. *Voltage Source at Light Load*

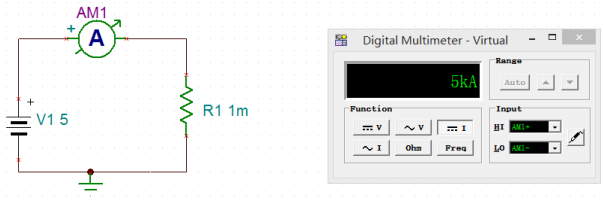


Figure 39. *Voltage Source at Heavy Load*

Internal Resistance of Voltage Source

In most textbooks, a voltage source is always presented as a series combination of an ideal electromotive force (EMF) and an internal resistance, and only a power supply with an extremely small internal resistance is considered a voltage source. Based on this understanding, it seems as if we could obtain ideal voltage sources by significantly investing in thicker copper wires for power supplies or generators. The internal resistance of a power supply cannot be regarded as the actual wire resistance, but rather as the equivalent resistance.

1. As shown in **Figure 40**, the "internal wire resistance" r of the voltage source V_1 is 2.5kΩ. With such a large "internal resistance", it is not typically considered a voltage source. However, as long as the load is sufficiently light, e.g., 1MΩ, the "black box" model on the left can provide an output voltage of 5V.
2. As **Figure 41** shows, when the load changes to 2.5kΩ, we "covertly" increase the voltage across V_1 to 10V. However, from the perspective of the external circuit, the power supply still provides an output voltage of 5V, appearing as a power supply with no internal resistance!
3. It is not challenging for us to make a power supply with zero internal resistance, but it is also true that a current of 2mA is required to produce the voltage of 5V across a 2.5kΩ load. Therefore, the voltage source is essentially a "current provider".

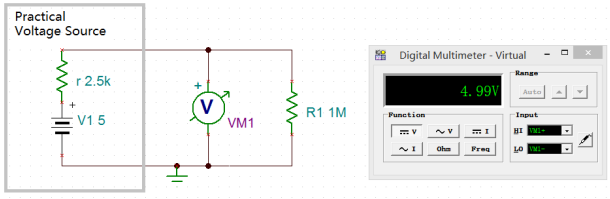


Figure 40. *Operation of High-Impedance Voltage Source at Light Load*

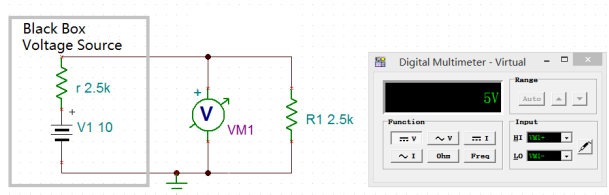


Figure 41. *Voltage Source without Internal Resistance*

Let's return to the 1mΩ heavy load shown in **Figure 39**. If it is impossible for the power supply to provide a current of 5000A to the load, the result will inevitably be a decrease in the power supply's output voltage. Assuming the output current has changed to 2500A, we can have several interpretations:

1. According to **Figure 42**, the voltage V_1 can be considered to remain at 5V, and the internal resistance r_1 is 1mΩ. In this case, the output voltage drops to 2.5V, and the power supply needs to provide a current of 2500A.
2. According to **Figure 42**, as the load current is too large for the power supply to provide, the voltage V_2 drops to 2.5V, and the internal resistance r_2 is 0Ω. This similarly results in an output voltage of 2.5V and a current of 2500A provided by the power supply.
3. According to **Figure 42**, both the voltage V_3 and the internal resistance r_3 can be considered to have changed, with the voltage V_3 dropping to 3.75V and the internal resistance r_3 changing to 500μΩ, which produces the same effect at a 1mΩ load.
4. According to **Figure 42**, assuming the internal resistance r_4 is 1Ω, the voltage V_4 must be "covertly" raised to 2500V to achieve the same effect.

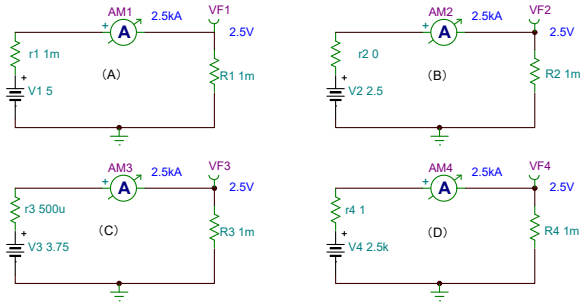


Figure 42. *Several Cases Where Sufficient Current Cannot Be Provided*

Based on the above analysis, we can draw a conclusion: When the load changes, there are many possibilities for how the electromotive force V and the internal resistance r of the power supply can vary to achieve the same output result. But typically, we assume that the EMF is constant to calculate the equivalent internal resistance of the black box model:

1. Definition of internal resistance: When the no-load output voltage is 5V and the loaded output voltage is 2.5V, the load resistance is equal to the equivalent internal resistance, as shown in **Figure 42**, where the internal resistance of the voltage source is recorded as 1mΩ.
2. The equivalent internal resistance of a voltage source does not reflect the actual power supply's EMF and wire resistance, but rather is a commonly recognized method for describing a circuit specification.

3. In practical applications, we often "covertly" alter the electromotive force to achieve a voltage source, rather than investing in thick copper wires for lower resistance.

Nature of Current Source

While voltage sources are more common than current sources, current sources are theoretically equal to voltage sources. The current source is that the output current is constant regardless of the load connected.

Given that voltage and current are theoretically equal, why is our mains supply not designed as a 10A constant-current source? Under normal circumstances, we cannot purchase any constant-current source batteries either. This is determined by the relative ease of obtaining conductors versus insulators in nature. If insulators were much more expensive than conductors, we would most likely use constant current sources instead.

1. Natural insulators are everywhere, and air itself is an exceptionally effective insulator. Conversely, conductors of comparable excellence must approach the performance of superconductors. The copper we utilize for economic reasons exhibits extremely poor electrical conductivity.
2. When the voltage source is idle, it is sufficient to not connect to the load, where the power dissipation is U^2/R. Given that insulators possess immense resistance, this power dissipation is virtually negligible.
3. When the current source is idle, the power dissipation without the load is I^2R. Since insulators exhibit extremely high resistance, the power dissipation becomes substantial. Therefore, when the current source is idle, it must be short-circuited with a conductor, preferably a superconductor, so that power is not dissipated.

The nature of the current source is a circuit that can supply enough voltage. If the current source is open-circuited, that is, air used as the load, the only option for an ideal current source is to produce a very high voltage that breaks through the air to conduct and maintain constant current.

1. As shown in **Figure 43**, IS_1 is a 1A current source and the output voltage of the current source is 1V with a 1Ω load, R_1.
2. As shown in **Figure 43**, IS_2 is also a 1A current source and the output voltage of the current source is 1MV with a 1MΩ load R_2.

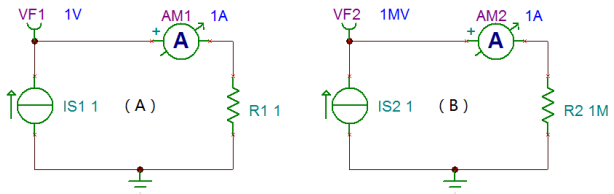


Figure 43. *Output Voltage of Current Source*

Internal Resistance of Current Source

In general textbooks, the internal resistance of a current source is always described as infinity. This is even more difficult to comprehend than the concept of voltage sources having infinitesimal internal resistance. If the current is constant and the internal resistance infinite, how much heat must be generated according to Joule's law? What a peculiar kind of power source this would be? Similar to the case of voltage sources, the internal resistance of current sources is in fact also "fictitious".

In reality, current sources are invariably derived from voltage sources through processing. It is not possible for a voltage source to achieve the function of a constant current source by means of an infinite series internal resistance, but only by "secretly" changing the supply voltage as shown in **Figure 44**.

1. Referring to **Figure 44**, the actual internal resistance of a 5mA equivalent current source is 100Ω, falling far short of the infinite resistance requirement for a current source. When a load resistance R_1 is 900Ω, V_1 outputs 5V to produce a 5mA current source.
2. Referring to **Figure 44**, when the load R_3 changes to 9.9kΩ, the internal resistance of the equivalent current source is still 100Ω, but V_2 voltage "secretly" changes to 50 V. Thus, from the load's perspective, the current remains at 5mA, and the equivalent internal resistance of the current source is infinite.

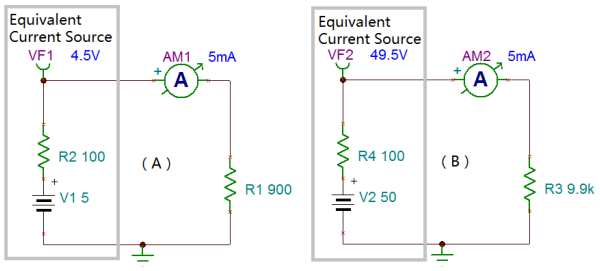


Figure 44. *Equivalent Circuit of Current Source*

Power Adapter 5V/2A

Let's return to the question of what a 5V/2A power adapter actually is. **Figure 45** shows a common DC power adapter. Since it is much more difficult to obtain conductors, especially superconductors, compared to insulators, the existing power supplies are all assumed to be voltage sources unless otherwise specified. A 5V/2A power supply indicates a constant-voltage source with an output voltage of 5V and a rated output current of 2A.

1. Under light-load conditions, the actual output voltage of the power adapter will exceed 5V, possibly reaching 5.5V, while the amount of the output current depends on the load resistance.
2. Under heavy-load conditions, such as with a load rated at 2.5Ω, the output voltage should be about 5V, and a reading of 4.8V is also acceptable.
3. When the load resistance is less than 2.5Ω, the power adapter may be over-current protected or may output a voltage much lower than 5V.
4. It is extremely hard to have a power supply that simultaneously provides a 5V voltage output and a 2A current output, since they conflict with each other. This is only possible with a 2.5Ω load. Therefore, you don't have to worry that a 5V/2A power adapter would burn out your device.

Figure 45. *Power Adapter*

Supercharger

This section provides another example to help understand the concept of voltage and current in the order of magnitude. One day, a group of students gathered around to watch an online video, the gist of which was "Israel invents supercharger that can fully charge mobile phone in 30 seconds". A screen shot of the video is shown in **Figure 46**. What struck me as peculiar was not the claim of such a supercharger existing, but the students' vehement defense of the claim when I dismissed it as utter nonsense. Their stance smacked of sour grapes - as if I were merely unable to replicate it myself.

Figure 46. *Video Screen Shot of a Supercharger Fully Charging a Mobile Phone Battery in 30 Seconds*

Whether superchargers are "nonsense" is actually quite easy to prove.

1. A cell phone battery takes 2000mAh as an example, regardless of its voltage. Regardless of its voltage, according to the law of conservation of energy, charging it requires at least a 2A current for 1h, or a 7200A current for 1s.
2. As claimed in the video, if a 2000mAh battery can be fully charged in just 30s, even assuming 100% charging efficiency, the average charging current would require 240A.

The approximate cable diameter required to properly transmit 240A is 10mm. What would happen if such a massive current were applied to the phone battery terminals as shown in **Figure 47**? When I recounted this scenario to a seasoned colleague, he blurted out one word: "welding machine."

Figure 47. *Contact Photo of a Phone Battery*

In truth, setting aside cost considerations, manufacturing chargers, capable of delivering hundreds of amperes or even greater currents, poses no technical challenge whatsoever. The real difficulty lies in the fact that no battery can withstand such high charging currents without being reduced to slag.

1. The battery capacity determines the appropriate charging current, and charging a 2000mAh battery at 2A is termed 1C charging.
2. For virtually all rechargeable battery types, 1C already qualifies as rapid charging. Consider Apple iPad4® (11560mAh battery) charger, rated merely at 2A or iPad mini® (4490mAh) charger at just 1A.
3. While some batteries might barely withstand 2C to 5C charging, this comes at the cost of drastically reduced lifespan. Higher currents inevitably lead to battery explosion - under no circumstances should this be attempted.

Nature of Electronic Devices

Now that the nature of voltage and current is not as simple as we thought before, do we truly understand the nature of electronic devices? These include resistors that we think we are extremely familiar with, capacitors that are commonly known, and inductors that we barely know. Actually, we can re-understand them from a different perspective.

Resistor

What is a resistor? As the name suggests, a resistor is a component that resists electricity. But does it resist current or voltage, or both?

1. As shown in **Figure 48**, the node voltages are equal whether or not there is a resistor R_1, indicating that the resistor does not resist the voltage, even when an AC power is applied.

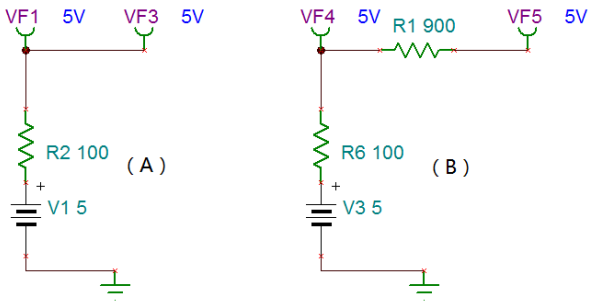


Figure 48. *Resistor's Resistance to Voltage*

2. As shown in **Figure 49**, whether connecting resistor R_3results in a significant difference in current.

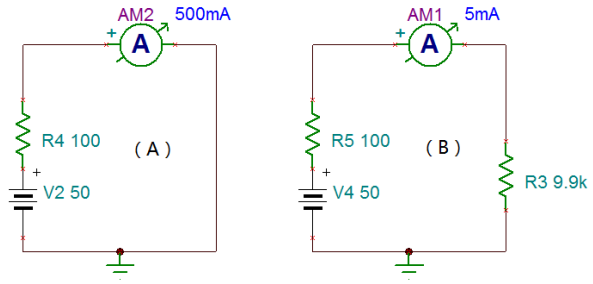


Figure 49. *Resistor's Resistance to Current*

A resistor is, in essence, a component that resists the current. As we mentioned before, a resistor cannot simply resist the current by "chanting a mantra". So how does it work? Actually, a resistor influences the current flowing through itself by changing the voltage across it.

The characteristic equation for a resistor can be written as follows, indicating that:

$$u = i \cdot R \tag{2}$$

1. Current flowing through the resistor generates a voltage opposite to the "excitation" voltage of the power supply;
2. As the current increases, when the reverse voltage generated by the resistor equals the supply voltage, the current will stop increasing, at which point the resistor effectively resists the current.

Capacitor

The resistor is somewhat familiar to us, but what is a capacitor?

1. Structurally, a capacitor is composed of metal plates with a dielectric (insulator) filled between them.
2. In terms of operation, a capacitor can be charged and discharged, generating an electric field.

At a deeper level, we consider a capacitor as a component that resists changes in voltage. A resistor doesn't just deliver such an effect out of nowhere; it does so by being able to absorb and release a large amount of current.

1. As shown in **Figure 50**, when the switch SW is not closed and in a steady state, the voltage across the load VF_1 is 4.5V; the load current AM_3 is entirely supplied by the power supply V_1; the supply current AM_2 is 5mA; and the current through the capacitor AM_1 is 0A.
2. As shown in **Figure 50**, at the very moment the switch is just closed, the voltage across the load VF_2 remains at 4.5V due to the filter capacitor; according to Ohm's Law, the load current AM_6 reaches 4.5A. At the same time, it can be calculated that the supply current AM_5 remains at 5mA; and the difference between AM_6 and AM_5 must be provided by the capacitor current AM_4, resulting in an instantaneous capacitor output current of 4.495A.

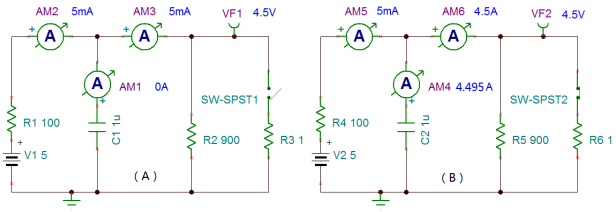


Figure 50. *Discharge Current of Capacitor Filter Circuit during Transient State*

3. As shown in **Figure 51**, when the switch is closed and in a steady state, the voltage across the load V_{F1} is 49.45mV; the load current AM_3 is entirely supplied by the power supply AM_2 and reaches 49.51mA; and the current through the capacitor AM_1 is 0A.
4. As shown in **Figure 51**, at the very moment when the switch is just opened, the voltage across the load V_{F2} remains at 49.45mV due to the filter capacitor; according to Ohm's Law, the load current AM_6 reaches only 0.055mA. At the same time, it can also be calculated that the supply current AM_5 remains at 49.51mA, and the instantaneous current difference between AM_5 and AM_6, approximately 49.5mA, must flow into the capacitor.

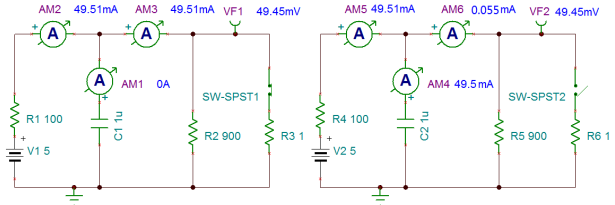


Figure 51. *Charging Current of Capacitor Filter Circuit during Transient State*

The characteristic equation for a capacitor is as follows, indicating that:

$$i_C = C\frac{du_C}{dt} \tag{3}$$

1. Capacitors sustain voltage by absorbing and releasing sufficient current.
2. The higher the rate of change in voltage is, the more current the capacitor will absorb or release.
3. Capacitors can be considered as ideal voltage sources for a short period.

Inductor

Among the three fundamental electronic components: resistor, capacitor and inductor, the inductor is the least familiar to us, and for profound reasons. When we simplify voltage sources to mere power supply, it is predetermined that inductors will never achieve the same breadth of application as capacitors. The effect of an inductor on a current source mirrors that of a capacitor on a voltage source; the two are dual in nature.

An inductor is a component that impedes changes in current. It cannot claim to obstruct current variation arbitrarily; rather, it relies on generating sufficiently high voltages to hinder current changes.

1. What happens when the switch SW is open in the circuit shown in **Figure 52**? When the switch is open, current ceases. However, the current through inductor L_1 cannot change abruptly. Consequently, a high voltage is generated on L_1 to help the supply maintain the current. How high might this voltage become? As high as it takes, until the air at the switch is ionized and conducts electricity, at which point we shall observe an electric arc.

2. The mathematical expression describing this high voltage reveals the essence of inductor: the rate of change in current determines the magnitude of the induced voltage. Thus, the inductor maintains a constant current by generating a high voltage.

$$u_L = L\frac{di_L}{dt} \tag{4}$$

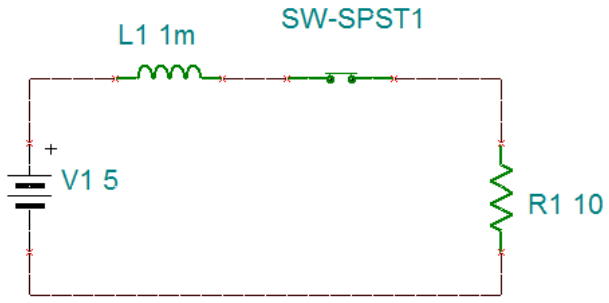


Figure 52. *Circuit Containing an Inductor*

Since parasitic inductance is virtually ubiquitous, the phenomenon of inductors, generating high voltages, is commonly observed. The most typical example is the electrical sparks produced when various switches are turned on or off.

1. Electric current itself does not emit light; the sparks we observe are actually thermoluminescence (the principle behind incandescent bulbs). This occurs when the air conducting the current heats to such a high temperature that it glows. The sparks we see reach temperatures exceeding 4000°C.
2. Electric sparks, while glittering, cause localized melting of switch and socket contacts. Low-power appliance switches require no special treatment, but high-power switches necessitate "arc quenching" mechanisms. Without this, the spark would persist indefinitely, burning out the switch contacts.

Let's take a look at a few more circuits to improve our understanding of the inductance characteristics. Can the circuit shown in **Figure 53** be shorted? Can't it? We might resolve this question through mathematical calculation.

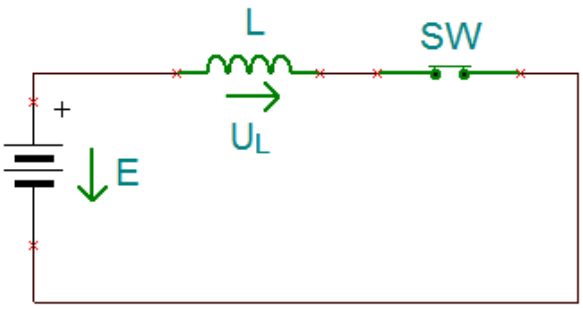


Figure 53. *Inductive Circuit for Power Supply*

1. Having calibrated the actual supply voltage and the positive direction of the inductor voltage, the characteristic equation for the inductor is:

$$U_L = L\frac{di}{dt} = E \tag{5}$$

$$\frac{di}{dt} = \frac{E}{L} \tag{6}$$

1. Since E/L is a constant, the inductor current increases linearly with a slope proportional to the supply voltage and inversely proportional to the inductance. Thus, the circuit shown in **Figure 53** will not be shorted. Do not mistake linear growth for a short circuit!

Looking at another circuit, like the one shown in **Figure 54**, what happens when the switch is turned to the right to turn on? Does the current short-circuit? Does it decay linearly? Let us not speculate. For an unfamiliar component like an inductor, mathematical analysis proves more reliable.

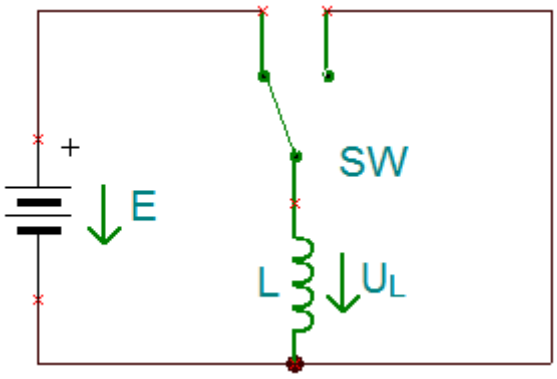


Figure 54. *Inductive Short-Circuited Discharge Circuit*

1. Having calibrated the actual supply voltage and the positive direction of the inductor voltage, the characteristic equation for the inductor is:

$$U_L = L\frac{di}{dt} = 0 \tag{7}$$

$$\frac{di}{dt} = 0 \tag{8}$$

2. This means that the current is changing at a rate of 0, isn't that a constant current source? If the conductor is superconductor without resistance, the current through the inductor would flow perpetually. Remarkable, is it not? In truth, it is not remarkable.
3. If I were to state that a fully charged capacitor, being perfectly insulated with no leakage, would maintain its voltage indefinitely, you would surely dismiss it as implausible? Yet when we compare the relationship between inductance and current to that between capacitance and voltage, the similarities are striking.

Our mental conditioning readily accepts the assumption that capacitors do not leak charge, yet stubbornly rejects the notion of superconducting inductors. So what happens when the switch in **Figure 55** is toggled to the right in a resistive circuit? Let us rely on mathematical derivation.

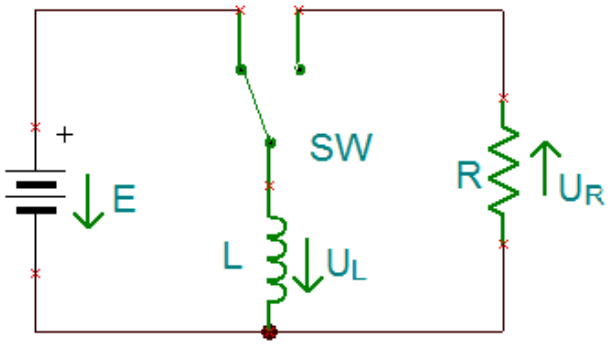


Figure 55. *LR Discharge Circuit*

1. Having calibrated the actual inductor voltage and the positive direction of the resistor voltage, note that the direction of the resistor voltage is determined by the actual current direction. From the characteristic equation for the inductor, it yields . Since , the rate of change in current is ultimately derived as .

$$u_L = L\frac{di}{dt} \tag{9}$$

$$u_L = -iR = L\frac{di}{dt} \tag{10}$$

$$\frac{di}{dt} = -\frac{iR}{L} \tag{11}$$

2. We shall not solve the differential equation, but conduct a qualitative analysis instead. Looking at the three quantities on the right side of the equation, the larger the resistance R, the larger the slope di/dt of the current decay: The larger the inductance L, the smaller the slope di/dt of the current decay; the larger inductance i at beginning leads to the fast decay. As i decreases, the decay is slow. So the qualitatively drawn current waveform of the resistive-inductive loop should be shown in **Figure 56**.

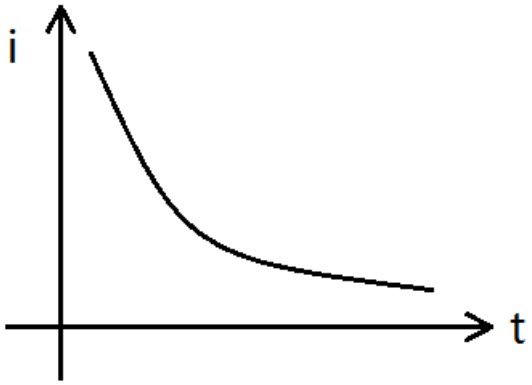


Figure 56. *LR Circuit Current Waveform*

Inductor is essentially the component dependent on the generation of a voltage to impede the change in current. Let's summarize the behavior of the 4 inductive circuits in this subsection:

1. Forcibly interrupting the current through an inductor generates a high voltage.

2. When an inductor is connected to a voltage source, the current increases linearly.
3. When an inductor is connected to a superconductor, the current remains constant.
4. When an inductor is connected to a resistor, the current decreases non-linearly.

Impedance and Filter

In the previous section, we analyzed the dynamic characteristics of circuits - specifically, the voltage and current conditions of circuits at any given instant - using the characteristic equations for a resistor, a capacitor, and an inductor. In this section, we will examine three electronic components - resistor, capacitor, and inductor - from the perspective of impedance. This will help us analyze how filters are created in circuits.

Impedance of Components

If there are only resistive components in a circuit, we can easily determine the voltage across each resistor using the voltage division principle derived from Ohm's law. The functions of capacitors and inductors in a circuit can be viewed as the effects of capacitive reactance and inductive reactance, which are collectively referred to as impedance. They share the same dimension, "ohm", as the resistance. **Table 1** is a list of component impedances.

Table 1. Impedance of Components

Component	Impedance	Voltage/current phase
Resistor	R	In phase
Capacitor	$1/j\omega C$	Current leads voltage by 90°
Inductor	$j\omega L$	Current lags voltage by 90°

1. A resistor's impedance is its resistance R, independent of the electrical signal's frequency. Besides, the current and voltage across the resistor are in phase.
2. A capacitor's impedance is in inverse proportion to the electrical signal's frequency. The higher the frequency is, the lower the impedance will be. We can interpret the capacitor's quiescent characteristics as "blocking DC current while passing AC current". Unlike resistance, when dealing with capacitive reactance, it is important to consider the phase difference between the voltage and current across the capacitor - the current leads the voltage by 90°. Instead of memorizing which one leads, focus on understanding this concept. One understanding is that, since a capacitor is a component that resists changes in voltage, it is natural that the voltage lags behind the current, i.e., the current leads the voltage by 90°.
3. An inductor's impedance is proportional to the electrical signal's frequency. The higher the frequency is, the higher the impedance will be. As the inductor is the component that resists changes in current, the current lags behind the voltage by 90° across the inductor.

There is a classic question that tests one's understanding of impedance, as shown in **Table 1**, asking for the voltage value at the midpoint. As both capacitive impedance and resistive impedance are equal to 1Ω, there is no need to specify the signal frequency. Most people would instinctively answer 0.5V, but the correct answer is 0.707V.

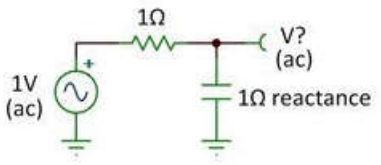


Figure 57. *Classic Question Testing One's Understanding of Impedance*

Filter Principles

It is because the impedance of capacitors and inductors is frequency-dependent that filters are present in circuits. By combining resistors, capacitors, and inductors, low-pass, high-pass, and band-pass filtering functions can be achieved. According to mathematical expressions, the characteristics of capacitors and inductors are symmetrical. However, the cost of inductive components is much higher than that of resistors and capacitors in the real world. Therefore, only resistors and capacitors are used to produce filters in most cases. This book will also only focus on RC filters.

As shown in **Figure 58**, a resistor and a capacitor form a voltage divider for the input signal, with the voltage across the capacitor taken as the output, thereby constituting a low-pass filter. (Since the voltage across the resistor is in phase with the current, the voltage across resistor R is used for simulation in **Figure 58**, instead of the current)

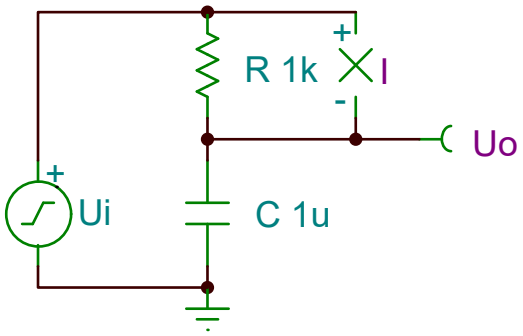


Figure 58. *Low-Pass Filter Circuit*

1. By the principle of impedance division, the expression for the output voltage u_O is:

$$u_O = \frac{Z_C}{Z_R + Z_C} \times u_I = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \times u_I = \frac{1}{j\omega CR + 1} u_I \tag{12}$$

2. **Equation 12** indicates that the output voltage amplitude decreases with increasing frequency, so the circuit shown in **Equation 13** is a low-pass filter.
3. According to the vector diagram **Figure 59**, the output voltage lags the input voltage, with an electrical angle of:

$$\tan \varphi = \left| \frac{Z_R}{Z_C} \right| = \frac{R}{\frac{1}{\omega C}} = \omega CR \tag{13}$$

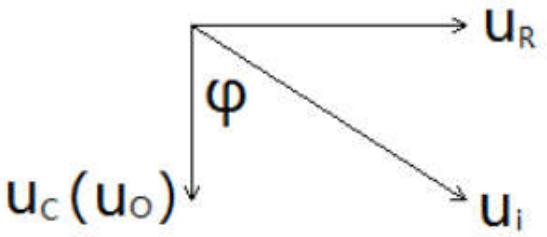


Figure 59. *Vectors of the Low-Pass Filter*

4. **Figure 60** shows the transient simulation of a low-pass filter circuit, where it can be observed that the output voltage u_O lags the input voltage u_I. The output voltage (capacitor voltage) lags the current by 90°.

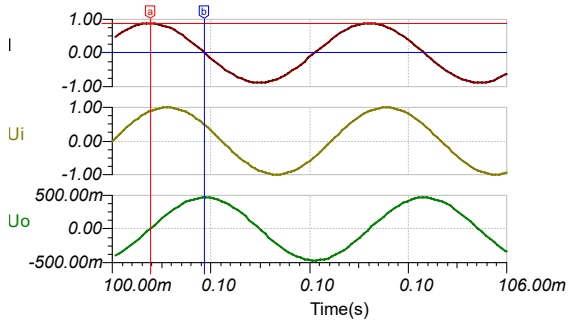


Figure 60. *Input/Output Current/Voltage Waveforms of the Low-pass Filter*

As shown in **Figure 61**, a resistor and a capacitor form a voltage divider for the input signal, with the voltage across the resistor taken as the output, thereby forming a high-pass filter.

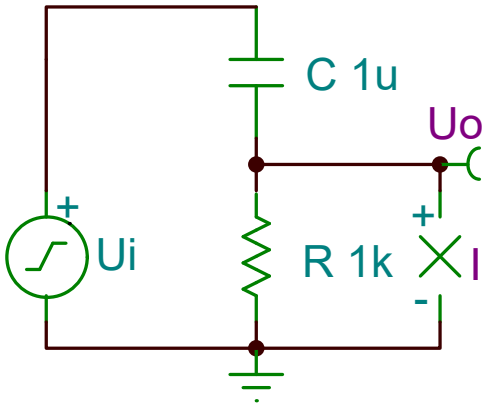


Figure 61. *High-Pass Filter Circuit*

1. By the principle of impedance division, the expression for the output voltage u_O is:

$$u_O = \frac{Z_R}{Z_R + Z_C} \times u_I = \frac{R}{R + \frac{1}{j\omega C}} \times u_I = \frac{1}{\frac{1}{j\omega CR} + 1} u_I \tag{14}$$

2. **Equation 14** indicates that the output voltage amplitude increases with increasing frequency, so the circuit shown in **Figure 61** is a high-pass filter.
3. According to the vector diagram **Figure 62**, the output voltage leads the input voltage, with an electrical angle of:

$$\tan\varphi = \left|\frac{Z_C}{Z_R}\right| = \frac{\frac{1}{\omega C}}{R} = \frac{1}{\omega CR} \tag{15}$$

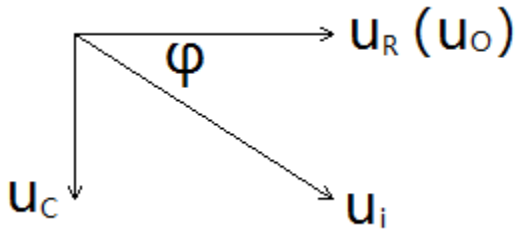


Figure 62. *Vectors of the High-Pass Filter*

4. **Figure 63** shows the transient simulation of a high-pass filter circuit, where it can be observed that the output voltage u_O leads the input voltage u_I. The output voltage (resistor voltage) is in phase with the current.

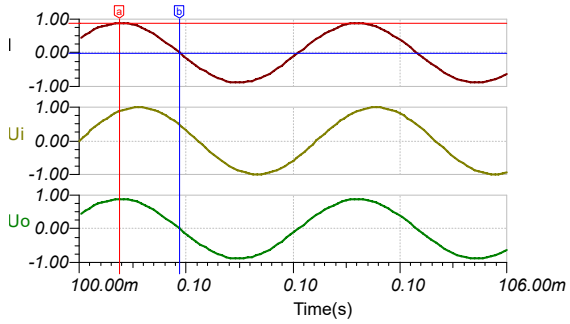


Figure 63. *Input/Output Current/Voltage Waveforms of the High-Pass Filter*

Bode Plot and Zeros/Poles

When the "characteristics" of the circuit are related to the frequency of the signal, it is clear that the time-based "time-domain waveform" (oscilloscope waveform) does not fully reflect the characteristics of the circuit. This necessitates frequency-domain analysis. The theory and methods of frequency-domain analysis are highly complex (falling within the domain of signals and systems courses), involving vast quantities of mathematical operations and transformations. This readily leads to the awkward predicament of "understanding the why, but not the how".

For analog circuits, frequency-domain analysis first demands an understanding of the true physical significance of Bode plots and zeros/poles. Without this, all mathematical transformations and derivations become torturous examination questions rather than genuinely practical tools.

Amplitude-Frequency and Phase-Frequency Characteristic Curves

Curves depicting the amplitude and phase of a circuit's output signal at different input frequencies are called amplitude-frequency and phase-frequency characteristic curves, respectively. When plotted on a logarithmic scale, they are known as Bode plots (invented by Hendrik Wade Bode in 1930).

In TINA, generating Bode plots is part of the AC transfer characteristic simulation. **Figure 64** shows a first-order passive low-pass RC filter, and its cutoff frequency is: $f_H = \frac{1}{2\pi RC} \approx 159\text{Hz}$.

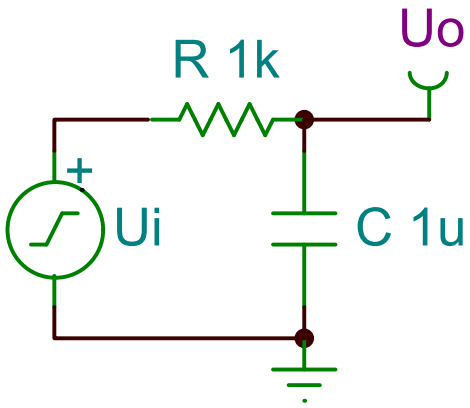


Figure 64. *First-Order Passive Low-Pass RC Filter*

1. On the TINA main window, click “Analysis”→“AC Analysis”→“AC Transfer Characteristics” to open the AC transfer characteristics settings window, as shown in **Figure 65**. Set the start and stop frequencies to 1Hz-100kHz, extending approximately 100 times from the cutoff frequency f_H on both sides for better observation.

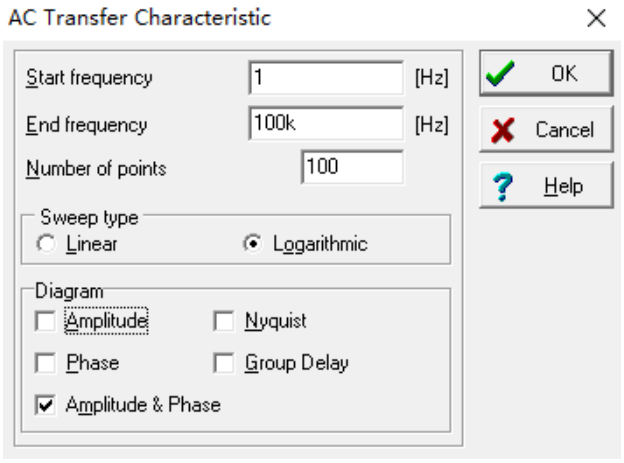


Figure 65. *AC Transfer Characteristics Settings Window*

2. **Figure 66** shows the amplitude-frequency and phase-frequency characteristic curves generated from the simulation. Double-click the vertical axis of the amplitude-frequency curve and set the upper and lower limits to 0 and –36 with 13 tick marks to display the –3dB scale. Double-click the vertical axis of the phase-frequency curve and set the upper and lower limits to 0 and –90 to display the –45° scale. Use Pointers A and B on the amplitude-frequency curve to mark the –3dB position (Pointer A) and the –20dB position (Pointer B).

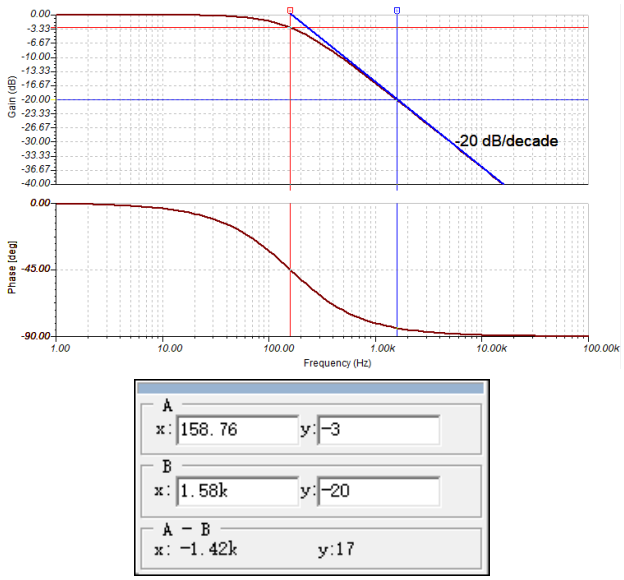


Figure 66. *Amplitude-Frequency and Phase-Frequency Characteristic Curves of the First-Order Passive Low-Pass Filter*

Analysis of **Figure 66** yields the following conclusions, which hold true for all first-order low-pass filters.

1. According to the amplitude-frequency characteristic curve, the –3dB gain marked by Pointer A exactly corresponds to the cutoff frequency f_H (158.76 Hz). This is not a coincidence, as the cutoff frequency is defined as the frequency at which the signal is attenuated by a gain of –3dB (0.707 times).
2. On the phase-frequency characteristic curve, it is not a coincidence, either, that the gain of –3dB corresponds to the phase shift of –45°. When Z_R is equal to Z_C, the phase shift is –45°, at which point the signal is attenuated by a gain of $Z_C/\sqrt{{Z_C}^2+{Z_R}^2}$, i.e., $1/\sqrt{2}=0.707=-3\text{dB}$.
3. For the extension of the amplitude-frequency characteristic curve, Pointers A and B help to identify two coordinate points on the sloped line: (158.76Hz, 0dB) and (1.58kHz, –20dB). Thus, the slope of this line is –20dB/decade. In other words, the amplitude-frequency characteristic curve shows that, at frequencies far from the cutoff frequency, the signal is attenuated by a gain of 20dB (a factor of 10) for every 10-fold increase in frequency.
4. On the phase-frequency characteristic curve, the phase shift is zero when the frequency is much lower than the cutoff frequency f_H (0.1 times can be considered much lower). At this point, $Z_R << Z_C$, producing a phase shift angle of $|\phi| = \arctan(Z_R/Z_C) \approx \arctan 0 \approx 0°$.
5. Again on the phase-frequency characteristic curve, the phase shift is –90° when the frequency is much higher than the cutoff frequency f_H (10 times can be considered much higher). At this point, $Z_R >> Z_C$, producing a phase shift angle of $|\phi| = \arctan(Z_R/Z_C) \approx \arctan \infty \approx 90°$.

AC Transfer Characteristics of Multi-Order Filter

As shown in **Figure 67**, cascading two first-order filters creates a second-order low-pass filter.

1. Acting as the load for the first-order filter, the second-order filter, composed of R_1 and C_1, will change the divider ratio between R and C. Therefore, an amplifier is used for isolation, as shown in **Figure 67**, to ensure that the cutoff frequency at each stage remains unchanged at 158Hz.

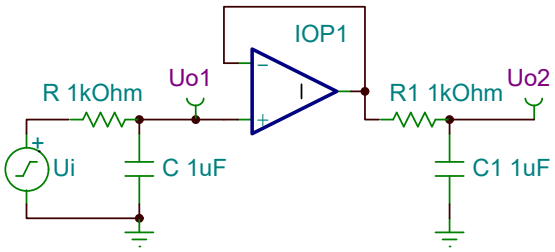


Figure 67. *Second-Order Low-Pass Filter*

2. The amplitude-frequency and phase-frequency characteristic curves (see **Figure 68**) of a second-order low-pass filter can be obtained using the same analysis method as for a first-order low-pass filter. Based on the reading of Pointer A, at the gain of –3dB, the first-order filter output U_{O1} shows a phase shift of –45°, and the second-order filter output U_{O2} shows a phase shift of –90°.
3. At frequencies much higher than the cutoff frequency (158Hz), the maximum phase shifts of the first-order filter and the second-order filter are –90° and –180°, respectively. This is consistent with the pattern derived from Equation 2.8, which is based on impedance calculations.
4. The second-order filter provides an attenuation rate of –40dB/decade at frequencies far from its cutoff frequency, following the rule that the overall gain is the product of individual stage gains for cascaded signals.

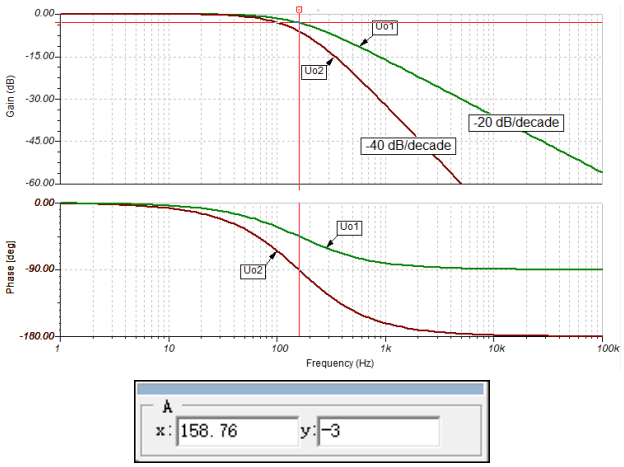


Figure 68. *Amplitude-Frequency and Phase-Frequency Characteristic Curves of the Second-Order Low-Pass Filter*

Theoretical calculations show that each additional order in a low-pass filter will:

1. Increase the attenuation by –3dB and the phase shift by –45° at the cutoff frequency;
2. Increase the attenuation rate by –20dB/decade in the high-frequency range;
3. Increase the maximum phase shift by –90°.

Due to the symmetry, swapping R and C can yield a high-pass filter with the same cutoff frequency, as shown in **Figure 69**.

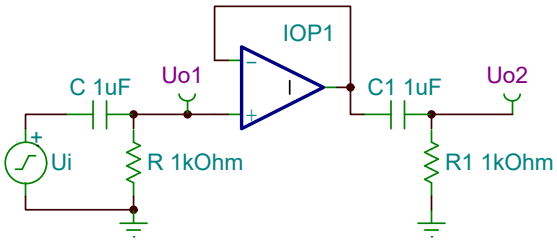


Figure 69. *Second-Order High-Pass Filter*

Analysis of the amplitude-frequency and phase-frequency characteristic curves of the high-pass filter, as shown in **Figure 70**, reveals that:

1. At the cutoff frequency, the phase shifts of the first-order high-pass filter and the second-order high-pass filter are 45° and 90°, respectively;
2. The maximum phase shifts of the first-order high-pass filter and the second-order high-pass filter are 90° and 180°, respectively;
3. The transition-band slopes for the first-order high-pass filter and the second-order high-pass filter are 20dB/decade and 40dB/decade, respectively.

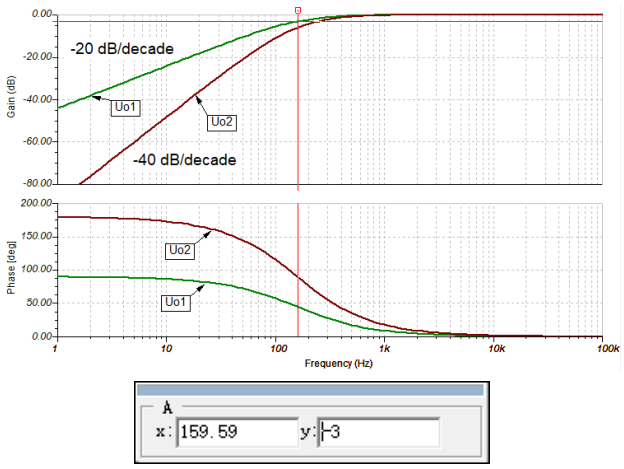


Figure 70. *Amplitude-Frequency and Phase-Frequency Characteristic Curves of the Second-Order High-Pass Filter*

Zeros and Poles

The concepts of zeros and poles are introduced into circuit analysis to help analyze the stability of feedback systems. While their definitions are not complicated, most people stop at this definitional stage, without further exploring their physical significance.

Transfer function

The transfer function in a circuit can be understood as an amplification factor. The circuit shown in **Figure 71** is isolated by an op amp into two stages: the first stage acts as a high-pass filter (cutoff frequency fL ≈ 1.6Hz), while the second stage functions as a low-pass filter (cutoff frequency fH ≈ 15.8kHz).

1. Based on the cutoff frequencies of the front and rear stages, it can be roughly understood that signals greater than 1.6Hz and less than 15.8kHz can pass through the filter. The circuit shown in **Figure 71** is a band-pass filter.

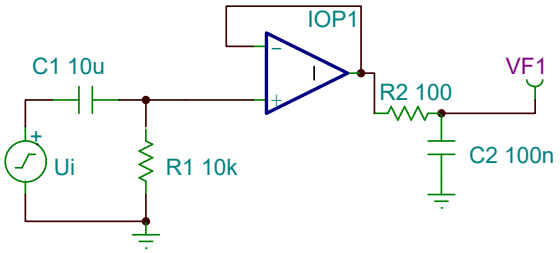


Figure 71. *Band-Pass Filter*

2. Assume that the first-stage amplification factor is A_1 and the second-stage amplification factor is A_2, and the total amplification factor is $A = A_1 \times A_2$. By the principle of impedance division, one can easily obtain **Equation 16**:

$$\begin{cases} A_1 = \dfrac{R_1}{\frac{1}{j\omega C_1} + R_1} = \dfrac{j\omega R_1 C_1}{1 + j\omega R_1 C_1} \\ A_2 = \dfrac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2} + R_2} = \dfrac{1}{1 + j\omega R_2 C_2} \end{cases} \tag{16}$$

3. Substituting s for jω (the Laplace transform) in Equation 2.9 yields **Equation 17**, and s-values that render the numerator zero are termed zeros, while those that render the denominator zero are termed poles. The highest exponent of s in the denominator is called the order of the filter.

$$\begin{cases} A_1 = \dfrac{sR_1C_1}{1 + sR_1C_1} \\ A_2 = \dfrac{1}{1 + sR_2C_2} \end{cases} \tag{17}$$

4. As can be seen from **Equation 17**, the high-pass filter represented by A_1 has a zero (0Hz) and a pole (1.6Hz) and the low-pass filter represented by A_2 has only one pole (15.8kHz). The order of the band-pass filter synthesized by A_1 and A_2 is 2nd order.

Zeros and poles in bode plots

It can be seen from **Equation 17** that in a band-pass filter as shown in **Figure 71**, there exists a zero at 0Hz and two poles at 1.6Hz and 15.8kHz. The physical significance of the zeros/poles at bode plots can be summarized as follows:

1. The slope change of the amplitude-frequency characteristic curve at zero is 20dB/decade with a phase shift of 45°.
2. The slope change of the amplitude-frequency characteristic curve at the pole is –20dB/decade with a phase shift of –45°.

Figure 72 shows the amplitude-frequency and phase-frequency characteristic curves of the band-pass filter.

1. At 0Hz zero (TINA simulation cannot start at 0Hz), the amplitude-frequency characteristic curve starts with a 20dB/decade slope.

2. The phase shift at the zero is 45°, but at frequencies significantly below zero, the phase shift is 90°, hence the phase-frequency characteristic curve commences at 90°.
3. At the first pole at 1.6Hz, the amplitude-frequency characteristic curve changes by –20dB/decade, resulting in a horizontal amplitude-frequency characteristic curve beyond 1.6Hz.
4. At the 1.6Hz pole, a –45° phase shift occurs, resulting in a total phase shift of 90°–45° = 45° at 1.6Hz. Far from the 1.6Hz pole, such as beyond 16Hz, the total phase shift becomes 90°–90° = 0°.
5. At the second pole at 15.8kHz, the amplitude-frequency characteristic curve changes by –20dB/decade, thus an amplitude-frequency characteristic curve becomes –20dB/decade beyond 15.8kHz.
6. At the 15.8kHz pole, a –45° phase shift occurs, resulting in a total phase shift of 90°–90°–45° = –45° at 15.8kHz. Far from the 15.8kHz pole, such as beyond 158kHz, the total phase shift becomes 90°–90°–90° = –90°.

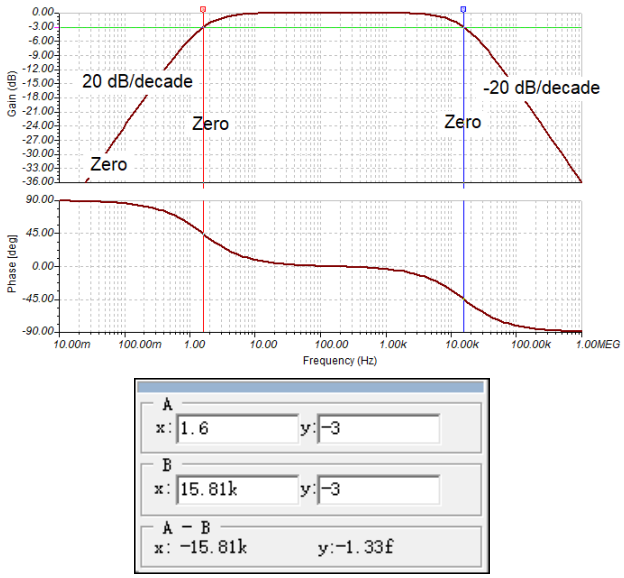


Figure 72. *Amplitude-Frequency and Phase-Frequency Characteristic Curves of the Band-Pass Filter*

Practical Equivalent Models of Resistor and Capacitor

Under low-frequency conditions, practical resistors and capacitors demonstrate characteristics closer to those of ideal components. However, at slightly higher frequencies, their high-frequency equivalent models must be considered. We are not going to discuss the equivalent models of inductors here, as inductor characteristics are closely related to magnetic materials, making the discussion somewhat complex.

High-Frequency Equivalent Model of Resistor

A practical resistor can be equivalently represented as an ideal resistor R in series with a parasitic inductor LS. The value of the parasitic inductor LS is very small, and the inductive reactance ZL is usually much lower than the impedance ZR, so the effect of the parasitic inductor is ignored. But when should we consider the parasitic inductor? Let's start with an example where a parasitic inductor plays a positive role.

1. In the circuit shown in **Figure 73**, the analog power supply AVDD and the digital power supply DVDD are actually sourced from the same power supply but are separated by a small-value resistor R.

Figure 73. *Power Supply Isolated by a Small Resistor*

2. When the current through resistor R reaches 10mA (such a current level typically allowing most chips to operate), the DC voltage difference between AVDD and DVDD is only 10mV (neglecting the voltage drop across Ls), which is lower than the ripple voltage of most DC supplies.
3. However, when there is high-frequency interference coupled through the power line generated by DVDD in a digital circuit, the parasitic inductor L_S, with its impedance much greater than 1Ω, can help isolate digital interference.

An example where the parasitic inductor has a negative effect:

1. The circuit shown in **Figure 74** is a switching circuit in power electronics. Current flows through the MOSFET switch when it conducts. However, when the switch is opened, the parasitic inductor L_S in the main circuit generates a high voltage across the switch to resist the current change, causing the switch to break down.

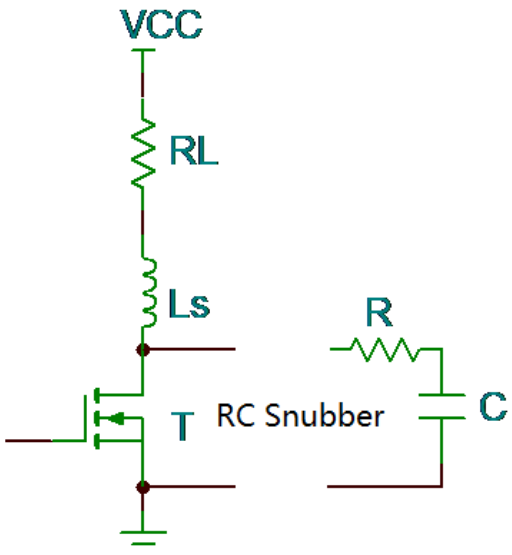


Figure 74. *MOSFET Switching Circuit*

2. It is a common practice to connect an RC snubber circuit in parallel with the switch for protection. When the switch is opened, the current from inductor L_S will flow into the RC circuit, preventing the generation of a high voltage.
3. As we mentioned earlier, the fundamental reason why a capacitor resists voltage changes lies in its ability to absorb and release a very large current. The parasitic inductance on resistor R will resist capacitor C from absorbing and releasing the "glitch" currents, significantly impairing the RC snubber circuit's ability to suppress high switching voltages.

4. Therefore, the resistor used for the RC snubber is a specially constructed "non-inductive resistor". Those "non-inductive resistors" are still inductive, but their parasitic inductance is lower than that of regular resistors. High-power non-inductive resistors generally employ the bifilar winding technique for the resistance wire, so the mutual inductance is canceled out to minimize parasitic inductance.
5. You may ask why we don't directly connect a capacitor C in parallel for snubbing, but instead include a series resistor R. Without resistor R, the effect of suppressing the glitch voltage would indeed be better. However, the energy stored in capacitor C will eventually be discharged through the switch T. Not including a series resistor R would cause over-current damage to the switch (resistor R may not be necessary if the value of capacitor C is sufficiently small).

Equivalent Model of Capacitors

As shown in **Figure 75**, a practical capacitor can be modeled as a series combination of a capacitor, a resistor, and an inductor. The equivalent series resistance (ESR) and equivalent series inductance (ESL) affect the characteristics of a capacitor in different ways.

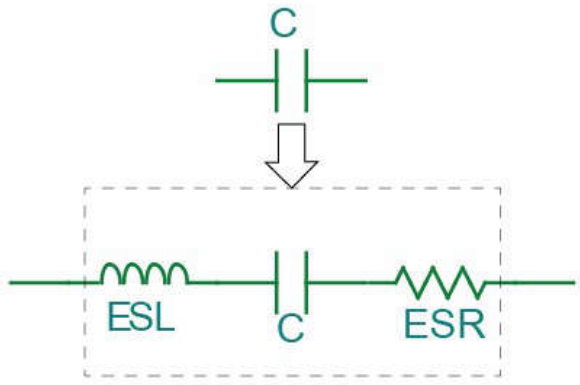


Figure 75. *Equivalent Model of Practical Capacitor*

Let's first learn about the impact of ESR. In addition to energy storage, another major application of capacitors is filtering. There are two types of large-capacitance filter capacitors: tantalum capacitors and aluminum electrolytic capacitors, with the former offering better performance at a higher cost. In fact, tantalum capacitors are also polarized electrolytic capacitors. Their major performance difference is their ESR.

1. The voltage across an ideal capacitor C will never "change abruptly"; even the largest charge or discharge current can only cause a "gradual" change in voltage. Theoretically, the voltage across a parallel capacitor in a circuit will not produce any voltage "glitches".
2. However, the voltage across the actual filter capacitor produces glitches, as shown in **Figure 76** (middle waveform; negative DC voltage).

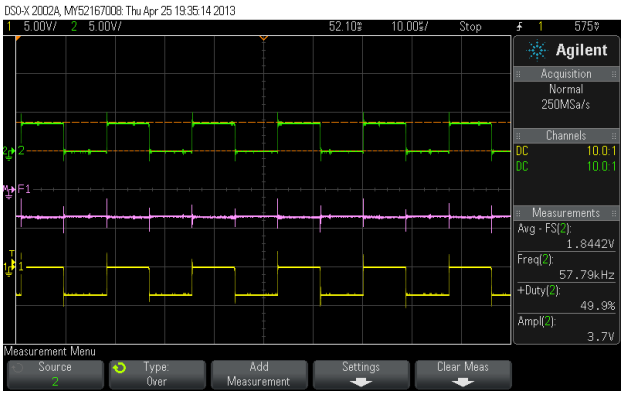


Figure 76. *Output of the TPS60400 Negative Voltage Chip*

3. The reason for the glitch voltage across the capacitor is the capacitor's ESR. The capacitor regulates its terminal voltage by absorbing and releasing current, which results in a voltage drop across the ESR, thus generating total voltage ripple and even voltage "glitches".
4. When the two types of capacitors have the same capacitance, the ESR of the tantalum electrolytic capacitor is much lower than that of the aluminum electrolytic capacitor. Therefore, the tantalum capacitor generates significantly lower voltage ripple in filtering, compared to the aluminum electrolytic capacitor. This is why, in many cases, we consider the filtering effect of a 1μF tantalum capacitor to be equivalent to that of a 10μF aluminum electrolytic capacitor.
5. Regarding tantalum capacitors as polarized capacitors, it is important to note their appearance markings: For those in through-hole packages, the longer lead serves as the anode. For those in surface-mount packages, however, the anode is the end marked with a line!

Next, let's learn about the impact of ESL. Due to the ESL, the capacitive and inductive reactance components within a capacitor vary with the frequency of the electrical signal. As shown in **Figure 77**:

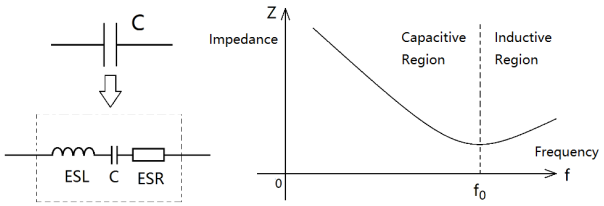


Figure 77. *Impedance of Practical Capacitor*

1. In the low-frequency band, all capacitors, without exception, exhibit capacitive characteristics (the higher the frequency, the lower the impedance). When the frequency exceeds the LC resonant frequency f_0, however, capacitors turn to exhibit inductive characteristics - the higher the frequency, the higher the impedance will be. Inductive characteristics, on the other hand, not only do not regulate the voltage, but also generate an induced voltage.
2. Capacitors with different materials and constructions have very different corner frequencies f_0. Generally speaking, large-capacitance capacitors have poor frequency characteristics (low corner frequency f_0), while small-capacitance ones have better frequency characteristics (high corner frequency f_0).

3. Thankfully, although the capacitance of high-frequency capacitors is small, their capacitive reactance, which truly plays a filtering role at high frequencies, is also very small. A "high-frequency low-capacitance" capacitor and a "low-frequency high-capacitance" capacitor can complement each other.
4. Different types of capacitors can be connected in parallel in a practical circuit to provide filtering over the full frequency range. In principle, when multiple capacitors are connected in parallel for filtering, their capacitive values should differ by at least a factor of 10, with a factor of 100 generally being preferable.

Input Impedance and Output Impedance

What are input impedance and output impedance? Let's introduce these two concepts from the simplest resistor circuit. As shown in **Figure 78**, the internal resistance of power supply E is r, and the load resistance is R. A line is drawn in the middle to divide the circuit into two parts: the power supply and the load. The internal resistance r is the output impedance of the power supply part, while the resistance R is the input impedance of the load part.

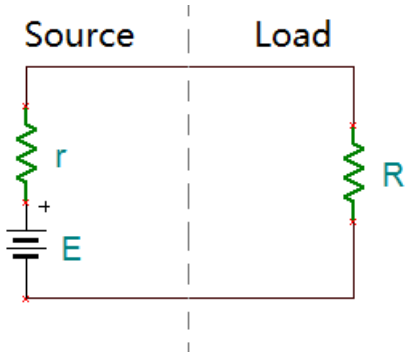


Figure 78. *Power Supply and Load Circuit*

Understand the input and output impedances qualitatively. Since the vast majority of power supplies in circuits are voltage sources and the signals are voltage signals, if we regard the circuit as a two-port network with two input terminals and two output terminals, as shown in **Figure 79**, the following conclusions can be drawn:

1. The output impedance R_O reflects the circuit's ability to drive a load. The lower the output impedance is (or the lower the internal resistance of the power supply is), the stronger the load drive ability will be.
2. The input impedance R_I reflects how "heavy" or "light" the circuit itself is as a load. The larger the input impedance is, the less current the circuit draws from its upper-level power supply. Such a circuit is a "light" load. Otherwise, it's a "heavy load".
3. We always want a circuit's output impedance R_O to be as small as possible, so that its load drive ability is stronger (the output voltage generally decreases as the load increases). At the same time, we hope that the input impedance R_I of this circuit is as high as possible, as this makes it easier for the preceding circuit to drive it.

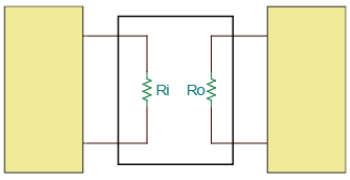


Figure 79. *Input and Output Impedances of Two-Port Network*

Calculate the input and output impedances quantitatively. Instead of literally understanding the input and output impedances as actual circuit resistance, we should view them from the perspective of an equivalent "black box" model.

1. As shown in **Figure 80**, when the circuit's output voltage is U_O at no load and $0.5U_O$ when a load of R_L is connected, its output impedance r can be considered equal to R_L.

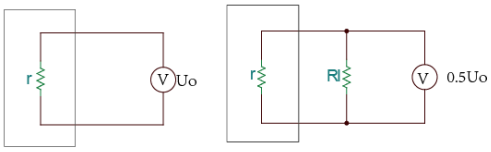


Figure 80. *Diagram for Output Impedance Calculation*

2. The output impedance does not necessarily come from a physically existing resistor. As shown in **Figure 81**, the actual internal resistance of the power supply is 1kΩ, and the measured output voltage is 10V at no load. After a 1kΩ load is applied, the power supply covertly raises the voltage to 20V, while the voltmeter still reads 10V for the output voltage. This indicates that the output impedance of the circuit on the left is 0Ω. The example shown in **Figure 81** is not a special case of a "brain teaser"; rather, most practical circuits we design exhibit conditions where the power supply's electromotive force (EMF) is "covertly altered", though not necessarily to the extreme of making the output impedance zero.

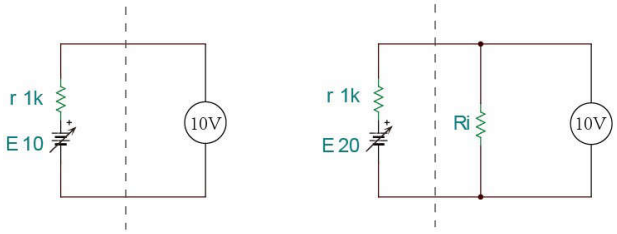


Figure 81. *Equivalent Output Impedance*

3. The input impedance of a circuit is measured in a similar way. As shown in **Figure 82**, connect a resistor R in series with the input signal U_I. When $U_I = 2U_I'$, the input impedance R_I equals the value of the series resistor R.

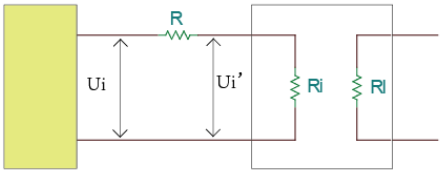


Figure 82. *Diagram for Input Impedance Calculation*

Bandwidth of Circuit

Oscilloscope is the most commonly used instruments in electronics labs, and we often hear the term "a 100MHz oscilloscope". So what does 100MHz mean here? Does it mean the oscilloscope can observe signals up to 100MHz? Before addressing this question, let's first clarify the concept of frequency within circuits.

1. Are the frequencies of the two signals shown in **Figure 83** identical? The answer is not the same. The frequency in a circuit exclusively refers to the frequency of a sinusoidal signal, and the frequencies of other waveforms must be Fourier decomposed into a series of sine waves that can be discussed.

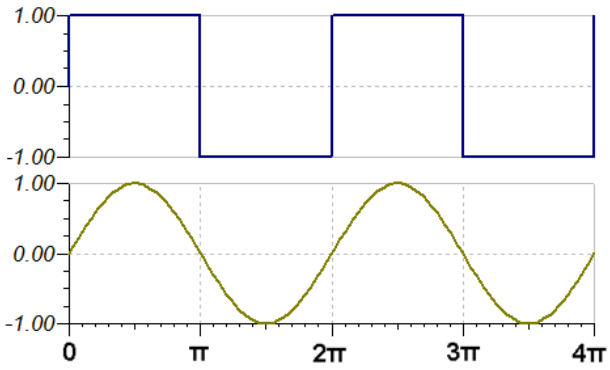


Figure 83. *Signal Frequency*

2. The amplitude shown in **Figure 83** is 1, and the Fourier decomposition for a standard square wave with a repetition period of 2π is:

$$f(t) = \frac{4}{\pi}\left(\sin t + \frac{1}{3}\sin 3t + \frac{1}{5}\sin 5t \cdot \cdot \cdot\right) \tag{18}$$

3. **Equation 18** indicates that the square wave is composed of a series of sine waves at odd multiples of the fundamental frequency. The wave with the same period as the square wave (2π) is termed the fundamental wave, while the others are designated as the third harmonic, the fifth harmonic, and so forth. By selecting the fundamental wave and a series of harmonics for superposition, it yields the effect shown in **Figure 84**.

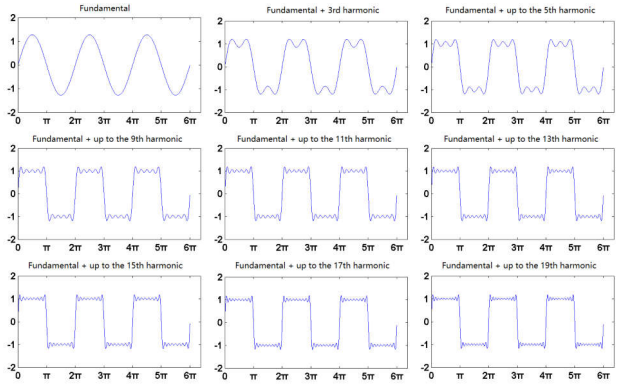


Figure 84. *Square Wave Effect Synthesized by Harmonics of Different Frequencies*

4. Why must we perform such a Fourier decomposition? This is because in the expressions for inductive and capacitive reactance, the angular frequency ω pertains to sine waves. In square wave signals, different harmonic frequency components encountering capacitors and inductors result in entirely distinct impedances, leading to completely different circuit characteristics.

Next, we shall explain what bandwidth is. Any conductor in a circuit possesses resistance, and an ungrounded conductor exhibits capacitance to ground. This gives rise to the ubiquitous low-pass circuit illustrated in **Figure 85**.

Not only conductors, but the internal structure of circuit components also inherently contains parasitic low-pass filter circuits.

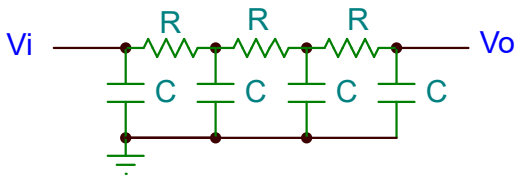


Figure 85. *Parasitic Low-pass Filter Circuit*

1. The presence of parasitic low-pass filter circuits makes any circuit challenging when dealing with high-frequency signals.
2. Oscilloscope, being an instrument composed of electronic circuits, is no exception. A 100MHz bandwidth oscilloscope implies that if a $1V_{PP}$/100MHz sine wave is input, the signal will have been attenuated to $0.707V_{PP}$/100MHz by the time it reaches the oscilloscope's "core processing unit". (Bandwidth is defined as the frequency at which the signal is attenuated to $1/\sqrt{2}$, or 0.707 times its original value)
3. For a 100MHz square wave signal with a "repetition frequency" entering the oscilloscope, the fundamental component of the square wave is attenuated by a factor of 0.707, while harmonic components suffer greater attenuation (due to their higher frequencies). On the oscilloscope screen, it will appear essentially as a sine wave.
4. As an instrument for observing signals, an oscilloscope naturally cannot capture a perfectly pure fundamental sine wave. To minimize the loss of other signal details (high-frequency components), a 100MHz bandwidth oscilloscope is typically only suitable for observing signals with repetition frequencies between 10-20MHz.

Generally, we strive to design circuits with the widest possible bandwidth to handle the "richest" signals. However, we sometimes employ low-pass filters to limit bandwidth, thereby avoiding amplification of unwanted high-frequency interference signals.

Temperature Characteristics of Electronic Components

Many environmental factors can affect the characteristics of electronic components, with temperature being the most significant one. This section will separately introduce the typical effects of temperature on resistors, capacitors, and semiconductor devices.

Temperature Characteristics of Resistors

Resistors can be classified into six series based on their accuracy: E6, E12, E24, E48, E96, and E192, with respective tolerances of ±20%, ±10%, ±5%, ±2%, ±1%, and ±0.5%. Taking the most commonly used E24 series as an example, its resistance values are determined as follows:

1. Expression for the base values: $\sqrt[24]{10^{n}}\left(n = 1,2,3\ldots 24\right)$. The calculated base values are: 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, 3, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1, and 10.
2. Multiplying a base value by a power of 10 yields resistance of different orders of magnitude, such as 5.1Ω, 51Ω, 510Ω, 5.1kΩ, 51kΩ, 510kΩ, 5.1MΩ, but no E24 resistor will have a value of 5Ω.

One way to obtain a sniper rifle is not to specially design and manufacture one, but to cherry-pick the most accurate one from regular rifles. So, are resistors in various series cherry-picked and classified as E24 or E96, based on their resistance values?

1. It is certainly possible that we may cherry-pick resistors with a resistance value of 9.9kΩ or higher from multiple 10kΩ resistors with a tolerance of 5%.
2. Resistors in various series are actually classified based on their materials and processes, not merely on their resistance values.
3. The resistance of all resistors increases with temperature. Low-accuracy resistors have poorer temperature stability than accurate resistors. Even if their resistance values are accurate, low-accuracy resistors may not be suitable substitutes for accurate resistors.

Temperature Characteristics of Capacitor

What do you think about a 1μF capacitor with an accuracy of –20% to +80%? This indicates that the actual capacitance of this capacitor is between 800nF and 1.8μF. Is it still useful? The accuracy of capacitors and resistors is not comparable, though a comparison is inevitable. In most cases, we can tolerate the error of capacitors, so the difference in capacitance values caused by temperature is negligible. The effect of temperature on capacitors is mainly reflected in their lifespan:

1. Compared to mechanical products, the lifespan of electronic products seems to be infinite. But circuit boards can also deteriorate and fail, with electrolytic capacitors being the most significantly affected.
2. When we find a possibly "brand new" circuit board in the warehouse, it is likely that its electrolytic capacitors should be replaced before we use it.
3. The lifespan of electrolytic capacitors is halved for every 10°C increase in operating temperature. Ideal capacitors generate neither active power nor heat, but the equivalent series resistor (ESR) within a capacitor can experience Joule heating when an AC current flows through it. Even capacitors used for DC filtering have an AC ripple current, which requires your attention.

Temperature Characteristics of Semiconductor Components

The semiconductor components referred in this section specifically denote bipolar semiconductor devices where both majority and minority carriers participate in conduction. The fundamental principle of semiconductor devices is to sacrifice conductivity for controllability. Unlike resistors, temperature significantly enhances the conductive properties of semiconductors. The detrimental effects of temperature on semiconductors manifest in two aspects: "temperature drift" and "negative temperature coefficient".

1. Temperature variations induce "temperature drift" in semiconductor devices, meaning alterations in circuit parameters, which are highly detrimental to circuit operation. Temperature drift and its mitigation will be detailed in Section 3.5 on differentiator circuits.
2. The so-called negative temperature coefficient refers to the decrease in a semiconductor's equivalent on-resistance as temperature increases. The resistance of a normal conductor features a positive temperature coefficient. When a conductor's current-carrying capacity proves insufficient, it is natural to consider using two conductors in parallel. As

shown in **Figure 86**, when a diode's current-carrying capacity is inadequate, can we simply connect two diodes in parallel?

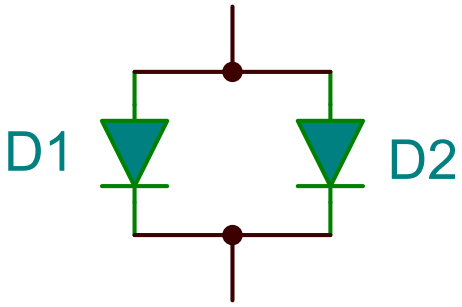


Figure 86. *Diodes in Parallel*

3. When two devices with negative temperature coefficients are connected in parallel, a "current sharing" issue arises. Assuming that when current reaches D_1 and D_2, the current on D_1 is greater than D_2, thus D_1 is much hotter than D_2. Because of the negative temperature coefficient, D_1 becomes more conductive, and the voltage drop on D_1 is lower, resulting in more current flow to D_1. The vicious cycle intensifies D_1 to heat up...
4. Typically, without additional current sharing control measures, identical D_1 and D_2 devices may exhibit current distribution ratios as extreme as 1:9. Think about current sharing in the positive temperature coefficient resistor and conductor?

Thermal Resistance and Thermal Dissipation

It is a common phenomenon among students that they become flustered, fearing something is about to burn out, when they find a component hot to the touch, and often assume everything is fine after attaching a "mini" heat sink.

1. In fact, it is not necessarily abnormal for a component to feel hot to the touch. Humans perceive temperatures above 55°C as hot, yet many high-speed components normally operate at 70-80°C due to their significant power dissipation. Insisting that these components should not feel hot to the touch is "unreasonable".
2. On the other hand, a heat sink may not solve all problems. In many cases, the thermal dissipation of the heat sinks added by students is so weak that it is barely better than nothing.

This section is going to cover the quantitative calculation of thermal dissipation. While cutting corners and using inferior materials is not advised, over-engineering in design is also a sign of incompetence. In a documentary about the design of a certain aircraft model, there is a segment on stress failure test: "The wing experienced failure at the predicted location when subjected to 102% of the design load; the fuselage experienced failure at the predicted location when subjected to 105% of the design load." A qualified design is one with its design margins clearly specified!

Junction Temperature vs. Ambient Temperature

The concept of thermal dissipation is based on a fundamental premise: The ambient temperature where the heat-generating device is located must be lower than the device's own temperature to allow for thermal dissipation.

1. If the ambient temperature reaches 200°C, it is apparently difficult for chips to dissipate heat. In this case, it is necessary to manufacture chips with a temperature resistance of up to 200°C. Some chips for sensors used in underground drilling applications fall into this category of being unable to sink heat.
2. If the ambient temperature remains constant, say at 25°C, and the "thermal dissipation pathway" is extremely unobstructed, the chip temperature would be consistent with the ambient temperature. However, it is obvious that the "thermal dissipation pathway" is somewhat obstructed, causing the actual temperature of the heat-generating chips to exceed 25°C. To determine the exact temperature difference, it is necessary to introduce the concept of thermal resistance.

As shown in **Equation 19**, P represents the chips' power dissipation, Ta is the ambient temperature, and Tj is the chips' junction temperature.

$$T_j = P \cdot R_T + T_a \tag{19}$$

1. Thermal resistance R_T is a physical term that describes the resistance to thermal dissipation. The higher the thermal resistance, the more difficult thermal dissipation will be. It is measured in °C/W. If a chip has a thermal resistance of 1°C/W, 1W of power dissipation will raise the chip temperature by 1°C.
2. The junction temperature of a chip, T_j (which cannot be felt by the hand; only the case temperature is tangible), must be higher than the ambient temperature T_a. The extent of this difference depends on the chip's power dissipation and thermal resistance.
3. Semiconductor devices made from silicon dioxide can typically withstand a maximum junction temperature of approximately 150°C. Considering the basic ambient temperature and a safety margin, the generally permissible temperature rise due to power dissipation should not exceed 100°C.

Calculation of Thermal Resistance

1. The heat sink has a decisive influence on the magnitude of the thermal resistance. **Equation 20** describes the thermal resistance of the chip without a heat sink, and **Equation 21** describes the thermal resistance when there is a heat sink.

$$R_T = R_{jc} + R_{ca} \tag{20}$$

$$R_T = \left(R_{jc} + R_{ca}\right) // \left(R_{jc} + R_{cs} + R_{sa}\right) \tag{21}$$

1. The concept of thermal resistance is similar to that of resistance. Since only the ambient temperature is considered to have the largest heat capacity and remain constant (analogous to the ground in a circuit), the thermal dissipation "pathways" must be connected "in series" from the junction all the way to the air.
2. According to **Equation 19**, the junction-to-case thermal resistance R_{jc} and the case-to-ambient thermal resistance R_{ca} are "connected in series" to form a complete "pathway" for thermal dissipation.

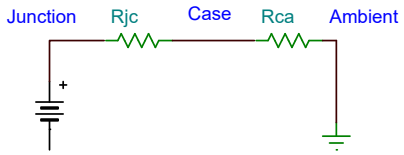


Figure 87. *Diagram for Thermal Resistance without Heat Sink*

3. As shown in **Figure 88**, the incorporation of a heat sink is equivalent to adding a thermal dissipation pathway. There is a thermal resistance R_{cs} between the case and the heat sink, and a thermal resistance R_{sa} between the heat sink and the ambient environment.

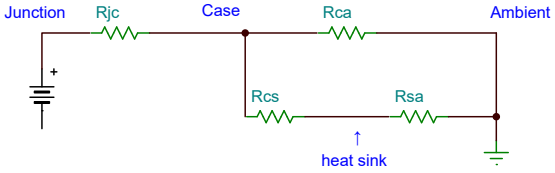


Figure 88. *Diagram for Thermal Resistance with Heat Sink*

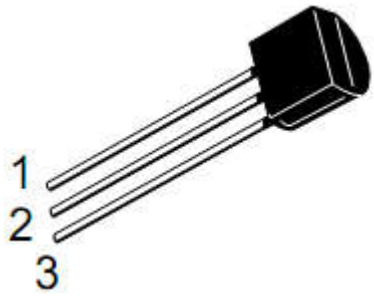
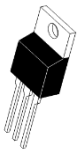
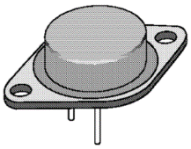
4. Since $R_{ca} >> (R_{cs} + R_{sa})$, the total thermal resistance can be approximated as **Equation 22** when a heat sink is connected. Generally, when high-quality thermal grease is applied, the case-to-heat-sink thermal resistance $R_{cs} << R_{sa}$, so R_{cs} can also be ignored.

$$R_T \approx R_{jc} + R_{cs} + R_{sa} \tag{22}$$

Thermal Resistance of Common Packages and Heat Sinks

The thermal resistance parameters of the packages for the three most commonly used power semiconductors, are shown in **Table 2**.

Table 2. Thermal Resistance of Common Packages

Package name	TO-92	TO-220	TO-03
Package appearance			
R_{jc}	83.3℃/W	1.92℃/W	1.4℃/W
R_{ca}	116.7℃/W	60.58℃/W	33.6℃/W

1. Referring to **Equation 20**, the junction-to-case thermal resistance, R_{jc}, cannot be reduced by a "parallel" heat sink, thus, once R_{jc} is very large, it means that this package cannot accommodate additional heat sinks. R_{jc} of TO-92

package is as high as 83.3°C/W. This implies that even with the case temperature maintained constant (even if cooled by liquid nitrogen), a 1W power dissipation would cause a temperature rise of 83.3°C.

2. Components in TO-220 and TO-03 packages are suitable for adding heat sinks, but without one, their inherent metal cases offer poor thermal dissipation. A rough estimate suggests that even a TO-03-packaged component can only dissipate no more than 4W power.

Figure 89 shows a heat sink for half-brick converters that can be fitted with fans for forced air cooling (corresponding to natural air cooling without fans). In addition, a good heat sink should have a passivated surface (not a mirror finish), preferably in black.

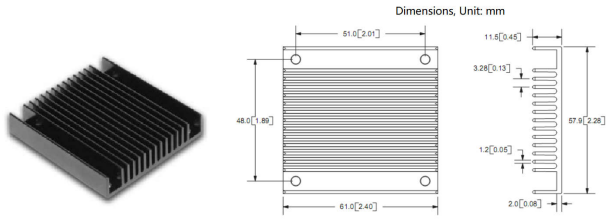


Figure 89. *Appearance and Size of a Heat Sink*

The thermal resistance of a half-brick heat sink is shown in **Figure 90**, with the vertical axis denoting thermal resistance and the horizontal axis indicating the airflow velocity under the forced air cooling.

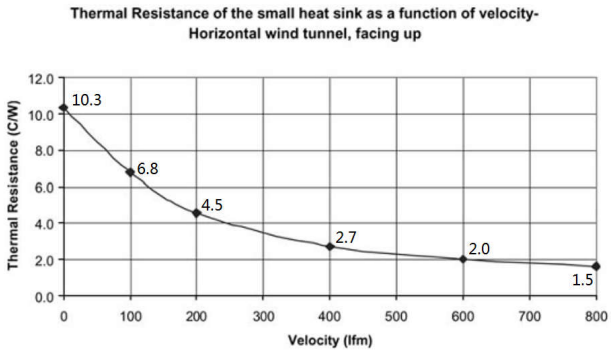


Figure 90. *Thermal Resistance in Case of Forced Air Cooling*

1. Without a fan, the thermal resistance of such a heat sink is 10.3°C/W.
2. With sufficient air cooling, the thermal resistance can be reduced to 1.5°C/W. If better thermal dissipation is required, water must be cooled.

Impedance matching

If you have seen the coaxial cable used by cable TV, you will notice that the cable will have 75Ω printed on its outer skin. As we learned from physics at childhood, the resistance of a wire is proportional to the length, so why is 75Ω printed directly on a coaxial cable that has nothing to do with the length? This is because the coaxial cable impedance no longer satisfies the conditions for "a lumped-parameter circuit".

The contents of the "distribution parameter circuit" are not typically covered in the analog electronic circuit book, but it is useful to know about impedance matching in the circuit.

Characteristic Impedance of Transmission Line

In high-speed circuits, conductors can no longer be treated as "lumped-parameter circuits" where potential is uniformly distributed across all points. The conductor should be considered a transmission line when the signal wavelength is less than 1/7 of the conductor length.

1. As shown in **Figure 91**, the parasitic inductance and capacitance of any conductor generate capacitive reactance and inductive reactance.
2. At high frequencies, when conductor is treated as transmission line, the capacitive and inductive components will be significantly greater than the conductor's resistance.
3. **Figure 91** indicates that the impedance of a transmission line is independent of its length. For coaxial cables made of uniform material, the characteristic impedance remains constant; for example, the characteristic impedance of coaxial cable used in cable television is 75Ω, while that for network applications is 50Ω.

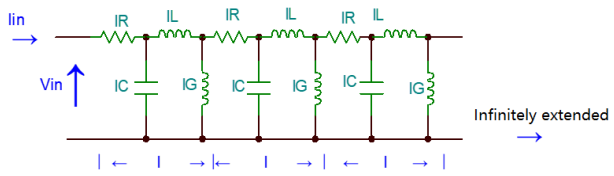


Figure 91. *Transmission Line Diagram*

$$Z_0 = lR + \sqrt{\frac{L}{C}} \approx \sqrt{\frac{L}{C}} \tag{23}$$

Impedance matching is essential from the "power supply" through the "transmission line" to the "load". Why is impedance matching required?

1. In the lumped-parameter circuit, impedance matching (internal resistance = external resistance) allows the load to receive the maximum power output.
2. In transmission line theory, impedance must be uniformly distributed along the line; otherwise, standing wave reflections occur. This not only reduces power delivered to the load but also causes signal distortion (overshoot, ringing) from reflected waves.
3. As shown in **Figure 92**, the PCB wiring is designed with the same consideration in mind to avoid right-angle traces. However, the impact of right-angle traces is negligible in circuits operating at frequencies of MHz or below; significant effects only manifest at GHz levels.

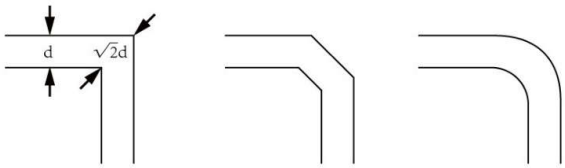


Figure 92. *Impedance Discontinuities due to Right-Angle Traces*

Impedance Matching Methods

A design approach typically based on a lumped-parameter circuit often leads to impedance mismatch. As shown in **Figure 93**, we usually want the "signal generator" output impedance r to be as low as possible, and the load impedance R to be as high as possible. However, their impedances will thus not match the 50-ohm transmission line, leading to a series of undesirable consequences such as standing wave reflections.

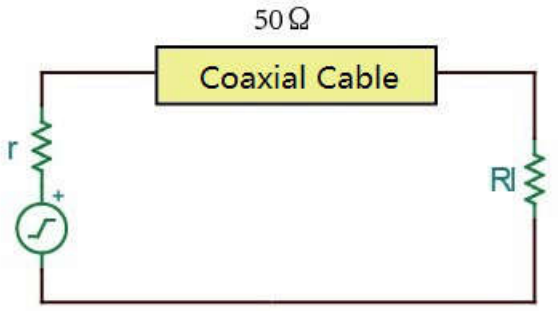


Figure 93. *Example of Unmatched Impedance*

Impedance matching methods include series connection and parallel connection.

1. Connect a resistor (e.g., 50Ω) in series with the "signal generator" to increase the internal resistance of the power supply and match the transmission line impedance.
2. Connect a resistor (e.g., 50Ω) in parallel with the "load" to reduce the load resistance and match the transmission line impedance.

Power factor

This section is based on real-life examples that have taken place recently, so it is arranged in the last section. The story is this, I bought a few nominal 3W LED bulbs that look exactly the same as a normal incandescent lamp, and the brightness is adequate. The hands are not hot to touch. I asked the students to measure the actual power output to see if they'd been misled by the seller.

The lab's power meter was not found, so the students measured it in this manner by referring to **Figure 94**:

1. We found a desk lamp, stripped one of its power cords, and connected it in series to the multimeter's AC current setting (It took me 10 seconds to realize that the red and black probes don't need to be distinguished by direction).
2. The multimeter reading was 0.072A, which confirmed my suspicion of encountering a dishonest trader. The actual power consumption was 15.84W (calculated by multiplying 220V by 0.072A).

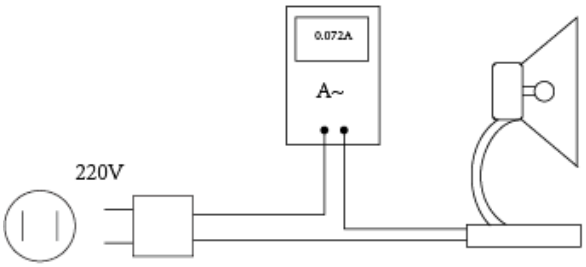


Figure 94. *Power Test Schematic Diagram*

Have they ever encountered a dishonest trader? That's rather difficult to say. For incandescent bulbs, measurements taken this way are generally reliable. However, with LED lights, the power factor is very low, so one cannot draw conclusions lightly. The concept of power factor may seem straightforward, but in practice it often proves to be a rather muddled affair. We will then start with the effective value (RMS value) and figure out what is actually active power, apparent power, and power factor.

Effective Value

When voltages or currents with the same average value are applied to the same load, their power outputs will differ.

1. As shown in **Figure 95**, the three voltage sources V_1, V_2, and V_3 exhibit different output amplitudes and duty cycles but identical average values of 1V, all connected to a 1Ω load.
2. The output powers of these three sources, namely P_1, P_2, and P_3, average 1W, 2W, and 4W, respectively.
3. This indicates that the effect (effective value) of V_1 is equivalent to a constant voltage of 1V applied to the same (pure resistive) load; that of V_2 is equivalent to a constant voltage of $\sqrt{2}$V applied; and that of V_3 is equivalent to a constant voltage of 2V applied.
4. The steeper the voltage (current) waveform is, the larger its effective value will be!
5. The concept of effective value applies only to current and voltage, not to power. As we will discuss later, the equivalent effect of the effective value is only valid for pure resistive loads and cannot be applied directly (without correction) to other loads.

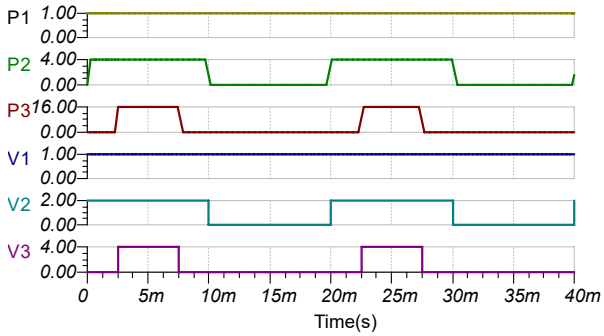


Figure 95. *Power Comparison for Voltages with Equal Average Value*

The effective value refers to the voltage or current calculated in a way that ensures equal power output. Since power can be expressed as U^2/R or I^2R, the effective value is defined as the root mean square (RMS) value, which is calculated by squaring, integrating, and then taking the square root.:

$$U = \sqrt{\int u^2 dt} \tag{24}$$

Or $I = \sqrt{\int i^2 dt}$

Displacement Factor

In high school physics, we learned that voltage and current being out of phase can cause the load power to alternate between positive and negative values, which gave us our initial understanding of power factor. In analog electronics, current and voltage being out of phase is only one of the causes of a decreased power factor, known as the displacement factor.

Calculations on the circuit shown in **Figure 96** using knowledge of impedance reveal that:

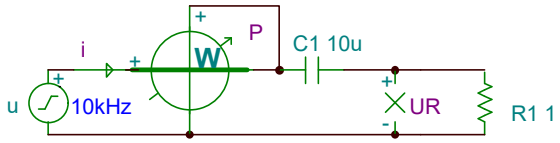


Figure 96. *Simulation of Displacement Factor*

1. Given a 10kHz, 1V amplitude (0.707Vrms) sinusoidal voltage source, the capacitive reactance of C_1 can be calculated as follows:

$$X_C = \frac{1}{\omega C} = \frac{1}{2 \times 3.14 \times 10 \times 10^3 \times 10 \times 10^{-6}} = 1.59\Omega \tag{25}$$

2. The total impedance of the resistor and capacitor is:

$$|Z| = \sqrt{R^2 + {X_C}^2} = \sqrt{1^2 + 1.59^2} = 1.88\Omega \tag{26}$$

3. The RMS value of the supply current i is:

$$I = \frac{U}{|Z|} = \frac{0.707}{1.88} = 0.376A \tag{27}$$

4. The phase by which current i leads voltage U is:

$$\varphi = \arctan\left(\frac{X_C}{R}\right) = \arctan\frac{1.59}{1} = 57.83^O \tag{28}$$

5. The power on the resistor is active power, and the current through the resistor equals the supply current i, so the active power can be calculated as follows:

$$P = I^2R = 0.376^2 \times 1 = 0.141W \tag{29}$$

6. According to high school physics, the power factor can be calculated as follows:

$$\lambda = \cos\phi = \cos 57.83^{o} = 0.532 \tag{30}$$

7. By official definition, the ratio of active power to apparent power is the power factor, and cosφ represents the displacement factor (which equals the power factor only in special cases). Apparent power is defined as the product of the RMS value of voltage and the RMS value of current, i.e.:

$$\lambda = \frac{P}{S} = \frac{P}{U \cdot I} \tag{31}$$

Next, the circuit shown in **Figure 96** is simulated using TINA to verify the above calculations. The simulation results are shown in 2.11.4, and the start/stop period for the transient analysis is set to 1s-1.0003s, respectively.

1. *P* represents the waveform of power meter readings. The average value of the power meter readings is the active power, 0.143W, which is consistent with the theoretical calculation of 0.141W.
2. *i* represents the waveform of the supply current and load current. The RMS value is 0.376A, which is consistent with the theoretical calculation of 0.376A. The consistency of P and i naturally ensures that the power factor is also consistent.

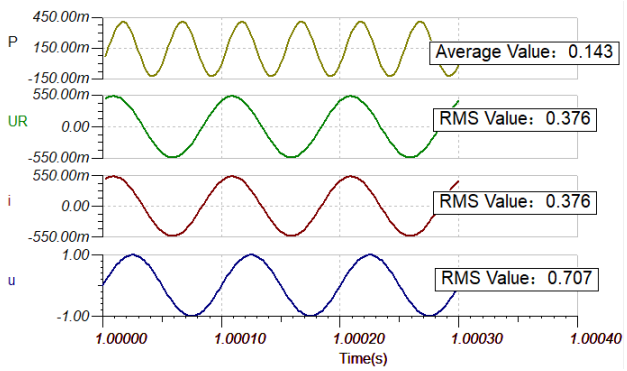


Figure 97. *TINA Simulated Waveforms of the RC Circuit*

3. Finally, let's examine the phase relationship between u and i. Right-click on the u and i waveforms, respectively, and select “Fourier Series” from the menu. Set parameters such as fundamental, sample number, harmonic number, and format, then generate fundamental phases shown in **Equation 27**.
4. The phase difference between *u* (–90°) and i (32.38°) is 57.62°, which is consistent with the theoretical calculation of 57.83°.

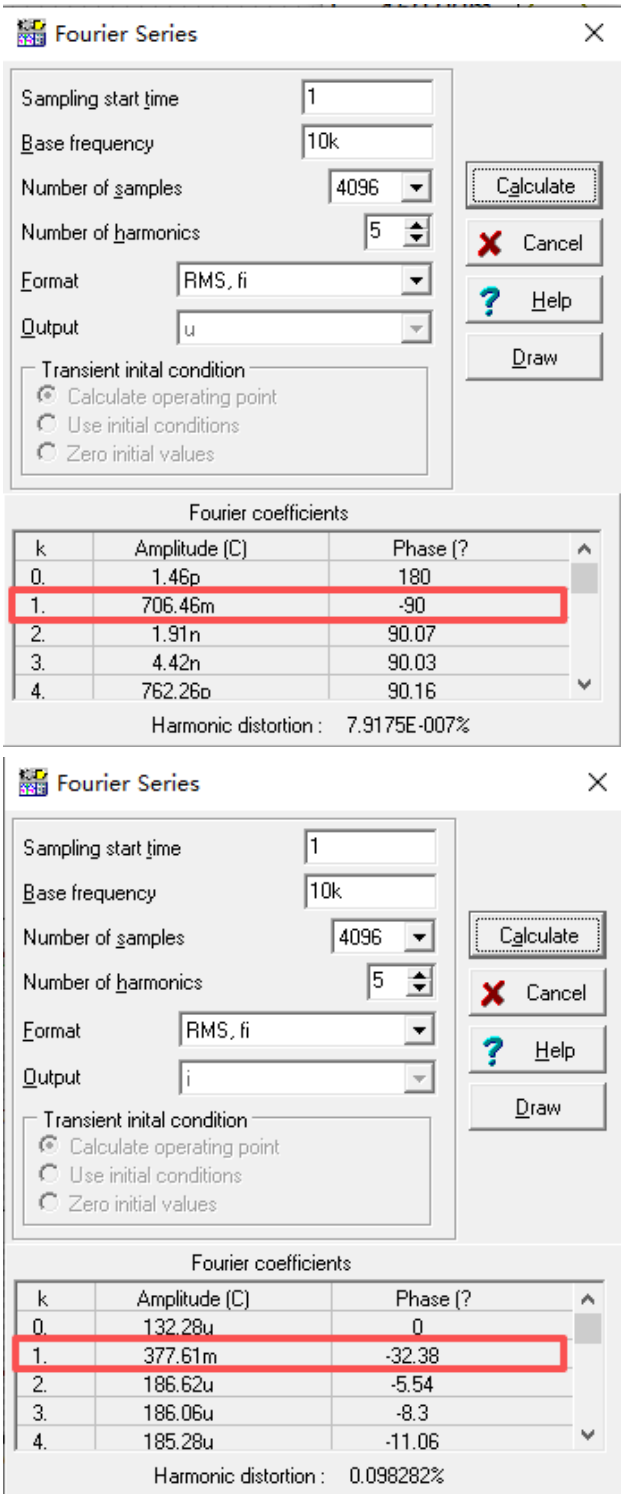


Figure 98. *Voltage-Current Phase Relationship*

Fundamental Factor

In the previous section, we mentioned that the phase shift between voltage and current, which causes instantaneous power to be sometimes positive or sometimes negative, is just one situation that affects the power factor. The circuit

shown in **Figure 99** is a bridge rectifier circuit with an inductor filter. For the power supply, voltage and current are always in phase. So, would the power factor of this circuit be 1?

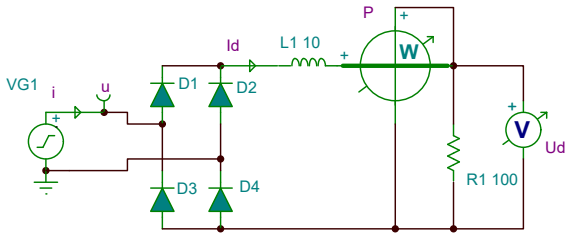


Figure 99. *Bridge Rectifier Circuit with Inductor Filter*

1. Given the significant inductance of inductor L_1, the current I_d flowing through it is generally a constant DC. Consequently, the current i from the voltage source VG_1 transforms into a square wave DC. Since it is a voltage source, the voltage u also naturally remains a sine wave, as shown in 2.11.7.
2. The parameters of the voltage source u are fully consistent with those of mains electricity: 50Hz, 220V RMS (310V peak).
3. The IN4007 rectifier diodes D_1-D_4 form a bridge rectifier circuit. Due to the high input voltage, the power dissipation of these diodes can generally be neglected (approximately 1%).
4. The simulated waveforms show that u and i are in phase, leading to no negative products of them.

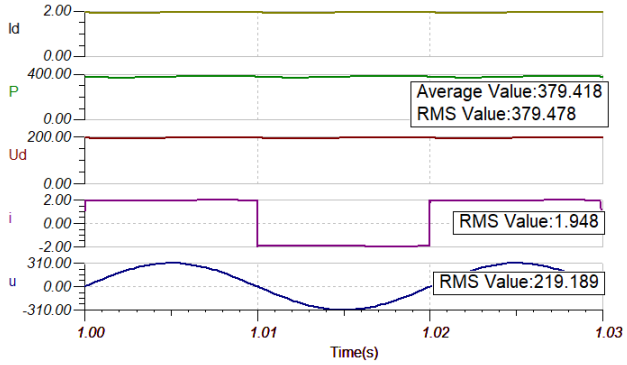


Figure 100. *TINA Simulated Waveforms of the Rectifier Circuit with Inductor Filter*

5. Based on the simulated waveforms, apparent power is calculated, as shown in **Equation 32**. Note: Apparent power is not measured in watts (W), but in volt-amperes (VA).

$$S = U \cdot I = 219.189 \times 1.948 = 426.98VA \tag{32}$$

6. The power on the load, which is active power, averages 379.418W. Therefore, the power factor can be calculated as:

$$\lambda = \frac{P}{S} = \frac{379.418}{426.98} \approx 0.89 \tag{33}$$

7. Why is the power factor below 0.9? When the diode power dissipation is taken into account, there should only be a 1% difference (estimated based on the ratio of the 2V voltage drop to the 220V supply voltage).

In addition to the displacement factor, there is also another element of the power factor, known as the fundamental factor.

1. According to official guidelines, we only discuss cases where the voltage has a sinusoidal shape. If it had unusual shapes, it would be challenging to continue our discussion. In general, the assumption that electrical appliances do not change the shape of the mains voltage is acceptable.
2. Continuing with the official guidelines, only the fundamental wave in the current contributes to active power. Other current shapes must be Fourier decomposed into their fundamental waves before their RMS values are calculated.
3. According to the previous guideline, the square wave shown in **Figure 100** should be Fourier decomposed. As shown in **Figure 101**, the RMS value of the fundamental wave is 1.75A. Such a conversion reveals that the active power produced by the fundamental current is 1.75 × 220 = 385W, and the power factor is 385/426 = 0.9, which is fully consistent with the theoretical value.

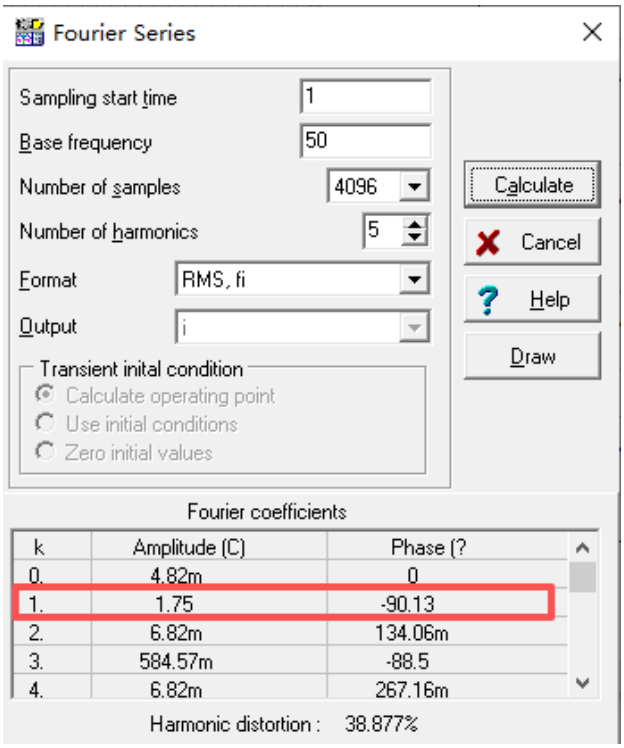


Figure 101. *Fourier Decomposition of Square Wave*

4. In fact, the RMS value of the fundamental wave Fourier decomposed from the pure square wave is 90% of its amplitude. The ratio of the RMS value of the fundamental current I_1 to the RMS value of the total current I is termed the fundamental factor, expressed as:

$$\upsilon = \frac{I_1}{I} \tag{34}$$

5. The power factor can be written as:

$$\lambda = \frac{P}{S} = \upsilon \cdot \cos\phi_1 \tag{35}$$

This indicates that the power factor is the product of the fundamental factor υ and the displacement factor $\cos\varphi_1$. The displacement factor describes the phase difference between the fundamental wave of the current and the voltage.

Three Questions about Power Factor

In the previous section, we performed a series of seemingly brilliant calculations and derivations based on the definition of power factor and official regulations. While they seemed coherent, we might still be in a muddle. A few questions will be addressed here.

Question 1: Why can only the fundamental current generate active power?

1. To be precise, it is not that the fundamental current generates active power. Rather, if one insists on calculating the active power by directly multiplying the RMS voltage by the RMS current, then only the fundamental current can generate active power.
2. If we don't involve the concept of "RMS value", any active power calculation should be the integral of the product of current and voltage, i.e.:

$$P = \int u \cdot idt \tag{36}$$

3. In the example shown in **Figure 100**, the power of the square wave current and sinusoidal voltage from the power supply should be:

$$P = \int u \cdot idt = \frac{1}{2\pi}\left(\int_0^{\pi} I \cdot U_m \sin\omega t d\omega t + \int_{\pi}^{2\pi} (-I) \cdot U_m \sin\omega t d\omega t\right) \tag{37}$$

4. The calculation of the power factor is fully consistent with the theoretical value, with the square wave current set at 2A.

$$\lambda = \frac{P}{S} = \frac{394.9}{220 \times 2} \approx 0.9 \tag{38}$$

5. What makes us in a muddle is that the concept of RMS value does not guarantee "power equivalence" when the voltage and current exhibit different shapes. Do you still remember how RMS values are derived? They are derived based on the special case where a pure resistor is used, satisfying the relationships $P = U^2/R$ and $P = I^2R$. In this case, the voltage across the resistor naturally has the same shape as the current. In other cases, however, the RMS values calculated this way are "invalid".
6. Existing theories on the RMS value already require constant refinement to patch inconsistencies when the current is non-sinusoidal, and they completely collapse when the voltage is also non-sinusoidal.

Question 2: What exactly is apparent power?

1. Now that the RMS current is no longer applicable when the voltage is sinusoidal but the current is non-sinusoidal, why do we still "turn a blind eye" and directly multiply the RMS voltage by the RMS current to calculate apparent power? This is akin to the trick of a bully landlord - taking in more while giving out less.
2. From the standpoint of the "landlord", doing so has physical significance. The landlord stands for the equipment. As long as the voltage reaches a certain level, the equipment's insulation must be designed accordingly, regardless of the magnitude or shape of the current.

3. Likewise, as long as the current reaches a certain level, the wires used in the equipment must be of a corresponding thickness, regardless of the voltage. This also applies to other electronic components, where not only power, but also the voltage and current can individually damage components.
4. The physical significance of apparent power is that it reflects "equipment capacity". From the viewpoint of the landlord and the laborer, the laborer shouldn't just focus on the landlord's gains (active power) without considering the landlord's total investment (apparent power).

Question 3: What is reactive power?

1. It is obviously outdated to consider reactive power as the load feeding energy back to the power supply. The power supply is always the source of energy in the example where it generates a sinusoidal voltage and a square wave current.
2. One definition of reactive power Q is:

$$S = \sqrt{P^2 + Q^2} \tag{39}$$

3. But this definition has no physical significance, because apparent power S has never truly existed, and what Q represents becomes even more ambiguous as to what it actually represents.
4. Since there is no consensus among experts in this field on how to define reactive power Q, we might as well regard P as "the loot of a thief", and Q as "the beating the thief endures".

Power Factor of Rectifier Circuits

We have covered the knowledge of power factor fairly well. As the problem with power factor arose from measuring the power of LED bulbs, we should address this practical problem instead of just discussing theories behind it.

Considering both cost and safety factors, the choice of 220V/50Hz for mains electricity was made. However, in reality, the vast majority of loads we use are DC-powered, except for AC motors. Therefore, most electrical appliances require AC-to-DC rectifier circuits.

1. The rectifier circuit shown previously in **Figure 99** uses an inductor for filtering, and this inductor is specifically called a smoothing reactor.
2. The power factor of a rectifier circuit using a smoothing reactor can be as high as 0.9, whereas in reality, such a high-end circuit is generally not affordable for us.
3. Theoretically, both inductors and capacitors can be used for filtering (to convert fluctuating DC into smooth DC), but inductors are really too expensive. Therefore, those "affordable" rectifier circuits all use capacitor filters, as shown in **Figure 102**.

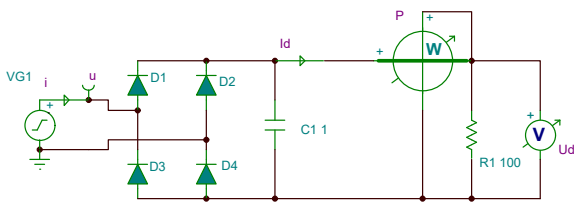


Figure 102. *Capacitor Filter Circuit*

The value of capacitor C1 shown in **Figure 102** is sufficiently large to ensure that the load voltage is essentially constant. However, this makes it difficult for the diode to conduct.

1. The power supply input voltage u has a sinusoidal shape. The diode can only conduct when the input voltage is higher than the voltage across C_1, which occurs only near its peak.
2. When the diode conducts, the power supply provides current. Therefore, the load current waveform, as the simulation shows in 2.11.10, exhibits small spikes.

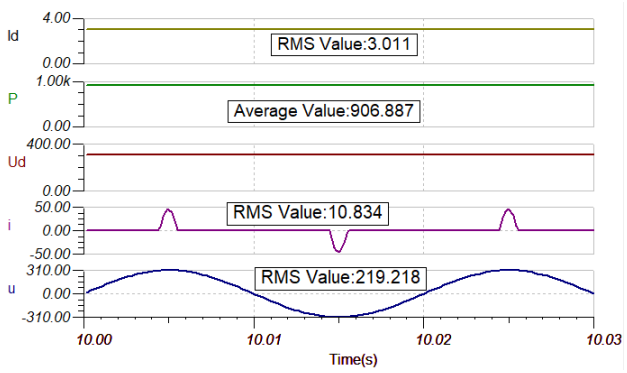


Figure 103. *TINA Simulation of Capacitor Filter Rectifier Circuit*

3. The simulation reveals that the actual load current is only 3.011A, yet the peak current of the power supply already approaches 50A, with an RMS value of 10.834A. This inevitably results in a low power factor.
4. The power factor is calculated as shown in **Equation 40**:

$$\lambda = \frac{P}{S} = \frac{906.887}{219.218 \times 10.834} = 38.2\% \tag{40}$$

5. From the simulation, we can find other issues. The RMS value of the load current is much smaller than that of the power supply current, which implies that power cables should be thicker and the diode must be rated for a higher current. This is why we want the power factor to be as high as possible.

Finally, let's review the LED bulb power measurement process shown in **Figure 94**. If we only measure the RMS value of the current and directly multiply it by 220V, the result is actually the apparent power. This "power" that has never truly existed is unconsciously exercised by people, which highlights the "universal value" of the practice of "taking in more while giving out less".

Summary

Regarding power factor, I initially intended to just briefly touch upon it. Unexpectedly, I ended up writing so much, so it's better to wrap it up with a summary.

RMS value:

1. Given the same average value, the square wave ensures the minimum RMS value, while the steepest waveform ensures the maximum RMS.
2. The RMS value of current and voltage reflects the equivalent power on a pure resistive load.
3. Power can be described in terms of a peak value or an average value, but not in terms of an RMS value.

Apparent power:

1. Apparent power is the product of the RMS value of voltage and the RMS value of current.
2. Apparent power has never truly existed; it is neither average power nor peak power.
3. Apparent power is used to quantify the cost of equipment. Regardless of whether there is current, insulation must be designed to withstand the corresponding voltage level. Regardless of whether voltage is present, wires of appropriate thickness must be chosen to handle the large current.

Active power:

1. Active power is the energy that is truly lost, and it is always calculated by integrating the product of the instantaneous voltage and current.
2. When calculating active power, leave the concept of RMS value behind.

Reactive power:

1. Since apparent power never truly exists, reactive power has not yet been scientifically defined.
2. Just regard it as the difference between apparent power and active power, and note that it is "difference", not "subtraction result".

Transistor Circuit Design

Whenever I see students using various high-performance op amps with almost no understanding of bipolar junction transistors, I can't help but exclaim: "Why give up on fundamental studies?" Pursuing quick results and immediate gains can be a very effective studying method for digital circuits and microcontroller units. However, studying analog circuits requires cultivating both internal expertise and external skills, and transistor circuit design reflects the "internal expertise".

This chapter will cover the following topics:

1. Diode circuits.
2. Basic characteristics of bipolar junction transistors.
3. Bipolar junction transistor constant current source circuits.
4. Common-emitter amplifier circuit.
5. Differential amplifier circuit.
6. Common-collector amplifier circuit.
7. Common-base amplifier circuits.
8. Other amplifier circuits.

Diode Circuits

Diodes are the simplest bipolar semiconductor components. Initially, we only learned about their unidirectional conductivity, but diodes have a wide range of uses in reality. To effectively use diodes, there is a considerable amount of knowledge to learn.

General Characteristics of Diodes

Diodes are nonlinear components. When analyzing the role of a diode in a circuit, it is important to determine whether it is conducting or not! As shown in **Figure 104**:

1. When a voltage above 0.7V is applied between the anode and the cathode, the diode will conduct; otherwise, it will not.
2. If the diode does not conduct, the circuit is open, and the diode can be directly removed from the circuit for analysis.
3. If the diode conducts, it's simply equivalent to a 0.7V battery.

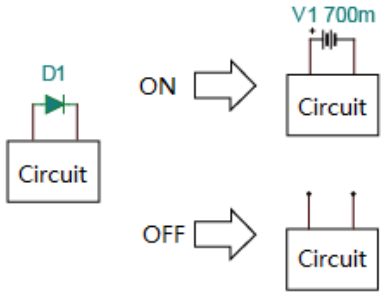


Figure 104. *Diode Equivalents in Circuits*

Volt-Ampere Characteristics of Diodes

Understanding that a conducting diode is equivalent to a 0.7V battery helps solve most problems, but it is also necessary to know what the actual volt-ampere characteristic curves of diodes look like. As shown in **Figure 105**:

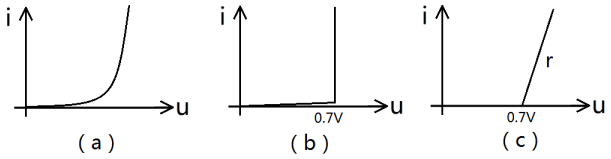


Figure 105. *Volt-Ampere Characteristic Curves of Diodes*

1. (a) shows the actual volt-ampere characteristic curve of diodes. The diode may actually start conducting at the voltage of 0.5V, and the voltage across it increases with the current, although the change is slow.
2. In most cases, we approximate it to the curve shown in (b), assuming that the diode conducts at a voltage above 0.7V (0.6V might also be a standard in some textbooks, which doesn't affect your study). The voltage across the diode no longer changes regardless of the current. While it does not actively generate energy, the diode essentially behaves like a battery in this case if we focus on the outcome rather than the process.

3. Sometimes, we might also approximate the curve of diodes as shown in (c). Since the voltage does increase with the current, we introduce the concept of a diode's equivalent resistance r. This approximation will be helpful when we discuss the bipolar junction transistor amplifier circuit later.

Dynamic Characteristics of Diodes

At low frequencies, diodes can be considered similar to batteries. When a high-frequency signal is applied to a diode, however, it is necessary to consider its dynamic characteristics.

The unidirectional conductivity of diodes is not ideal because a diode is fundamentally a PN junction created through the contact between P-type and N-type semiconductors (Let's stop here and not search online about holes and carriers).

1. As shown in **Figure 106**, a PN junction creates a junction capacitor in addition to forming a unidirectional conductive diode.

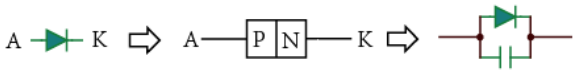


Figure 106. *Junction Capacitance of Diode*

2. The junction capacitor is not beneficial for a diode, as it actually allows a certain amount of reverse charge to flow through the diode.
3. Different manufacturing processes and structures can result in varying junction capacitances. Point contact in PN junctions can reduce the junction capacitance, but this obviously compromises the current-carrying capability of the diode. Conversely, the surface contact in PN junctions allows for stronger current-carrying capability, but also increases the junction capacitance.

The junction capacitance causes practical diodes to take some time to "recover" their reverse blocking capability, with their reverse recovery characteristic curve as shown in **Figure 107**:

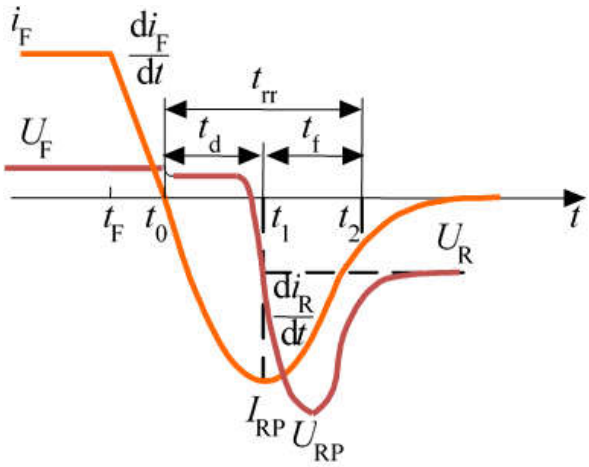


Figure 107. *Reverse Recovery of Diode*

1. Before t_F, the diode is biased forward, with U_F at a typical 0.7V and i_F being quite large.
2. The circuit then attempts to apply a reverse voltage to the diode, but this process is not completed immediately, and the diode current i_F drops to 0 at t_0.

3. During the interval between t_0 and t_1, not only does the diode current not disappear, but it becomes a constantly increasing reverse current. This interval is called t_d (delay), indicating the delay time (out of control).
4. The reverse current reaches its maximum at t_1 and gradually decreases to 0 during the t_1–t_2 interval. This interval is called the fall time, t_f (fall).
5. T_d and t_f add up to t_{rr} (reverse recovery), or the reverse recovery time. The diode is in a reverse-biased state during this period.
6. It can be inferred that the diode will actually behave as if it were "bidirectional conductive" if the signal period T applied to the diode is comparable in the order of magnitude to the reverse recovery time t_{rr}. Therefore, t_{rr} determines the applicable circuit frequency range for diodes.
7. A simple analysis of diode reverse recovery voltage shows that the reverse current decreases sharply after reaching its peak. In other words, t_f is actually very short, resulting in a spike voltage U_{RP} (reverse peak) across the parasitic inductor in the circuit. This spike voltage is calculated as $L\frac{di}{dt}$. This is very harmful and can break down the diode.
8. The recovery coefficient = t_f/t_d describes the "softness" of diode reverse recovery. A larger recovery coefficient indicates that it is less likely to produce harmful high voltage.

Fast Recovery Epitaxial Diode and Schottky Diode

Based on their reverse recovery time (trr), diodes can be categorized into regular diodes, fast recovery epitaxial diodes (FREDs), and Schottky barrier diodes (SBDs).

1. The t_{rr} of regular diodes can reach milliseconds, making them primarily suitable for rectifying AC power with a 50Hz line frequency. Therefore, they are also referred to as rectifier diodes. The typical 1N400x series consists of rectifier diodes.
2. FREDs have a t_{rr} shorter than 200ns, typically below 50ns, thus being used in higher-frequency circuits. The 1N4148, commonly used in digital circuits, is a typical FRED.
3. SBDs have an even shorter t_{rr}, which can reach the order of magnitude of 10ns. They also offer two distinct advantages: One is the small conduction voltage drop (ensuring low power dissipation), and the other is the significantly soft recovery (less prone to reverse recovery high voltage). These two advantages make them particularly suitable for low-voltage switching power supply circuits, with the 1N5819 being a typical example.

Zener Diode

When forward-biased, a Zener diode is characterized as a regular diode. When reverse-biased, it behaves like a battery with a specific voltage. This is actually similar to being forward-biased, except that the voltage is not a fixed 0.7V.

1. To be equivalent to a battery, the Zener diode must be conducting; otherwise, the circuit is open, and the diode can be removed.
2. A Zener diode regulates its terminal voltage by changing the current flow through it. Can the Zener diode, as shown in **Figure 108**, regulate the voltage to 5V regardless of how the current flowing through it changes?

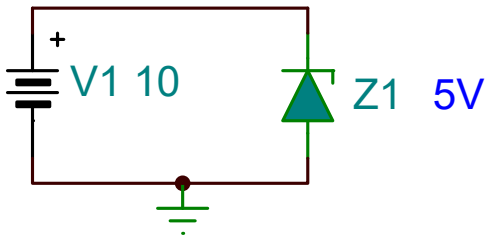


Figure 108. *Incorrect Circuit Connection of Zener Diode*

3. As shown in **Figure 109**, a Zener diode must be connected in series with a resistor to achieve voltage regulation. It regulates the current flowing through itself (which is also the current flowing through R), thereby changing the voltage drop across R to regulate the voltage across itself to 5V.

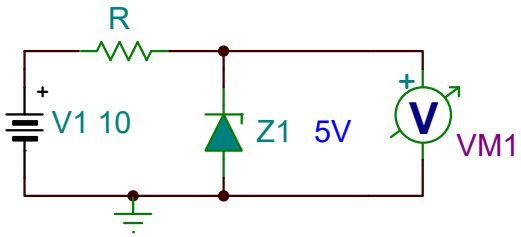
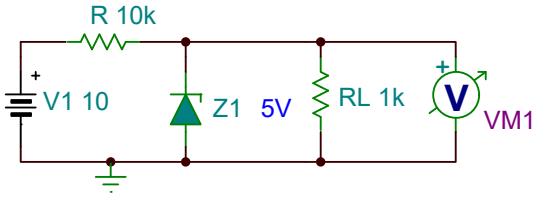


Figure 109. *Correct Use of Zener Diode*

4. The value of the series resistor R for the Zener diode needs to be calculated. Can the desired regulated voltage be obtained across the load in the voltage regulation application shown in **Figure 110**? Obviously not. No matter how the Zener diode changes the current flowing through itself, the terminal voltage cannot reach 5V. The analysis method is simple. The Zener diode is connected in parallel with the load in the circuit, so it can only increase the load (thereby reducing the parallel resistance). In the circuit shown in **Figure 110**, even without the Zener diode, the voltage divided by the load and the series resistor is less than 1V. Therefore, it is impossible to regulate the voltage to 5V under any circumstances.



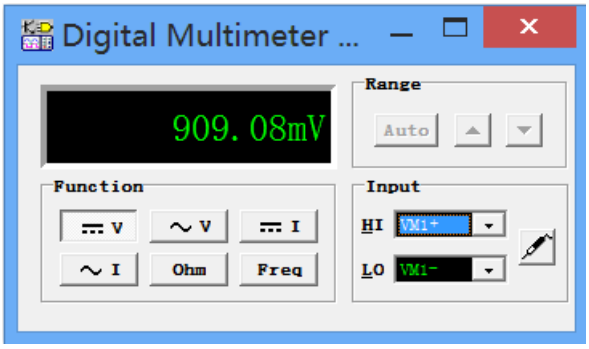


Figure 110. *Example of Incorrect Parameter Calculation for the Zener Diode*

5. In the future, we will find that many components' "claimed" characteristics (e.g., voltage regulation) are conditional. These components always achieve B (e.g., voltage regulation) by adjusting A (e.g., current). If B cannot be achieved no matter how A is adjusted, then the "claimed" characteristic does not hold true.

Light-Emitting Diode

Light-emitting diode (LED) is the diode that emits light of a specific wavelength after turned on.

1. The conduction voltage drop of LEDs is higher than that of regular diodes and is determined by the wavelength of the emitted light (color).
2. The volt-ampere characteristics of LEDs are similar to those of regular diodes. It is the current, not the voltage, that determines the brightness of LEDs (the power is mainly related to the current because the voltage variation is small while the current variation is large).
3. As shown in **Figure 111**, the LED is connected in series with a current-limiting resistor when used for indication.

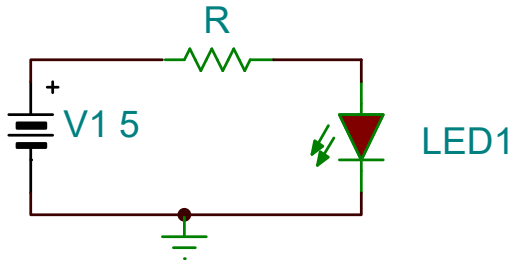


Figure 111. *LED Circuit*

Red, green, and blue (RGB) are the three primary colors of light. The blue LED was the last to be developed (first realized in 1989 and winning the 2014 Nobel Prize in Physics), which enabled the synthesis of white light for LEDs and led to the rapid development of LED lighting.

1. Using a current-limiting resistor to limit the current, as shown in **Figure 111**, will consume additional power, affecting the efficiency of LED lighting.
2. High-quality LED lighting driver power supplies provide constant current sources instead of regular constant voltage sources.

3. A constant voltage source can be transformed into a constant current source by adding current feedback control. Design examples will be provided in the subsequent chapters on power supply management.

Basic Characteristics of Bipolar Junction Transistors

Transistors are divided into bipolar junction transistors (BJTs) and field-effect transistors (FETs). The study of BJT circuits is more universal, while the application of FETs will be introduced later in Chapter 5, "Power Supply Management".

1. Transistors can also be classified into N-type and P-type. More specifically, BJTs include NPN transistors and PNP transistors. We will primarily focus on commonly used NPN transistors, while also interspersing the introduction with knowledge about some circuits involving PNP transistors.
2. As shown in **Figure 112**, the three pins of a BJT are the Base, Emitter, and Collector.

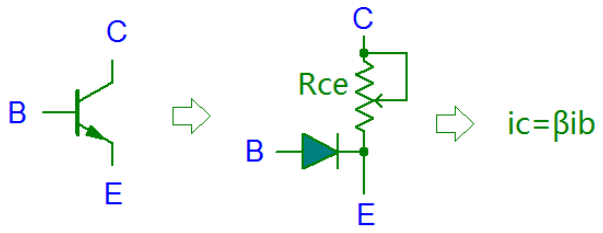


Figure 112. *BJT Equivalent Circuit*

3. The junction between the base and emitter is a diode, while the junction between the collector and emitter is equivalent to an adjustable resistor whose value can range from several ohms to infinity (open circuit).
4. The characteristic equation for a BJT is $i_C = \beta i_B$. For an N-type transistor, the directions of currents i_B and i_C are B→E and C→E, respectively.
5. The so-called β is the amplification factor of the BJT itself, which can be considered a constant dependent on the production process, ranging from tens to hundreds.
6. It should be noted that BJTs can only satisfy the relationship ic = βib by adjusting the equivalent resistance R_{CE} between the collector and emitter.
7. If R_{CE} has been reduced to its minimum value, but the relationship $i_C = \beta i_B$ is still not satisfied, this condition is referred to as "saturation".
8. If R_{CE} has been increased to its maximum value, but the relationship $I_C = \beta i_B$ is still not satisfied, this condition is referred to as "cutoff".
9. If it can satisfy the relationship $i_C = \beta i_B$, the BJT is said to operate in the active region.

Bipolar Junction Transistor Constant Current Source Circuits

The characteristic of a transistor is simply $i_C = \beta i_B$; there is nothing amazing. What is amazing are the various circuits built using transistors. In an era when one transistor cost as much as a month's food expense, countless classic transistor circuits were born. Starting from this section, we will introduce those circuits that are still in use today.

Constant Current Source Discharge Circuit

Connect a resistor to a capacitor (pre-charged) as shown in **Figure 113**. The discharge current will be $i_C = \frac{u_C}{R}$. Since u_C continuously decreases, the discharge current is not constant.

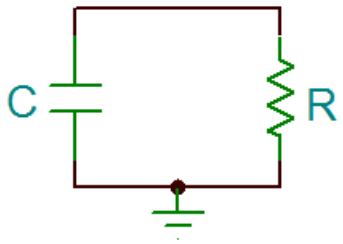


Figure 113. *Capacitor Discharge Circuit*

Figure 114 shows a constant current discharge circuit for a capacitor. We can calculate the IC value to be a constant 1mA, independent of the capacitor voltage. For **Figure 114**, **Equation 41** must hold true, but the approximation in **Equation 42** is valid only when the bipolar junction transistor operates in the active region, i.e., when ic = βib. Since β is generally considered to be on the order of 100, the approximation ie = ic + ib ≈ ic is established.

$$V_E = 5 - 0.7 = 4.3V \tag{41}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{4.3}{4.3} = 1mA \tag{42}$$

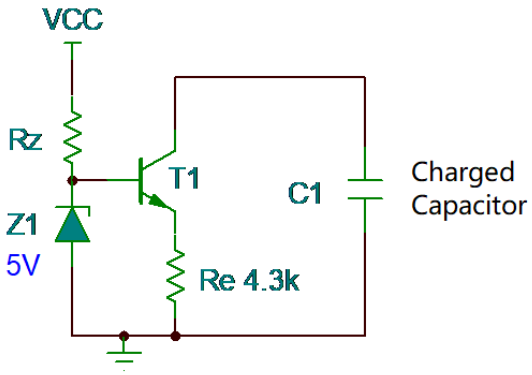


Figure 114. *Constant Current Source Discharge Circuit*

When analyzing a circuit containing a transistor, one can first assume that the transistor is in the active region, satisfying the relationships iC = βiB and iC ≈ iE. Then, based on the calculation results, deduce the value of UCE to determine if the assumption is correct.

According to **Figure 114**, assume the voltage across capacitor C1 is 10V:

1. Thus, it is easy to obtain U_{CE} = 10 – 4.3 = 5.7V, which is consistent. Therefore, the calculation in **Equation 42** is valid.
2. Furthermore, it can be derived that the equivalent $R_{CE} = U_{CE}/1mA$ = 5.7kΩ, indicating that the transistor can maintain the discharge current of the capacitor at 1mA by adjusting R_{CE} to 5.7kΩ.

According to **Figure 114**, assume the voltage across the capacitor drops to 8V:

1. Thus, U_{CE} = 8 – 4.3 = 3.7V, which is also consistent. Therefore, the calculation in **Equation 42** is still valid, and i_C remains constant at 1mA.

2. Furthermore, it can be derived that the equivalent $R_{CE} = U_{CE}/1mA = 3.7k\Omega$, indicating that the transistor can maintain the discharge current of the capacitor at 1mA by adjusting R_{CE} to 3.7kΩ.

According to **Figure 114**, assume the voltage across the capacitor drops to 3V:

1. Thus, $U_{CE} = 3 - 4.3 = -1.3V$, which is obviously inconsistent, indicating that the relationship $i_C = \beta i_B$ could not be satisfied even if R_{CE} decreases to 0.
2. Assuming that U_{CE} could drop to 0, we can calculate the minimum capacitor voltage $U_{CM}I_N = V_E = 4.3V$ to satisfy the constant current conditions.
3. In fact, the resistance between the collector and emitter will never drop to 0 since the collector and emitter are both semiconductors. Generally, the voltage U_{CE} can only drop to about 0.2V, known as the saturation voltage drop U_{CES}.

Here is a summary of what we have learned about transistor constant current source discharge circuits:

1. The circuit shown in **Figure 114** can achieve constant current discharge under a certain condition.
2. The "certain condition" is that the value of the voltage U_{CE} (or resistor R_{CE}) does not violate "common sense".

Constant Current Source Charge Circuit

It is not possible to implement a constant current charge circuit with an NPN transistor. If you don't believe it, try designing one yourself. A PNP transistor is necessary to implement a constant current charge source.

Figure 115 shows the equivalent circuit for PNP transistors:

1. The characteristic equation for a PNP transistor is also $i_C = \beta i_B$. For a P-type transistor, the actual directions of the currents ib and ic are E→B and E→C, respectively.
2. Different books may define the positive directions of i_B and i_C differently. If the same standard as for NPN transistors is followed, the actual i_B and i_C for P-type transistors would both be negative. In this book, we try to define the positive direction according to the actual current flow, avoiding negative values that cause misunderstanding.

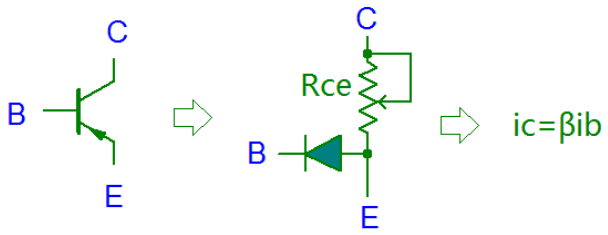


Figure 115. *Equivalent Circuit for PNP Transistor*

As shown in **Figure 116**, a corresponding PNP transistor circuit can be obtained by swapping VCC and GND in the NPN transistor circuit:

1. Do not design PNP circuits directly before you are proficient in transistor circuit design. Instead, focus on NPN circuits. PNP circuits are always transformed from NPN circuits.
2. In addition to swapping V_{CC} and GND, the polarities of directional components in the circuit are also reversed (because the current directions in PNP and NPN circuits are opposite). Therefore, the orientation of Zener diode Z_1 in the circuit shown in **Figure 116** must be reversed, while resistors need no modification.

3. Naturally, the NPN and PNP symbols should be switched, and the actual directions of currents i_C and i_B are opposite.
4. Finally, to conform to the convention of placing V_{CC} at the top and GND at the bottom, the layout can be modified to be as shown in **Figure 116**.

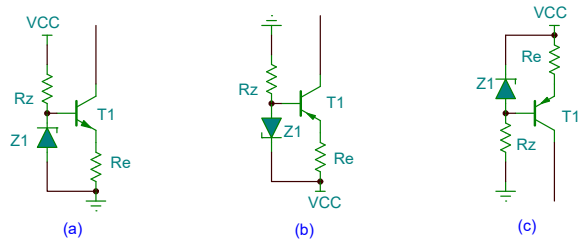


Figure 116. *PNP Transistor Circuit Replacement*

Figure 117 shows a constant current charge circuit. We can calculate the IC value to be a constant 1mA, which is independent of the load resistor's value.

$$U_{Re} = 5 - 0.7 = 4.3V \tag{43}$$

$$I_C \approx I_E = \frac{U_{Re}}{R_E} = \frac{4.3}{4.3} = 1mA \tag{44}$$

1. **Equation 44** also holds true only when the bipolar junction transistor is in the active region.
2. For a constant current source, a heavy load is a high-resistance load, and a light load is a low-resistance load, which is exactly the opposite of a voltage source!

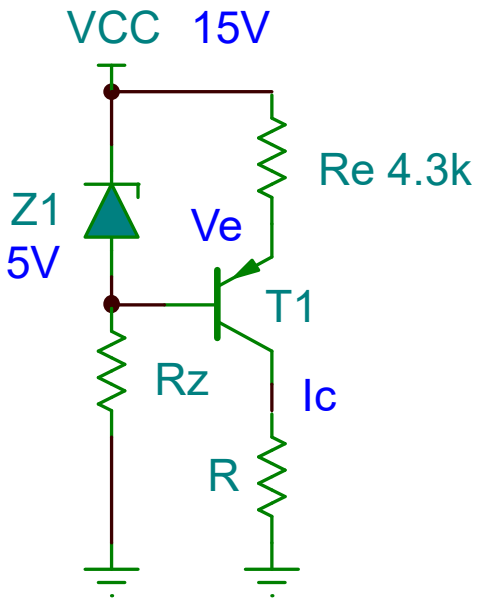


Figure 117. *Instance of Constant Current Source Charge Circuit*

According to **Figure 117**, assume the resistor value is 1kΩ:

1. Given that $V_R = I_C \times R = 1 \times 1 = 1V$, then $V_E = 15V - U_{RE} = 15 - 4.3 = 10.7V$.
2. Thus, $U_{EC} = V_E - V_R = 10.7 - 1 = 9.7V$, which is consistent. Therefore, the transistor can operate in the active region, and the calculation in **Equation 44** is valid.
3. Furthermore, it can be derived that the equivalent $R_{CE} = 9.7V/1mA = 9.7k\Omega$, indicating that the transistor can maintain the resistor current at 1mA by adjusting R_{CE} to 9.7kΩ.

According to **Figure 117**, assume the resistor value is 20kΩ:

1. Given that $V_R = I_C \times R = 1 \times 20 = 20V$, then $V_E = 15V - U_{RE} = 15 - 4.3 = 10.7V$.
2. Thus, $U_{EC} = V_E - V_R = 10.7 - 20 = -9.3V$, which is obviously inconsistent. Therefore, the transistor operates in the saturated region, and the calculation in **Equation 44** is not valid.
3. If we neglect the saturation voltage drop U_{CES} of the transistor, we can further calculate that the actual $I_C = V_E/R = 10.7/20 \approx 0.5mA$.

Summary

The methods for analyzing bipolar junction transistor circuits are introduced through the design of a constant current source circuit, and a few key points are summarized as follows:

1. Just as the conduction state of a diode fundamentally changes its properties, whether a transistor operates in the active region also leads to entirely different behaviors.
2. We generally assume that the transistor is in the active region to analyze the circuit using the approximation $i_C \approx i_E$, and then verify whether U_{CE} is reasonable.
3. If U_{CE} is reasonable, then the original calculation does not need any modification. Unreasonable U_{CE} indicates that the transistor is saturated, then additional conditions such as $U_{CE} = 0$ or $U_{CE} = 0.2V$ will apply (depending on whether the saturation voltage drop is ignored). The circuit can also be re-analyzed accordingly.
4. When calculating, we generally consider the β value of a transistor to be on the order of 100, but we don't need to be precise about its value. If a circuit design requires a specific β value to work, then this is a failed design. How challenging it would be to find a transistor with the right amplification factor!
5. In practical manufacturing, transistors undergo a screening process for their amplification factor (β). The suffix in their model reflects the general range of their amplification factor. However, a larger β value does not always indicate a higher-grade transistor.
6. Finally, transistors do not "know" their specific role in circuits; they simply strive to satisfy the relationship ic = βib. The overall characteristics exhibited by the circuit (such as a constant current source) are the result of human design and naming.

Common-Emitter Amplifier Circuit

An important task of analog circuits is to amplify analog signals, and the common-emitter amplifier circuit is one of the most crucial analog amplifier circuits.

General Characteristics of Common-Emitter Amplifier Circuit

Let's start with the circuit shown in **Figure 118** to derive the output voltage expression:

$$v_E = u_I - U_{BE} = u_I - 0.7 \tag{45}$$

$$I_C \approx I_E \approx \frac{v_E}{R_E} = \frac{u_I - 0.7}{R_E} \tag{46}$$

$$u_O = V_{CC} - I_C \times R_C = V_{CC} - \frac{R_C(u_I - 0.7)}{R_E} \tag{47}$$

$$\Delta u_O = -\frac{R_C}{R_E} \times \Delta u_I \tag{48}$$

1. **Equation 46** assumes that the bipolar junction transistor operates in the active region. If it is discovered later that the transistor is not in the active region, recalculations are necessary.
2. **Equation 47** represents the input-output voltage relationship obtained from calculations, which is unrelated to the type of this circuit.
3. **Equation 48** examines the relationship between the changes in input and output (via differentiation), where constant terms such as V_{CC} and 0.7 are eliminated. It is clear that there is an inverse proportional relationship between the input and output signals.

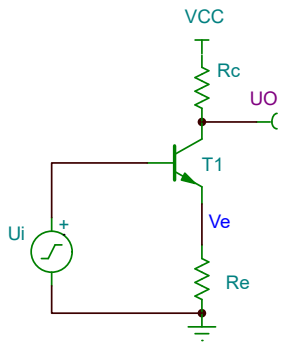


Figure 118. *Transistor Circuit*

Figure 118 shows the well-known common-emitter amplifier circuit. We can specify a set of parameters and perform an actual calculation. Let VCC = 15V; RE = 2kΩ; RC = 10kΩ; and $u_i = 2 + \sin \omega t$. Thus:

$$u_O = VCC - \frac{R_C(u_i - 0.7)}{R_E} = 8.5 - 5\sin \omega t \tag{49}$$

The hand-drawn waveforms are shown in **Figure 119**, and the TINA simulated circuit and waveforms are shown in **Figure 120**.

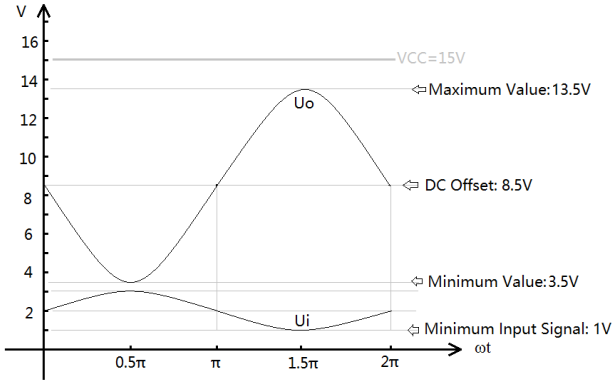


Figure 119. *Hand-drawn Input and Output Waveforms of a Common-Emitter Amplifier Circuit*

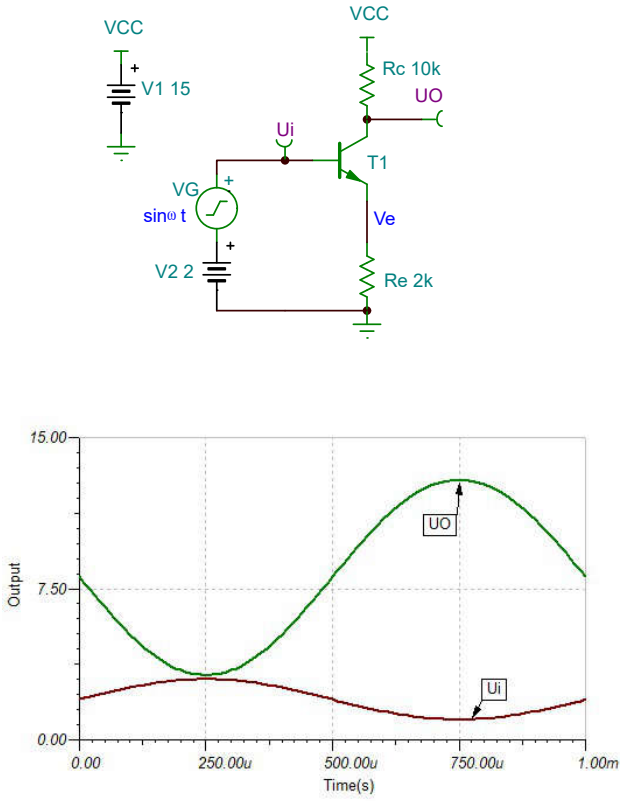


Figure 120. *TINA Simulation of Common-Emitter Amplifier Circuit*

1. Waveform analysis is a very "reliable" method in circuit analysis. It is great to plot the voltage waveforms of various nodes in the circuit and the current waveforms of each loop.
2. As shown in **Figure 119**, the horizontal and vertical axes should be plotted first. Then mark two horizontal lines for 8.5V and 15V.
3. According to **Equation 49**, the maximum uo value is 13.5V, and the minimum value is 3.5V. Then, these two horizontal lines should be marked.
4. According to **Equation 49**, when $\omega t = 0.5\pi$, u_O takes the minimum value of 3.5V; when $\omega t = 1.5\pi$, u_O takes the maximum value of 13.5V. Plot the waveform of u_O. Similarly, plot the waveform of u_I.

An analysis of **Figure 119** can reveal a lot of useful details:

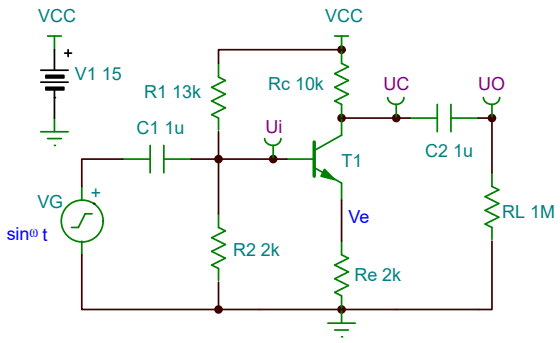
1. The amplification factor is –5, making this really an "amplifier circuit".
2. The maximum and minimum values of u_O are within the supply voltage range of 0-15V, which means that the transistor is neither saturated nor cut off but always operates in the active region throughout the entire ui input signal range.
3. The minimum value of the input signal ui is 1V, which is sufficient to ensure that the base-emitter junction conducts, i.e., ib is always present. Otherwise, the transistor would also be cut off (without ib, there would be no ic).

DC Offset of Amplifier Circuits

In many cases, the input signal vI is a pure AC signal, and the output signal vO is also required to be a pure AC signal. How to provide the 2V DC offset voltage for the input signal uI, and how to eliminate the 8.5V DC offset voltage shown in **Equation 49**? According to **Figure 121**:

1. For the input part, a 2V DC power supply is generally not used due to its high cost. Resistor dividers are usually used to provide a 2V DC bias.
2. In amplifier circuits, electrolytic capacitors are always considered as batteries, and all we have to do is calculate the equivalent battery voltage of the capacitor.
3. If it is a pure AC signal, u_I will charge and discharge capacitor C_1 equally each cycle, which does not affect the final equivalent battery voltage of C_1.
4. The voltage divided by R_1 and R_2 will charge capacitor C_1, thereby raising u_I to the required voltage before it enters the base.
5. For the output part, the electrolytic capacitor C_2 also acts as a battery. The 8.5V offset voltage of u_O in **Equation 49** will charge capacitor C_2, making it an 8.5V battery with its left terminal positive and right terminal negative. Therefore, u_O after passing through C_2 must be a pure AC signal.
6. The function of capacitor C_2 is DC blocking, which can also be explained from the perspective of high-pass filtering. The pure DC voltage component in u_O is certainly not able to pass through the high-pass filter composed of C_2.

Simulating the circuit shown in **Figure 121** using TINA yields the voltage waveforms of each node of the circuit. You can verify whether you are able to sketch these waveforms by hand.



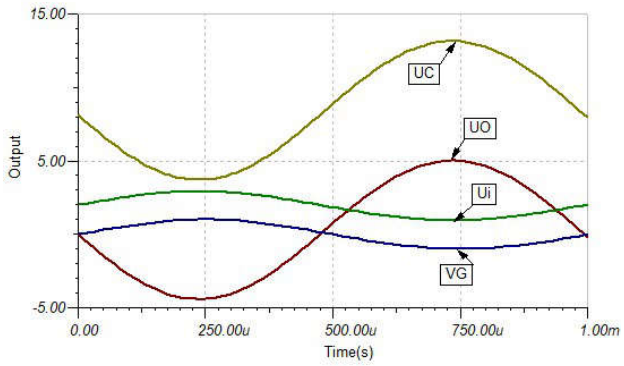


Figure 121. *Simulation of a Common-Emitter Amplifier Circuit with DC Bias*

Saturation in Common-Emitter Amplifier Circuits

The parameters in the example shown in **Figure 121** are carefully designed to ensure that the bipolar junction transistor always operates in the active region (i.e., always satisfying the relationship ic = βib). In this section, we will design some other examples where the transistor does not always operate in the active region.

Let's return to the hand-drawn waveforms shown in **Figure 119**. What would happen if the minimum value of uO falls below 0V? How can the given parameters be adjusted to produce such a phenomenon for observation?

1. Let the input signal

$$u_i = 3 + \sin \omega t \tag{50}$$

, thus:

$$u_O = VCC - \frac{R_C(u_i - 0.7)}{R_E} = 3.5 - 5\sin \omega t \tag{51}$$

2. Based on **Equation 51**, it is clear that the maximum uo value is 8.5V, while the minimum value is –1.5V. However, even in an ideal situation (U_{CES} and U_{RE} neglected), the output voltage u_O can only have the waveform as shown in **Figure 122** and absolutely cannot reach a negative value.
3. The so-called "saturation" distortion is the phenomenon where the transistor's R_{CE} has been decreased to its minimum, yet it still cannot achieve the desired minimum u_O value of –1.5V in **Equation 51**, causing the signal to appear to be "trough clipped".

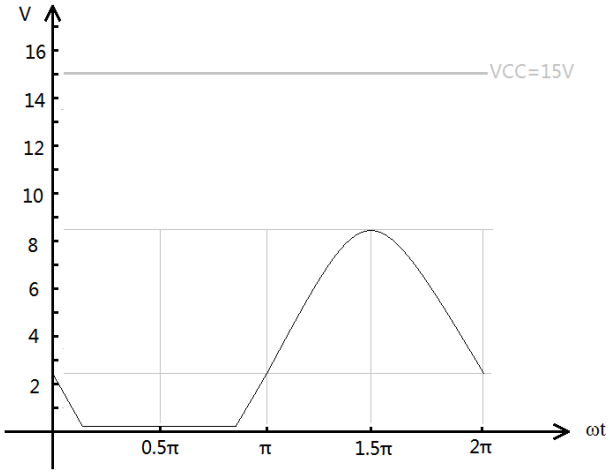


Figure 122. *Saturation Distortion in the Transistor Amplifier Circuit*

The above analysis can be further corrected using TINA simulation. The TINA simulated waveforms are shown in **Figure 123**:

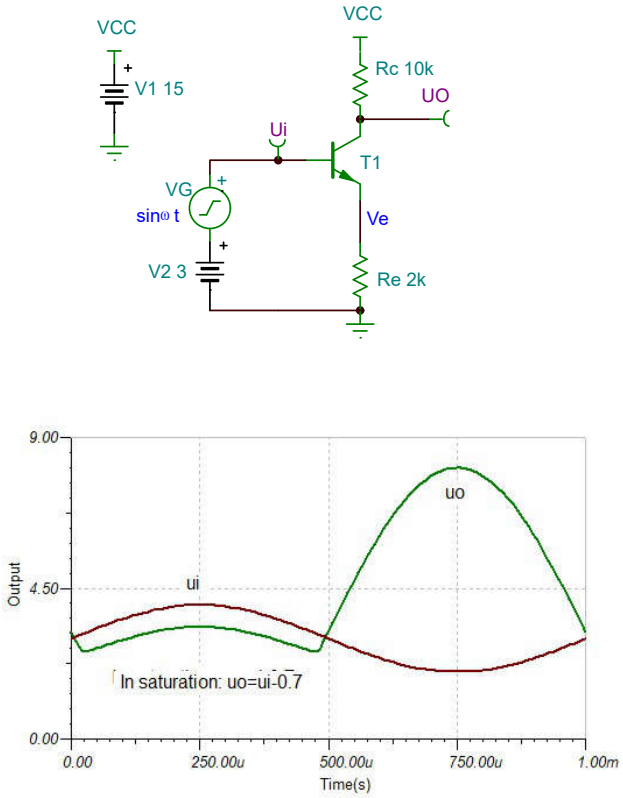


Figure 123. *TINA Simulation of Saturation Distortion in the Common-Emitter Amplifier Circuit*

1. Because of the divided voltage U_{RE} across R_E, the output voltage u_O is also clamped by U_{RE} In other words, the output voltage cannot fall below U_{RE} Thus, the voltage U_{RE} typically appears as u_I–0.7V.

2. When the transistor is saturated (U_{CES} is approximately 0 in the TINA simulation), the voltage U_C (or u_O) is approximately equal to the voltage V_E, leading to the similar shapes of u_O and u_I in **Figure 123** (differing by U_{BE} of 0.7V).

Cutoff in Common-Emitter Amplifier Circuit

What corresponds to saturation distortion is cutoff distortion. What would happen if the maximum value of the output signal uO in **Equation 51** exceeds VCC? How can the given parameters be adjusted to produce such a phenomenon for observation?

1. Let the input signal u_I be

$$u_i = 1 + \sin \omega t \tag{52}$$

, then the output signal u_O is:

$$u_O = VCC - \frac{R_C(u_i - 0.7)}{R_E} = 13.5 - 5\sin \omega t \tag{53}$$

2. Based on **Equation 53**, it is clear that the maximum u_O value is 18.5V, while the minimum value is 8.5V. However, even in an ideal situation, the output voltage u_O can only have a waveform as shown in **Equation 53** and cannot exceed the supply voltage V_{CC}.

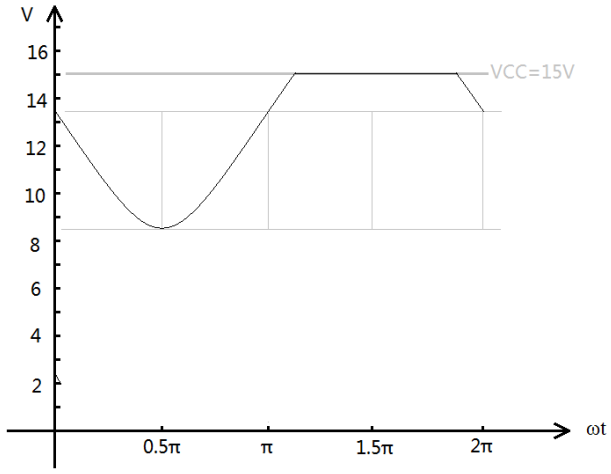


Figure 124. *Saturation Distortion in the Transistor Amplifier Circuit*

The TINA simulated waveforms are shown in **Figure 125**:

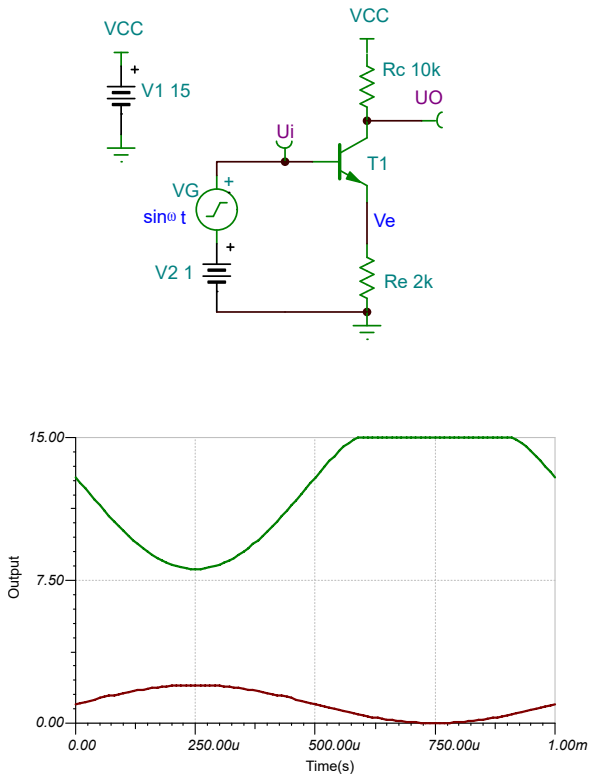


Figure 125. *TINA Simulation of Cutoff Distortion of the Common-Emitter Amplifier Circuit*

1. It is different from saturation distortion. The maximum output of u_O can reach the V_{CC} power rail.
2. The so-called "cutoff" distortion is the phenomenon where the signal appears to be "trough clipped" because the transistor's R_{CE} has reached its maximum value (causing an open circuit) and it still cannot achieve the desired maximum uo value of 18.5V in **Equation 53**.

AC Equipotential of Voltage Sources

In practical circuits, the impedance and potential vary for signals of different frequencies. In the voltage source circuit shown in **Figure 126**, the DC potentials at points A and B are obviously different, with a difference of one VCC. However, the AC potentials at points A and B are equal.

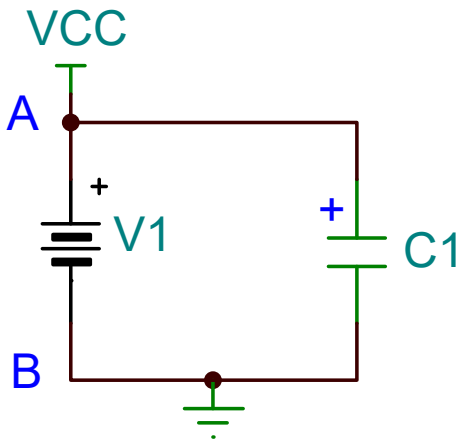


Figure 126. *Potential of DC Power Supply*

1. For a DC power supply, $\Delta V_A = \Delta V_B$ can be easily derived from $V_A = V_B + V_{CC}$, which is the concept of AC equipotential.
2. From the perspective of impedance, the impedance of a capacitor is given by

$$1/j\omega C \tag{54}$$

   Both ends of the voltage source should be connected in parallel with "huge-capacitance" capacitors. Therefore, the AC impedance across the voltage source is 0, and it can further be considered as being AC equipotential across the voltage source.
3. Based on the above analysis, batteries, high-capacitance capacitors, on-state diodes, on-state Zener diodes, and the base-emitter junction of on-state bipolar junction transistors in a circuit can, in most cases, be regarded as offering zero AC impedance and being AC equipotential at both ends.

Input and Output Impedances of Common-Emitter Amplifier Circuit

It is essential to analyze the input and output impedances of circuits, as they partly reveal the circuits' performance. The input and output impedances of amplifier circuits apply to AC signals unless specifically stated. A circuit has excellent performance when it has a high input impedance and a low output impedance to typical voltage signals.

Figure 121 The equivalent circuit for the input impedance of the common-emitter amplifier circuit can be represented by the circuit as shown in **Figure 127**:

1. V_{CC} is not present in the AC equivalent circuit, and R_1 and R_2 are equivalent to being connected in parallel and then grounded.
2. Another branch can only provide impedance equivalent to R_E', which is determined based on **Figure 127**.
3. According to **Figure 127**, the equivalent impedance R_E' can be derived as:

$$\begin{cases} i_b \approx \frac{i_e}{\beta} = \frac{v_e}{\beta R_e} \\ v_i = v_e \quad \Rightarrow R_E{}' = \beta R_e \\ R_E{}' = \frac{v_i}{i_b} \end{cases} \tag{55}$$

4. Considering all three branches, the total input impedance is given by **Equation 56**.

$$r_i = R_1 // R_2 // \beta R_E \tag{56}$$

Equation 56 indicates that, apart from resistors R_1 and R_2 required for DC bias, R_E is amplified by a factor of β before being applied to the input, making the input impedance of the common-emitter amplifier circuit relatively large. This is an advantage.

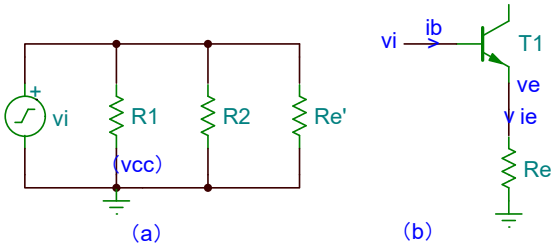


Figure 127. *Diagram for Common-Emitter Amplifier Circuit Impedance*

It is easy to calculate the output impedance of a common-emitter amplifier circuit, as shown in **Figure 128**:

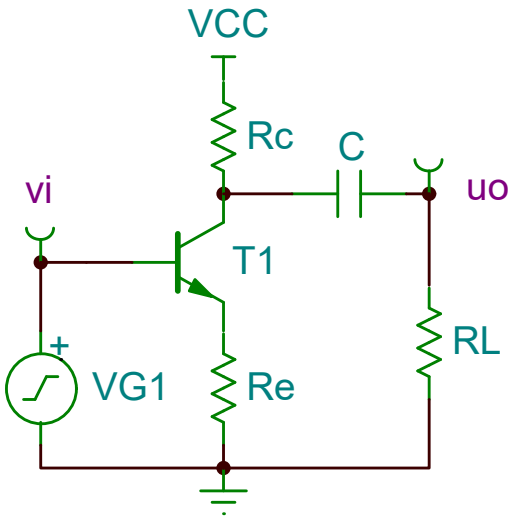


Figure 128. *Circuit for Calculating the Output Impedance of the Common-Emitter Amplifier Circuit*

1. When no load is applied, the amplification factor of the circuit is

$$A_V = -\frac{R_C}{R_E} \tag{57}$$

.

2. When R_L is connected (assuming $R_L = R_C$), R_L and R_C are in parallel because the electrolytic capacitor is shorted to AC. Thus, the amplification factor of the circuit becomes

$$A_V = -\frac{R_C//R_L}{R_E} = -\frac{1}{2}\cdot\frac{R_C}{R_E} \tag{58}$$

, or half of that at no load. According to the definition of output impedance, its value is equal to R_C.

3. Due to factors such as power dissipation, R_C is typically at least on the order of 1kΩ, so the output impedance characteristics of common-emitter amplifier circuits are less ideal (unable to drive heavy loads with low resistance).

Miller Effect of Common-Emitter Amplifier Circuit

As shown in **Figure 129**, the bipolar junction transistor has junction capacitors CBC and CBE, which, along with the base resistor r, form low-pass filters.

1. The low-pass filter formed by capacitor C_{BE} is unavoidable and not too detrimental.
2. However, the low-pass filter formed by C_{BC} multiplies the low-pass effect due to the common-emitter amplifier circuit connection.
3. The AC potential at the other terminal of C_{BC} is actually $-Av_I$. Therefore, the voltage applied across C_{BC} is $(1 + A)v_I$, making the effective capacitance of C_{BC} to be considered as $(1 + A)C_{BC}$. This is the Miller effect. ($A = |v_O/v_I|$)
4. The Miller effect causes common-emitter amplifier circuits to have the narrowest bandwidth and the poorest frequency characteristics (unable to amplify high-frequency signals).

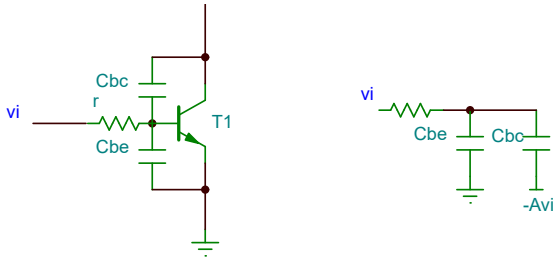


Figure 129. *Miller Effect*

Design of Common-Emitter Amplifier Circuit

It's easy to get a basic understanding of how a common-emitter amplifier works; all it takes is a few lines of mathematical derivation from the chapter on common-emitter amplifiers. But it's not easy to design an effective common-emitter amplifier circuit. We have discussed the "details" for common-emitter amplifier circuits in several subsections. With these fundamentals, we can begin to truly design a circuit.

Taking the circuit shown in **Figure 130** as an example, let's illustrate the ideas and steps for designing a 5x amplifier circuit for a 2VPP, 1kHz sinusoidal signal with a 100kΩ load:

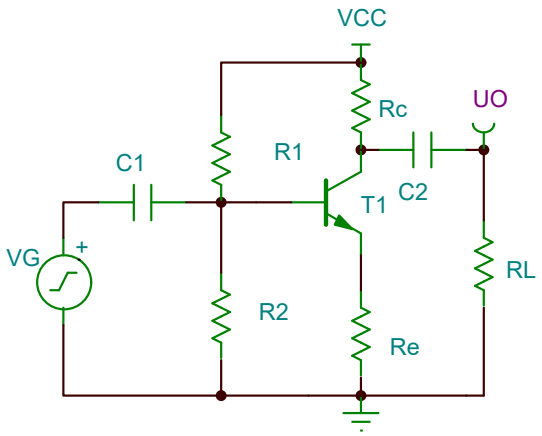


Figure 130. *Common-Emitter RC Coupled Amplifier Circuit*

First of all, the supply voltage VCC should be selected.

1. In a circuit, a higher supply voltage leads to higher power dissipation. Where possible, the supply voltage is continuously decreased to achieve lower power dissipation.
2. In an amplifier circuit, the minimum supply voltage depends on the amplitude of the signal. For example, to amplify a $2V_{PP}$ signal by 5 times, the minimum V_{CC} needs to be greater than 10.5V (0.5V accounts for U_{CES} and U_{RE}).
3. The larger the supply voltage margin, the less the design stress, so we select a common voltage of 15V here.

The next step is to determine the values for RC and RE.

1. The output impedance R_C of the common-emitter amplifier circuit should be set based on the load resistance. The smaller the R_C value is, the lower the output impedance will be, resulting in a more stable amplification factor when a load is applied.
2. However, a smaller R_C value will lead to higher quiescent power dissipation of the amplifier circuit, which is the power "wasted" when no load is applied.
3. Considering the load conditions comprehensively, the R_C value is set to 10kΩ, which is one-tenth of the load resistance, meeting the circuit standard of being much smaller. Therefore, applying a load will not significantly affect the amplifier circuit.
4. Next, set the R_E value based on the amplification factor. When the R_C value is 10kΩ, the R_E value should be 2kΩ.

Then, design the magnitude of the bias voltage for the input signal.

1. The common-emitter amplifier circuit is an inverting amplifier. Therefore, a higher DC offset in the input signal shifts the output signal downwards, while a lower DC offset in the input signal shifts the output signal upwards.
2. The output signal can be centered directly on the supply rail unless otherwise specified (this allows for the maximum undistorted gain), as shown in **Figure 131**.
3. Since V_C = 7.5V when v_I = 0V (the so-called quiescent state), the DC offset V_B in the input signal can be deduced.

$$i_E \approx i_C = \frac{VCC - V_C}{R_C} = \frac{15 - 7.5}{10} = 0.75mA \quad (59)$$

$$V_B = 0.7 + V_E = 0.7 + i_E R_E = 0.7 + 0.75 \times 2 = 2.2V \quad (60)$$

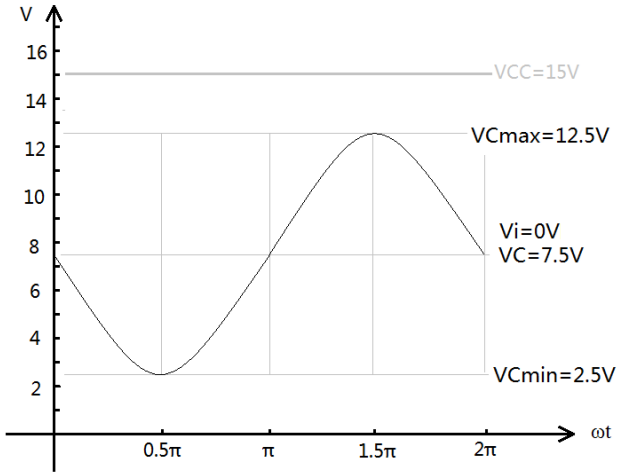


Figure 131. *DC Offset of Output Signal*

Then set resistor dividers R1 and R2 according to the bias voltage.

1. To obtain 2.2V from 15V, there are infinite combinations for the resistor dividers. Naturally, larger resistance leads to lower "wasted" power. As indicated in **Equation 60**, this also results in higher input impedance.
2. As shown in **Figure 132**, R_2 value must be small enough to neglect the current from another branch in the resistor divider network.
3. Assuming a β value of 100, the R_E' value should be 200kΩ, and the R_2 value can be chosen as 20kΩ, which is "much smaller" than the R_E' value.
4. Given that R_2 = 20kΩ, R_1 is calculated as 116kΩ. A 116kΩ resistor is not available in the E24 series, so the closest value for R_1 is 120kΩ. This causes a small DC error, but it has no impact due to the large V_{CC} margin.
5. In addition, when only accurate resistance is required, two low-accuracy resistors can be connected in series to achieve a high-accuracy resistor, for example, 100kΩ + 16kΩ = 116kΩ.

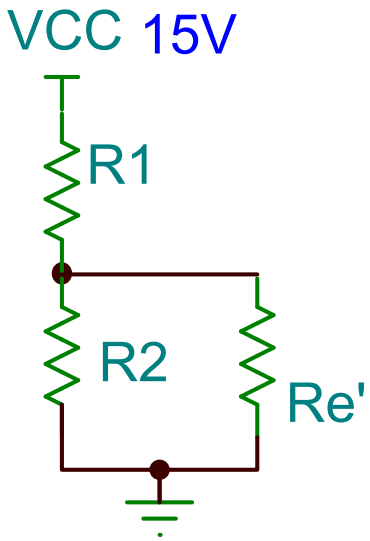


Figure 132. *Diagram for Resistor Dividers*

Finally, select electrolytic capacitors C1 and C2.

1. As mentioned earlier, electrolytic capacitors in analog circuits can all be considered as "batteries".
2. To achieve this effect, they must have an impedance close to 0 for signals. In other words, the required capacitance of an electrolytic capacitor is related to the signal frequency.
3. As shown in **Figure 133**, from the perspective of filters, capacitors C_1 and C_2 form two high-pass filters. They can be considered to present 0 impedance to a signal as long as their cutoff frequencies are below 1/10 of the signal frequency, with the calculation process shown in **Equation 61**-**Equation 64**.

$$\because f_{L1} = \frac{1}{2\pi R_i C_1} < 100\text{Hz} \tag{61}$$

$$\therefore C_1 > \frac{1}{200\pi R_i} = \frac{1}{628 \times (20\text{k}//120\text{k}//200\text{k})} = 102\text{nF} \tag{62}$$

$$\because f_{L2} = \frac{1}{2\pi R_L C_2} < 100\text{Hz} \tag{63}$$

$$\therefore C_2 > \frac{1}{200\pi R_L} = \frac{1}{628 \times 100\text{k}} = 15.9\text{nF} \tag{64}$$

4. **Equation 62** and **Equation 64** indicate that a small capacitance is sufficient to achieve the goal. From an economic point of view, 0.1μF ceramic capacitors and 10μF electrolytic capacitors are already very affordable. Here we select 10μF electrolytic capacitors.

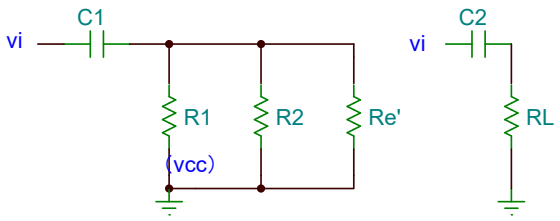


Figure 133. *High-Pass Filters in Common-Emitter Amplifier Circuit*

Finally, we arrive at the design shown in **Figure 134**. **Figure 135** shows the TINA simulated waveforms.

1. Since all resistors used in the circuit have resistance above 1kΩ, there is generally no issue with component power dissipation. If resistors of a very small resistance are used in the circuit, it is necessary to verify whether the power dissipation of each component is reasonable.
2. Finally, the criterion to verify that you have truly mastered the knowledge in this section is that you are able to sketch by hand the voltage waveforms of all nodes in the circuit.

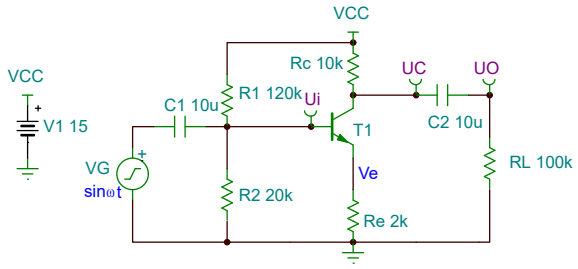


Figure 134. *Completed Common-Emitter Amplifier Circuit Design*

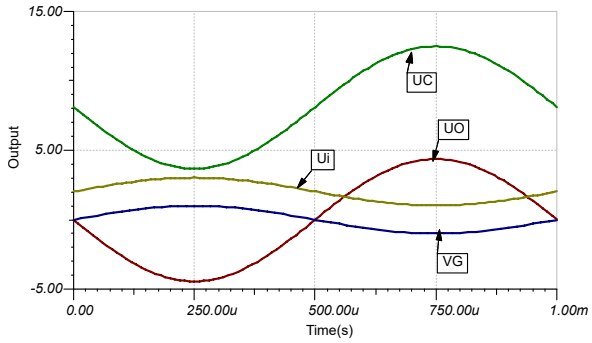


Figure 135. *TINA Simulated Waveforms*

Expanded Circuits for Common-Emitter Amplifier Circuit

This section will introduce some expanded designs for common-emitter amplifier circuits to broaden your thinking and horizons.

Using a capacitor to bypass resistor R_E in common-emitter amplifier circuits

When we want to increase the amplification factor without modifying the DC bias circuit, we can achieve this by partially bypassing resistor RE with a capacitor, as shown in **Figure 136**:

1. In the analysis of a DC bias circuit, capacitor C_3 regulates the voltage across resistor R_{E2} without altering it.
2. In the analysis of an AC path, the AC impedance of C_3 is 0, thus short-circuiting R_{E2}. Therefore, the amplification factor of the common-emitter amplifier circuit is as follows:

$$A = \frac{u_O}{u_I} = -\frac{R_C}{R_{E1}} \tag{65}$$

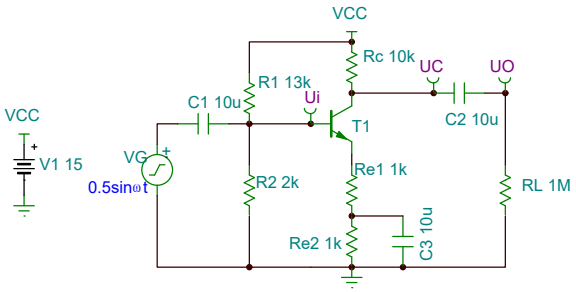


Figure 136. *Adjusting the AC Amplification Factor to 10*

3. In the TINA simulation of the circuit, as shown in **Figure 137**, the output amplitude of the signal generator V_G has been changed to 0.5V to prevent saturation, resulting in a 10x amplifier circuit. The "average" of each signal remains unchanged (the DC bias is not altered).

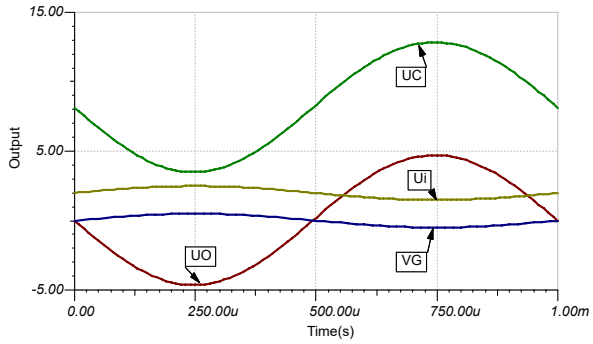


Figure 137. *TINA Simulation of the 10x Amplifier Circuit*

As shown in **Figure 138**, we can achieve the maximum amplification factor by completely bypassing RE. Will ΔvB cause ΔiE to be infinite when RE is bypassed by capacitor C3? To analyze this question, it is necessary to discuss the diode equivalent circuit again.

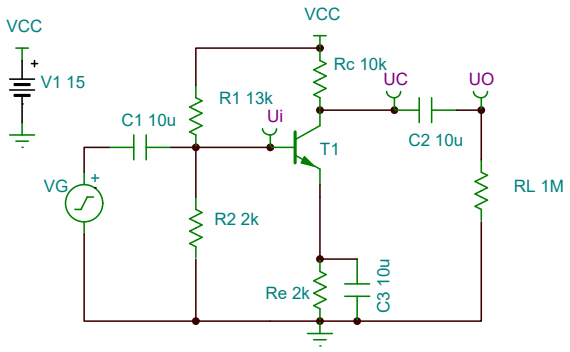


Figure 138. *Maximum Amplification Factor Achieved*

1. **Figure 139** shows several approximations of the diodes' volt-ampere characteristic curve. The base-emitter junction of a bipolar junction transistor behaves as a diode.

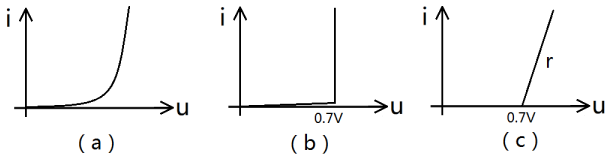


Figure 139. *Volt-Ampere Characteristic Curves of Diodes*

2. When considering the effect of RE, we always use approximation (b), assuming that U_{BE} remains constant at 0.7V. This approximation works in most cases. However, when R_E is bypassed, this approximation will lead to the incorrect conclusion that Δu_B causes an infinite Δi_E.
3. As (a) shows, with changes in voltage across a practical diode, the current i will not be infinite. Approximation (c) implies the existence of an equivalent base resistor r_{be}, whose value is not constant, but rather the tangent slope at each point in (a).

   With the introduction of rbe, the transistor should be equivalent to the model shown in **Figure 140**, with a base resistor rbe added between the base and emitter. This resistor is connected in series with the 0.7V battery to form the PN junction between the base and emitter.

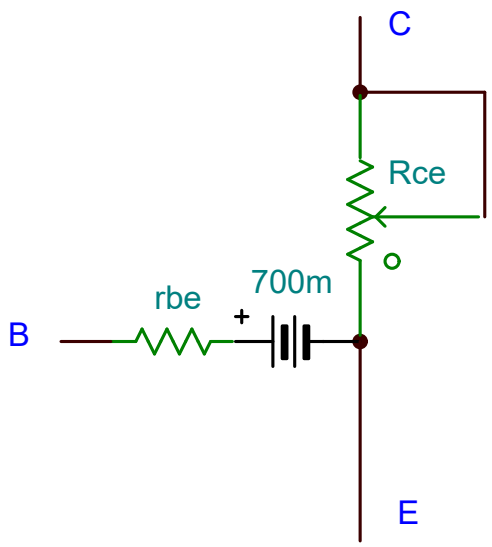


Figure 140. *Transistor Equivalent Model with Base Resistor*

1. Based on the new equivalent model shown in **Figure 140**, the amplification factor of the circuit shown in **Figure 138** can be calculated. Using r_{be}, Δi_B can be determined:

$$\Delta i_B = \frac{\Delta u_{BE}}{r_{be}} = \frac{\Delta u_I}{r_{be}} \tag{66}$$

$$\Delta i_E \approx \Delta i_C = \beta \Delta i_B \tag{67}$$

$$A = \frac{\Delta u_O}{\Delta u_I} = \frac{-R_C \Delta i_E}{\Delta u_I} = \frac{-R_C \beta \Delta i_B}{\Delta u_I} = \frac{-R_C \beta \frac{\Delta u_I}{r_{be}}}{\Delta u_I} = -\frac{\beta R_C}{r_{be}} = -\frac{R_C}{\frac{r_{be}}{\beta}} \tag{68}$$

2. As **Equation 68** shows, the r_{be} resistance is equivalent to being scaled down by a factor of β and "transformed" to the position of R_E. The value of r_{be} is on the order of magnitude of kilo-ohms, and it makes no sense to discuss its exact value of r_{be}. Just keep in mind that the amplification factor of the circuit shown in **Figure 138** is very large - just consider it as β.

1. Note: Theoretically, the r_{be} resistance should be equivalent to being scaled down by a factor of $(1 + \beta)$ and "transformed" to the position of R_E (whether performing an approximation to **Equation 67** or not). Previous discussions in this book have largely avoided specific β values, instead relying on the characteristic that the β value is very large to complete circuit analysis. This subsection inevitably involves a β value, but fussing over whether it should be $(1 + \beta)$ has no practical engineering significance. For simplicity, it is always approximated as β.

The TINA simulation results are shown in **Figure 141**, with the VG input signal amplitudes being 5mV and 20mV, respectively.

1. The left graph shows an amplification factor of about 200, where the distortion is not very noticeable. The right graph also shows an amplification factor of about 200. Distortion is significant, leading to a "top-heavy" waveform instead of a true sine wave.

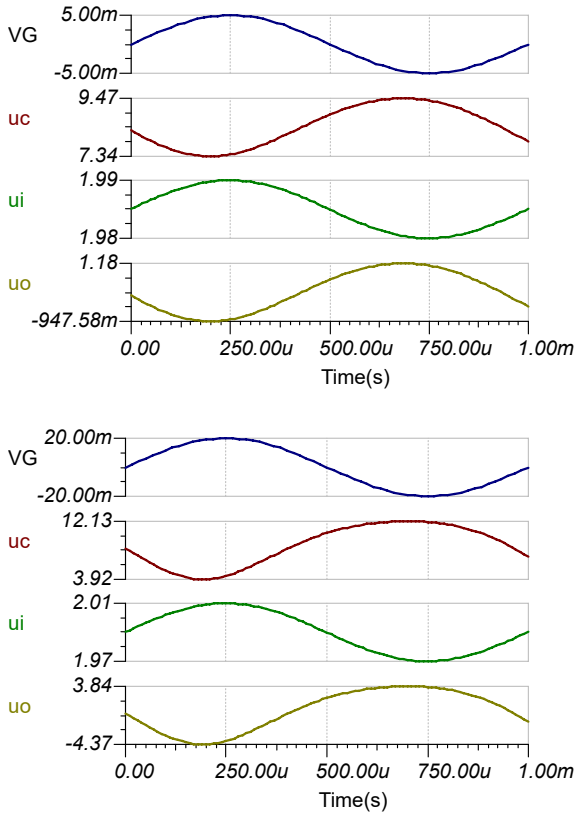


Figure 141. *TINA Simulated Waveforms of the "Extreme" Amplifier Circuit*

1. The reason for the generation of top-heavy waveforms is simple. According to **Figure 139**, the slope of the diode's volt-ampere characteristic curve is not constant, so the r_{be} value is not constant, either. The amplification factor A, calculated from **Equation 68**, also changes with the base (PN junction equivalent diode) current. The larger the base current variation is, the more noticeable the distortion will be. For example, the right graph in **Figure 141** shows more noticeable distortion than the left one.
2. Why is there no "top-heavy distortion" in a common-emitter amplifier circuit that contains (non-bypassed) R_E? If R_E is considered, **Equation 68** should be corrected to **Equation 69**, where the weight of R_E in the denominator is much higher than that of r_{be}/β. Therefore, changes in r_{be} have little effect on the amplified waveforms.

$$A = \frac{\Delta u_O}{\Delta u_I} = -\frac{R_C}{\frac{r_{be}}{\beta} + R_E} \tag{69}$$

Frequency-selective amplifier circuit

As shown in **Figure 142**, replacing the RC circuit with a parallel LC circuit creates a frequency-selective amplifier circuit that amplifies signals of a specific frequency.

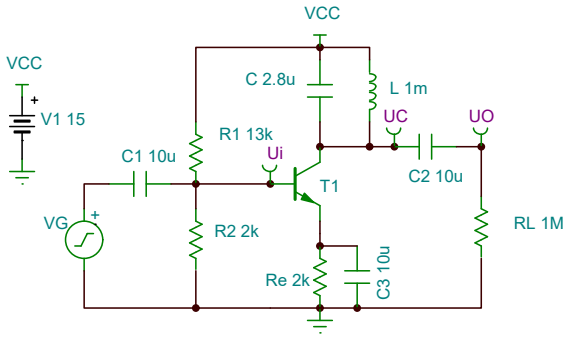


Figure 142. *Frequency-Selective Amplifier Circuit*

1. The impedance of the parallel LC circuit is related to frequency, as shown in **Figure 143**. Low-frequency signals are shorted by L and cannot be amplified as the equivalent R_C impedance is extremely low; high-frequency signals are shorted by C and cannot be amplified, either. Only signals of a specific intermediate frequency, where the impedance is extremely high, can be amplified.
2. Theoretically, the impedance at the natural frequency f_0 is infinite. However, it is actually still finite due to the presence of resistance.
3. The "sharper" the curve in **Figure 142** is, the higher the Q factor of the LC circuit is, and the better the frequency-selective amplifier performs.

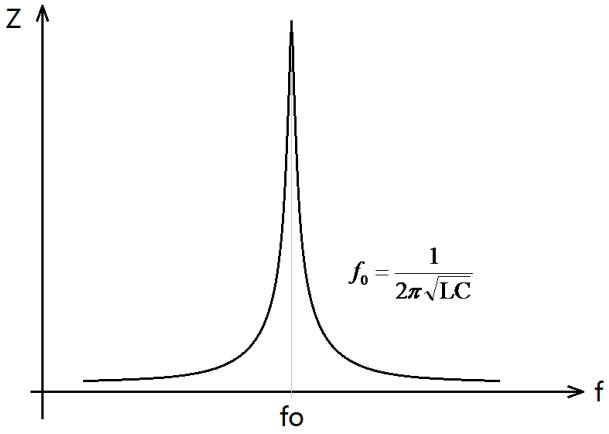


Figure 143. *Impedance Characteristic Curve of the Parallel LC Circuit*

4. TINA is available to simulate the frequency-impedance characteristics of the LC tank circuit. As shown in **Figure 144**, by dividing the voltage across the LC tank circuit and resistor R_3, and clicking "Analysis" > "AC Analysis" > "AC Transfer Characteristics" in TINA, a frequency-impedance characteristic curve can be obtained. Furthermore, by using the graph tool "Pointer A", the abscissa for the highest point can be found to be 3.16kHz. In other words, the natural frequency f_0 of the LC circuit equals 3.16kHz, which is nearly consistent with the theoretical calculation of 3.008kHz (the difference is caused by the limited sample point number for simulation).

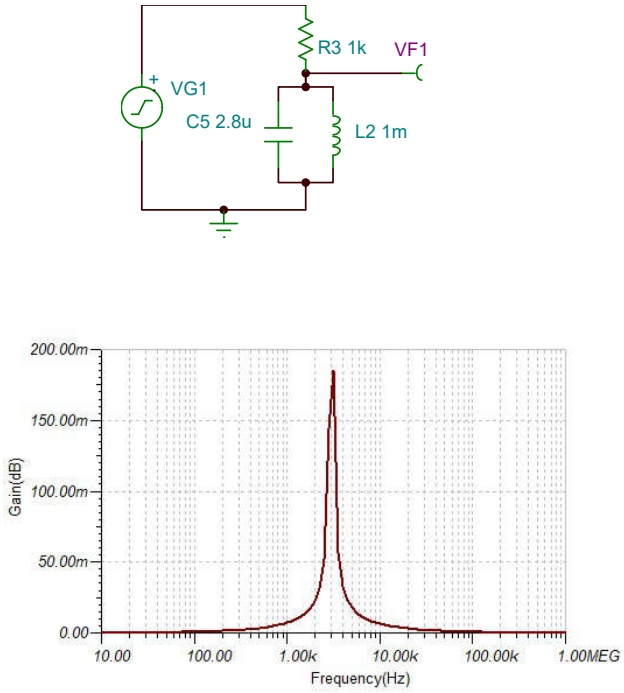


Figure 144. *Impedance Characteristics of the Parallel LC Tank Circuit*

5. Simulate the circuit shown in **Figure 142** using TINA, selecting a 1.05kHz square wave for the input signal. A square wave is chosen because its spectrum contains high-order harmonics, providing a wide range of frequency components. The natural frequency of the LC tank circuit (3.16kHz) is exactly 3 times the frequency of the square wave signal (1.05kHz). From the simulated waveforms shown in **Figure 145**, it is clear that the amplified output is the 3rd harmonic of the square wave. If LC parameters are adjusted, it is also possible to simulate the amplification of the 5th, 7th, and other harmonics.

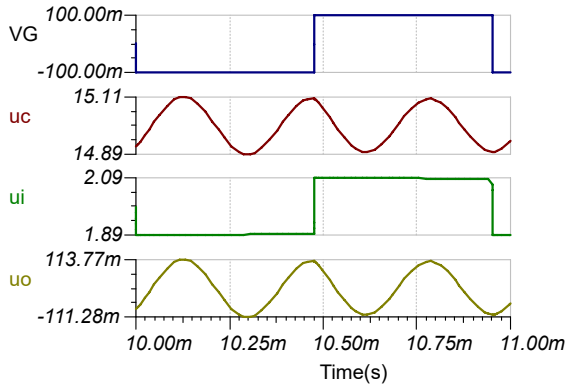


Figure 145. *Simulated Waveforms of the Frequency-Selective Amplifier*

High-frequency filter circuit

A suitable capacitor connected in parallel with RC can form the high-frequency filter circuit shown in **Figure 148**.

1. Capacitor C_3 reduces the impedance of R_C to high-frequency signals, so the circuit shown in **Figure 146** applies different amplification factors to signals of various frequencies. This circuit is used in real-world applications to eliminate high-frequency interference.
2. This filtering effect can be experimentally verified using a Tina simulation. **Figure 146** an interference generator V_{G1} is added, with its interference signal set to 100kHz/0.2V_{PP}. V_G and V_{G1} are combined and raised by a 2V DC level to form u_i, which then enters the filter amplifier circuit. Note that the effect of V_G and V_{G1} will be halved according to the superposition principle, i.e., $u_i = 0.5 \times (V_G + V_{G1}) + 2$.
3. The value of C_3 needs to be calculated. By setting the cutoff frequency of the low-pass filter (considering R_C as the output impedance and AC grounding the upper terminal of C_3, thus forming a low-pass filter from R_C and C_3) to be 5 times the signal frequency, the value of C_3 can be calculated as approximately 3.2nF. Design the switch SW to simulate the effect of the filter capacitor.

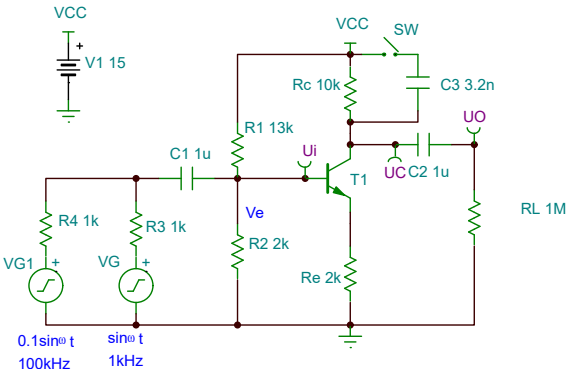


Figure 146. *High-Frequency Filter Amplifier Circuit*

4. **Figure 147** shows the simulated waveforms of the condition where SW is open. It is clear that the 100kHz interference signal is also amplified.

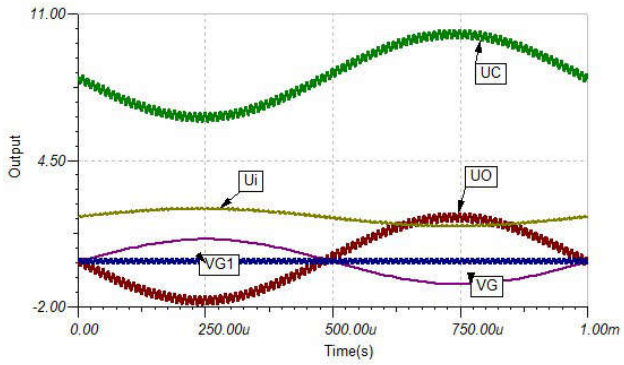


Figure 147. *Amplified Waveforms of High-Frequency Interference without Filtering*

5. **Figure 148** shows the simulated waveforms of the conditions where SW is closed. It is clear that the 100kHz interference signal is effectively suppressed.

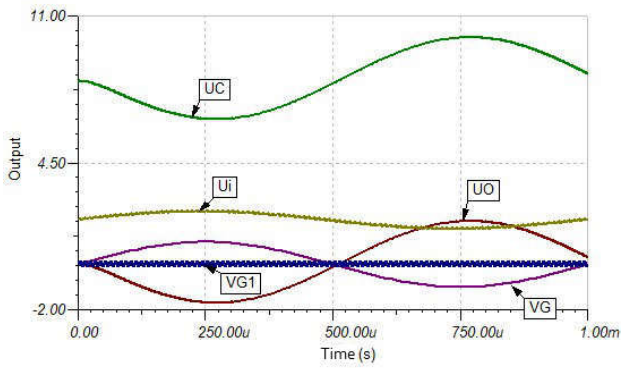


Figure 148. *Amplified Waveforms of High-Frequency Interference after Filtering*

High-frequency enhancement circuits

Similarly, placing a capacitor in parallel with RE results in a high-frequency enhancement circuit.

1. If the signal has a wide bandwidth, like audio, we would naturally want both the high-frequency and low-frequency components to be amplified by an equal factor. Otherwise, the amplified signal will be "out of tune".
2. However, normal circuits exhibit a low-pass effect due to the distributed capacitance, so the amplification factor for high-frequency signals is "naturally" smaller than that for low-frequency signals.
3. **Figure 149** shows the "pre-emphasis" of high-frequency signals to compensate for the high-frequency attenuation in the subsequent circuit.

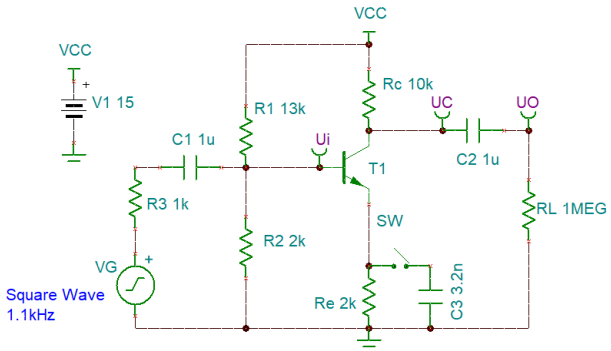


Figure 149. *Pre-Emphasis Amplifier Circuit*

During the TINA simulation, a 1.1kHz square wave is used as the "wide-band" signal.

1. When the SW switch is open, the simulated output waveform is shown in **Figure 150** on the left. It is not flat but slightly sloped, which is due to the bandwidth of the amplifier circuit. An extremely high bandwidth is required to fully reproduce a square wave.
2. When the SW switch is closed, the simulated output waveform is shown in **Figure 150** on the right. It exhibits "glitches," which are the result of high-frequency enhancement.

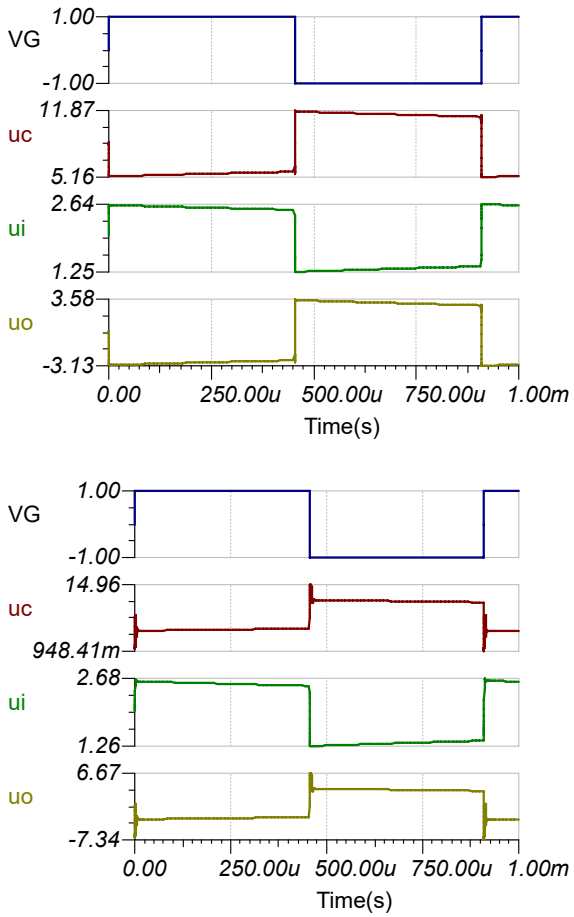


Figure 150. *Simulated Waveforms of the Pre-Emphasis Circuit*

Differential Amplifier Circuit

In the chapter "Fundamentals of Analog Circuits", we discussed that the characteristics of all electronic components are more or less affected by temperature, though semiconductor materials exhibit the most pronounced effect.

1. For PN junctions, the temperature coefficient is as high as –2.5mV/°C. This signifies that the diode voltage drop, U_{AK}, or the bipolar junction transistor voltage drop, U_{BE}, decreases with rising temperature (becoming more conductive).
2. In common-emitter amplifier circuit, ΔU_{BE}, due to the change in temperature, is actually equivalent to the "position" of the input signal, u_i. The output signal is therefore not altered independently of the input signal, a disruptive phenomenon known as "temperature drift."

The differential circuit shown in **Equation 70** is the basic idea to eliminate temperature drift:

1. The input signal is applied to the inputs of two common-emitter amplifier circuits (u_{i1}-u_{i2}), and the output signal is derived from their difference ($u_{O1} - u_{O2}$).
2. Because the temperature drift produces the same ΔU_{BE} on both transistors, the results cancel each other at the output.

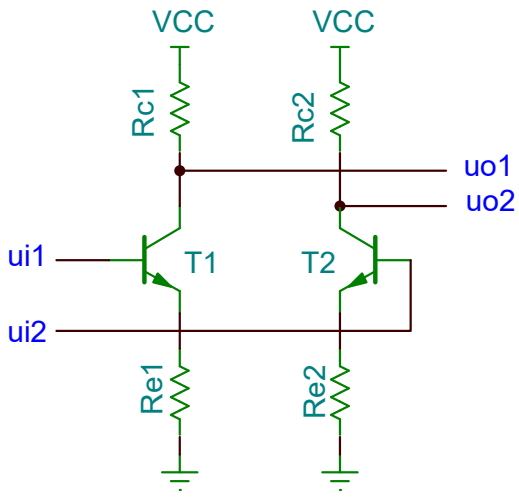


Figure 151. *Basic Structure of Differential Circuits*

3. The circuit shown in **Equation 70** is not practical to either single-ended input or single-ended output of the input signal.

A practical differential circuit is shown in **Equation 71**.

1. For simplicity, the circuit shown in **Equation 71** uses positive and negative power supplies to avoid excessive bias circuit that might distract from the key points.
2. **Equation 71** features two signal inputs and two signal outputs, yet it supports both single-ended input and single-ended output.
3. V_E point is connected to a constant current source, not to ground, so there is:

$$I_{E1} + I_{E2} = I_E \tag{70}$$

$$\frac{u_{i1} - u_{BE} - V_E}{R_E} + \frac{u_{i2} - u_{BE} - V_E}{R_E} = I_E \tag{71}$$

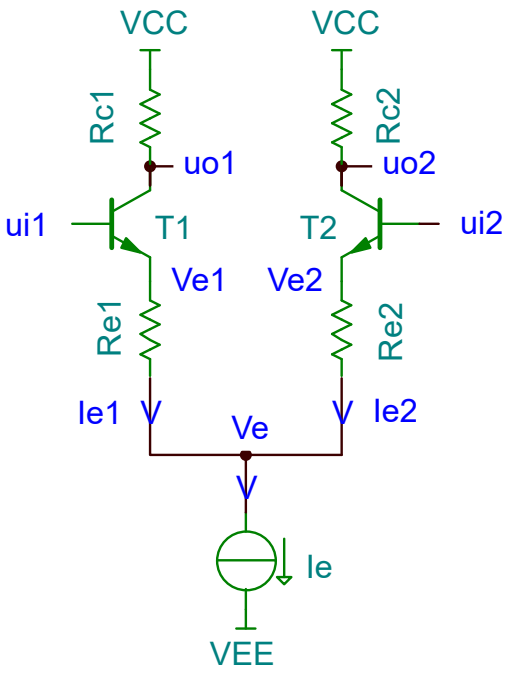


Figure 152. *Long-Tail Differential Circuit*

Considering only temperature drift, that is, the input value ui remains constant while temperature varies:

1. Taking the derivative of **Equation 71** (Taking Δ), it gets

$$\frac{0-\Delta u_{BE}-\Delta V_E}{R_E}+\frac{0-\Delta u_{BE}-\Delta V_E}{R_E}=0\Rightarrow\Delta u_{BE}=-\Delta V_E \tag{72}$$

2. **Equation 72** means that the change in Δu_{BE} caused by temperature drift is compensated by ΔV_E.
3. Therefore, the voltage loaded on R_E does not change, I_{E1} and I_{E2} do not change, and the outputs u_{O1} and u_{O2} are unchanged (single-ended output possible).

Temperature drift is not considered now, when there is only one input, ui1 (single-ended input signal):

1. Taking the derivative of **Equation 71** (Taking Δ), it gets

$$\frac{\Delta u_{i1}-0-\Delta V_E}{R_E}+\frac{0-0-\Delta V_E}{R_E}=0\Rightarrow\Delta u_{i1}=2\Delta V_E \tag{73}$$

2. Considering only the AC path, the emitter resistor R_E is connected to u_i and V_E at its two ends. **Equation 73** means that the voltage variation Δu_{RE} at two ends of R_E is 0.5Δui.

$$\Delta u_{R_{E1}}=\Delta u_{i1}-\Delta V_E=\frac{1}{2}\Delta u_{i1} \tag{74}$$

$$\Delta u_{O1}=-R_{C1}\times\frac{\Delta u_{R_{E1}}}{R_{E1}}=-\frac{1}{2}\times\frac{R_{C1}}{R_{E1}}\Delta u_{i1} \tag{75}$$

3. **Equation 75** shows that the amplification factor of a differential circuit with single-ended input and single-ended output is half (1/2) that of a conventional common-emitter amplifier circuit.
4. Furthermore, since $\Delta I_{E1} = -\Delta I_{E2}$, it follows that $\Delta u_{O2} = -\Delta u_{O1}$. Therefore, the amplification factor for differential output is identical to that of a conventional common-emitter amplifier.

The differential amplifier circuit's common-mode rejection capability and voltage amplification factor characteristics can be observed via TINA simulation, as shown in **Equation 72**.

1. Introducing DC power supply $V_3 = V_4$, which is equivalent to a common-mode signal, or Δu_{BE} caused by temperature drift. The simulated waveform is unchanged by giving V_3 and V_4 any settings (Taking care not to saturate or cut off the transistor). This demonstrates the differential circuit's ability to suppress common-mode signals.
2. u_{O1} is a single-ended output with a simulated amplification factor of (12.46 – 7.64)/2 = 2.41 times, approximately half that of a conventional common-emitter amplifier circuit (10kΩ/2kΩ = 5).
3. u_O is a double-ended output with a simulated amplification factor of (4.81 + 4.81)/2 = 4.81 times, approximately equivalent to that of a conventional common-emitter amplifier circuit.

Note: Common-mode signals are defined as 0.5 ($V_1 + V_2$) and differential-mode signals as ($V_1 – V_2$). V_1 and V_2 are the two input signals to the differential circuit, respectively.

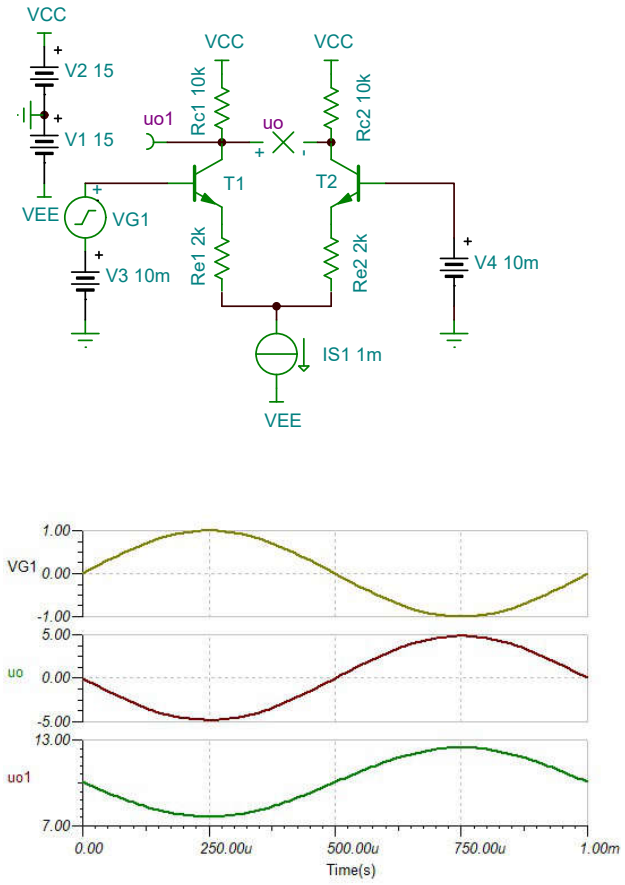


Figure 153. *Differential Circuit Simulation*

For amplifier circuits, halving the amplification factor is scarcely a drawback, whereas the ability to suppress common-mode signals is particularly crucial. Consequently, high-performance common-emitter amplifier circuits invariably adopt differential circuit configurations.

1. The input stage of op amp is thus constituted by differential circuits.
2. The equation derivation for the differential circuit is entirely based on the assumption of perfect symmetry between two common-emitter amplifier circuits.
3. Practical circuits inevitably exhibit deviations, giving rise to various critical performance parameters for actual op amps, such as common-mode rejection ratio, bias current, and offset current.
4. Therefore, a high-performance op amp can only be used if you have a solid knowledge of the transistor amplifier circuit.

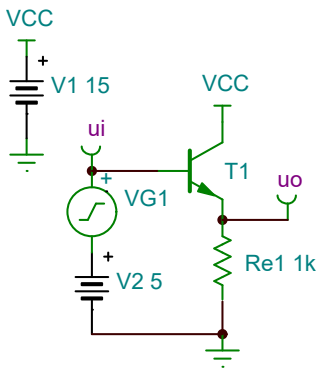
Common-Collector Amplifier Circuit

In this section, we'll discuss the common-collector amplifier circuits, also known as the "power amplifier" circuits. It's probable that you always associated "power amplifier" with sound systems the first time you heard this term. There's a good reason for this. The loudspeaker, as the final load in a sound system, typically has an impedance of 8Ω or 4Ω. It is impossible for a typical circuit to drive such a heavy load.

Strictly speaking, power amplifiers in sound systems are divided into "preamplifiers" and "post-amplifiers", which use common-emitter amplifier circuits to regulate the volume and common-collector amplifier circuits to drive the loudspeaker, respectively.

Emitter Follower

In fact, the common-collector amplifier circuit is also known as an emitter follower. In the circuit shown in **Figure 154**, the relationship between input and output is as follows:



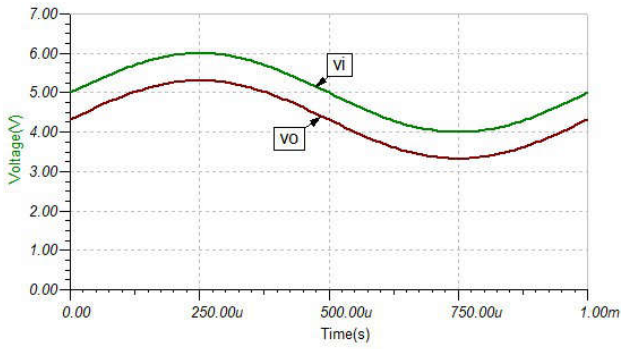


Figure 154. *Emitter Follower*

1. The common-collector amplifier circuit provides a 1x AC voltage amplification, so it is also referred to as an emitter follower.
2. As long as the base-emitter junction of the bipolar junction transistor conducts, the "emitter follower" characteristic holds true.
3. An emitter follower is used to connect two circuits, acting as a "buffer" to solve problems or to enhance performance.

To function as a "buffer" in a circuit, the device must feature the following excellent characteristics:

1. No impact on the amplitude and bandwidth of the signal.
2. Extremely high input impedance, making it easy to drive the preceding circuit.
3. Extremely low output impedance, making it easy to drive the subsequent load circuit.

Input and Output Impedances of Emitter Follower Circuit

By referring to **Figure 154**, the (AC) input impedance of the emitter follower circuit is calculated as shown in **Equation 76**:

$$\begin{cases} R_I = \dfrac{\Delta u_I}{\Delta i_I} \\ \Delta i_I = \dfrac{\Delta i_C}{\beta} \approx \dfrac{\Delta i_E}{\beta} \Rightarrow R_I \approx \beta R_E \\ \Delta i_E = \dfrac{\Delta V_E}{R_E} = \dfrac{\Delta u_I}{R_E} \end{cases} \tag{76}$$

By referring to **Figure 154**, the output voltage at no load is: ΔuO = Δui. When a load RL is applied, the output voltage is: ΔuO = Δui. Therefore, the output impedance of the emitter follower circuit is 0. Naturally, this is the result of neglecting the equivalent resistance between the base and emitter (base resistance), rbe. In reality, RO is approximately a few ohms to tens of ohms.

Considering the equivalent resistance rbe, the output voltage ΔuO is calculated as shown in **Equation 76**.

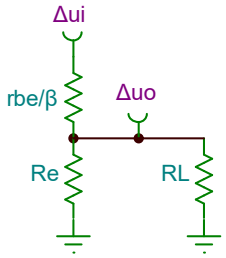


Figure 155. *Circuit for Calculating the Output Impedance of the Emitter Follower Circuit*

1. The (AC) output voltage Δu_O is no longer directly equal to the (AC) input voltage Δu_I, because the resistance r_{be} needs to be scaled down by a factor of β and transformed to the position of R_E.
2. At no load, the expression for the output voltage Δu_O is shown as **Equation 77**:

$$\Delta u_O = \Delta u_I \times \frac{R_E}{R_E + \frac{r_{be}}{\beta}} \tag{77}$$

4. When a load is applied, the expression for the output voltage Δu_O is shown as **Equation 78**:

$$\Delta u_O = \Delta u_I \times \frac{R_E // R_L}{R_E // R_L + \frac{r_{be}}{\beta}} \tag{78}$$

6. The value of R_L, when the loaded output voltage **Equation 78** equals 0.5 times the no-load output voltage **Equation 77**, is the output impedance R_O. Since neither r_{be} nor β is an exact value, the specific expression for R_O has little practical significance and will not be given here.
7. It is more meaningful to assume a set of data to determine the order of magnitude of R_O. Assuming r_{be} is 1kΩ, R_E is also 1kΩ, and the β value is 100, then $R_O \approx rbe/\beta = 10\Omega$ (i.e., when R_L equals 10Ω, the output voltage drops to half of the no-load voltage).

The above analysis shows that the emitter follower circuit, with its high input impedance and low output impedance, is an excellent "isolation buffer circuit".

Bandwidth of Emitter Follower Circuit

As shown in **Figure 156**, both the common-emitter amplifier and the common-collector amplifier can demonstrate their output within the same circuit.

1. The signal generator is selected as a 2Vpp/1kHz square wave with a voltage rise rate set to 1ns.
2. The amplification factor of the common-emitter amplifier circuit is –1, and that of the emitter follower circuit is 1.

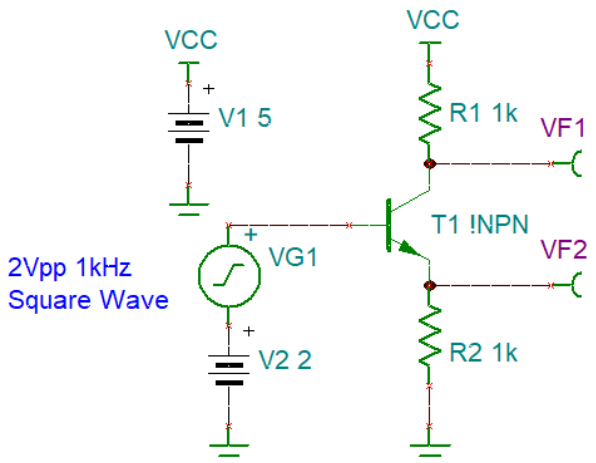


Figure 156. *Amplifier Circuit Bandwidth Test*

While it seems that their frequency characteristics should be similar, the actual circuits or simulation results show that the in-phase output (emitter follower output) has a lower delay and a higher slew rate.

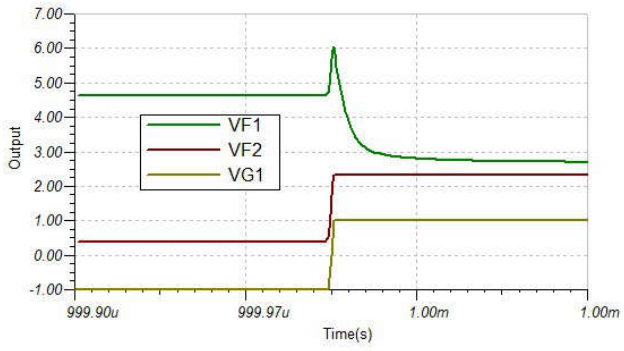


Figure 157. *Comparisons of Delay and Slew Rate*

The emitter follower circuit inherently features an extremely high bandwidth, so high that its impact on the circuit is almost negligible.

Class A Power Amplifier Circuit

If it is not required to filter the output signal to a pure AC signal, the value of the emitter resistor RE can be as large as possible to reduce "quiescent" power dissipation with minimal adverse effects.

If the circuit requires AC input and AC output while driving a load, the selection of the emitter resistor RE's value is critical. The simulated circuits shown in **Figure 158** to **Figure 160** are Class A power amplifier circuits. Theoretically, the input and output voltage waveforms should be identical. All input signals have a DC offset of 7.7V, and the signal amplitudes are set to 2VPP and 8VPP, respectively. The values of emitter resistor RE and load resistor RL are chosen as 1kΩ/6kΩ and 6kΩ/1kΩ, respectively.

1. **Figure 158** shows the case with an $8V_{PP}$ large-amplitude input, a 1kΩ heavy-load output, and a 6kΩ R_E. Obviously, the output waveform exhibits trough distortion.

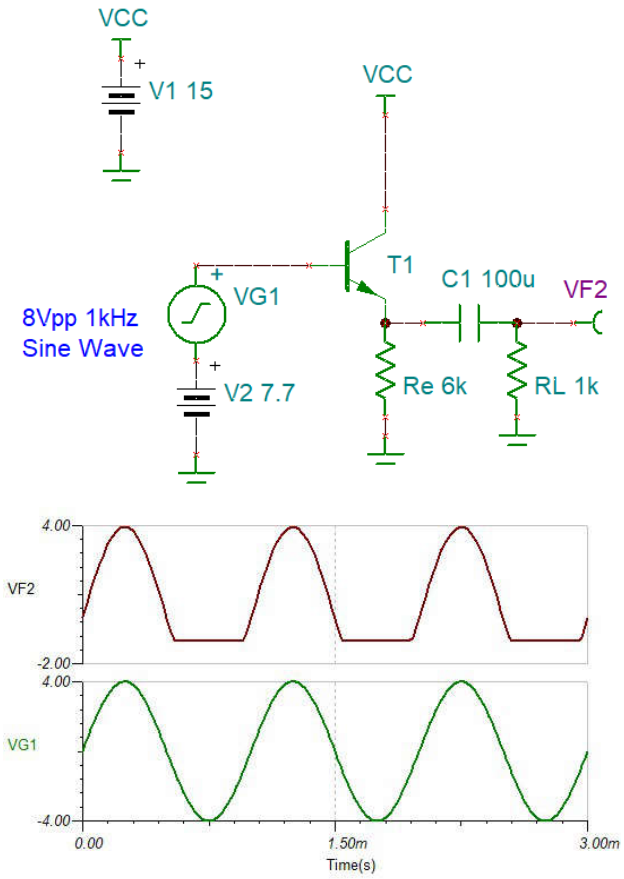
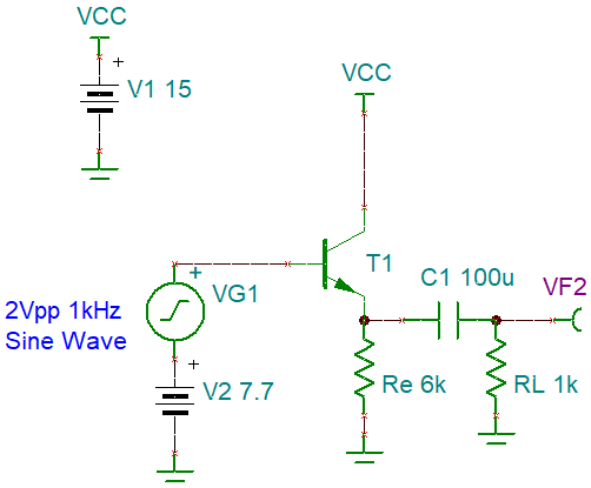


Figure 158. *Class A Power Amplifier with Large Amplitude and Heavy Load*

2. **Figure 159** shows that the output waveform is normal and experiences no trough clipping when the amplitude of the input signal is decreased.



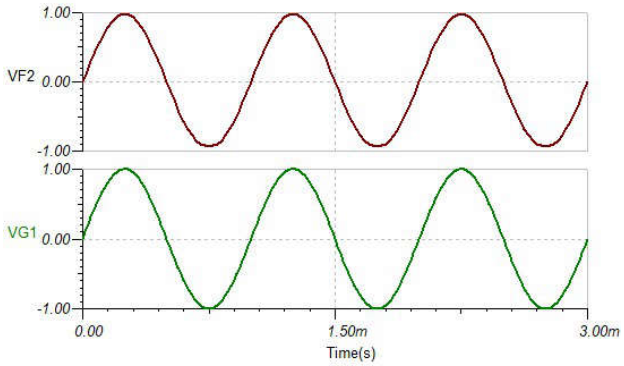


Figure 159. *Class A Power Amplifier with Small Amplitude and Heavy Load*

3. **Figure 160** shows the case with an $8V_{PP}$ large-amplitude input, a 6kΩ light-load output, and a 1kΩ R_E. Obviously, the output waveform exhibits no trough distortion.

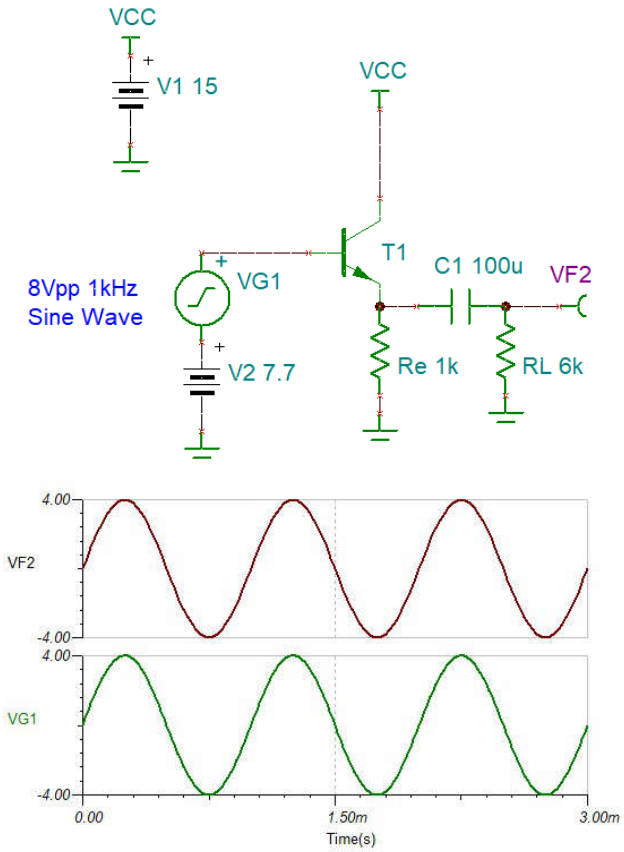


Figure 160. *Class A Power Amplifier with Large Amplitude and Light Load*

So, what causes distortion in a Class A power amplifier?

1. In a steady state, C_1 is equivalent to a battery. With no AC signal input, the potential at V_E is 7.7 – 0.7 = 7V, which equals the voltage across capacitor C_1. Thus, R_E, C_1, and R_L form the loop shown in **Figure 161**.

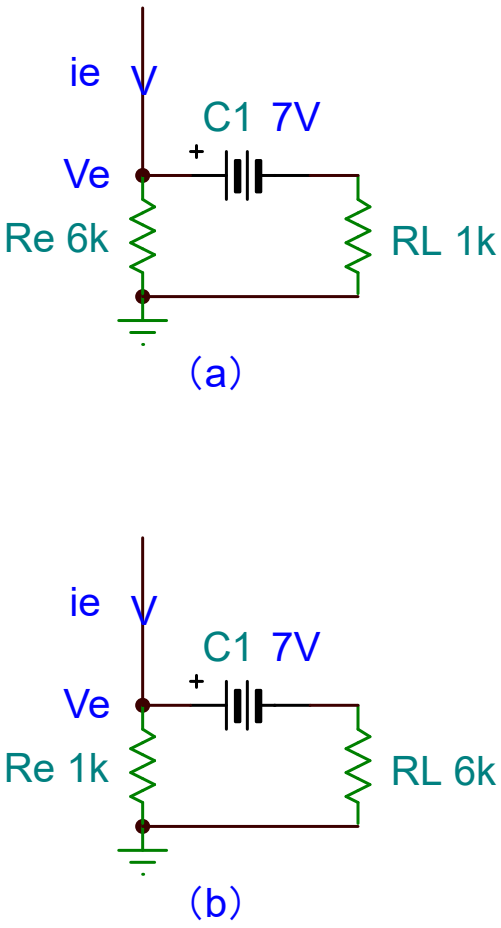


Figure 161. *Load Circuit for the Class A Power Amplifier*

2. Since i_E cannot be negative, the minimum value of the voltage V_E can be calculated. When i_E is 0, the voltage division across the battery (capacitor C_1) by R_E and R_L results in a minimum V_E value of 6V for the circuit shown in **Figure 160** (a) and a minimum V_E value of 1V for the circuit shown in (b).
3. When the value of the input signal is less than V_E + 0.7V, the PN junction between the base and emitter will be cut off, resulting in trough clipping distortion. As the minimum V_E value for the circuit shown in **Figure 160**(a) reaches 6V, "trough clipping distortion" will occur whenever the instantaneous value of the input signal is less than 6.7V.
4. The V_{Emin} value is related to the ratio of R_E to R_L. The lower the load R_L is, the lower R_E must be to avoid distortion.
5. In audio systems, R_L can be as low as 4Ω/8Ω, and R_E must also be on this order of magnitude, thus causing significant quiescent power dissipation on R_E.

Class A power amplifiers deliver the best sound quality, but this comes at the cost of high quiescent power dissipation.

Class B Power Amplifier Circuit

In a Class A amplifier circuit, current always flows from VCC through RE to GND, regardless of whether there is an input signal. To overcome the drawback of low efficiency in Class A power amplifiers, RE can be replaced with a PNP transistor, as shown in **Figure 162**. The basic idea is that:

1. During the positive half cycle of the input signal, T_1 conducts, forming an emitter follower;
2. During the negative half cycle of the input signal, T_2 conducts, also forming an emitter follower;
3. T_1 and T_2 will never conduct simultaneously, so there is no quiescent power loss.

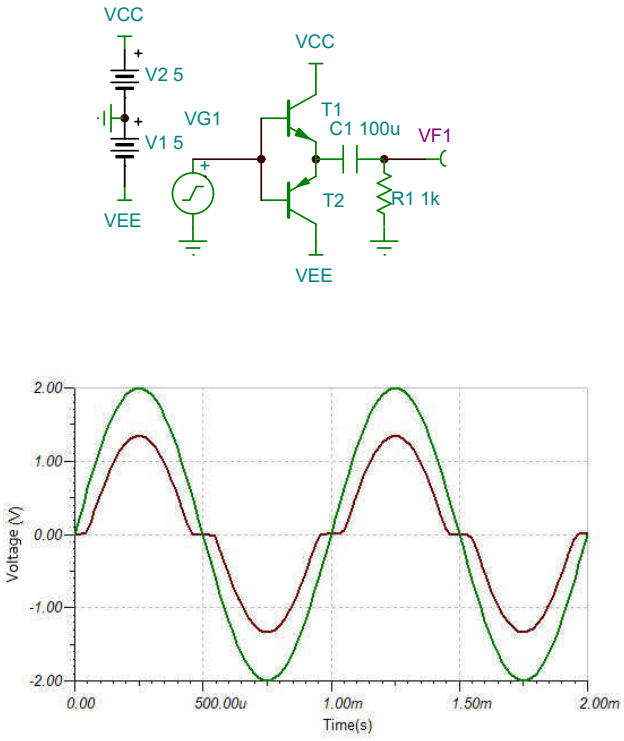


Figure 162. *Class B Power Amplifier Circuit*

It is observed from **Figure 162** that the output signal exhibits "crossover distortion".

1. Since neither T_1 nor T_2 always conducts, the expression for the output voltage is nonlinear:

$$u_O = \begin{cases} u_I - 0.7 (u_I > 0.7) \\ 0 (-0.7 \le u_I \le 0.7) \\ u_I + 0.7 (u_I < 0.7) \end{cases} \tag{79}$$

2. When the input signal is between ±0.7V, there is no change in the output, which is always at 0. This situation is called crossover distortion.

The method for eliminating crossover distortion is shown **Figure 163** below:

1. The incorporation of D_1 and D_2 can cancel out the voltage U_{BE} of T1 and T2.

2. As long as D_1 and D_2 are conducting, each can be considered as a 0.7V battery, resulting in the following derivations:

$$\text{ua>0, } \begin{cases} u_B = u_A + 0.7 \\ u_B = u_D + 0.7 \end{cases} \Rightarrow u_A = u_D \tag{80}$$

$$\text{ua<0, } \begin{cases} u_C = u_A - 0.7 \\ u_C = u_D - 0.7 \end{cases} \Rightarrow u_A = u_D \tag{81}$$

There are several considerations for eliminating crossover distortion in the circuit:

1. During simulation, D_1 and D_2 should be regular diodes, such as the 1N4007, so that the voltage drop can reach 0.7V. If Schottky diodes are chosen, the voltage drop is only around 0.5V, which is not sufficient to cancel out U_{BE}.
2. Without R_3 and R_2, D_1 and D_2 would not conduct, **Equation 78** and **Equation 79** cannot be established.
3. From the perspective of reducing power dissipation, we hope the values of R_3 and R_2 are as large as possible. However, R_3 and R_2 values cannot be too large, but should be designed based on the load current. The load current is the emitter current I_E, and $I_E = \beta I_B$. Insufficient I_B can also cause distortion.
4. Base current I_B of T_1 and T_2 flows through R_3 and R_2. Excessive R_3 and R_2 values may result in insufficient base current.

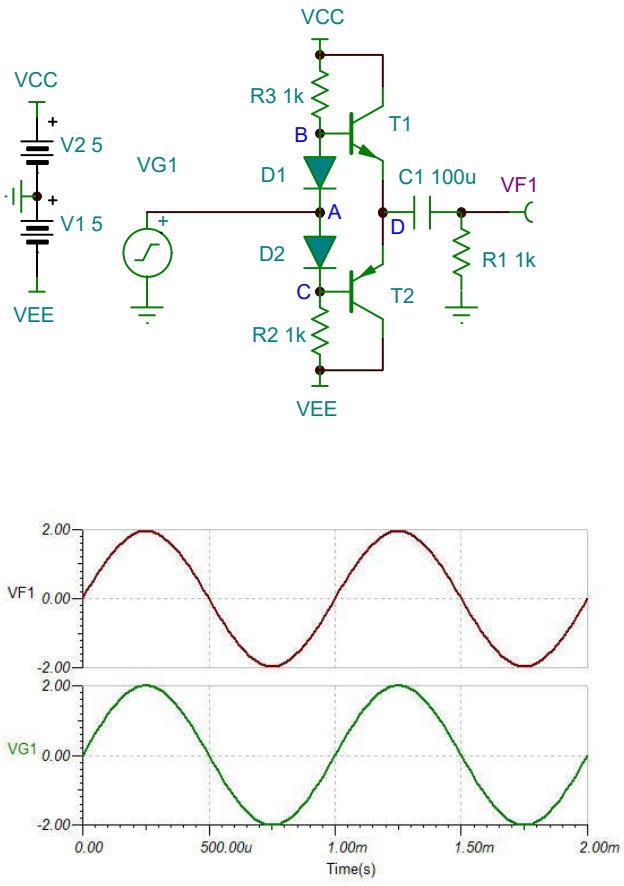


Figure 163. *Class B Power Amplifier for Crossover Distortion Elimination*

Class AB Power Amplifier Circuit

The Class B power amplifier circuit shown in **Figure 163** performs well at small currents but presents significant problems when used in high-power amplifier circuits.

1. Under high-power conditions, bipolar junction transistors T_1 and T_2 generate much more heat than D_1 and D_2 because the currents flowing through them differ significantly.
2. Due to the –2.5mV/°C temperature drift, U_{BE} will decrease, but the diode voltage drop generally remains unchanged.
3. Use the circuit shown in **Figure 164** to simulate this phenomenon, adding diodes D_3 and D_4 to simulate the case where the diode voltage drop is higher than the transistor's u_{BE}. The ammeter reading is as high as 256mA, far exceeding the 5mA limit when a 5V voltage is applied to a 1kΩ load.
4. This large current is generated by the simultaneous conduction of T_1 and T_2 (not flowing through the load), and it does not increase further due to the limiting effect of R_3 and R_4 on the transistor base current.
5. The temperature drift will finally cause T_1 and T_2 to be damaged due to over-current heating. This phenomenon is known as thermal breakdown.

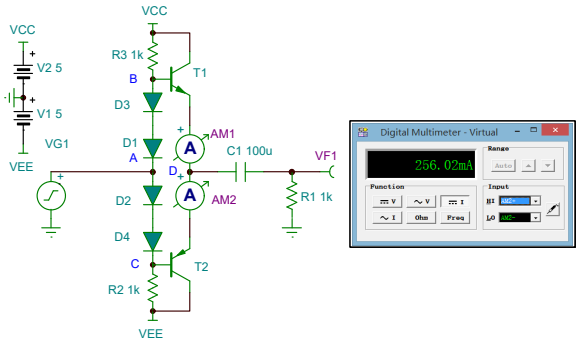


Figure 164. *Thermal Breakdown due to Temperature Drift*

Although high-power Class B power amplifier circuits can rely on "thermal coupling" to mitigate thermal breakdown, the ultimate solution is to use Class AB power amplifier circuits. As shown in **Figure 165**, adding emitter resistors R4 and R5 to T1 and T2 can limit the thermal current.

1. The incorporation of R_4 and R_5 is similar to partially incorporating R_E, which will result in additional power dissipation. However, this additional power dissipation is much lower than the power dissipation on R_E in a Class A amplifier.
2. The larger the R_4 and R_5 values are, the more significant the effect of limiting the thermal current will be. However, the maximum current available to the load will also be limited.

Note: Thermal coupling involves placing a heat-generating component close to a non-heat-generating component (with their heat-sinking surfaces in close contact, coated with thermal grease, and pressure applied) so that their final temperatures are similar, thereby reducing the temperature drift caused by their temperature difference.

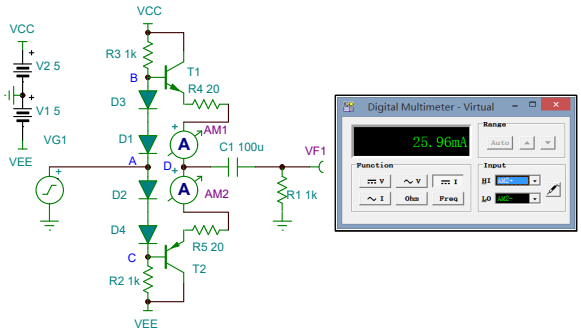


Figure 165. *Class AB Power Amplifier Circuit*

Common-Emitter-to-Common-Collector Cascade Amplifier Circuit

Let's summarize the advantages and disadvantages of common-emitter amplifier circuits and common-collector amplifier circuits:

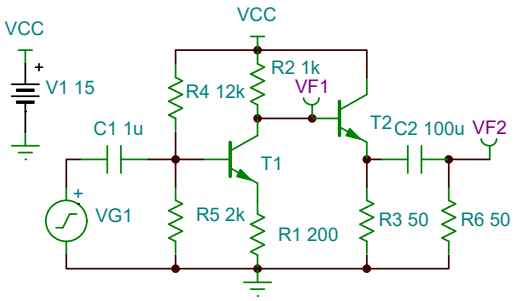
Table 3. Characteristic Comparison of Common-Emitter Amplifier and Common-Collector Amplifier

Name	Input Impedance	Output Impedance	Voltage Amplification	Frequency Characteristics
Common-Emitter Amplifier Circuit	High	High	Yes	Poor
Common-Collector Amplifier Circuit	High	Low	No	Good

1. The two major drawbacks of common-emitter amplifiers are high output impedance (unable to drive heavy loads) and poor frequency characteristics (unable to amplify high-frequency signals).
2. Common-collector amplifier circuits have only one drawback: they cannot amplify voltage.
3. The cascade of a common-emitter amplifier circuit and a common-collector amplifier circuit can solve the problem of the high output impedance in common-emitter amplifiers.

The combined amplifier circuit shown in **Figure 166** achieves a 5x amplification for a 2VPP/1kHz sinusoidal signal while driving a 50ohm load:

1. The design process must start from the load and work backward. Select an appropriate resistor R_3 based on the load R_6, following the no-trough-clipping principle of the common-collector amplifier circuit.
2. The common-emitter amplifier circuit is based on the design in **Figure 121**, but the overall resistance is decreased by a factor of 10 due to the heavier load (βR_3).



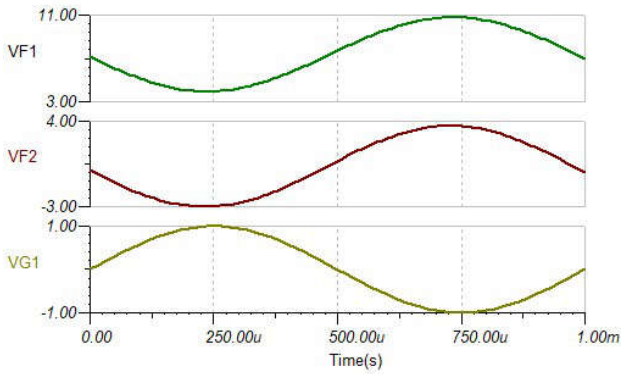


Figure 166. *CE-CC Cascade Amplifier Circuit*

Common-Base Amplifier Circuit

The combination of common-emitter and common-collector amplifier circuits can address the drawback of the high output impedance of the common-emitter amplifier circuit, but it does not solve the issue of poor frequency characteristics because the two amplifier circuits are in a cascaded configuration. The subsequent circuit can at most prevent further bandwidth reduction, but it cannot improve the bandwidth of the preceding circuit. To solve the bandwidth issue of common-emitter amplifier circuits, a common-base amplifier circuit should be introduced.

Basic Common-Base Amplifier Circuit

In a common-emitter amplifier circuit, its output uO is, in essence, the change in voltage across RC caused by the change in iC (approximated as iE). iE can be changed by altering the voltage at the upper terminal of RE or the voltage at the lower terminal of RE. The former yields a common-emitter amplifier, while the latter results in a common-base amplifier. **Equation 82** shows a common-base amplifier circuit:

1. A bulk capacitor C_2 is connected to the base, so the AC potential is 0. Assuming that the DC bias circuit ensures the existence of the base current i_B in the bipolar junction transistor T_1 (with the PN junction between the base and emitter conducting), then the AC potentials at the emitter and base will be equal, both being 0. Thus:

$$\Delta i_E = \frac{0 - \Delta u_i}{R_E} = \frac{-\Delta u_i}{R_E} \approx \Delta i_C \tag{82}$$

$$\Delta u_O = -R_C \times \Delta i_C = \frac{R_C}{R_E} \times \Delta u_i \tag{83}$$

2. **Equation 83** indicates that the gain of a common-base amplifier is the same as that of a common-emitter amplifier, but in the opposite direction.

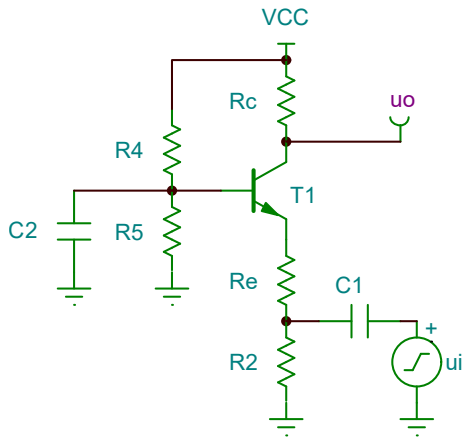


Figure 167. *Common-Base Amplifier Circuit*

3. **Figure 168** shows a TINA simulated circuit. When there is no signal input, the DC voltages at each node of the circuit should be exactly equal to those in the common-emitter amplifier circuit designed in **Figure 121**.
4. It can be seen from **Equation 83** that the amplification factor of this circuit is +10. To prevent saturation caused by this 10x amplifier circuit, the amplitude of the signal generator's u_I has been changed to 0.5V.

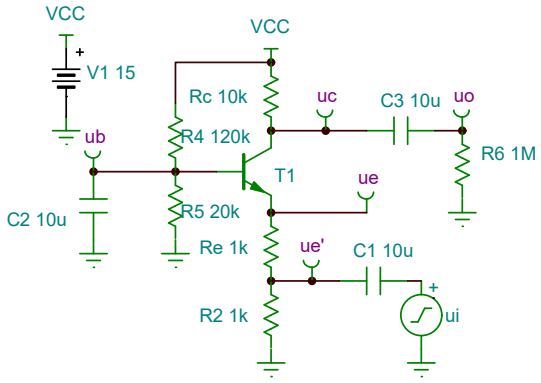


Figure 168. *TINA Simulation of the Common-Base Amplifier Circuit*

5. Simulated waveforms are output for the critical node voltages in the circuit. For clarity, both the combined and separated waveforms of each signal are shown in **Figure 169**.
6. Analysis of the waveforms reveals that the potentials at the base and emitter are essentially DC, with a difference equal to the base-emitter voltage drop u_{BE}.
7. With a non-inverting amplification, the amplification factor is 9.37, which is generally consistent with (**Equation 83**).
8. u_E' exceeds u_I by one DC potential, which is provided by C_1, which is equivalent to a battery. This prevents u_I from introducing an inappropriate DC bias (which could cause i_B to disappear during certain periods). Readers can independently simulate the (distorted) waveforms of the case where C_1 is removed.

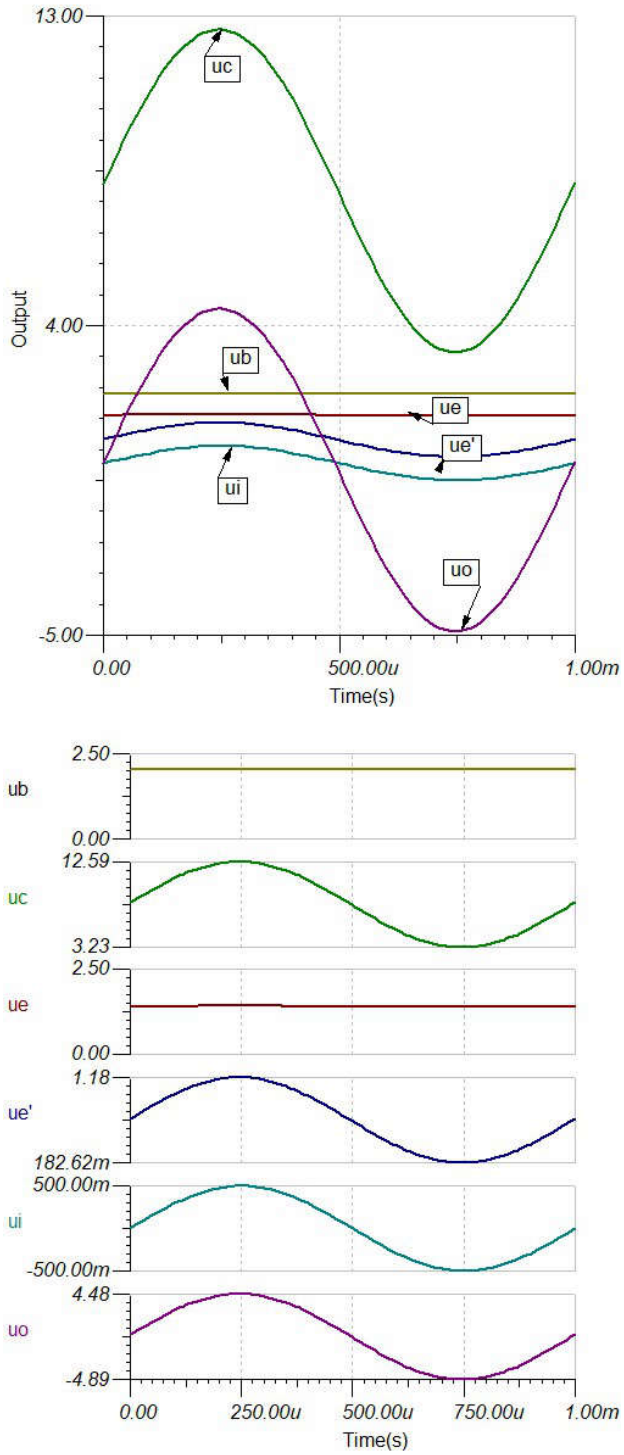


Figure 169. *Simulated Waveforms of the Common-Base Amplifier Circuit*

Input and Output Impedances of Common-Base Amplifier Circuits

The output impedance of the common-base amplifier circuit equals that of the common-emitter amplifier circuit, both being R_C. This can be verified by connecting a load equal to R_C, which will halve the amplification factor.

Since the signal of the common-base amplifier is not input via the base, it lacks the "isolation" effect amplified by a factor of β, and the equivalent input circuit, as shown in **Figure 170**, has an input impedance of $R_E//R_2$.

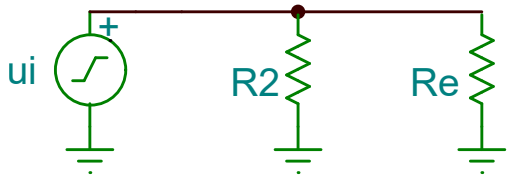


Figure 170. *Input Impedance Loop of the Common-Base Amplifier Circuit*

Frequency Characteristics of Common-Base Amplifier Circuits

Common-base amplifier circuits have a low input impedance but a high output impedance, both of which are drawbacks. So, common-base amplifier circuits must have their own advantages; otherwise, they would not have remained in use until today.

As shown in **Figure 171**, this is the input equivalent low-pass circuit of a common-base amplifier circuit. Although the bipolar junction transistor's inter-electrode capacitance is also present, R_E and C_{BE} do not form a low-pass filter, and the Miller effect present in common-emitter amplifier circuits does not occur, because the AC potential at point V_E is 0. Therefore, its frequency characteristics are superior to those of a common-emitter amplifier circuit.

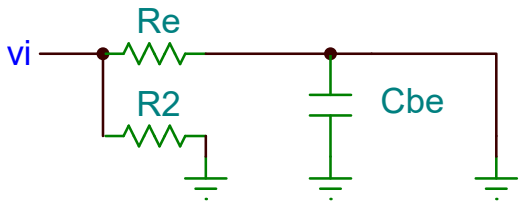


Figure 171. *Input Equivalent of Common-Base Amplifier Circuit*

Simulation of TINA AC transfer characteristics is available in **Figure 172**. Set the lower limit of the vertical axis to the upper limit minus 3, resulting in a bandwidth of –3db.

1. The maximum gain is 19.51dB, and the minimum gain is set to 16.51dB. Then Pointer A can be used to obtain the exact –3dB bandwidth.
2. This 10x non-inverting amplifier circuit has a bandwidth of 4.78MHz. (The simulation software computes DC and low-frequency parameters accurately, but the results of the high-frequency simulation are for reference only.)

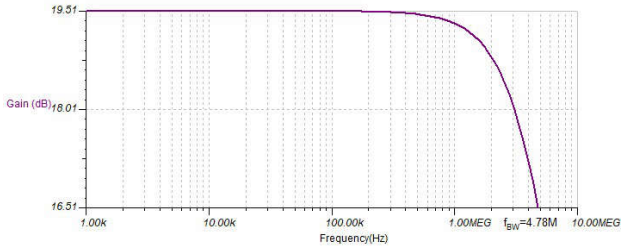


Figure 172. *–3dB Bandwidth of the Common-Base Amplifier Circuit*

Cascode Amplifier Circuit

A common-base amplifier circuit has good frequency characteristics but low input impedances. One solution is to extend the bandwidth of the common-emitter amplifier circuit with a common-base amplifier circuit, called "Walmanization".

If it is a matter of course to use a common-collector amplifier (emitter-follower) circuit to help reduce the output impedance of a common-emitter amplifier circuit, then the idea of "Walmanization" can be described as truly ingenious. Let's start with a question: In the common-emitter amplifier circuit shown in **Figure 173**, will the amplification factor change with the value of resistor R, while the transistor remains in its active region?

1. Our calculations are the same as before, **Equation 84** ~ **Equation 87** nothing has changed.

$$v_E = u_I - U_{BE} = u_I - 0.7 \tag{84}$$

$$I_C \approx I_E \approx \frac{v_E}{R_E} = \frac{u_I - 0.7}{R_E} \tag{85}$$

$$u_O = V_{CC} - I_C \times R_C = V_{CC} - \frac{R_C(u_I - 0.7)}{R_E} \tag{86}$$

$$\Delta u_O = -\frac{R_C}{R_E} \times \Delta u_I \tag{87}$$

2. This indicates that the amplification factor of the common-emitter amplifier circuit does not change if R is replaced with any circuit. Of course, the premise is to ensure that the transistor operates in the active region. If R is disconnected or has a very large resistance, then i_C can never equal βi_B.

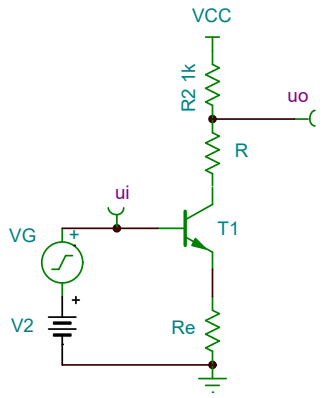


Figure 173. *Inserting a Resistor into the Collector of the Common-Emitter Amplifier Circuit*

Replacing resistor R in **Figure 173** with a transistor results in the circuit shown in **Figure 174**:

1. The circuit shown in **Figure 174** is a "Walmanized" common-emitter circuit, which can extend the bandwidth of the common-emitter amplifier circuit. It is an organic combination of common-emitter and common-base amplifier circuits, rather than a simple cascaded configuration.
2. According to the analysis of **Figure 173**, the amplification factor of the common-emitter amplifier circuit formed by transistor T_1 will not be affected as long as T_2 conducts.
3. R_3 and R_4 provide the base voltage required for T_2 to conduct, and C_3 ensures that the base of T_2 is AC grounded.
4. The incorporation of T_2 allows the collector of T_1 to be AC grounded, thus eliminating the "Miller effect" mentioned earlier.

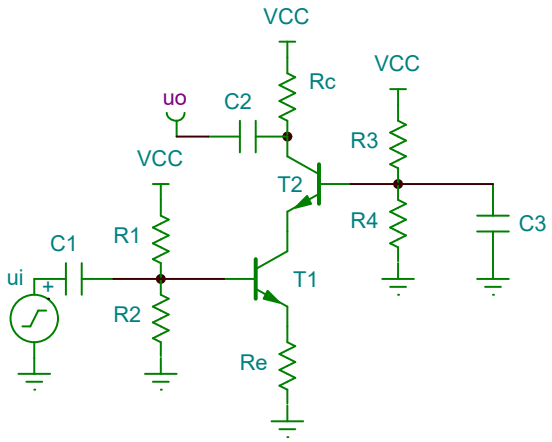


Figure 174. *Cascode Amplifier Circuit*

Simulate the "classic" 5x common-emitter amplifier circuit shown in **Figure 175**.

1. Incorporate a transistor T_2 to form a cascode amplifier circuit.
2. Configure R_3 and R_4 appropriately to ensure that T_2 always conducts. C_3 ensures that the AC potential at the base of T_2 is 0.

3. A switch SW is added to compare simulated waveforms before and after the incorporation of T_2.

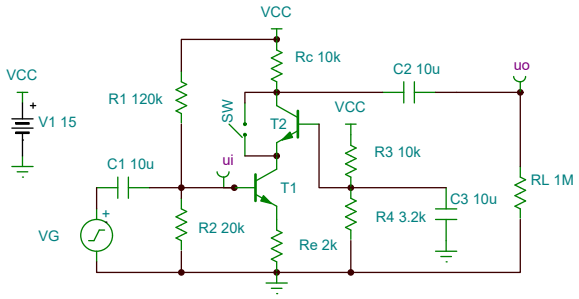


Figure 175. *Simulated Cascode Amplifier Circuit*

4. As shown in **Figure 176**, the simulated waveforms on the left depict the situation when the SW switch is open (i.e., the T_2 common-base circuit is incorporated), while the waveforms on the right depict the situation when the SW switch is closed (i.e., transistor T_2 is bypassed). The difference in their output u_O is very small.

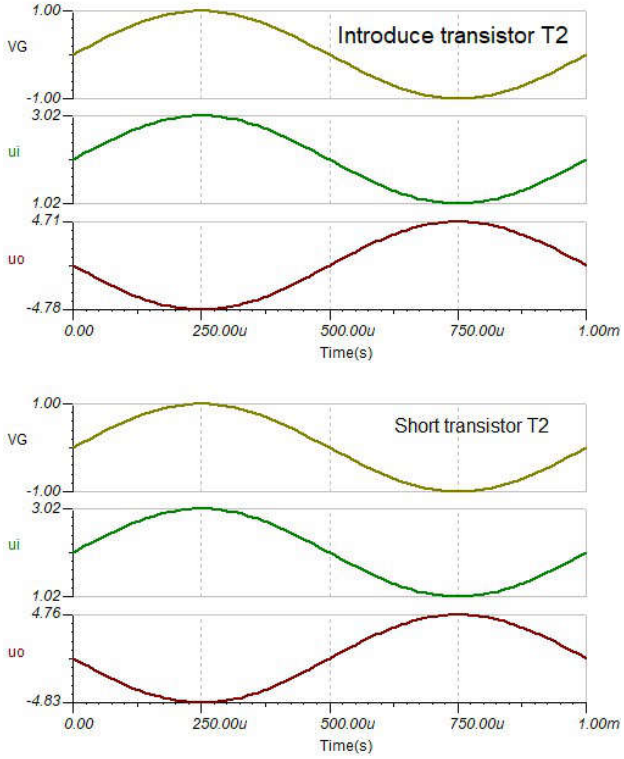


Figure 176. *Simulated Waveforms of the Cascode Amplifier Circuit*

Other Amplifier Circuits

We started studying mathematics from an early age, beginning with basic axioms and progressing all the way to advanced mathematics. In theory, understanding axioms enables us to derive all mathematical formulas and solve all problems independently. However, this is not the case. The human brain is not a computer and cannot store all knowledge exhaustively. Human divergent thinking is quite limited; we can only engage in further limited thinking based on imitation.

In the study of circuits, mastering the characteristics of each component and circuit theorems is far from sufficient for solving practical problems. Given a completely new circuit, simulation software can analyze it, but a human would struggle to do this. We need to encounter a sufficient number of circuits to develop basic analytical skills.

This section provides a qualitative introduction to some mature circuits to help broaden your thinking and improve your ability to analyze specific circuits.

Darlington Circuit

Combining two bipolar junction transistors to form a Darlington transistor can yield an equivalent transistor with an extremely high β value. Darlington transistors, identical in appearance to regular transistors, are readily available for purchase (those with β values exceeding 1000 are Darlington transistors). There are 4 methods to exhaustively combine NPN and PNP transistors into a Darlington transistor, as illustrated in **Figure 177**(A)(B)(C)(D):

1. First, position all transistor bases (B) facing leftwards. Place NPN transistor collectors (C) facing upwards and PNP transistor emitters (E) facing upwards.
2. If the first transistor is NPN, this determines the entire Darlington transistor as NPN. And vice versa.
3. Whether the base B of the second transistor connects to the collector C or emitter E of the first transistor depends on whether the base current direction is correct.
4. Taking (B) as an example, if the base of T_2 is connected to E of T_7, the base current of T_2 is not flowing. So N+N, N+P, P+P, P+N have only one correct connection.
5. (A)(B) are equivalent to NPN transistors and (C)(D) are equivalent to PNP transistors.
6. The difference between (A) and (B) is that the U_{BE} voltage of Darlington transistor A will be 1.4V instead of 0.7V, which means more "DC voltage" is reserved for base conduction, which is detrimental to circuit design. The situations for (C) and (D) are similar.
7. (B) also has drawbacks: constrained by real-world material limitations, NPN transistors generally exhibit superior performance to PNP transistors, hence PNP transistors are typically avoided.

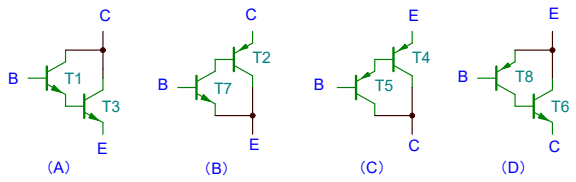


Figure 177. *4 Configurations of Darlington Transistors*

Push-Pull Amplifier Circuits

In the previous chapter, we introduced Class B amplifier circuits, also known as push-pull circuits. In addition to using diodes, crossover distortion can also be eliminated using bipolar junction transistors. As shown in **Figure 178**:

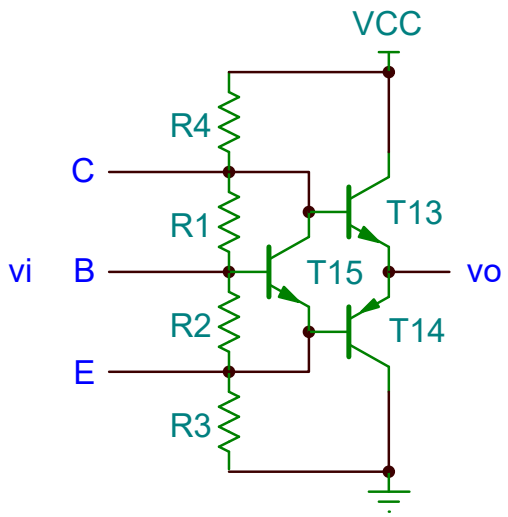


Figure 178. *Eliminating Crossover Distortion Using a Transistor*

1. Let $R_1 = R_2$. If the base current of T_{15} is ignored, then $U_{CE} = 2U_{BE} = 1.4V$, which is used to eliminate crossover distortion.
2. R_3 and R_4 are also necessary to supply the base current for transistors T_{13} and T_{14}.
3. Compared to diodes, using transistors to eliminate crossover distortion allows for easier "thermal coupling" within a package.
4. Since the DC voltage difference at points C, B, and E in **Figure 178** is only 0.7V, the signal v_i can be input to any of these three points. This property is a bit strange, but it is indeed the case. Please think it through clearly.
5. In practice, the signal v_i is input to the point with an appropriate DC bias.

Let's move on to the "Compound-Pair Quasi-Complementary Output Circuit" shown in **Figure 179**:

1. In high-power push-pull circuits, the formerly used **Figure 178** output-stage transistors T_{13} and T_{14} are replaced by a Darlington transistor. The reason is that high-power transistors have a very low amplification factor (ten to tens). As a result, the base current cannot be ignored, and the resistance value of the preceding bias circuit must be very small as well. In other words, without a Darlington transistor, the preceding circuit would not effectively drive the subsequent circuit.
2. The Darlington transistor construction is also carefully designed. Because the characteristics of PNP transistors are inferior to those of NPN transistors (the larger the current, the larger the difference), it is difficult to achieve "complementary symmetry". In circuit operation, the current through T_{10} (T_{11}) is much larger than that through T_9 (T_{12}). Therefore, it will be easier to achieve "complementary symmetry" by using identical NPN transistors in the last stage.
3. U_{BE} of the NPN Darlington transistor consisting of T_9 and T_{10} is 1.4V, while U_{BE} of the PNP Darlington transistor composed of T_{12} and T_{11} is 0.7V. Therefore, the crossover distortion voltage difference that T_{15} needs to compensate for is 2.1V, with $R_1 = 2R_2$.

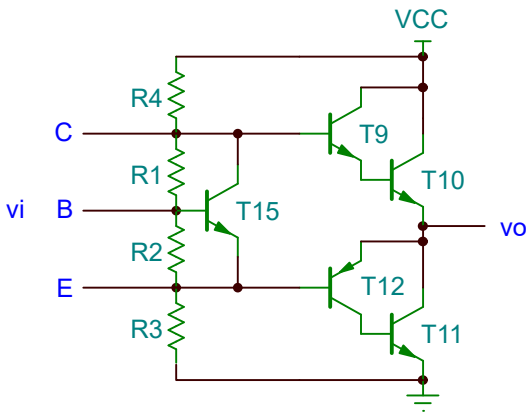


Figure 179. *Compound-Pair Quasi-Complementary Output Circuit*

Directly Coupled Multi-Stage Amplifier Circuit

A directly coupled multi-stage amplifier circuit, as shown in **Figure 180**, is actually a simplified op amp circuit.

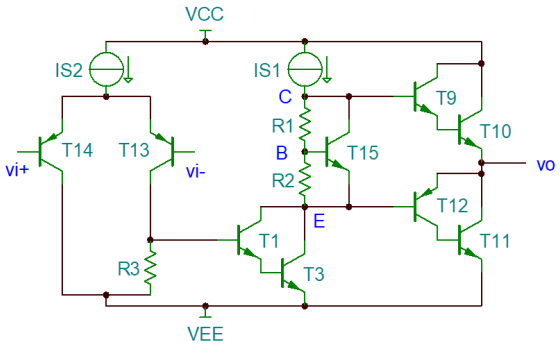


Figure 180. *Directly Coupled Multi-Stage Amplifier Circuit*

1. The internal structure of an op amp circuit is divided into 3 stages: the differential input stage, responsible for common-mode signal rejection (temperature drift is also considered a common-mode signal); the intermediate amplifier stage, which significantly increases the amplification factor; and the push-pull output stage, which enhances drive capability.
2. In op amps, R_C and R_E are commonly replaced by a current source circuit. This ensures the presence of DC bias current while making the AC impedances of R_C and R_E "infinite". Providing that a resistor with an extremely large value is used for this purpose, it wouldn't be possible to set the DC bias current.
3. The reason for incorporating PNP transistors in the differential input stage is that, in multi-stage amplification, to avoid excessive DC offset (where U_{BE} continuously accumulates in one direction), an NPN transistor is often followed by a PNP transistor for amplification. This "compensates for" the 0.7V U_{BE}, allowing efficient utilization of the supply rails.
4. The intermediate amplifier stage is simply a common-emitter amplifier circuit designed for extreme amplification, where the AC potentials at the three points (C, B, and E) are equal. Any of these points can be used as the output. Moreover, the incorporation of T_{15}, R_1, and R_2 does not affect the amplification factor of the common-emitter amplifier.

5. The current source I_{S1} acts as a resistor R_C, as its internal AC resistance R_{IS1} is "infinite". The Darlington transistor composed of T_1 and T_3 features an extremely high amplification factor ($\beta_1\beta_3$). R_E is converted from the dynamic resistance r_{be} between the base and emitter and then transformed to its position, at which point the amplification factor is approximately:

$$A = \frac{u_O}{u_I} = -\frac{R_{IS1}}{R_E} = -\frac{R_{IS1}}{\frac{r_{be}}{\beta_{T1}\beta_{T2}}} = -\beta_{T1}\beta_{T2}\frac{R_{IS1}}{r_{be}} \tag{88}$$

6. The final output stage uses a Class B power amplifier circuit with a Darlington transistor, resulting in extremely low output impedance to drive heavy loads.

Fundamentals of Op Amp Application

The use of op amps is both simple and complex. It is simple because complex parameter calculations required for transistor circuits can be avoided in the design of op amp circuits, while it is complex because many times op amps are not "ideal" and designing circuits as if they were ideal op amps always leads to incorrect results.

Based on simulation software, this chapter will explain the principles of basic op amp circuits; the performance of practical op amps; the functions of special op amps; and the topological differences of active filters, focusing on the principles, performance, functions, and differences, respectively.

Basic Op Amp Circuits

As its full name, operational amplifier, suggests, an op amp can perform various mathematical operations on analog signals. These mathematical operations are not intended for "calculation". Rather, they are the operations that may be required by us to simulate analog signal conditioning, such as proportional, addition, subtraction, multiplication, integration, and differentiation.

From the perspective of ideal op amps, the analysis of op amps applies the two principles of "virtual short" and "virtual open". An ideal op amp circuit is shown in **Figure 181**. If the output voltage is not saturated:

$$u_O = A(u_P - u_N) \tag{89}$$

1. In **Figure 181**, A represents the amplification factor of an op amp, which ranges from tens of thousands (80dB) to 1 million (120dB). However, the output voltage u_O is at most a few tens of volts. Therefore, the difference between the voltage u_P at the non-inverting input and the voltage u_N at the inverting input is extremely small, and the two inputs can be considered equipotential, which is the origin of "virtual short".

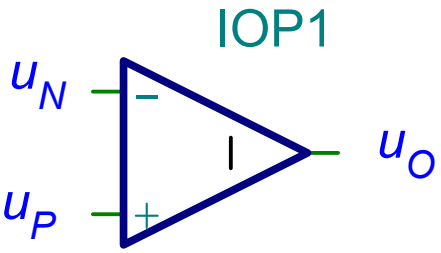


Figure 181. *Ideal Op Amp Circuit*

2. In the previous section on transistor amplifier circuits, we analyzed the actual structure of operational amplifier circuits. The input impedance of op amps is relatively high, reaching at least 1MΩ. To some extent, the op amp input current can be considered as zero. This is the origin of "virtual open".

Inverting Proportional Circuit

When analyzing op amp circuits, we don't need to dwell on how the design is conceived; instead, we can simply calculate the results based on the principles of virtual short and virtual open.

Theoretical derivation for the inverting proportional circuit

Figure 182 is the schematic for an inverting proportional circuit:

1. Based on the principle of virtual open, there is no current through resistor R_2, so the voltage u_P is 0V, the same as ground.
2. Based on the principle of virtual short, the voltage u_N is equal to the voltage u_P, both at 0V.
3. According to Kirchhoff's Law, we can obtain **Figure 182**, and simplifying it gives us **Figure 183**.

$$\frac{u_O - u_N}{R_F} = \frac{u_N - u_I}{R_1} \tag{90}$$

$$u_O = -\frac{R_F}{R_1} u_I \tag{91}$$

4. As **Figure 183** indicates, the circuit shown in **Figure 182** is an inverting proportional circuit under the conditions where virtual short and virtual open hold true.
5. Ideally, the values of the input resistor R_2 and the load resistor R_L have no effect on the amplification factor. However, the value of resistor R_2 is preferably equal to that of the parallel combination of R_1 and R_F so that the impedances at the non-inverting and inverting terminals of the op amp are symmetrical.

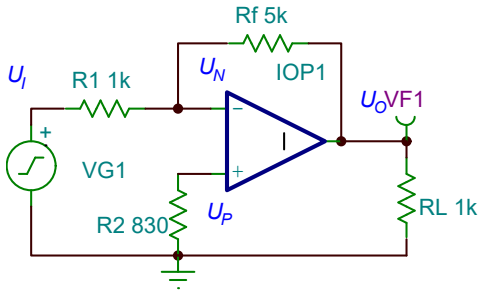


Figure 182. *Inverting Proportional Circuit*

TINA simulation of the inverting proportional circuit

Figure 183 shows the transient simulation results of the inverting proportional circuit (**Equation 90**), where the output voltage waveform VM1 and the input voltage waveform VG1 (a 1kHz unit-amplitude sine wave) exhibit a precise fivefold inverting amplification relationship.

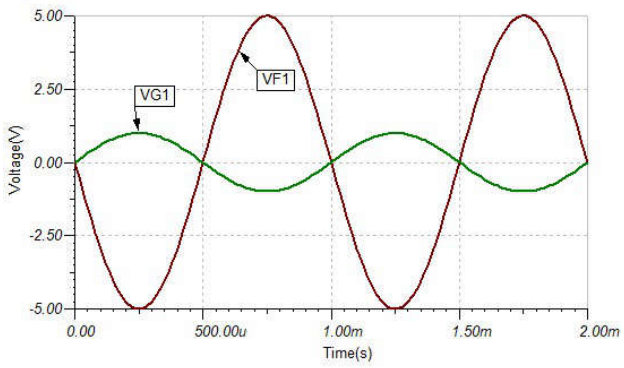


Figure 183. *TINA Simulated Transient Waveforms of the Inverting Proportional Circuit*

Advantages and disadvantages of the inverting proportional circuit

The advantages and disadvantages of inverting amplifier circuits are as follows:

1. For op amps, the voltage at the input is approximately 0V, so there is no common-mode signal input, which significantly improves the performance of the op amp. That's an advantage.

2. For the signal generator V_{G1}, the impedance of the connected "load" is not ∞, but equals R_1, which is a disadvantage.

Non-Inverting Proportional Circuit

A common-emitter amplifier circuit is an inverting amplifier, and an emitter follower circuit is a non-inverting amplifier, but the difference between the two is not merely in polarity. Similarly, the characteristics of inverting proportional circuits and non-inverting proportional circuits formed by op amps are also significantly different.

Theoretical derivation of the non-inverting proportional circuit

The schematic for a non-inverting proportional circuit is shown in **Figure 184**:

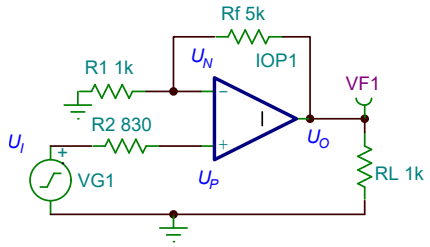


Figure 184. *Non-Inverting Proportional Circuit*

1. Based on the principle of virtual open, there is no current flowing through resistor R_2, so $u_P = u_I$.
2. Based on the principles of virtual short, $u_N = u_P = u_I$.
3. According to Kirchhoff's Law, we can obtain **Equation 92**, whose simplified form, **Equation 93**, defines the relationship between the input and output.

$$\frac{u_O - u_I}{R_F} = \frac{u_I - 0}{R_1} \tag{92}$$

$$u_O = \left(1 + \frac{R_F}{R_1}\right) u_I \tag{93}$$

4. As **Equation 93** indicates, the circuit shown in **Equation 92** is a non-inverting proportional circuit under the conditions where virtual short and virtual open hold true.
5. It is similar to inverting proportional circuits. The values of input resistor R_2 and load resistor R_L have no effect on the amplification factor when an ideal op amp is used. For the same purpose, however, it is also best to set the value of resistor R_2 equal to the parallel combination of R_1 and R_F.

TINA simulation of the non-inverting proportional circuit

Figure 185 shows the transient simulation results of the non-inverting proportional circuit **Equation 93**. The output voltage waveform VM1 indeed exhibits a precise 6x non-inverting amplification relationship with the input voltage waveform VG1 (a 1kHz unit-amplitude sine wave).

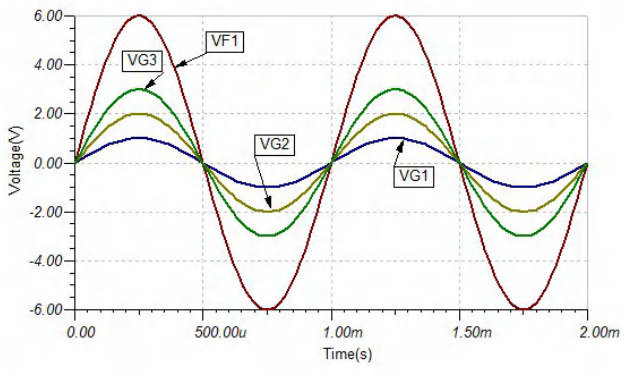
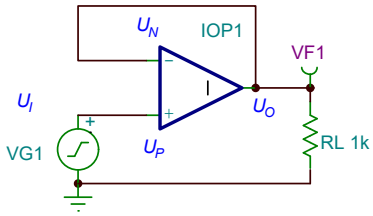


Figure 185. *TINA Simulated Transient Waveforms of the Non-Inverting Proportional Circuit*

Advantages and disadvantages of the non-inverting proportional circuit

The advantages and disadvantages of non-inverting proportional circuits include:

1. For an op amp, the voltages at its two inputs are no longer 0V, thus causing a common-mode signal input, which will degrade the performance of the op amp. This is a disadvantage.
2. For the signal generator V_{G1}, the impedance of the connected "load" is ∞. This is an advantage.
3. For high-impedance signals, using a non-inverting proportional circuit would be a wise choice. The 1x non-inverting proportional circuit shown in **Figure 186** acts as a buffer, similar in function to the emitter follower circuit in a bipolar junction transistor amplifier circuit, which serves to solve problems and enhance performance.



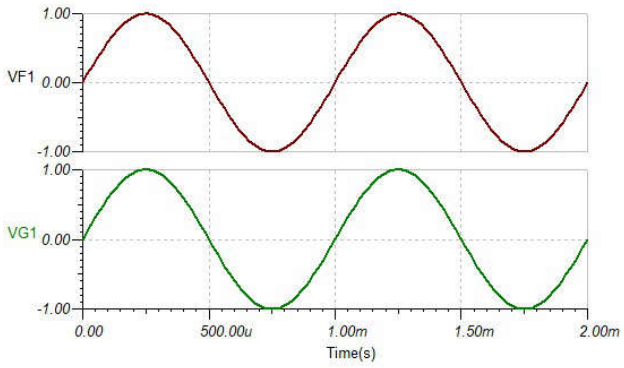


Figure 186. *TINA Simulation of Buffer Circuit*

Non-inverting proportional circuit with a gain less than 1

In non-inverting amplifier circuits, the amplification factor is greater than or equal to 1, as shown in **Figure 185**. So, how can an amplification factor less than 1 be achieved?

1. A common solution is the circuit shown in **Figure 187**, which uses resistors R_2 and R_3 to divide the input voltage before feeding it to the op amp's non-inverting terminal. The voltage division by R_2 and R_3 is accurate and reliable due to a virtual break at the non-inverting input.

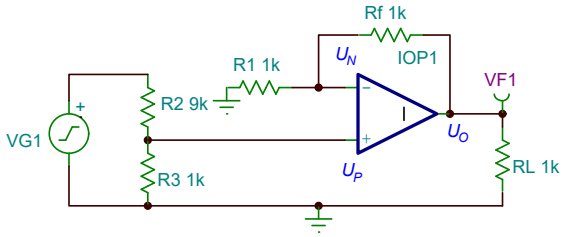


Figure 187. *Non-Inverting Proportional Circuit with a Amplification Factor Less Than 1*

2. **Figure 188** shows the transient simulation results. Based on the resistor values in **Figure 187**, the resistor divider network achieves a 10x attenuation, while the non-inverting proportional op amp circuit achieves a 2x amplification. Therefore, the final result is a 5x attenuation, which is consistent with the simulation results.

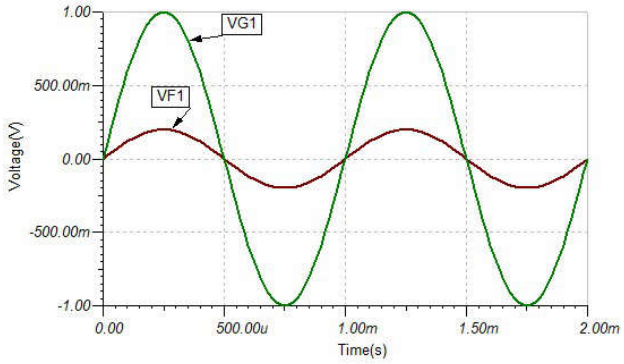


Figure 188. *Transient Simulation of the Non-Inverting Proportional Circuit with a Amplification Factor Less Than 1*

Adder Circuits

In analog signal processing, the need to combine two signals is common. Both non-inverting and inverting proportional circuits, as two basic op amp topologies, can implement addition (summing) operations.

Inverting Proportional Adder Circuit

Let's start with adder circuits based on the inverting proportional circuit. In the inverting proportional adder circuit shown in **Figure 189**:

1. The voltages u_P and u_N are both 0V according to the principles of virtual short and virtual open.
2. It can be derived as follows, according to Kirchhoff's Law:

$$\frac{u_O - u_N}{R_F} = \frac{u_N - u_{I1}}{R_1} + \frac{u_N - u_{I2}}{R_3} + \frac{u_N - u_{I3}}{R_4} \tag{94}$$

3. Substituting the actual resistor values from **Figure 189** into **Equation 94** yields **Equation 95**. As **Equation 95** shows, when the values of series resistors are equal, an inverting adder circuit can be formed for each input signal.

$$u_O = -(u_{I1} + u_{I2} + u_{I3}) \tag{95}$$

4. If the values of R_1, R_3, and R_4 are not equal, then the proportional "weight" of each signal will be altered.

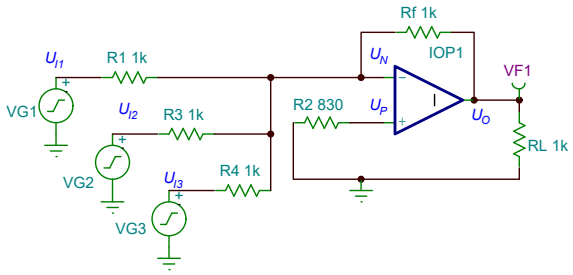


Figure 189. *Inverting Proportional Adder Circuit*

Figure 190 shows the transient simulation results of the inverting proportional adder circuit. The three input signals VG1-VG3 have an amplitude of 1V, 2V, and 3V, respectively, while the output signal VF1 is inverted, with an amplitude of 6V.

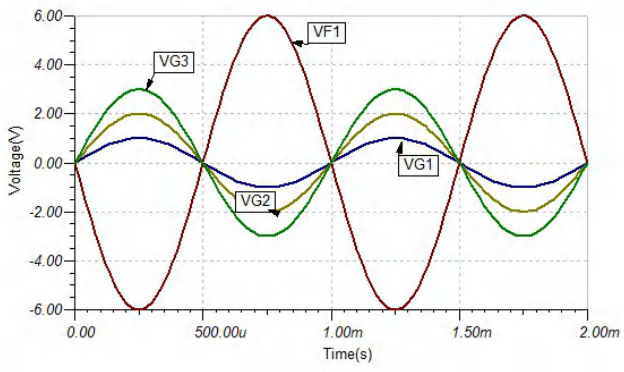


Figure 190. *Transients of the Inverting Proportional Adder Circuit*

Non-inverting proportional adder circuit

A non-inverting proportional circuit can also form an adder circuit. We would naturally design a "non-inverting proportional adder circuit" as shown in **Figure 191**, which should theoretically be feasible.

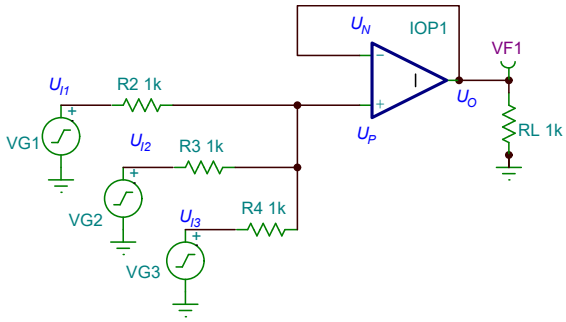


Figure 191. *Non-Inverting Proportional "Adder" Circuit*

Instead of doing calculations, let's run the simulation to check the results. As shown in **Figure 192**, the amplitudes of the three input signals V_{G1}, V_{G2}, and V_{G3} are still 1V, 2V, and 3V, respectively. However, the amplitude of the output voltage V_{F1} is only 2V, which is not scientific.

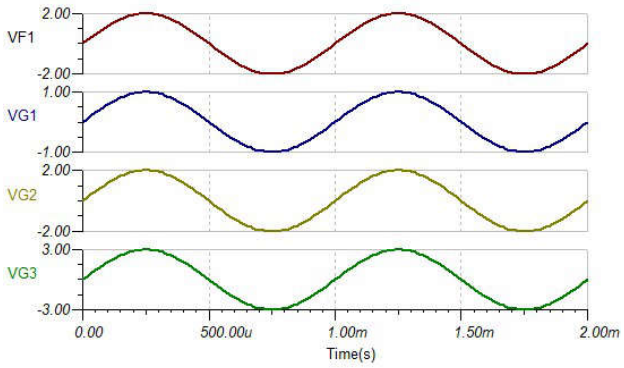


Figure 192. *Non-Inverting Adder Circuit*

Why is the reality different from the assumption? When the op amp input terminal voltage is 0V (GND), each signal can be calculated independently using the superposition principle, as there is no mutual influence between the input signals. However, the input signals of a non-inverting amplifier circuit interact with each other.

The correct analysis method for the circuit shown in **Figure 191** is:

1. Due to the virtual short and virtual open, $u_N = u_P = u_O$.
2. The circuit is equivalent to the one shown in **Figure 193** for calculating the voltage at the center point. The simplest calculation method is to use the superposition principle: Calculate the effects of the three input signals separately and then sum them, resulting in **Equation 96**.

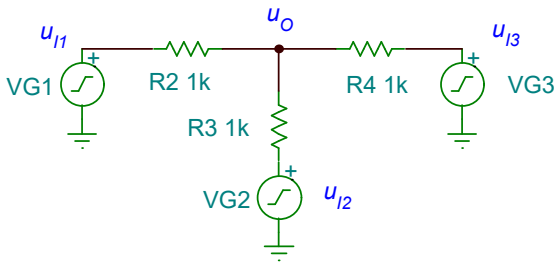


Figure 193. *Non-Inverting Proportional "Adder" Equivalent Circuit*

$$u_O = u_{I1}\frac{R_3//R_4}{R_3//R_4 + R_2} + u_{I2}\frac{R_2//R_4}{R_2//R_4 + R_3} + u_{I3}\frac{R_3//R_2}{R_3//R_2 + R_4} \tag{96}$$

3. When $R_2 = R_3 = R_4$, this equation can be simplified to **Equation 97**, indicating that the circuit shown in **Figure 191** is actually an adder circuit scaled down by a factor of 3.

$$u_O = \frac{1}{3}\left(u_{I1} + u_{I2} + u_{I3}\right) \tag{97}$$

As shown in **Figure 194**, after adding resistors R1 and R5 to achieve a 3x amplification, a 1:1 proportional adder circuit can be constructed, and the simulation results shown in **Figure 195** are also consistent with the logic of the adder circuit.

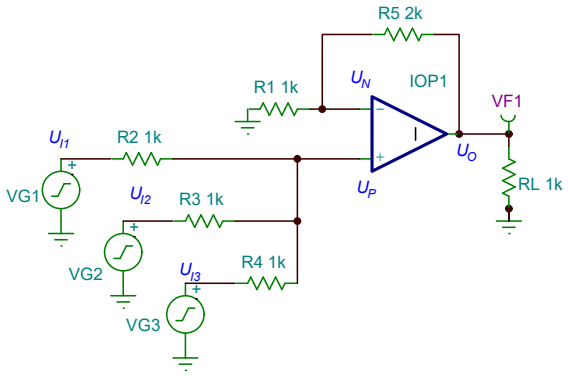


Figure 194. *Improved Non-Inverting Proportional Adder Circuit*

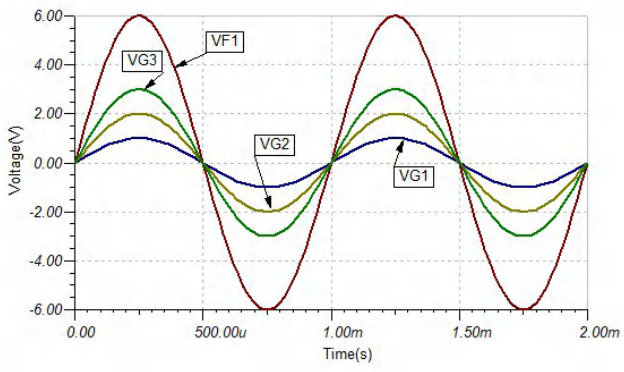


Figure 195. *Transient Simulation of the Non-Inverting Proportional Adder Circuit*

Subtractor Circuit

In real-world applications, it is very common to determine the difference between two analog signals (by subtraction), such as measuring the voltage difference across a resistor to determine the current value. Although the basic characteristic of an op amp is amplification of the difference between its two inputs, a standalone op amp cannot be implemented as a subtractor circuit because even an input difference of only 1mV can cause the op amp output to saturate.

TINA simulation of subtractor circuit

Based on the concept of combining non-inverting and inverting proportional circuits, the most straightforward subtractor circuit is shown in **Figure 196**:

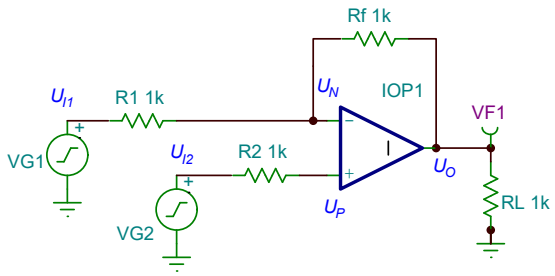


Figure 196. *A Subtractor Circuit*

Let's skip theoretical calculations for now and directly simulate the circuit shown in **Figure 196**, with the results shown in **Figure 197**:

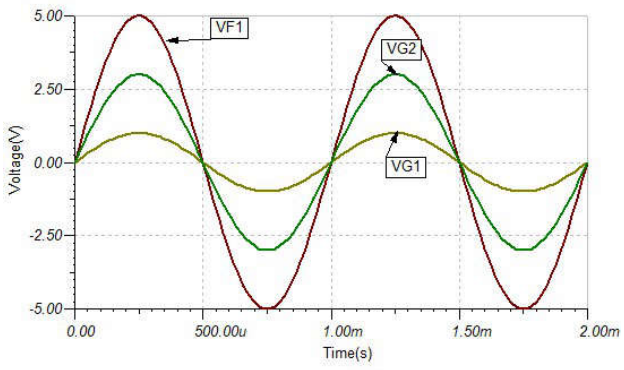


Figure 197. *Transient Simulation of the Subtractor Circuit*

1. The input signals V_{G2} and V_{G1} have amplitudes of 3V and 1V, respectively. According to the subtractor circuit design, the expected output is 2V, but the simulated output V_{M1} has an amplitude of 5V.
2. The cause is that the circuit shown in **Figure 196** provides a –1x amplification for the signal from the inverting input but a +2x amplification for the signal from the non-inverting input. As a result, the circuit voltage actually becomes:

$$u_O = -u_{I1} + 2u_{I2} \tag{98}$$

Improvements in the subtractor circuit

To transform the circuit shown in **Figure 196** into a pure subtractor circuit, it is necessary to individually scale down the non-inverting amplifier part. The modified subtractor circuit is shown in **Figure 198**.

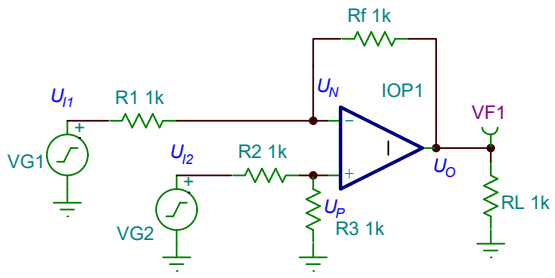


Figure 198. *Subtractor Circuit*

1. Unlike the subtractor circuit shown in **Figure 196**, the subtractor circuit shown in **Figure 198** has a non-inverting input signal that has been pre-attenuated using resistors R_2 and R_3.
2. **Figure 199** shows the transient simulation of the circuit. It is clear that the input voltage V_{G2} has an amplitude of 3V, V_{G1} has an amplitude of 1V, and the output voltage V_{F1} has an amplitude of 2V, all meeting the subtractor circuit requirements.

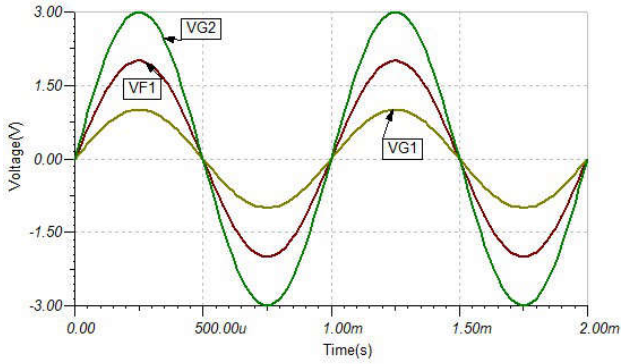


Figure 199. *Transient Simulation of the Subtractor Circuit*

3. Based on the principles of virtual short and virtual open and Kirchhoff's Law, the relationship between the input and output voltages of the circuit shown in **Figure 198** is as follows:

$$u_P = 0.5u_{I2} = u_N = 0.5(u_{I1} + u_O) \tag{99}$$

$$u_O = u_{I2} - u_{I1} \tag{100}$$

Subtractor circuit for DC biasing

It is very common to take advantage of op amps to scale signal amplitudes and control DC offsets.

1. Since most ADCs are unipolar, in ADC sampling applications, it is necessary to positively shift (and possibly scale) bipolar signals to convert them into unipolar signals before feeding them into an ADC for sampling.
2. Most DACs are unipolar. Therefore, if a DAC needs to output bipolar signals, an op amp is required to negatively shift (and possibly scale) unipolar signals to convert them into bipolar signals for output (R-2R type DACs inherently require an op amp connection, so bipolar signal output can be directly achieved).

The circuit shown in **Figure 200** provides a method for shifting signals to be sampled by ADCs.

1. Assuming the ADC reference voltage range is 0-2V and the amplitude of the signal to be measured is 1V, the signal to be measured should be shifted up by 1V.
2. The bipolar signal is input via the inverting terminal, undergoing a –1x amplification. A 0.5V signal is obtained through resistance division and input into the non-inverting terminal of the op amp. Then the feedback network provides a 2x amplification, resulting in a shift by 1V. The relationship between the input and output voltages is expressed as:

$$u_O = 5 \times \frac{1k}{9k + 1k} \times 2 - u_i = 1 - u_i \tag{101}$$

3. Please note that the DC voltage source used for signal shifting must have low internal resistance, so capacitor C2 is essential.

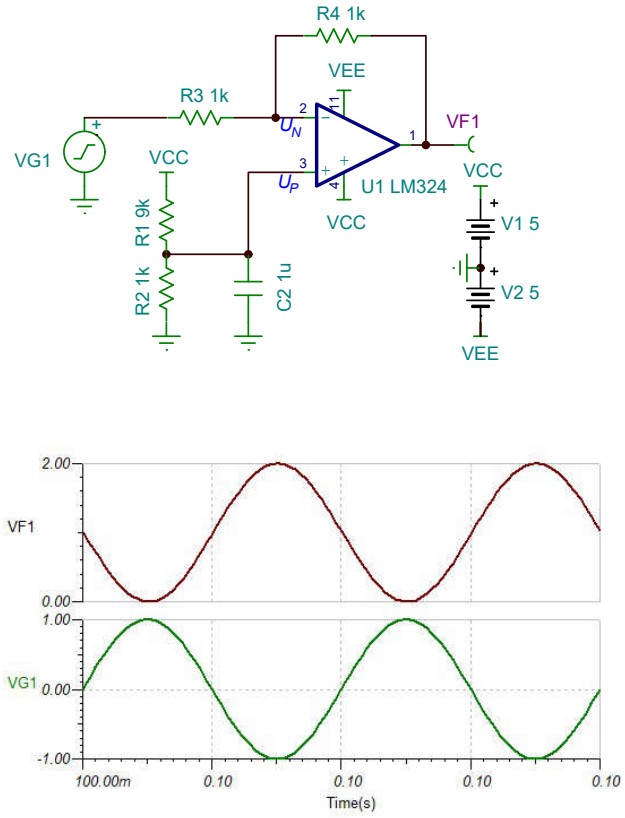


Figure 200. *Positive Level Shifting Circuit*

The circuit shown in **Figure 201** provides a method for achieving a DAC bipolar output using op amps.

1. The DAC signal is input via the non-inverting terminal, and the offset voltage is input via the inverting terminal and is directly sourced by V_{CC}, as the figure shows. It can also be obtained through resistance division. Regardless of the bias voltage origin, a parallel bulk capacitor C_1 is required to reduce the AC impedance.
2. Based on the principle of virtual short, **Equation 102** can be derived. It can be simplified to **Equation 103** as the expression for the output voltage.

$$\frac{VCC - u_I}{R_1} = \frac{u_I - u_O}{R_2} \tag{102}$$

$$u_O = 2u_I - VCC \tag{103}$$

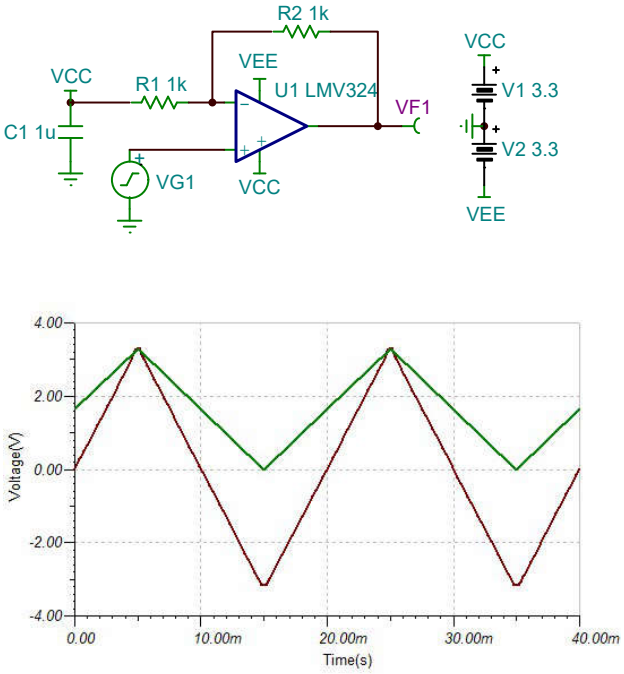
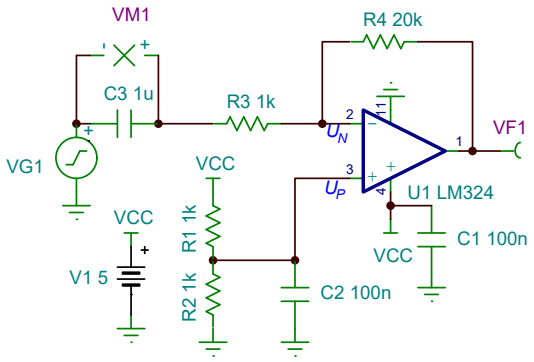


Figure 201. *Negative Level Shifting Circuit*

Improvements in the DC bias circuit

One disadvantage of the DC bias circuits shown in **Figure 200** and **Figure 201** is that the actual bias voltage is related to the gain. Improve the circuit shown in **Figure 200** by connecting the signal generator VG1 in series with capacitor C3, yielding the improved DC bias circuit shown in **Figure 202**. Its DC offset voltage is independent of the gain, and it is often used in single-supply op amp applications.



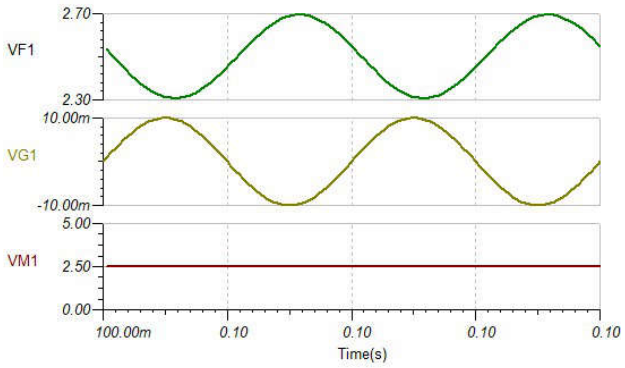


Figure 202. *Fixed DC Bias Circuit*

1. In analog circuits, apart from the capacitors used for timing and oscillation purposes, all other capacitors above 0.1μF act as the "DC batteries" in the circuit. When analyzing this type of circuit, it is important to first figure out the voltage charged to the capacitor.
2. As long as the input signal V_{G1} is regarded as 0V, the voltage of each capacitor as a "DC battery" in a steady state can be determined. The voltage across capacitor C_3, V_{M1}, is equal to $u_N = u_P = 2.5V$.
3. With this C3 voltage value, the input-output voltage relationship can be determined:

$$\frac{u_O - u_N}{R_4} = \frac{u_N - VM1 - u_I}{R_3} \tag{104}$$

$$\frac{u_O - 2.5V}{20k\Omega} = \frac{2.5V - 2.5V - u_I}{1k\Omega} \tag{105}$$

$$u_O = -20u_I + 2.5 \tag{106}$$

Beyond the theoretical calculations in **Equation 104** to **Equation 106**, the results of DC biasing can also be analyzed directly based on the amplification factors of the non-inverting and inverting proportional configurations.

1. In **Figure 202**, the voltage across C_3 (V_{M1}) is equal to the DC voltage u_P at the non-inverting terminal and will be amplified by a factor of $-R_4/R_1$.
2. Meanwhile, the DC voltage u_P at the non-inverting terminal will be amplified by a factor of $1 + R_4/R_1$.
3. Therefore, the final result is that the output voltage is shifted by 1x u_P.

Integrator Circuit

In inverting proportional operation configurations, the op amp's input terminals are virtually grounded, making the circuit's operational relationship relatively simple. Therefore, the following several operational circuits will be designed based on the inverting proportional configuration.

Theoretical derivation for the integrator circuit

Replacing the feedback resistor RF of the inverting proportional circuit with CF forms an op amp integrator circuit. In the op amp integrator circuit shown in **Figure 203**:

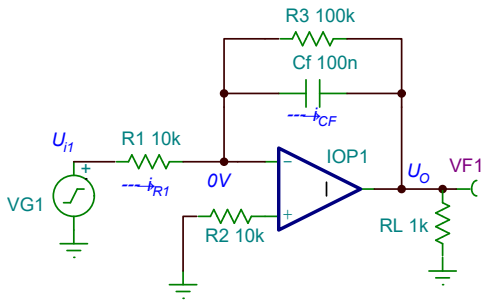


Figure 203. *Op Amp Integrator Circuit*

1. The purpose of R_3 is to prevent saturation caused by the excessive DC gain. In an inverting proportional circuit, the amplification factor is equal to $-Z_F/R_1$. As DC power is applied, without R_3, Z_F would be ∞ (the DC impedance of C_f is infinite), leading to a DC saturation.
2. In the parallel network of R_3 and C_F, R_3 can be ignored as long as the impedance of R_3 is much higher than that of C_F. Therefore, R_3 will not be considered in the subsequent quantitative analysis and calculations.
3. Based on the characteristic that the resistor current i_{R1} is equal to the capacitor current i_{CF}, the input-output voltage expression can be derived:

$$u_O = -u_C = -\frac{1}{C_F}\int i_C dt = -\frac{1}{C_F}\int i_R dt = -\frac{1}{R_1 C_F}\int u_{I1} dt \quad (107)$$

4. **Equation 107** indicates that the circuit shown in **Figure 203** is an inverting proportional op amp integrator circuit.

TINA simulation of the integrator circuit

Figure 204 depicts the transient simulation. The input signal is set to a 1kHz square wave. A square wave input should produce a triangular wave output signal according to the characteristics of integrator circuits.

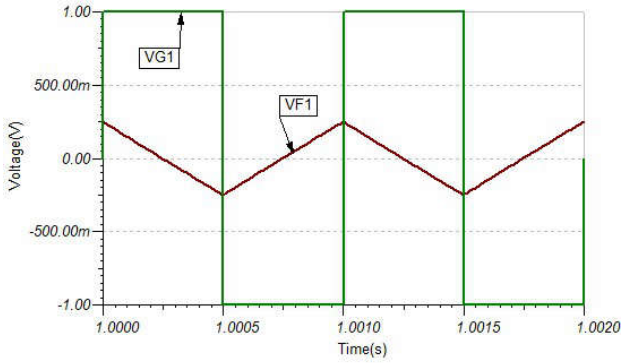


Figure 204. *Transient Simulation of the Op Amp Integrator Circuit*

When running a transient simulation, ensure that the simulation period is set to 1.000s-1.002s (i.e., displaying two cycles after the circuit has run for 1000 cycles) so that the circuit can reach a stable state. Double-click the time axis and set the time resolution to 4 decimal places to observe the changes along the time axis.

Impedance analysis method for the integrator circuit

Next, we'll quantitatively calculate the output amplitude of an integrator circuit through impedance analysis.

1. Any calculation for a circuit containing capacitors and inductors must take the signal frequency into account, as the impedance of these two types of components is dependent on the signal frequency.
2. The square wave shown in **Figure 204** is synthesized from a series of harmonics, which is not easy to explain. Therefore, we will modify the signal to a 1kHz/2V_{PP} sine wave. **Figure 205** shows the simulated waveforms of the integral of the sinusoidal signal.

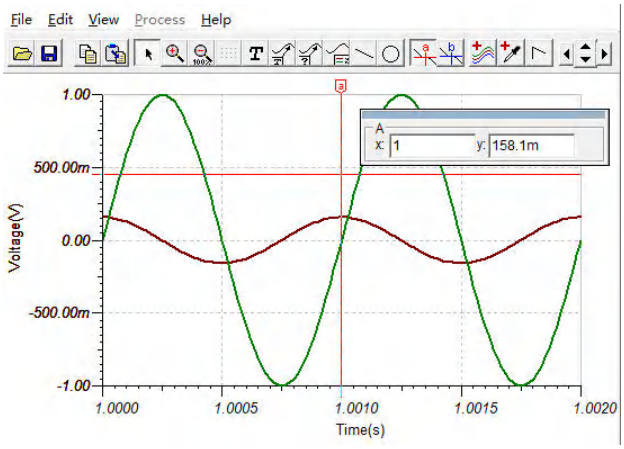


Figure 205. *Quantitative Calculation for the Integrator Circuit*

3. As shown in **Figure 205**, the integral of a sinusoidal signal yields a cosine wave, which aligns with the mathematical rules of integration. For the 1kHz signal, the capacitive reactance of the 100nF feedback capacitor Cf is calculated as:

$$X_C = \frac{1}{\omega C} = \frac{1}{2 \times 3.14 \times 1000 \times 100 \times 10^{-9}} \approx 1.59k\Omega \tag{108}$$

4. According to the inverting proportional circuit design, the voltage amplification factor is:

$$\left|A\right| = \left|\frac{X_C}{R_1}\right| = \frac{1.59k\Omega}{10k\Omega} = 0.159 \tag{109}$$

5. Since the input voltage has a sinusoidal shape with an amplitude of 1V, the output signal should have an amplitude of 159mV according to the quantitative calculation results. This is perfectly consistent with the scale reading of "158.01m" on the simulated waveform shown in **Figure 205**. The difference between them arises from the 100kΩ "anti-saturation" resistor R_3. The actual Z_F should be a parallel combination of R_3 and Z_C.

As the above quantitative calculations show, it is convenient and accurate to analyze circuits containing capacitors and inductors from the perspective of impedance.

Differentiator Circuit

Integration and differentiation, multiplication and division, as well as multiplication and square root extraction, are inverse operations to each other. In op amp circuits, there is a common method for constructing an inverse operational circuit: swapping the series impedance Z1 and the feedback impedance ZF at the inverting input.

Theoretical derivation for the differentiator circuits

As the inverse operation of integrator circuits, a differentiator circuit is constructed by swapping R and C. In the differentiator circuit shown in **Figure 206**:

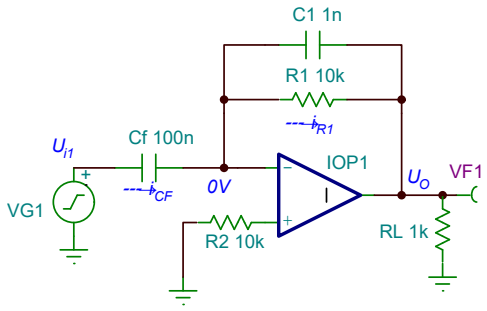


Figure 206. *Op Amp Differentiator Circuit*

1. The purpose of C_1 is to prevent excessive AC gain. This is similar to how integrator circuits prevent excessive DC gain. As long as the impedance of C_1 is much higher than that of R_1, circuit characteristics can be analyzed without considering C_1.
2. Based on the characteristic that the resistor current i_{R1} is equal to the capacitor current i_{CF}, the input-output voltage expression can be derived:

$$i_{CF} = C_F\frac{du_1}{dt} = -\frac{u_o}{R_1} \tag{110}$$

$$u_O = -R_1C_F\frac{du_I}{dt} \tag{111}$$

3. **Equation 110** indicates that the circuit shown in **Equation 111** is an op amp differentiator circuit.

TINA simulation of the differentiator circuit

Figure 207 shows the transient simulation. As the input signal is set to a 1kHz square wave, the output signal should show a waveform with "glitches" due to the characteristics of the differentiator circuit.

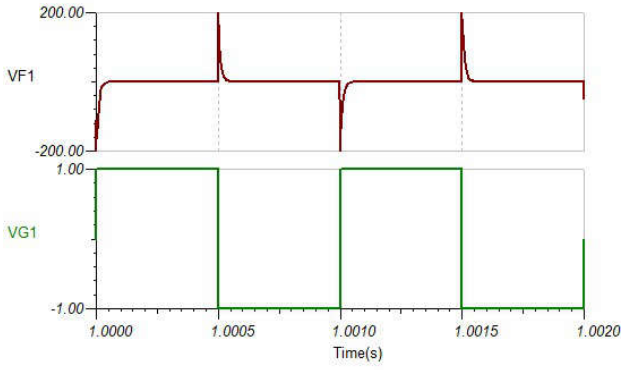


Figure 207. *Transient Simulation of the Op Amp Differentiator Circuit*

Impedance analysis method for the differentiator circuit

Quantitative calculation for the differentiator circuit is also based on the impedance principle.

1. Since the differentiator circuit and the integrator circuit are essentially the configurations with the R and C swapped, their amplification factors are inversely related. Therefore, the amplification factor of the differentiator circuit should be:

$$\left|A\right| = \left|\frac{R_1}{X_C}\right| = \frac{10k\Omega}{1.59k\Omega} = 6.29 \tag{112}$$

2. **Figure 208** depicts simulated waveforms of the differentiator circuit when the input signal is set to a 1kHz/2V_{PP} sine wave. V_{G1} is the input signal with 1V amplitude, and V_{M1} is the output signal. The pointer reads "6.3" for the output voltage V_{F1}, which is perfectly consistent with the theoretical calculation in **Equation 112**.

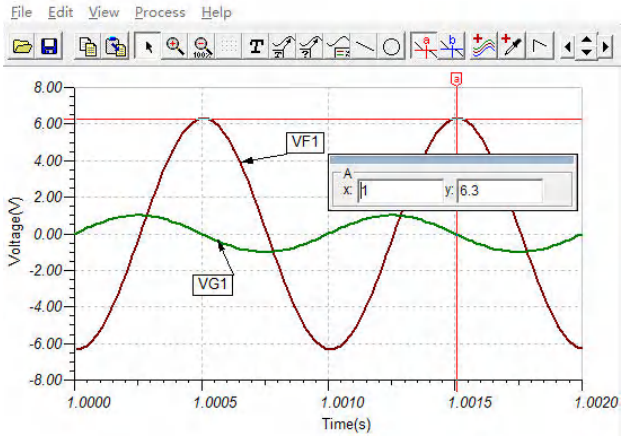


Figure 208. *Quantitative Calculation for the Differentiator Circuit*

Op-Amp PID Circuit

The logarithmic, exponential, and multiplication circuits (analog multipliers), as well as the division, N-th power, and square root circuits derived from analog multipliers, which are covered in analog circuit textbooks, will not be introduced one by one in this book. To conclude our discussion of ideal op-amp circuits, this section introduces the PID circuit, which combines proportional, integral, and derivative actions.

Input-output relationship of PID circuit

The circuit shown in **Figure 209** incorporates the components of three operational circuits: proportional, integrator, and differentiator:

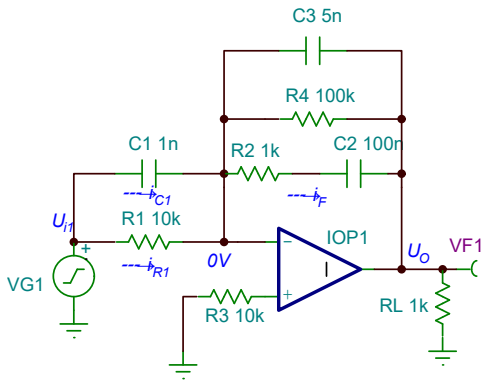


Figure 209. *PID Circuit*

1. The function of C_3 and R_4 is to prevent saturation of the amplification factor for both high-frequency and low-frequency components. These components have previously been employed in the integrator and differentiator circuits. Neglecting these two electronic components does not affect the analysis of the overall circuit.
2. Based on the nodal current theorem of $i_{C1} + i_{R1} = i_F$, the input-output voltage relationship is derived:

   $$u_O = -\left(\frac{R_2}{R_1} + \frac{C_1}{C_2}\right) \cdot u_I - \frac{1}{R_1 C_2} \cdot \int u_I dt - R_2 C_1 \cdot \frac{du_I}{dt}$$

3. In the equation we've just described, $\left(\frac{R_2}{R_1} + \frac{C_1}{C_2}\right)$ is called (Proportion), $\frac{1}{R_1 C_2}$ is called (Integral), $R_2 C_1$ is called (Differential). So **Figure 209** circuit is generally called a PID circuit.

TINA simulation of PID circuit

From the output voltage expression **Figure 205** alone, we cannot discern what makes this circuit exceptional; at this point, circuit simulation becomes essential. **Figure 210** shows the simulated transient waveforms for PID circuit. PID circuit is typically employed for feedback regulation:

1. V_{G1}, as shown in **Figure 210**, represents error input to the circuit for PID operation (square wave represents +1V error in the first half cycle and –1V error in the second half cycle).
2. V_{F1} represents the output of the PID circuit, assuming that the output will affect V_{G1}. In simple terms, an increase in V_{F1} should lead to an increase in V_{G1}. Conversely, a decrease in V_{F1} should lead to a decrease in V_{G1}.

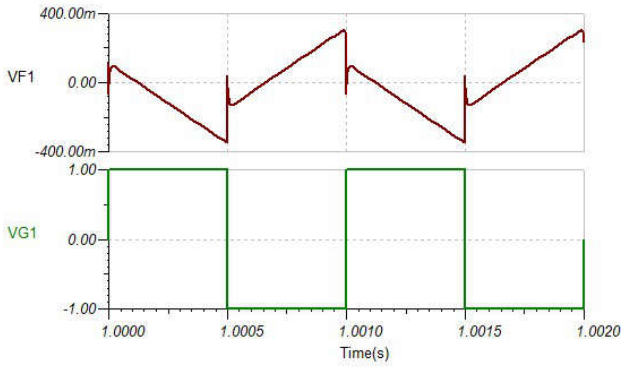


Figure 210. *Transient Simulation of PID Circuit*

Characterization of the PID circuit

Zoom in **Figure 210** simulated waveform details to obtain the waveforms shown in **Figure 211**. Using the analogy of treating illness, our objective is to expect a VG1 error value ideally at 0, signifying no disease.

1. At the time mark of 1.0005s, the error V_{G1} suddenly changes from +1V to –1V (the disease is worsening in the opposite direction). In this case, V_{F1} changes from negative to positive due to the proportional operation mechanism (Commencing treatment with medication, the dosage being proportional to the degree of deviation from health).
2. Meanwhile, as V_{G1} undergoes a "sudden change", V_{F1} creates an additional "spike" that will help the error V_{G1} to return to normal as quickly as possible (a strong dose is administered for a short period due to the abrupt change in condition).
3. In the time ahead, V_{G1} value remains unchanged at –1V while V_{F1} value steadily increases. This is the mechanism of integral adjustment (that is, when "prolonged illness proves ineffective", the dosage must be continually increased).

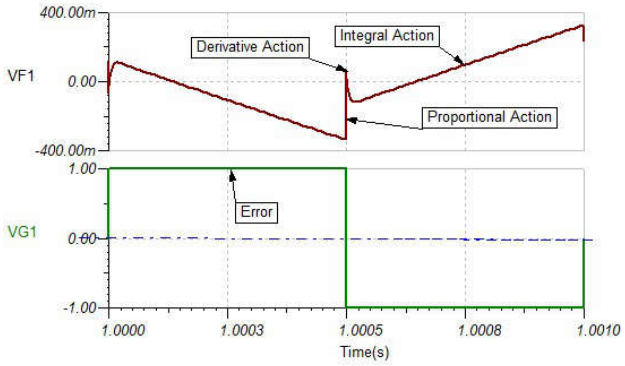


Figure 211. *Detailed Simulated Waveforms of PID Circuit*

The essence of the PID circuit is to build on the "present", bear in mind the "past", and look to the "future":

1. P represents the present. It is responsible for responding to current errors (punishment), and the more serious the mistake, the heavier the penalty. This is common sense. In the feedback, P regulation is always required.
2. I represents the past. The distinction between recidivist and first-time offender is made by taking into account past circumstances and responding to them. To punish repeat offenders, we must, of course, step up the crackdown.
3. D represents the future. This is the mechanism of prevention and control: detecting early warning signs and striking decisively. As the saying goes, without thunderous measures, one cannot demonstrate a compassionate heart.

The proportions of P, I, and D coefficients depend on the specific feedback system. For example, PID coefficients for a temperature control feedback system differ significantly from those for an electric motor speed control system, as their transfer functions are distinct (the same remedy applied to different ailments yields varying efficacy). Configuring appropriate PID parameters can be aided by sophisticated instruments, but more often relies on extensive commissioning experience.

Practical Op Amp Circuits

Ideal op amps idealize many parameters of practical op amps, most of which remain consistent, such as the open-loop gain and common-mode rejection ratio. However, some parameters cannot be idealized in some cases.

The differences between practical op amps and ideal op amps are mainly reflected in the following:

1. Ideal op amps do not account for the chip supply voltage and input/output signal amplitudes; these factors must be considered when we select a practical op amp.
2. Any circuit exhibits a low-pass effect, so practical op amps will have issues with the bandwidth.
3. The assumption of virtual short virtually applies to op amps, but the assumption of virtual open does not necessarily hold true. To deal with high-impedance signals, the input current of the op amp cannot be ignored.
4. Within the op amp product lines, there "lurks" a category of "current-feedback" op amps. They are used quite differently compared to regular "voltage-feedback" op amps.
5. Ideal op amps will not experience self-excited oscillation, but practical op amps may oscillate.
6. Noise is present in any circuit. For high-accuracy applications, the quantitative calculation of noise magnitude in an op amp circuit needs to be considered.

For the first four issues, it is necessary for even beginners to address them; otherwise, it will be nearly impossible to use op amps correctly. As for the issues of op amp oscillation and noise, they can be set aside for now and will be covered in Appendices A and B for later study.

Rail-to-Rail and Op Amp Power Supply

In the context of rail-to-rail, the term "rail" refers to the supply voltage. Rail-to-rail means that the "input" voltage that the device can withstand and the "output" voltage it can generate can reach (or be close to) the supply voltage.

TINA simulation of single-supply op amp comparator

The zero-cross voltage comparator circuit represents a common application where op amp serve as comparators. Most beginners perceive no necessity for dual-supply op-amps, readily yielding the "zero-crossing voltage comparison" circuit depicted in **Figure 212**.

1. The LM324 op amp operates from a single 5V supply.
2. The non-inverting input signal shows a 1kHz/2V_{PP} sine wave, while the inverting input is connected to 0V.

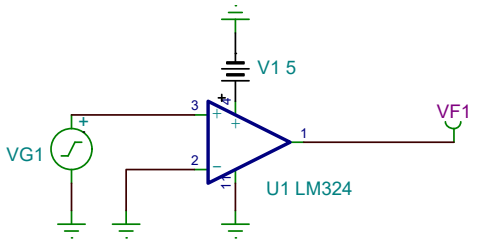


Figure 212. *Zero-Crossing Voltage Comparator Circuit*

For the circuit and input signal shown in **Figure 212**, the desired output should show a square wave (zero-crossing voltage comparison) with a 50% duty cycle and an amplitude of 0-5V. But the actual simulation results are as shown in **Figure 213**:

1. V_{G1} positive half-cycle is normal, but the output voltage is less than 5V, only about 4V.

2. V_{G1} negative half cycle exhibits issues, with the output logic becoming erratic.

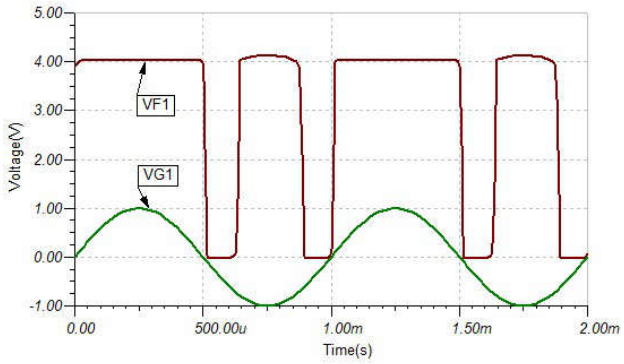


Figure 213. *Transient Simulation of the Zero-Crossing Voltage Comparator Circuit*

As **Figure 212** shows, the circuit error lies in feeding a bipolar signal into a single-supply op amp. The internal circuit of the op amp dictates that:

1. The amplitude of the input signal "should" not exceed the supply voltage (otherwise the op amp cannot process such high-amplitude signals).
2. The amplitude of the output signal "will not" exceed the supply voltage (there is no boost circuit inside the op amp).

TINA simulation of dual-supply op amp comparator

As long as it is a single-supply op amp, it is impossible to input a "bipolar" signal! In fact, only specially designed "rail-to-rail" op amps have inputs/outputs that are "close" to the supply voltage, while other types of op amps maintain a significant difference between their inputs/outputs and the supply voltage.

1. Generally, we will focus on the power rail V_{CC} (V_{EE}) and assume that the input/output signals should not exceed it. However, in a single-supply op amp, GND also acts as a power rail, which should not be exceeded by input/output voltages, either.
2. There are four parameters for practical rail-to-rail op amps, distinguishing between the input and the output, as well as between the positive power rail and the negative power rail, i.e., input rail-to-rail or output rail-to-rail, as well as to reach the positive power rail (V_{CC}) or to reach the negative power rail (GND). According to the simulated waveforms shown in **Figure 213**, the LM324 can only reach the GND power rail at its output.

A correct zero-crossing voltage comparator circuit should be powered by a dual-supply configuration, as shown in **Figure 214**, ensuring that the simulation produces a 50% duty cycle square wave from the zero-crossing voltage comparison.

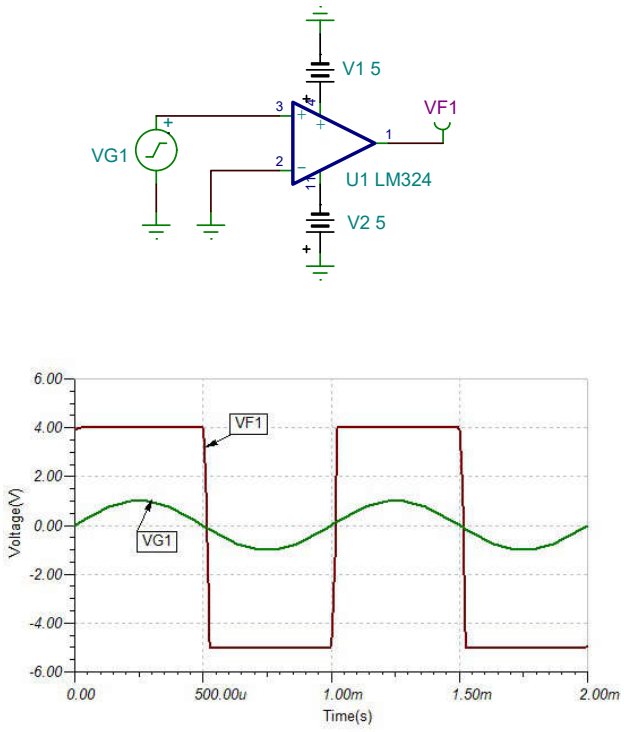
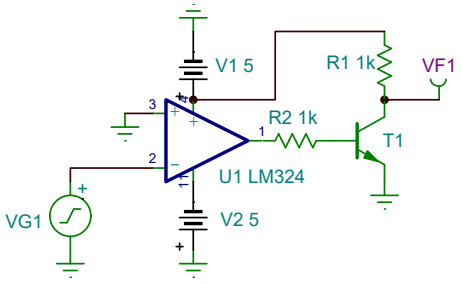


Figure 214. *Correct Zero-Crossing Voltage Comparator Circuit*

Converting an Op Amp's Bipolar Output into Unipolar Output

To be processed by the IO port of a microcontroller unit (MCU), the bipolar square wave signal output by the op amp shown in **Figure 214** needs to be converted into a unipolar square wave signal; otherwise, it will damage the IO port or cause unknown errors.

1. As shown in **Figure 215**, a bipolar junction transistor inverter can be connected afterwards to convert the bipolar square wave signal into a unipolar one. In this case, the op amp's input signals should be swapped to correct the logic of the transistor inverter.
2. The simulation results are more ideal than real-world conditions, achieving a 0-5V square wave output. Actual transistor inverters can only achieve V_{CC} rail output and cannot achieve GND rail output because transistors have a saturation voltage drop (U_{CES}), making it impossible to output 0V.



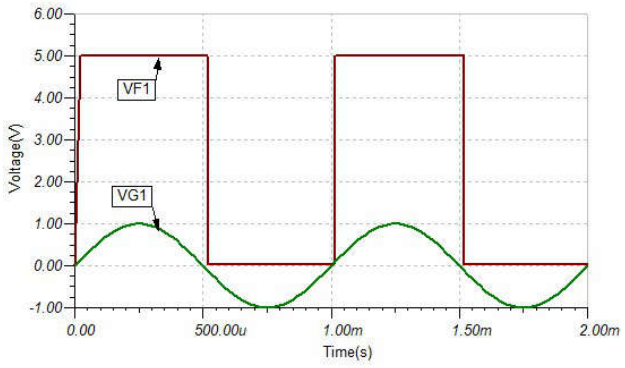


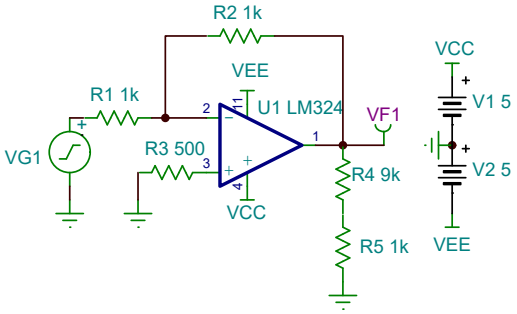
Figure 215. *Improved Zero-Crossing Voltage Comparator Circuit*

Bandwidth and Slew Rate of Op Amps

The bandwidth of an ideal op amp is infinite, ensuring to handle signals of any frequency without limitations. However, the actual bandwidth of op amps is finite, and it will be challenging and costly to increase it.

TINA simulation of op amp bandwidth

Let's begin with a simulated circuit again. **Figure 216** the theoretical amplification factor is –1. With the input signal VG1 at 1kHz, the simulation result (as shown in **Figure 216** on the right) indicates that the output signal VF1 has the same amplitude as the input signal, with a phase difference of 180 degrees.



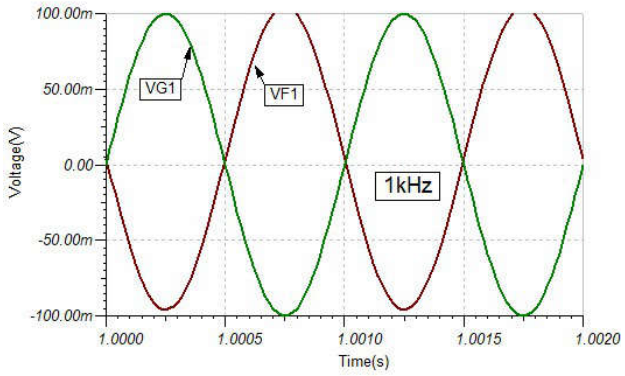


Figure 216. *Inverting Proportional Circuit*

Observe the transient simulation by setting the input signal VG1 shown in **Figure 216** to 100kHz/200mVPP and 1MHz/200mVPP, respectively, with the results shown in **Figure 217**.

1. It is important to set an appropriate display period to ensure the simulated waveform reaches stability (e.g., set to 2 cycles after 1000 cycles of the signal), and to modify the resolution of the time axis for clarity (e.g., 4 decimal places).
2. With the input signal V_{G1} at 100kHz (**Figure 217**), the output V_{F1} has an amplitude that is nearly the same as the input signal, with a slight phase shift.
3. With the input signal V_{G1} at 1MHz (**Figure 217**), the output V_{F1} has an amplitude smaller than that of the input signal and exhibits a significant phase shift.

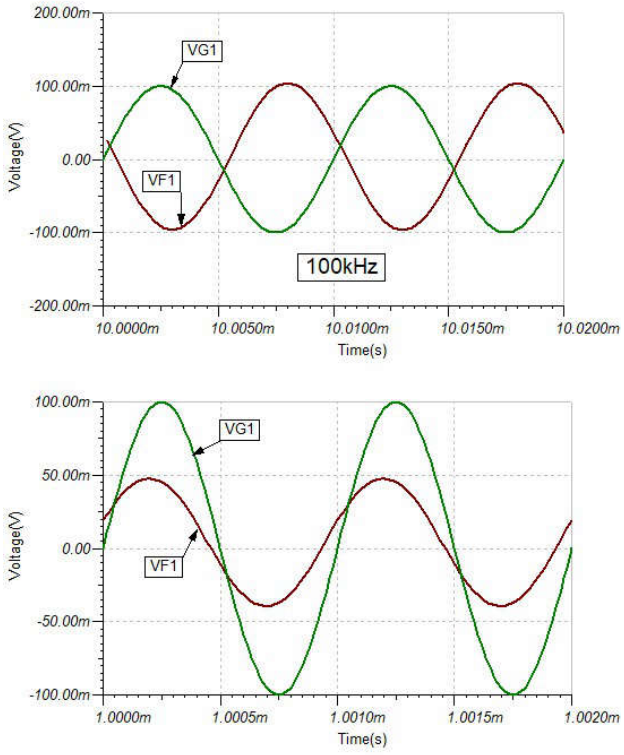
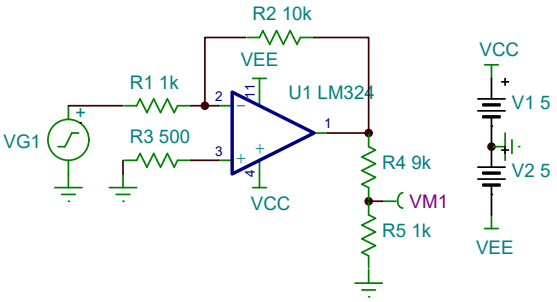


Figure 217. *Simulated Transient Waveforms of the Inverting Proportional Circuit*

Let's examine whether the op amp circuit's gain is bandwidth-dependent. **Figure 218** the amplification factor of the inverting proportional circuit is increased to 10 times. To facilitate comparison with the previous 1x amplifier circuit, resistor dividers R4 and R5 are used in the output part to reduce the gain back to 1x.



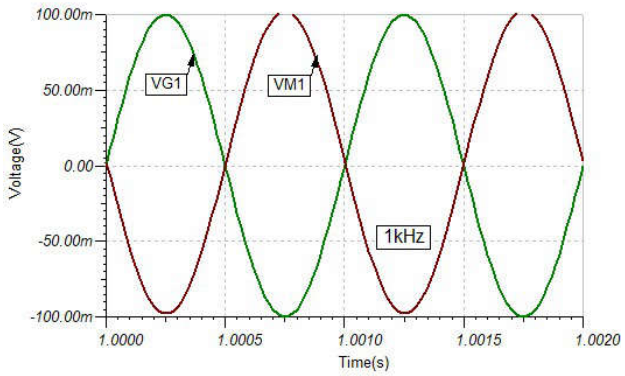


Figure 218. *10x Inverting Amplifier Circuit*

1. At a low frequency of 1kHz (**Figure 218**), the final output V_{M1} has the same amplitude as V_{G1}, with a phase difference of 180 degrees. This result is the same as that observed in the 1x amplifier circuit shown in **Figure 216**.
2. At a low frequency of 100kHz (**Figure 219**), V_{M1} has already been significantly attenuated, and the phase shift is noticeable. However, the 1x amplifier circuit shown in **Figure 216** exhibits little attenuation at 100kHz.
3. At a low frequency of 1MHz (**Figure 219**), V_{M1} has nearly been attenuated to zero.

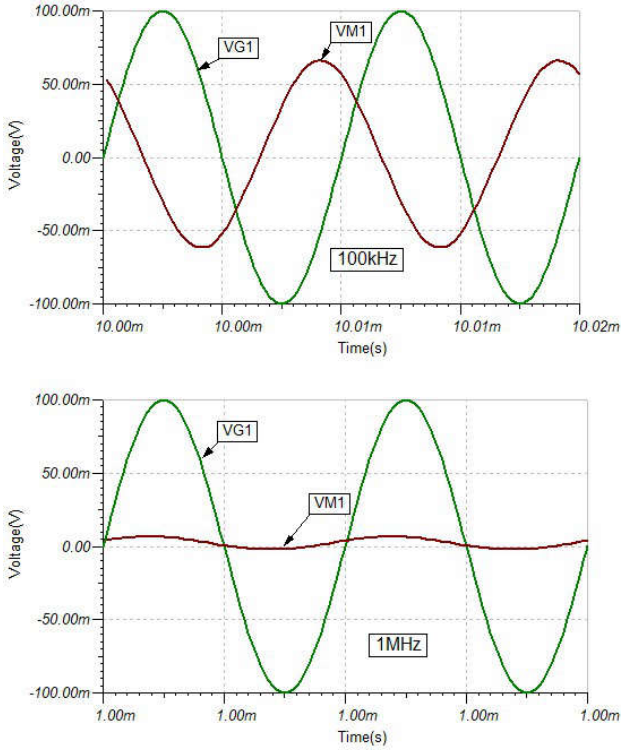


Figure 219. *Transient Simulation of the 10x Inverting Amplifier Circuit*

Simulating the circuit shown in **Figure 218** leads us to the conclusion that the amplification factor can affect the bandwidth. The behavior of the 10x amplifier circuit at 100kHz is similar to that of the 1x amplifier circuit at 1MHz. This leads to the concept of gain-bandwidth product, which states that for an op amp configured in the same type of

amplifier circuit, the product of gain and bandwidth is approximately equal (i.e., the gain-bandwidth product remains constant). In other words, the higher the op amp circuit's amplification factor is, the narrower its bandwidth will be.

TINA simulation of op amp slew rate

Only high-bandwidth op amps can be used to amplify high-frequency signals (otherwise, they will be attenuated to zero prematurely), so they are also called high-speed (high-frequency means high-speed) op amps. Another parameter used to measure the speed of op amps is "slew rate". Bandwidth and slew rate are related specifications for op amps - high-bandwidth op amps will correspondingly have a high slew rate, and vice versa.

1. As shown in **Figure 220**, use the same inverting proportional circuit and select the same signal generator V_{G1}, but replace the op amp with the OPA842 high-speed op amp.

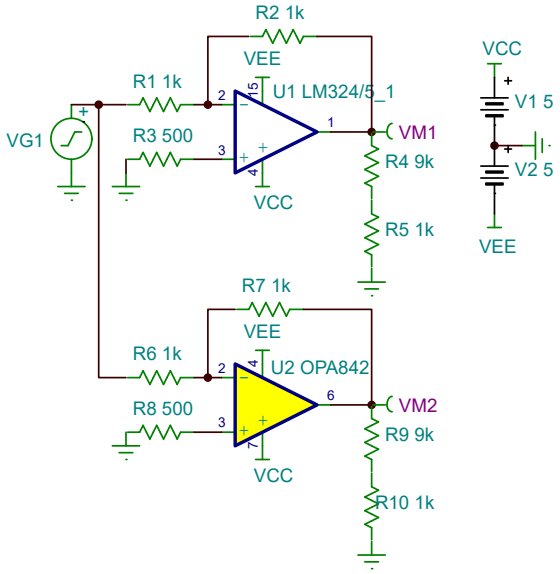


Figure 220. *Circuit for Slew Rate Simulation*

2. **Figure 221** shows the transient simulation (with magnified details). The slew rate (SR) is measured in V/μs, indicating how many volts the output voltage of the op amp can change per microsecond. The OPA842 has a slew rate orders of magnitude higher than the LM324, so the V_{M2} output responds much faster (with a steeper edge) than the V_{M1} output.
3. The typical SR values for the OPA842 and the LM324 can be found in their chip datasheets, being 250V/μs (gain bandwidth GBP of 400MHz) and 0.4V/μs (gain bandwidth GBP of 1.3MHz), respectively. The ratio of gain bandwidth to slew rate follows the same pattern.

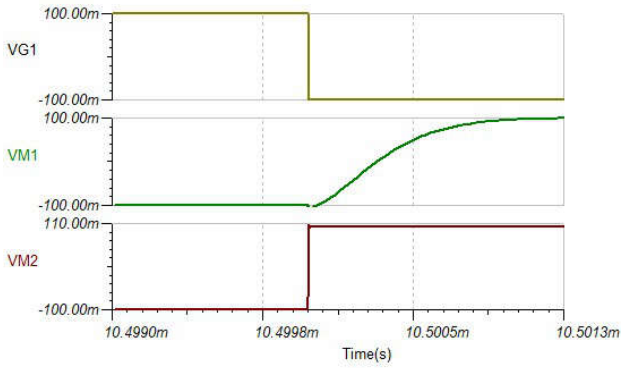


Figure 221. *Simulated Transient Waveforms of Slew Rate*

Why can the slew rate be used to measure the speed (bandwidth) of op amps?

1. The edge of the square wave signal in **Figure 221** is actually composed of very high-frequency components (to be Fourier decomposed). If the edge of the square wave can be magnified, it means that the high-frequency components can be amplified.
2. A typical result is that the output becomes "rounded" when a square wave signal is input into a low-bandwidth amplifier circuit. This can be attributed to insufficient bandwidth or insufficient slew rate.
3. The oscilloscope's probe self-test calibration signal only requires a 1kHz square wave to complete the full-bandwidth compensation setup for the probe. The ability to perfectly reproduce a square wave, regardless of its repetition frequency, contributes to a high-bandwidth circuit (device).

Input Impedance and Bias Current

Before moving on to the input impedance and bias current parameters of practical op amps, let's first examine the simulated circuit shown in **Figure 222**. **Figure 222** shows an attenuator and isolator circuit commonly used as the first stage in an oscilloscope's signal conditioning circuit.

1. The values of resistor dividers R_1 and R_2 used for attenuation must be sufficiently large to ensure the oscilloscope probe's input impedance is sufficiently high (as not to affect the circuit under test).
2. The buffer circuit used for isolation is constructed from a non-inverting proportional circuit to ensure that the divider ratio of the resistor dividers is not affected.
3. Any signal conditioning circuit will reduce the system bandwidth. Therefore, a high-speed op amp, such as the OPA842, is chosen to minimize the impact on the bandwidth.

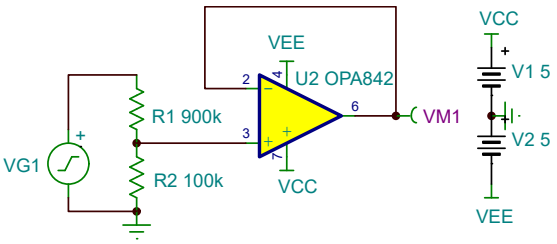


Figure 222. *Attenuator and Isolator Circuit*

The input signal for the circuit shown in **Figure 222** is chosen as a 1kHz/2VPP sine wave. Normally, the op amp output should be a 1kHz/200mVPP sinusoidal pure AC, but the transient simulation results, as shown in **Figure 223**, indicate that:

1. The output signal V_{M1} deviates significantly from 0V. After the curve is separated, the pointer tool can be used to determine the DC offset of V_{M1} as:

$$\overline{V_{M1}} = \frac{(-1.66)+(-1.85)}{2} = -1.775\text{V} \tag{113}$$

2. The pointer tool directly reads the peak-to-peak value of V_{M1} as 190.85mV, which is also slightly less than the theoretical value. The theoretical value should be 200mV peak-to-peak (twice the amplitude) for a 1V amplitude signal attenuated by a factor of 10.

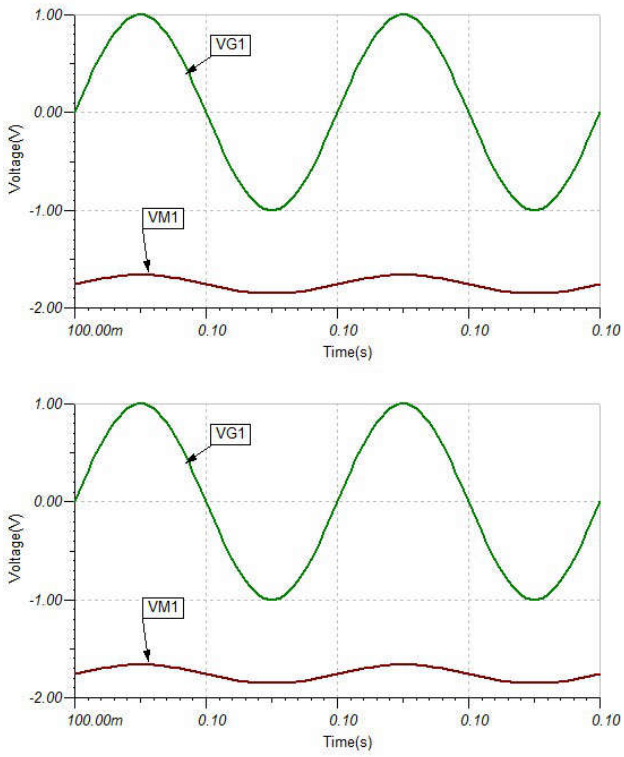


Figure 223. *Transient Simulation of the Attenuator and Isolator Circuit*

Before explaining the simulation results, let's consult the OPA842 datasheet. An excerpt from the table "ELECTRICAL CHARACTERISTICS: V = ±5V" is shown in **Figure 224**:

PARAMETER	CONDITIONS	OPA842ID, OPA842IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 1)								
Slew Rate	2V Step	400	300	250	225	V/µs	min	B
DC PERFORMANCE[4]								
Input Bias Current	V_{CM} = 0V	–20	–35	–36	–37	µA	max	A
INPUT								
Common-Mode Rejection (CMRR)	V_{CM} = ±1V, Input Referred	95	85	84	82	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0V	.14 || 1				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	3.1 || 1.2				MΩ || pF	typ	C

Figure 224. *Excerpt from the Table "Electrical Characteristics: V = ±5V" for the OPA842*

1. In the AC PERFORMANCE column, we can find that the typical value of the previously mentioned Slew Rate is 400V/μs, and the worst-case value is 225V/μs. Leading manufacturers often demonstrate their professionalism by including limit values in their datasheets, while small-scale chip makers always only provide typical values, but no limit values.
2. The DC PERFORMANCE column shows that the typical value of the input bias current is –20μA. The input bias current means that the transistor needs to be "pre-biased" even if no AC signal is applied; this is the function of the bias circuit. Ideally, the input bias current should be minimized; otherwise, the op amp may not be considered to have a virtual open condition. In general, the input bias current through a BJT-input op amp is on the order of microamps, while that through a FET-input op amp is in the range from picoamps to nanoamps.
3. The common-mode rejection ratio (CMRR) mentioned earlier can be found in the INPUT column. The OPA842 has a typical CMRR of 95dB. This means that the op amp's ability to amplify differential-mode signals is 560,000 ($10^{95/20}$) times its ability to amplify common-mode signals. A differential-mode signal is defined as the difference between the two input signals of an op amp, and a common-mode signal is defined as their average.
4. In the INPUT column, parameters for the Input Impedance can also be found. Input impedance includes input resistance and input capacitance. In general, the input impedance of a BJT-input op amp is on the order of megaohms, while that of a FET-input op amp is on the order of gigaohms.

The simulation anomalies shown in **Figure 225** can be attributed to the input bias current and input impedance.

1. The OPA842's input bias current has a typical value of –20μA. Although seemingly small, this current flowing through the 100kΩ resistor R_2 generates a voltage of –2V. This is the actual voltage at the op amp's non-inverting input when there is no signal input. The simulation result is –1.775V, which is basically consistent.
2. The OPA842's input impedance is on the order of megaohms. When connected in parallel with the 100kΩ resistor R_2, it will affect the combined resistance value. Therefore, the resistor divider ratio will be slightly lower than 1:10.

For applications such as the first-stage signal conditioning in an oscilloscope, the isolation op amp must be a high-speed FET-input type, such as the OPA659, as shown in **Figure 225**. The simulation results, as shown in **Figure 226**, perfectly satisfy all performance indicators.

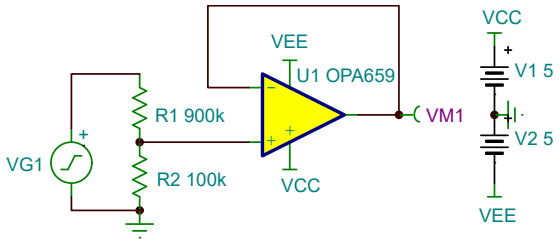


Figure 225. *Attenuator and Buffer Circuit Using a High-Speed FET-Input Op Amp Instead*

1. According to the OPA659 datasheet, the input bias current varies with temperature, ranging from an optimal ±10pA to a worst-case 3200pA. As a result, the bias voltage generated at this op amp's inputs is at least 10,000 times lower than that generated at the OPA842's inputs. Therefore, it can be ignored.

2. The input impedance of the OPA659 is also extremely high, with a typical value of $10^{12}\Omega$ in the datasheet, so its impact when connected in parallel with R_2 is negligible as well. The simulation results also confirm this, with the output voltage peak-to-peak value reaching 199.75mV.
3. Are FET-input op amps always better than BJT-input op amps? The price difference between the OPA842 and OPA659 is not significant. However, there is a trade-off. The OPA659 has a larger input offset voltage than the OPA842, which means that FET-input op amps are inferior to BJT-input op amps in terms of DC characteristics. Moreover, the OPA659's typical CMRR is only 70dB, which is also worse than the OPA842's.

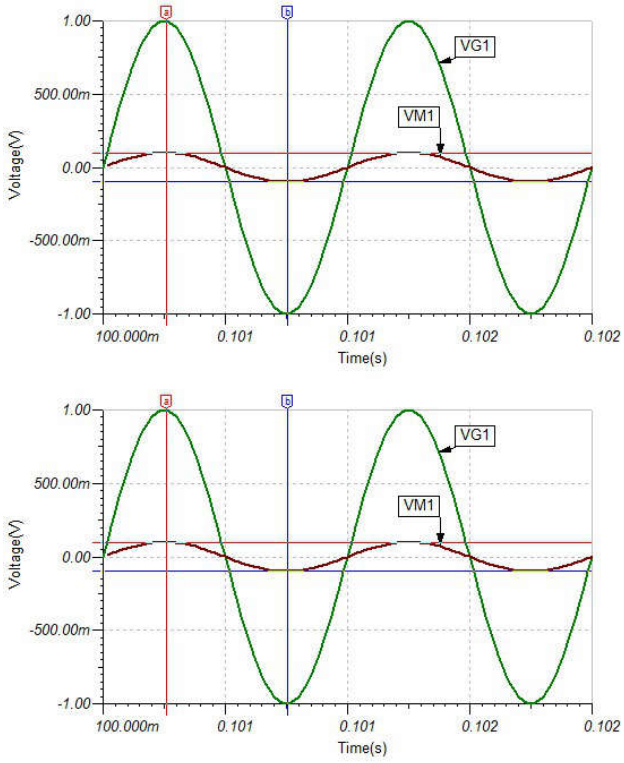


Figure 226. *Transient Simulation of the Attenuator and Buffer Circuit with High-Speed FET-Input Op Amp*

Offset Voltage and Zero-Drift Amplifiers

Input offset voltage was mentioned in the previous section, and its significance will be explained in this section. If the op amp inputs are short-circuited (e.g., being grounded), the output should theoretically be 0V, but the actual output is not 0. Gradually adjust the input voltages until the output is exactly zero when the input voltage difference reaches VOFFSET. This voltage VOFFSET is referred to as the input offset voltage. The offset current has a similar definition and describes the same phenomenon. Both offset voltage and offset current are essentially caused by op amp drift; they are merely definitions artificially used to quantify the extent of drift.

While the offset voltage is clearly defined, we still don't understand what this parameter indicates. The simulation shown in **Figure 227** can help us understand the significance of offset voltage in op amp applications.

1. Both op amps are configured for 1000x amplification, and they share the same signal generator. Given an actual input of a 1mV step signal, the output voltage should be 1V DC voltage.
2. The OPA659 is a high-speed amplifier, and the LMP2021 is a zero-drift precision amplifier.

3. The simulation results shown in **Figure 228** reveal that the output of the LMP2021 is precisely 1V, while the output of the OPA659 is around 1.3V (which might be worse in practical applications), which is the effect of drift.
4. Regular amplifiers typically use an external zeroing circuit for drift compensation, whereas zero-drift amplifiers employ an internal self-calibration circuit to achieve this function. Zero drift not only indicates extremely small input offset voltage, but also a much lower temperature drift compared to regular op amps.
5. By further examining the simulation shown in **Figure 228**, we can find that the OPA659 high-speed amplifier has a much higher slew rate (SR) than the LMP2021, which allows the voltage to settle so quickly. This is why this type of op amp is described as "high-speed".

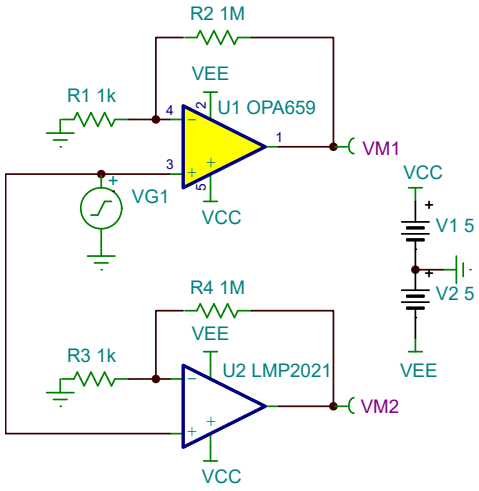


Figure 227. *Simulation of Offset Voltage Circuit*

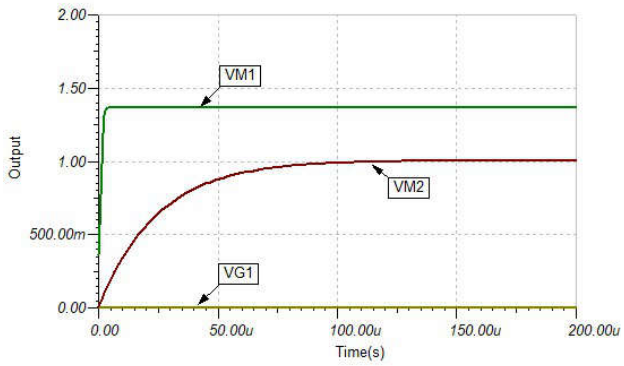


Figure 228. *Transient Simulation of the Offset Voltage Circuit*

Current Feedback Operational Amplifier

To date, all op amps discussed in this text, including their internal construction principles, have referred to voltage feedback (VFB) op amps. In fact, there is another major category of specially structured current feedback (CFB) op amps. In principle, they are not constrained by the gain-bandwidth product (GBW) and are specifically designed for high-speed amplification applications. GBW theory for both amplifier types can be independently researched online.

Compared to VFB, CFB op amps require certain special considerations during use. These may be noted for future reference; when issues arise, specific solutions can then be sought:

1. The fundamental op amp equations for CFB op amps remain identical to those for VFB op amps.
2. The non-inverting and inverting terminals of the CFB op amp exhibit asymmetrical circuit structures, with the inverting input exhibiting comparatively lower impedance. For instance, the OPA691 features a non-inverting input impedance of 100kΩ, whereas the inverting input impedance is merely 35Ω. Because the input structure is asymmetrical, the input resistance does not need to be matched.
3. In a CFB op amp circuit, the feedback capacitor C_F is strictly prohibited as it induces severe oscillation. Consequently, CFB op amp cannot act as an integrator nor eliminate oscillation via C_F as VFB op amp does.
4. The CFB op amp performance and stability are closely related to R_F, whose value should be taken in accordance with the chip datasheet. Reducing R_F gives more bandwidth, but excessively low R_F may oscillate. Similarly, CFB op amp cannot be used as a buffer (R_F = 0).

Special Op Amps

An op amp alone cannot achieve amplification; an amplifier circuit also requires external resistors, capacitors, or other components. Integrating these external components with the op amp can simplify applications or improve performance, thus forming some special amplifiers. Several types of special amplifiers will be introduced in this section.

Differential amplifier

A differential amplifier can directly form a subtractor circuit without requiring external resistors, amplifying the difference between two signals by a specific factor. In this **Figure 184** section, we introduced the subtractor circuit formed by the op amp with the resistor. In the circuit shown in **Equation 114**:

1. Based on the principles of virtual short and superposition, the relationship between input and output voltages is listed as follows:

$$u_{I2}\frac{R_3}{R_2+R_3}=u_{I1}\frac{R_F}{R_1+R_F}+u_O\frac{R_1}{R_1+R_F} \tag{114}$$

2. When the relationship $R_1 \times R_3 = R_2 \times R_F$ is precisely established, the relationship of the output voltage can be simplified to **Figure 230**, and output voltage is 1V.

$$u_O=\frac{R_F}{R_1}\left(u_{I2}-u_{I1}\right)=100\left(u_{I2}-u_{I1}\right)=100\times 0.01=1 \tag{115}$$

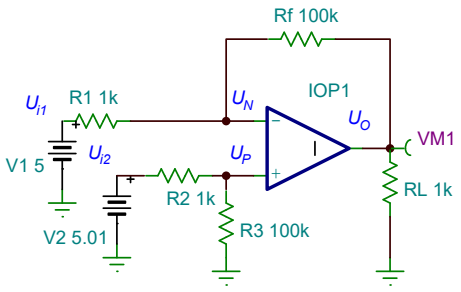


Figure 229. *Subtractor Circuit*

3. The resistance is accurate, and $R_1 \times R_3 = R_2 \times R_F$ is difficult to hold precisely. Assuming that all other resistor values are fully accurate and only resistor R_1 is 5% accurate, the phenomenon can be observed by simulation of the DC transfer characteristics.
4. **Figure 230** shows the DC characteristic simulation of a resistor R_1 set at 950Ω to 1050Ω. The output voltage is no longer constant at 1V, approximately between 800mV and 1.2V.

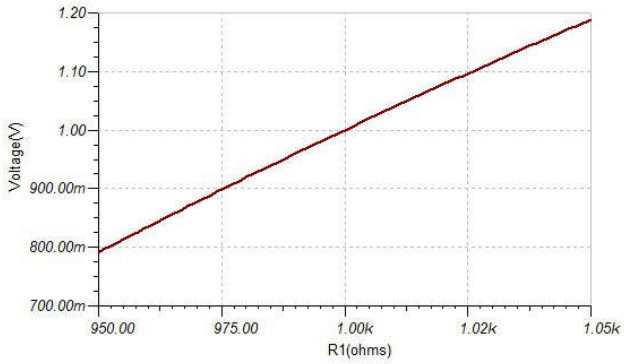
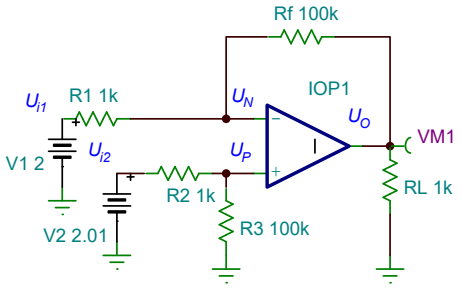


Figure 230. *DC Transfer Characteristic Simulation of the Subtractor Circuit*

5. As shown in **Figure 231**, altering the common-mode voltage of the input signal (from 5.005V to approximately 2.005V) while maintaining the differential-mode input signal at 0.01V causes the DC transfer characteristic simulation to change. This time, the output voltage range fluctuates between approximately 950mV and 1.05V.



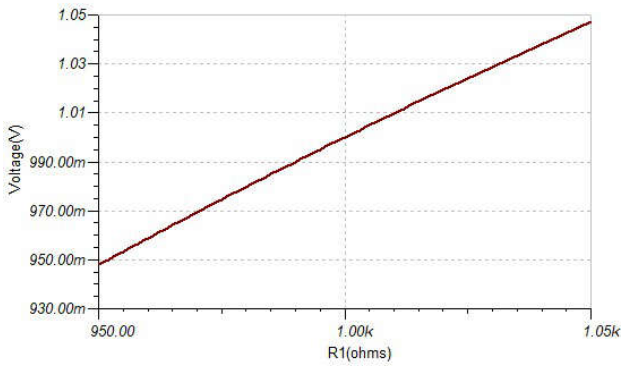


Figure 231. *DC Transfer Characteristic Simulation When Varying the Common-Mode Input Voltage*

6. By comparing **Figure 230** with **Equation 116**, it demonstrates that the subtractor circuit not only amplifies the differential-mode signal, but also the common-mode signal. And what we're simulating is the ideal op amp, that is, an inherent CMRR of the op amp is ∞. The arrangement of **Figure 229** can lead to **Equation 116**, that is, the output signal is not proportional to the difference in the input signal under normal circumstances ($R_1 \times R_3 = R_2 \times R_F$ is not satisfied).

$$u_O = u_{I2}\frac{R_3}{R_2 + R_3} \cdot \left(\frac{R_1 + R_F}{R_1}\right) - u_{I1}\frac{R_F}{R_1} \tag{116}$$

7. In the subtractor circuit constructed from ideal op amps, shown in **Equation 116**, an error of 0.1% in any single resistor reduces the total CMRR to 66dB. Should the resistor error reach 1%, the total CMRR drops to 46dB.

Differential amplifiers integrate 4 resistors of the subtractor circuit within the op amp itself, employing techniques such as laser trimming to achieve extremely high precision in resistance values.

1. The schematic for the INA143 differential amplifier is illustrated in **Figure 232**. The INA143 integrates 4 resistors internally, forming a 10× amplification option.
2. As the resistor structure is symmetrical, it can be configured as either a 10× differential amplifier or a 0.1× differential amplifier. Naturally, we cannot simply add external resistors to achieve other amplification factors, lest we end up with the effect of mixing red wine with fizzy drinks.

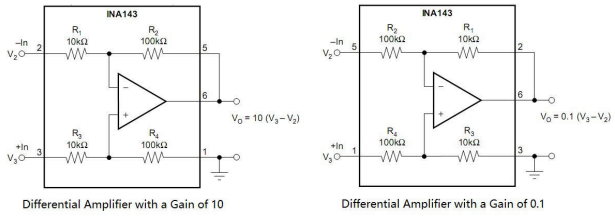


Figure 232. *Two Methods of Connecting with Differential Amplifiers*

Particular attention must be paid to ensuring that the input signal to the differential amplifier is of low impedance, as the impedance of the signal generator is entirely equivalent to that of the resistors integrated within the differential amplifier itself. **Figure 233** makes it easy to understand the effect of a high-impedance signal on a differential circuit.

1. While R_1 is accurate, the internal resistance of the input signal, R_5, is no different from R_1 and is equivalent to the accuracy error of R_1.

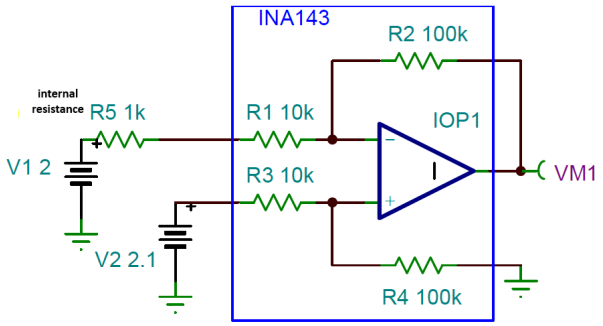


Figure 233. *Impact of the Impedance of the Signal Generator on the Differential Amplifier Circuit*

2. The simulation shown in **Figure 234** illustrates the impact of high-impedance signals on differential circuits. If the impedance of the signal generator reaches 1kΩ, it will affect approximately 8% of the output voltage. If the impedance is 10Ω, the effect will be less than 1‰ of the output voltage.

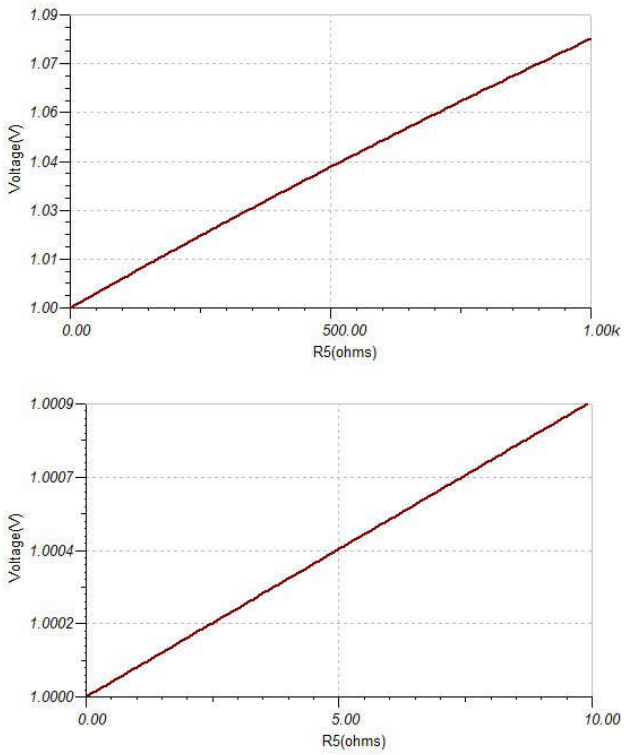


Figure 234. *Effects of Different Impedance of Signals on Differential Circuits*

Instrumentation Amplifier

As mentioned earlier, differential amplifiers cannot handle high-impedance signals, and their amplification factors are also limited.

1. The basic approach to improving a differential amplifier's inability to handle high-impedance signals is to isolate the input terminals with a buffer, as shown in **Figure 235**.

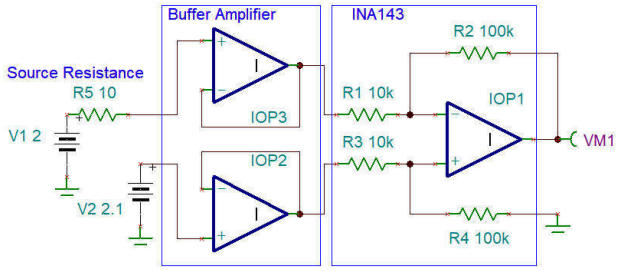


Figure 235. *Differential Amplifier Circuit with Input Buffer*

2. Simulate the circuit shown in **Figure 235**, varying the value of the internal resistance R_5 of the signal generator from 0Ω to 10kΩ, to observe the DC transfer characteristics. The waveform is shown in **Figure 236**. The result indicates that the buffer perfectly resolves issues with input and output impedances and functions in the circuit to "solve problems and enhance performance".

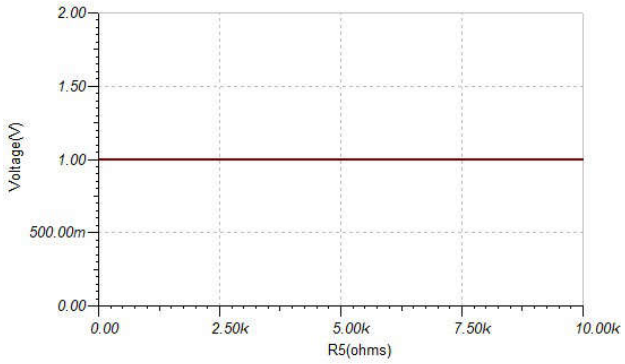


Figure 236. *DC Transfer Characteristic Simulation of the Differential Amplifier with Input Buffer*

The approach to resolving issues with the voltage amplification factor of the differential amplifier can also rely on a buffer.

1. If amplification is done at the buffer stage (in a non-inverting proportional circuit), the circuit shown in **Figure 235** can be modified to that shown in **Figure 237**. R_6, R_7, R_8, and R_9 are added to change the amplification factor of the circuit. Its amplification factor is given by:

$$u_O = \left(1 + \frac{R_6}{R_8}\right)\left(V_2 - V_1\right) \tag{117}$$

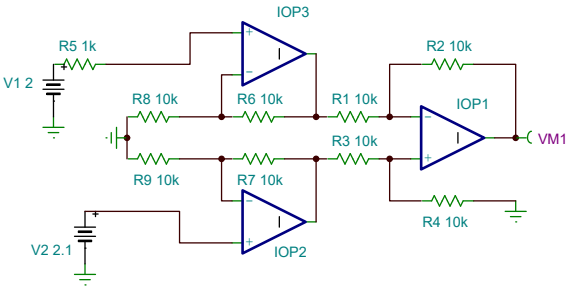


Figure 237. *Non-Inverting Proportional Operation-Based Differential Amplifier Circuit with Isolated Inputs*

2. Furthermore, due to the circuit's symmetry, the grounding between R_8 and R_9 can be omitted, and R_8 and R_9 can be combined into a single resistor R_G, thus forming the well-known instrumentation amplifier circuit. The optimized circuit is shown in **Figure 238**. Its amplification factor is given by:

$$u_O = \left(1 + \frac{R_6}{\frac{R_G}{2}}\right)\left(V_2 - V_1\right) = \left(1 + \frac{2R_6}{R_G}\right)\left(V_2 - V_1\right) \tag{118}$$

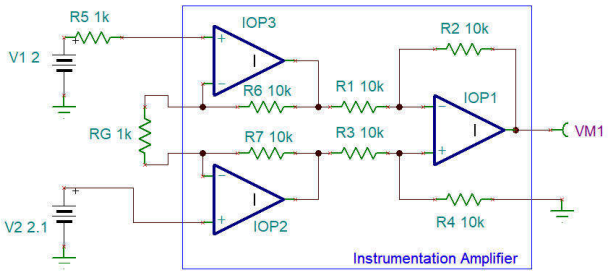


Figure 238. *Three-Op-Amp Instrumentation Amplifier Circuit*

3. **Equation 118** shows that if all resistors other than R_G are integrated inside the chip, the amplification factor of the circuit can be adjusted by altering the value of R_G, without compromising the characteristics of the subtractor (differential) circuit (due to the extremely high accuracy of the integrated resistors).

Figure 239 shows the schematic for the three-op-amp instrumentation amplifiers INA128 and INA129. An amplification factor can be derived from **Equation 118**:

$$u_O = \left(1 + \frac{2R_6}{R_G}\right)\left(V2 - V1\right) = \left(1 + \frac{2 \times 25k\Omega}{R_G}\right)\left(V_{IN}^{+} - V_{IN}^{-}\right) \tag{119}$$

$$G = \frac{u_O}{V_{IN}^{+} - V_{IN}^{-}} = 1 + \frac{50k\Omega}{R_G} \tag{120}$$

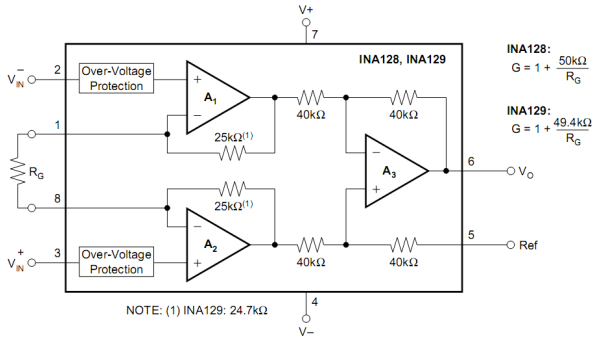


Figure 239. *INA12x Series of Instrumentation Amplifier*

Instrumentation amplifiers address two drawbacks of differential amplifiers - insufficiently high input impedance and a non-adjustable amplification factor - but simultaneously eliminate one of their advantages: the ability to handle significantly higher input signal voltages compared to op amps.

1. For the circuit shown in **Figure 240**, the actual input differential voltages are 100V and 120V. It is extremely challenging to find an op amp with such a high supply voltage. Therefore, there are obviously no suitable instrumentation amplifiers that can handle these high voltages.
2. This issue can be solved using a differential amplifier, where the voltage has dropped to about 9V when the actual signal reaches the input terminal of OP_1 in the differential amplifier. The simulation results verify this conclusion, with an output voltage of –2V.

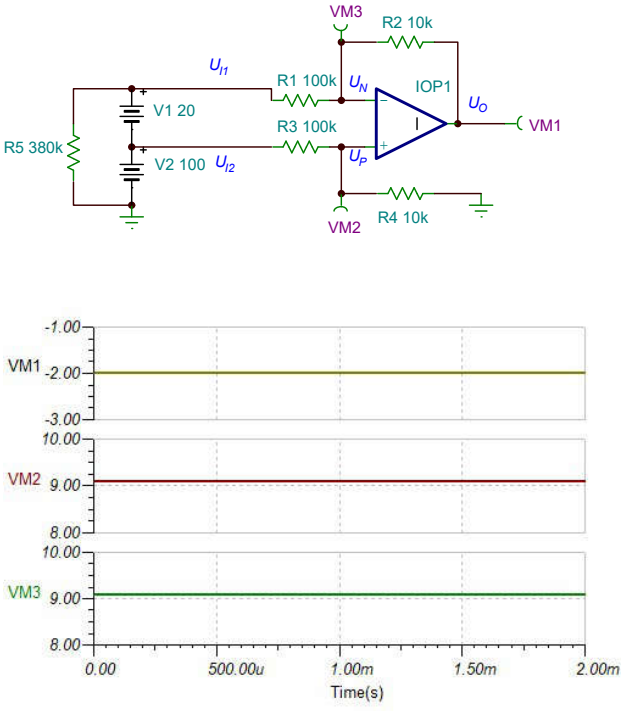


Figure 240. *Differential Amplifier for High-Voltage Sensing*

Current Sense Amplifier

In real-world applications, we often need to detect the magnitude of the current. Voltage sensing can be readily achieved using a resistor divider method, whereas current sensing proves somewhat more complex. There are usually two main types of methods to sense current, isolated or non-isolated.

For line-frequency sinusoidal alternating current, current transformers may be employed for isolated detection. Utilizing transformer principles, the primary-side current is transformed to the secondary side. Several considerations apply when using current transformers:

1. Current transformers in different sizes are shown in **Figure 241**. The current conductor under test passes through the center of the transformer, functioning as the primary winding. Typically, this consists of a single turn (though multiple turns can be achieved by passing the conductor through the core multiple times), while the secondary winding comprises multiple turns.
2. The parameters of the transformer are not labeled as a turns ratio, but as 100A:1A. The transformer current ratio is equal to the inverse voltage ratio (turns ratio), "100A:1A", also giving the parameters for the rated current. The extremely small current transformers employ a solid-core design, effectively incorporating the through-core conductor in advance, with terminals or pins directly accessible for connection.

Figure 241. *Current Transformer*

3. **Remember that the secondary winding of a current transformer remains continuously energized**. In the simulated circuit shown in **Figure 242**, a 1MΩ resistor is connected to the secondary winding to simulate an open-circuit condition. V_{G1} voltage employs a sine wave with an amplitude of 1000V, while the current under test shows precisely a 100A amplitude sine wave.

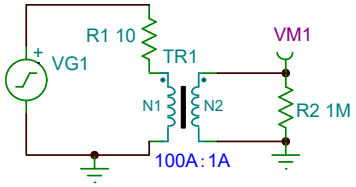


Figure 242. *Current Measurement via Transformer*

4. The simulation results are shown in **Figure 243**. The phenomenon is well explained. The current of the secondary winding will be 1A in magnitude, multiplied by R_2 of 1MΩ resistance. The resulting voltage value is indeed 100,000V high voltage. The transformer used in the simulation is an ideal transformer and the actual voltage may not be as high as 100,000V, but the qualitative results are similar.

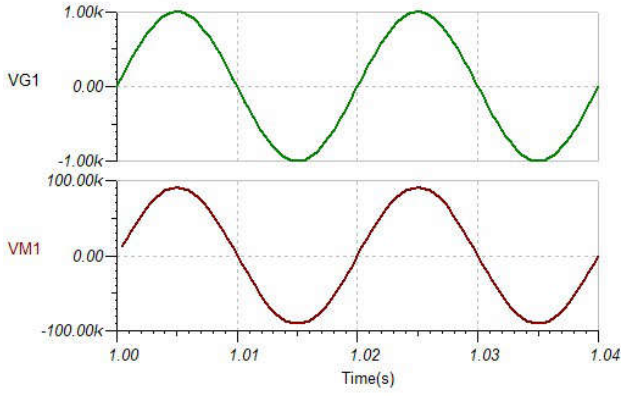


Figure 243. *Simulation of High Voltage at Secondary Open Circuit of Current Transformer*

5. The error in the circuit shown in **Figure 242** stems from our longstanding confusion regarding the concepts of current source and voltage source. The voltage source cannot be short-circuited and the current source cannot be open-circuited. Voltage source is commonplace, whereas current source is less so. The output terminal of a current

transformer should always be connected in parallel with a resistor or conductor to prevent accidental high-voltage generation, which could cause danger or damage.

6. Another consideration when using a current transformer is the power issue of R_2 resistor in **Figure 242**. Typically, we need not calculate whether a resistor's power dissipation meets requirements in standard circuits. However, resistors used with current transformers often require careful calculation of their power dissipation.
7. Specifically, the resistance value of R_2 is adjusted according to signal requirements to obtain a measurement voltage of sufficient amplitude. For example, if you want 100A current to be measured to correspond to 5V, you can set R_2 to 5Ω. Then calculate the rated power of the resistor as 5W using I^2R (rated current of the secondary winding: 1A). Generally, a 1:1 safety margin is applied for power resistors, so a 5Ω/10W power resistor is selected.

Transformers cannot be used if the signal under test is DC or non-line frequency sinusoidal AC (commercially available transformers are designed for line frequency only). At this stage, one may employ costly Hall-effect current sensors for isolated measurement (refer to resources independently for Hall-effect sensors), or utilize a non-isolated shunt capable of handling any AC/DC waveform.

Though the term "shunt" sounds sophisticated, it essentially functions as a current sense resistor. However, not any resistor can serve this purpose.

1. The current sense resistor is connected in series in the main circuit and the current is large and heating is inevitable. Since we do not measure the resistance value any more during use, the resistance of the sense resistor must be stable, that is, not change significantly over temperature. As illustrated in **Figure 244**, this high-power shunt features a black section typically made of constantan material, with a notch for resistance adjustment. The silver-white section comprises zinc-plated copper terminals.
2. The resistance value of a sense resistor is typically very low, and the resulting voltage drop must not affect the main circuit. The general standard for shunt is XXA/75mV, that is, 75mV voltage drop at rated current. In addition to direct connection to the pointer-type instruments, the shunt signal requires amplification before sampling.

Figure 244. *Shunt*

3. In low-power applications within the range of several amperes, we frequently employ dedicated power resistors in the milliohm range for current sensing. Such resistors must be non-inductive, typically presented in through-hole or surface-mount packages for convenient installation on printed circuit boards (PCB).

Whether high-power shunts or small-scale current sense resistors, to minimize interference with the circuit under test, the voltages they generate are typically very low and require further amplification. The fundamental configurations for

amplifier circuits fall into two main categories: low-side current sensing and high-side current sensing. Let's start with the low-side current sensing method.

1. As shown in **Figure 245**, a current sense resistor R_1 is positioned "below" the load R_L. By measuring the voltage at the upper end of R_1, the current can be detected.

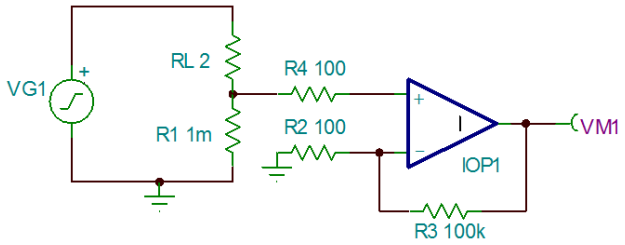


Figure 245. *Low-Side Current Sense Circuit*

2. An op amp non-inverting proportional circuit amplifies the voltage signal on R_1 by a factor of 1000, yielding an output voltage V_{M1}. The simulation results are shown in **Figure 246**. The main current amplitude is about 500mA and the voltage amplitude on R_1 is about 500μV. After amplification, this yields a 500mV square wave voltage.

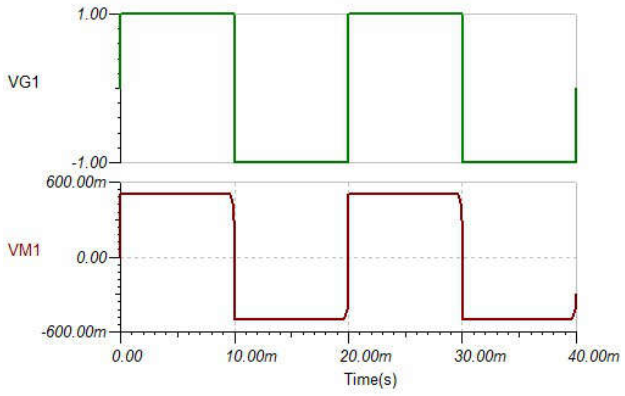


Figure 246. *Simulation of Low-Side Current Sensing*

Low-side current sense circuits require only regular op amps, making them cost-effective, though their applicability is subject to certain conditions.

1. As shown in **Figure 245**, the load R_L is no longer a common ground output. In scenarios where loads are followed by subsequent processing circuits, the output signal must be common grounded. Loads that do not require common ground are typically terminal loads, such as buzzers, loudspeakers, motors, lamps, and other electrical appliances.
2. In particular, low-side current sensing is not suitable for non-linear and strongly interfering loads such as motors. As shown in **Figure 245**, the basic principle of low-side current sensing is to assume that the voltage at the "lower end" of R_1 is 0, hence only the voltage at the upper end of R_1 needs to be detected.
3. For loads like motors, the main circuit's earth wire should be regarded as a "power earth". This requires "isolation" from the "analog earth" where the op amp resides, inherently creating a voltage difference between the two "earths". Therefore, it is not enough to only detect the single-ended voltage of R_1.

The schematic for dedicated current sense amplifier is shown in **Figure 247**.

1. V_{SENSE} is converted to a current signal by a resistor and high-voltage transistor, or then R_{OUT} is converted to a voltage output.

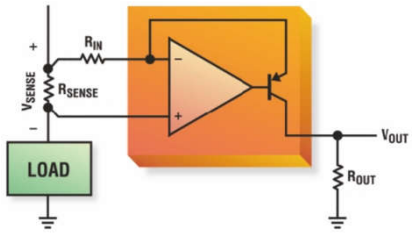


Figure 247. *Schematic for Current Sense Amplifier*

2. The input-output relationship of **Figure 247** is readily derived:

$$I_{OUT} = I_{R_{IN}} = \frac{V_{SENSE}}{R_{IN}} \tag{121}$$

$$V_{OUT} = I_{OUT} \cdot R_{OUT} \tag{122}$$

The high-side current sensing based on the differential principle is suitable for all current sensing applications. But should one select a differential amplifier, instrumentation amplifier, or current sense amplifier? The (common-mode) voltage of the high-side sense resistor is typically high, precluding the use of instrumentation amplifiers.

Key comparisons between differential amplifiers and current sense amplifiers are shown in **Table 4**. Current sense amplifiers outperform differential amplifiers on almost every performance metric, especially in the adjustable speed and gain.

Table 4. Comparison of Differential Amplifiers and Current Sense Amplifiers

Features	Current sense amplifier	Differential amplifier
Speed	Fast, capable of measuring transient current	Slow, suitable for measuring average current
Gain	Adjustable	Fixed
CMRR (DC)	>100dB	80dB
CMRR (PWM)	80dB	80dB
Input stage leakage current	Low	Voltage divider network causes high leakage current
External filter	Post-input stage	Before and after the input stage
Input over-voltage	Damaging the input stage transistors	Voltage divider network positioned upfront, minimizes risk

Not only are current-output current sense amplifiers faster, but we shall also discover that current-output DAC outperform voltage-output DAC in speed. Why is the speed of "current" higher than that of "voltage"?

1. The speed of the "voltage" is limited by the capacitance, and the speed of the current is limited by the "inductance", which is completely dual, so the filter circuit can be capacitor or inductor filter.
2. However, in practice, capacitors are far easier to "get" than inductors, so we generally employ capacitor filters.
3. Similarly, "parasitic" capacitance is significantly greater than "parasitic" inductance, hence "current" travels faster than "voltage".

Variable Gain Amplifiers

In analog-to-digital conversion applications, if the dynamic range of a signal is wide (with amplitude varying significantly), the sampling accuracy (resolution) of the ADC may not be sufficient to meet the requirements. This is where variable gain amplification of the signal is necessary before the signal is sampled by the ADC.

1. Apply high-gain amplification to weak signals to achieve full-scale use of the ADC resolution.
2. Apply low-gain amplification to high-amplitude signals to avoid exceeding the ADC reference range.
3. The amplifier whose gain is controlled by voltage is referred to as a voltage-controlled gain amplifier (VCA).
4. The amplifier whose gain is digitally controlled by an MCU is referred to as a programmable gain amplifier (PGA).

First, let's introduce the use of VCAs. **Figure 248** shows the circuit for the VCA610 amplifier.

1. The VCA610 features a gain ranging from –40dB to 40dB. Simply put, it can attenuate or amplify signals by a factor of 100.
2. The control voltage VM2 ranges from 0 to –2V, with 0V corresponding to a gain of –40dB and –2V corresponding to a gain of 40dB, enabling linear control in dB/V. Furthermore, 1V corresponds to 0dB (1x amplification), –0.5V corresponds to –20dB (0.1x amplification), and 1.5V corresponds to 20dB (10x amplification).

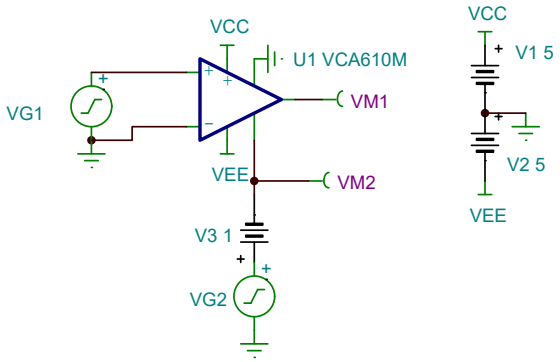


Figure 248. *VCA Circuit*

3. **Figure 249** shows the transient simulation. The input signal V_{G1} has an amplitude of 10mV. During the period from 250μs to 500μs, the attenuation is already hard to discern. At 750μs, the control voltage is –2V, and the signal is amplified to 1V.
4. It is necessary to ensure the stability and reliability of the signals at the voltage-controlled terminal when using a VCA, and necessary filter circuits should be incorporated.

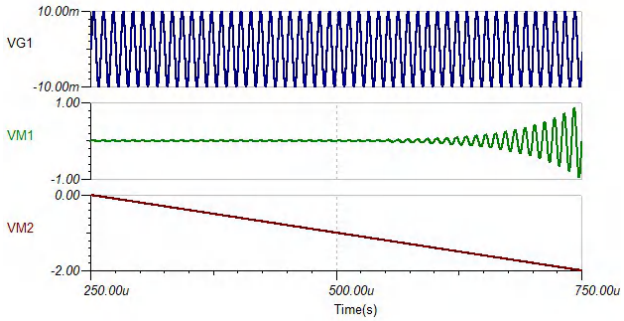


Figure 249. *Transient Simulation of the VCA*

VCAs are generally controlled by negative voltage. Negative voltage signal generation can be an issue if the MCU+DAC is used for programmable control.

1. If the DAC used can output negative voltage, such as the R-2R type (inherently requiring an op amp connection), then negative voltage can be normally output to control the VCA.
2. If the DAC provides unipolar output, such as the R-String type, it also requires a subsequent op amp configured as an inverter (or a negative voltage shifting circuit) to achieve voltage control.

The use of PGAs is a bit easier. Generally, the gain can be controlled by applying high or low levels to a few programming pins. Compared to VCAs, PGAs generally have a narrower bandwidth and are less cost-effective.

A regular op amp circuit, as shown in **Figure 250**, can be used as a PGA in some applications.

1. Adjusting the value of the feedback resistor R_F can control the gain.
2. R_F is switched by a mechanical relay, an optocoupler relay, or an analog switch chip.
3. The advantage of using a mechanical relay is that it ensures no introduction of additional resistance, an accurate R_F value, and an extremely wide bandwidth.

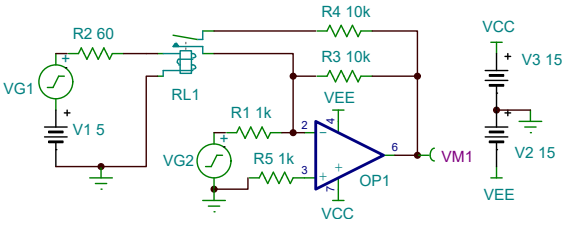


Figure 250. *Affordable PGA*

4. In the simulation shown in **Figure 250**, V_{G1} periodically controls the opening and closing of relay R_{L1}. This causes the value of the feedback resistor R_F to periodically switch between 5k and 10k, resulting in a 5x or 10x amplification, respectively. **Figure 251** It shows the transient simulation, where V_{G2} is the input signal and V_{M1} is the output signal.
5. In real-world applications, R_3, R_4, and even more feedback resistors are controlled by relays. They can be arranged in an array, following a certain pattern.

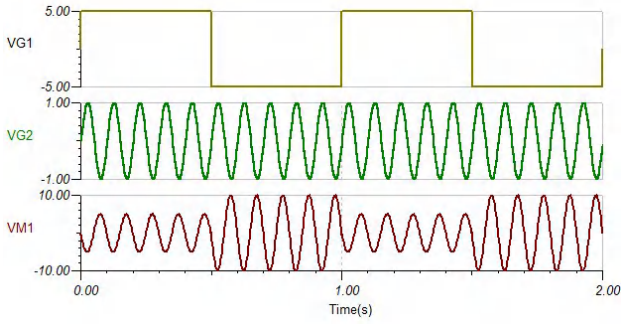


Figure 251. *Simulation of the PGA*

Using a regular op amp plus a switch to achieve programmable gain has advantages and disadvantages:

1. The advantages are high accuracy and a wide bandwidth that could be provided by a high-speed amplifier.
2. The disadvantage is that it cannot achieve many programmable gain levels. If a relay is used for switching, the gain switching will be relatively slow.

Voltage-to-Frequency Converter

As shown in **Figure 252**, the classic 555 timer can be configured as a voltage-controlled oscillator (VCO). However, general VCOs have poor voltage-frequency linearity and can only be used for phase-locked loops (PLLs)/frequency-locked loops (FLLs). The precision voltage-to-frequency converter (VFC) LM331 can achieve 0.1% linearity at a frequency below 100kHz. This type of VFC can be used as an ADC.

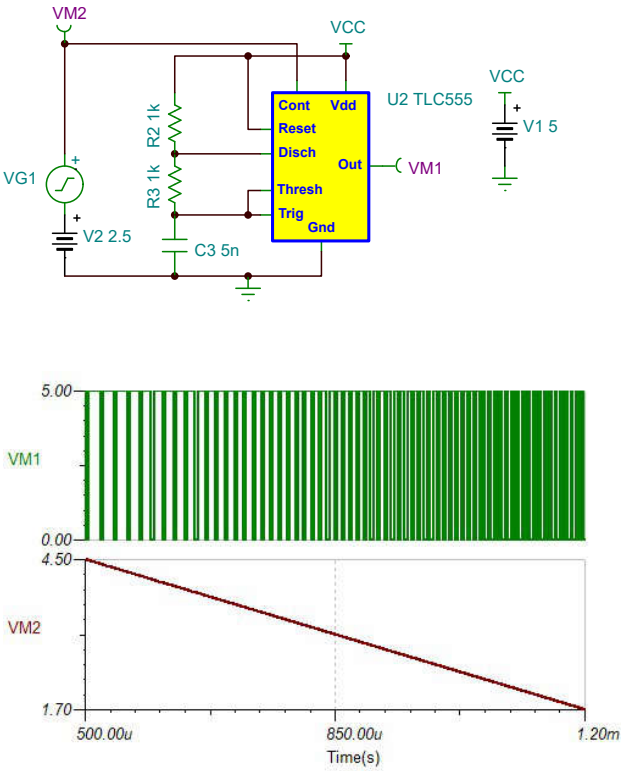


Figure 252. *VCO Configured by 555 Timer*

Why do we need to convert voltage to frequency? There could be many reasons; here, an application related to signal transmission is provided.

1. When the sensor is very far from the processor and the path is fraught with challenges (in a harsh electromagnetic environment), it is unwise to transmit an analog voltage signal.
2. If the analog voltage signal is converted into a frequency signal at the sensor end before transmission, what is transmitted is a digital signal.
3. Compared to digital bus communication, VFC communication has a slower rate, but offers much stronger interference resistance and eliminates issues with bit error rates and data verification.

Isolation Amplifiers

When the potential (not voltage) of the signal to be measured reaches hundreds or even thousands of volts, both differential amplifiers and current sense amplifiers are vulnerable.

Isolation amplifiers are those specifically designed for high-voltage applications. In the schematic for isolation amplifiers in **Figure 253**, the classic triangular symbol for an amplifier is vividly split to represent a two-stage circuit:

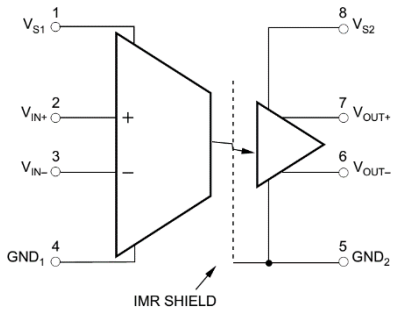


Figure 253. *Schematic for the ISO130 Isolation Amplifier*

1. The preceding circuit on the left is the high-voltage signal input terminal (main circuit). As the circuit always requires power, the potentials of V_{S1} and GND_1 are also high voltages.
2. The subsequent circuit on the right is the low-voltage signal output terminal (control circuit). As the low-voltage part requires a separate power supply, V_{S2} and GND_2 are completely isolated and independent from the power supply for the preceding stage.
3. To prevent high voltage from the main circuit from transferring to the control circuit, isolation amplifiers do not use any feedback resistor. Instead, they use transformers or optocouplers to transmit signals to the subsequent stage, maintaining a fixed voltage ratio. The ISO130 isolation amplifier is optocoupler isolated. From **Figure 254**, the amplification factor of the ISO130 can be estimated as 8.
4. It is quite challenging to transmit analog signals using transformers and optocouplers. Even with careful design, their precision will be far from that of regular op amp conditioning circuits. Neither the sinusoidal signals nor the square wave signals shown in **Figure 254** are ideal, but transformers and optocouplers can provide insulation withstand voltages ranging from several thousand to tens of thousands of volts between their input and output sides.

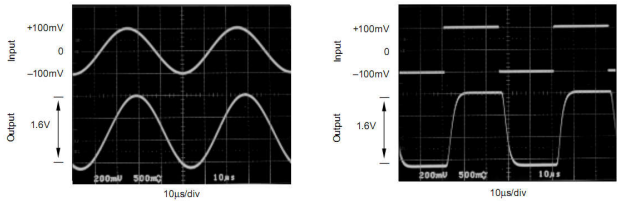


Figure 254. *Input and Output Characteristic Curves of the ISO130*

As shown in **Figure 255**, the voltage rating of the chip's power supply system should be fully considered when an isolation amplifier is used.

1. Many beginners, when first introduced to electrical isolation, might believe that adding an optocoupler can ensure the isolation. Practical electrical isolation is far from just adding an optocoupler or a transformer; its challenge lies in the isolation of the chip's power supply.
2. Unless powered by a battery, the two stages of an electrically isolated chip are ultimately powered by the 220V/50Hz mains electricity indicated by V_{G1}.
3. V_1 indicates the high-voltage main circuit, which is electrically connected to V_{CC1} and GND_1, so their potentials are similar (differing by only a few volts).
4. The voltage sensing point VM_3 is connected to the control circuit, and the potentials of V_{CC2} and GND_2 are similar to that of the control circuit.
5. The two power supplies are sourced from the secondary windings of transformers TR_1 and TR_2. Therefore, it is clear that there can be a high voltage of up to several kilovolts between the secondary windings. The two secondary windings N_2 appear far apart, but the primary windings N_1 of transformers TR_1 and TR_2 are electrically connected. This means that the primary and secondary windings of the transformers must be able to withstand a voltage of several kilovolts.
6. Electrical isolation is, in essence, power isolation, with transformers being used ultimately, no matter how advanced the optocouplers are.

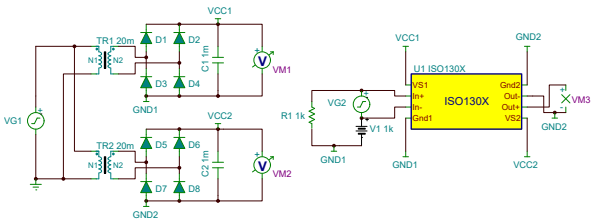


Figure 255. *Power Supply Systems for an Isolation Amplifier*

Audio Power Amplifiers

There is a famous saying online: "**SLRs drain three generations of wealth, while high-end audio systems will destroy your whole life**" (or vice versa). This suggests that humans, as the masters of the world, are endlessly pursuing sensory (audio-visual) enjoyment. The first half of this section will explain the principles of amplifier circuits in audio systems, and the second half will introduce "regular" integrated audio amplifiers.

Audio amplifiers are also known as power amplifiers, which may be familiar to most people. However, few are aware that power amplifiers are categorized into preamplifiers (front-stage amplifiers) and post-amplifiers (rear-stage amplifiers).

1. The impedance of loudspeaker loads is very low, and standard speakers are typically available with only two specifications: 4Ω and 8Ω. Without amplifier circuits featuring extremely low output resistance (internal resistance), it would be impossible to drive them.
2. Since it is challenging to drive loudspeakers, post-amplifiers are used to achieve extremely low output impedance.
3. Circuits for this purpose, as we learned earlier, include Class A, Class B, and Class AB amplifiers based on the emitter follower (common-collector) circuit, as well as Class D amplifier circuits based on the switching circuit. They can all be used as post-amplifiers.
4. High-quality post-amplifiers are often low-efficiency Class A amplifiers, and Class D amplifier circuits are used in battery-powered portable devices.

In addition to producing sound, we also want to adjust the volume level, which cannot be achieved by post-amplifiers. In this case, a preamplifier is necessary.

1. Volume adjustment simply involves the regulation of voltage amplitude, which is achieved through a voltage amplifier circuit. An op amp circuit based on the common-emitter amplifier can achieve this purpose - the volume can be adjusted by modifying the feedback resistance R_F.
2. High-performance audio op amps used in the front stage exhibit very low noise and total harmonic distortion (some with the THD as low as 0.00003%), typically in metallic or ceramic packages.

Furthermore, achieving distortion-free adjustment of RF is highly demanding. The digitally controlled adjustment of high-quality audio signals is actually a very complex process, as the non-linearity error introduced by digital components will greatly affect the sound quality.

1. A more professional approach is to use specialized digitally controlled microphone preamplifiers, such as the PGA2500 from TI, which costs about $10 per unit.
2. An even more professional approach is to use a digitally controlled motor-driven high-accuracy mechanical potentiometer, such as professional motor potentiometers, whose cost ranges from tens to hundreds of yuan.

Figure 256. *Motor Potentiometer*

3. To minimize the issues of regular mechanical potentiometers - sliding wear and poor contact over long-term use - high-end tuning potentiometers are designed similarly to encoders. They consist of multiple precision resistors connected at one end, with the other end featuring contacts. During tuning, the common contact connects with one of these resistor contacts, allowing for the selection of different resistances. All of these contacts are made of

gold-plated silver. Typical potentiometers of this type include DACT 24-stage stepping potentiometer, which costs around RMB 1,000 per unit.

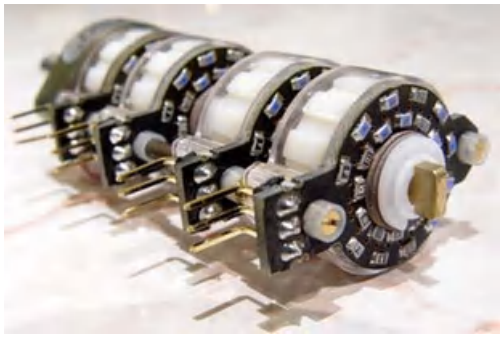


Figure 257. *Stepping Potentiometer*

4. In particular, the resistance of a tuning potentiometer does not change linearly, but follows a logarithmic pattern. This is because the human ear perceives only a doubling of loudness when sound intensity increases by a factor of 10.

A power amplifier that combines a preamplifier and a post-amplifier is called an "integrated amplifier". In modern amplifiers, you can also find those constructed from vacuum tube circuits. These are known as "tube amplifiers", as shown in **Figure 258**. The transistor amplifier circuit described earlier is called a "solid-state amplifier". The combination of both is called a "hybrid" amplifier.

Figure 258. *Tube Integrated Amplifier*

Naturally, many cheap audio amplifier chips are available to perform both pre-amplification and post-amplification functions at the cost of sound quality. **Figure 259** shows the schematic block for the TPA301 in bridge-tied load (BTL) topology.

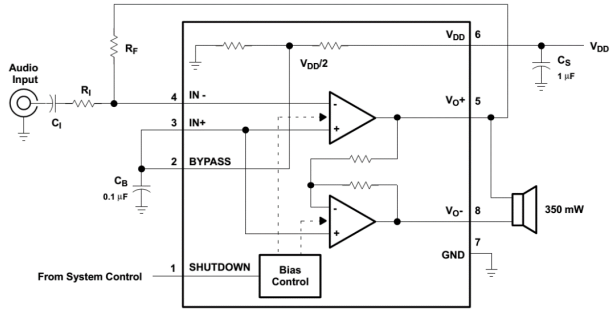


Figure 259. *TPA301 Mono Audio Power Amplifier*

1. The BTL circuit is essentially a Class B (or Class AB) amplifier circuit. However, to eliminate coupling capacitors and avoid dual-supply operation, two Class B amplifier circuits are incorporated to form the BTL topology.
2. In the schematic for the BTL circuit in **Figure 260**, the upper and lower push-pull circuits behave as the two op amps in the TPA301 (the last stage of any regular op amp is a push-pull circuit). The output of the op amp will not be negative due to single-supply operation.
3. If the input signals of the two op amps are out of phase by 180°, then the voltage applied to R_L (the loudspeaker) is pure AC, with an amplitude twice that of a single op amp output. This is the principle behind BTL configurations, which enable AC output with a single power supply.

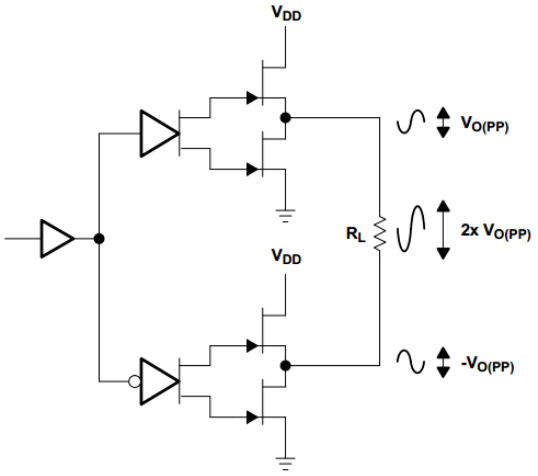


Figure 260. *Schematic for the BTL Circuit*

4. Based on the schematic shown in **Figure 259**, the op amp in the TPA301 forms an inverting proportional circuit with a feedback resistor R_F. Therefore, the amplification factor of the "front stage" is:

$$A = -2\frac{R_F}{R_1} \tag{123}$$

Active Filter

As described earlier, the load of the passive filter is also a part of the filter and therefore causes a shift of the cutoff frequency. To isolate the load, the filter is incorporated with an op amp, which is thus referred to as an "active filter". It should be noted that active filters are not suitable for every application.

1. When the filters are not highly required for the cutoff frequency but merely to filter out some high-frequency glitches, using RC or LC filters obviously enables a simple structure and low cost.
2. When the signal frequency is very high, e.g., ranging from a few hundred MHz to GHz, LC filters are generally used, as op amps with a high bandwidth are scarce and expensive.
3. Considering efficiency, op amp filters cannot be used when filtering power supplies instead of signals. Instead, LC filters or power active filters (which are switching circuits, not the typical op amp active filters) are generally used.

Simple Active Filter

As shown in **Figure 261**, a simple active filter is formed by using an op amp for isolation at the final output stage of a passive filter (regardless of the number of stages), making the filter immune to load effects.

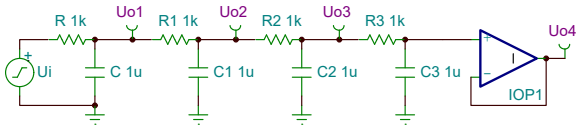


Figure 261. *Simple Fourth-Order Active Low-Pass Filter*

Simulating the AC transfer characteristics of the outputs of each stage shown in **Figure 261** yields the amplitude-frequency and phase-frequency characteristic curves shown in **Figure 262**.

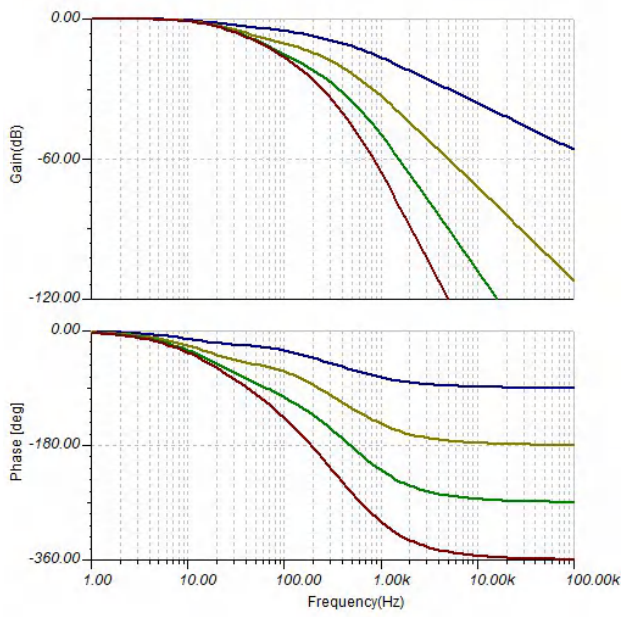


Figure 262. *Amplitude-Frequency and Phase-Frequency Characteristic Curves of the Fourth-Order Low-Pass Filter*

Take a low-pass filter as an example. While an ideal filter cannot "cut off" the signal abruptly at the cutoff frequency, a filter with "high selectivity" will minimize signal attenuation before the cutoff frequency and ensure rapid attenuation with the theoretical slope after the cutoff frequency.

As shown in **Figure 263**, a regular filter attenuates signals significantly before the cutoff frequency, but does not attenuate them quickly after the cutoff frequency. "Poor selectivity" is theoretically characterized as a low Q factor.

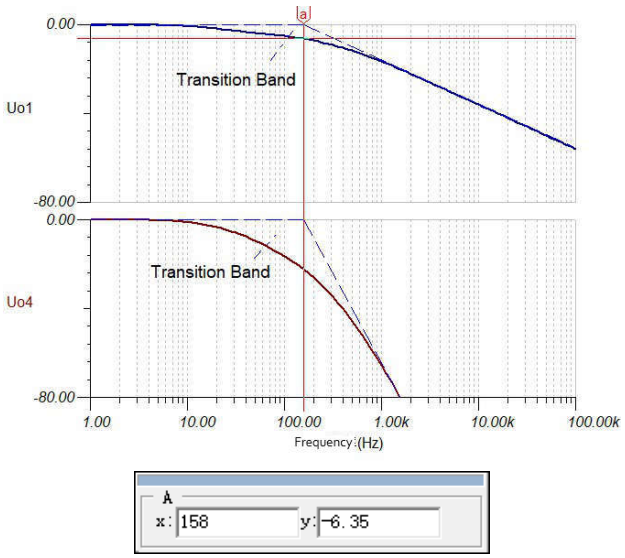


Figure 263. *Transition Band of the Filter*

"Complex" active filter circuits (in Sallen-Key and MFB topologies) allow for Q factor adjustment, ultimately forming different filter (response) types with various Q factors, such as Bessel, Butterworth, and Chebyshev.

The amplitude-frequency characteristic curves of the three types of filters are shown in **Figure 264**.

1. The Bessel filter has the lowest Q factor (0.58 shown in the figure) and thus poor (frequency) selectivity. To achieve the same filtering effect, a higher-order filter is required.
2. The Chebyshev filter has the highest Q factor (1.305 shown in the figure), providing rapid attenuation in the transition band and the best (frequency) selectivity. However, its amplitude-frequency curve exhibits overshoot and is not as smooth as those of the other two filters.
3. The Butterworth filter has a moderate Q factor (0.71 shown in the figure), offering the smoothest gain within the passband and comprehensively balanced characteristics.

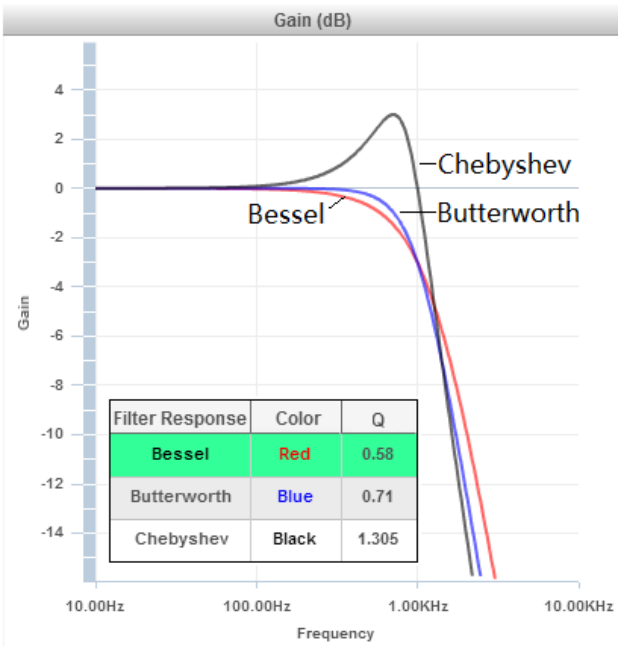


Figure 264. *Amplitude-Frequency Characteristic Curves for the Three Filtering Responses*

Figure 265 shows the group delay characteristic curves for the three types of filters.

1. The so-called group delay, simply put, describes whether a group of signals entering a filter simultaneously can still exit the filter simultaneously.
2. If a filter provides a uniform attenuation rate for signals within its passband (with smooth passband gain) but inconsistent delays, its output signals will be significantly "distorted".
3. The Bessel filter offers the smoothest group delay characteristics (an advantage), making it suitable for audio filtering applications (ensuring no sound distortion).

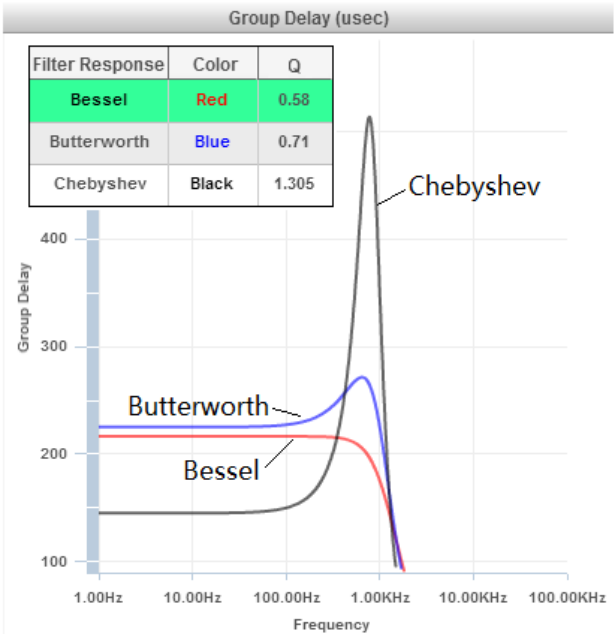


Figure 265. *Group Delay Characteristic Curves for the Three Filtering Responses*

The step characteristic curves of the three types of filters are shown in **Figure 266**.

1. When an "abruptly changing" signal is input into the filter, it may or may not experience overshoot (ringing) and will take some time to recover. These reactions are referred to as its step responses. Obviously, we expect no overshoot and to reach stability as quickly as possible.
2. A DAC output signal can be seen as a step signal; a high-frequency interference signal can also be seen as a step signal. They both do not require high (frequency) selectivity from the filter.
3. The Bessel filter experiences no overshoot in its step response, making it suitable as a low-pass filter at the DAC output and as an anti-aliasing low-pass filter at the ADC input (primarily to filter out high-frequency interference).

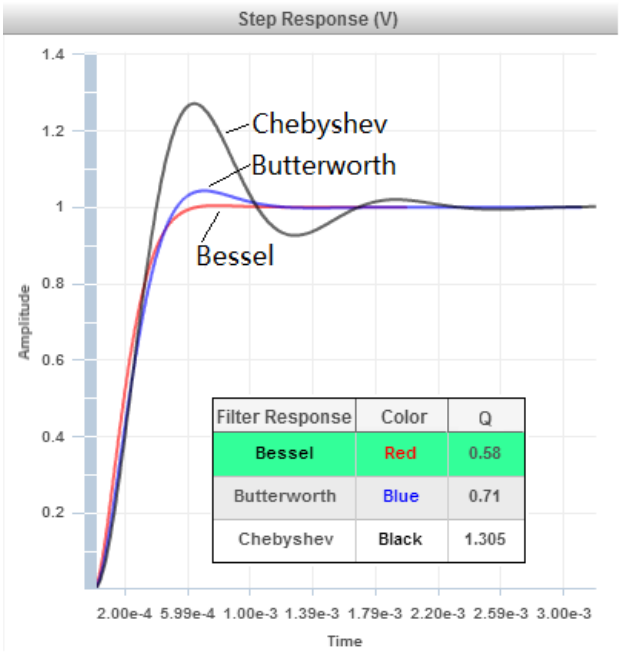


Figure 266. *Step Characteristic Curves for the Three Filtering Responses*

Active Filter Design Software

The design of filters is a very extensive field, and the easiest way is to use various filter design software to aid in the design. Here, we'll briefly introduce how to aid in the design of active filters with TI's online software, WEBENCH®. WEBENCH is a powerful online design and simulation tool developed by the former National Semiconductor (now acquired by TI). It allows for the design and simulation of power supplies, LEDs, amplifiers, filters, audio systems, interfaces, wireless configurations, and signal paths.

1. As shown in **Figure 267**, on the TI homepage, register/log in to your my.TI account. This free account allows you to download and use TI software, request free TI demos, and more.

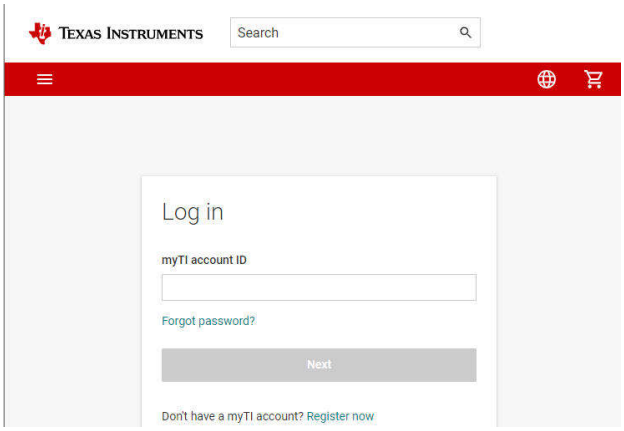


Figure 267. *Log in/Register a TI Account*

2. On the TI homepage, locate the online design software, WEBENCH Designer. Taking the widely used low-pass filter as an example, select "Filters" → "Lowpass", and click "Start Design".

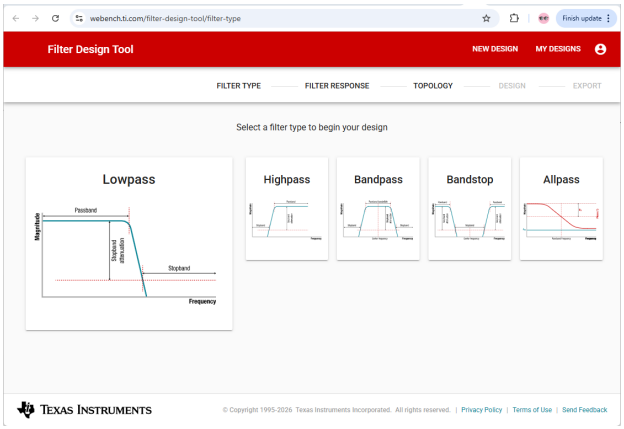


Figure 268. *Online Design Software WEBENCH Designer Portal*

3. Refer to **Figure 269**. A wide range of options is provided on the filter design interface. To specify the order of the filter, select "Pick Filter Response". For example, select the second-order Butterworth filter with a cutoff frequency of 1000Hz, powered by a single 5V supply. Click Select to proceed to the next step.

Figure 269. *Filter Design Interface*

Figure 270 shows a second-order active filter in the default Sallen-Key topology, which can be further modified to update the default design.

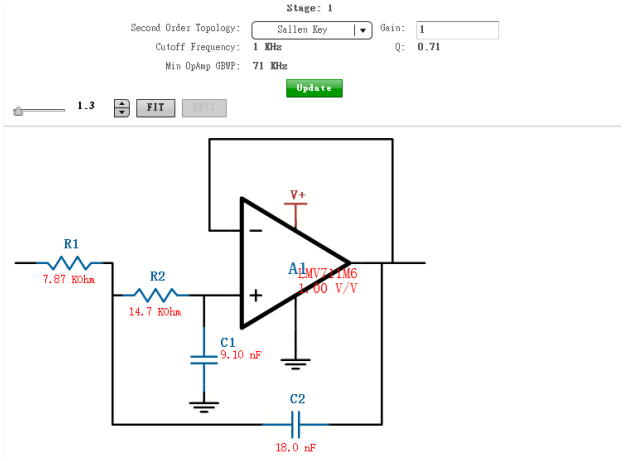


Figure 270. *Schematic for Second-Order Active Filter in the Sallen-Key Topology*

1. As shown in **Figure 271**, you can modify the recommended design strategies in terms of circuit size, cost, and sensitivity, which will result in different op amp selections during the filter design.

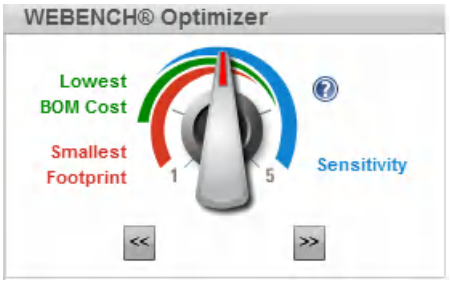


Figure 271. *Recommended Design Selection*

2. **Figure 272** shows the op amp type, which can be changed directly. Note that the op amp is powered by a single 5V supply, which is determined by the actual power supply of the active filter on the experimenter board (located in the ultrasonic module).

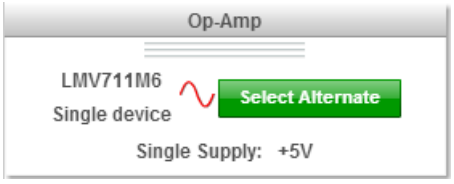


Figure 272. *Op Amp and Power Supply Selections*

3. On the screen shown in **Figure 273**, you can select the circuit topology and the accuracy of passive components. After modification, click Update to update the circuit.

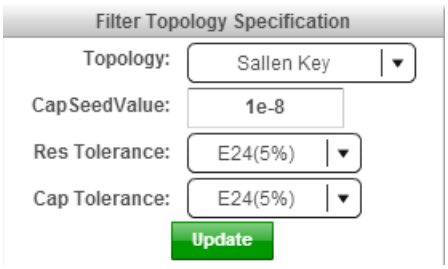


Figure 273. *Circuit Topology and Passive Component Accuracy Selections*

4. As shown in **Figure 274**, the filter's response can be modified among several options, including Bessel, Butterworth, and Chebyshev. The filter order can also be modified.

Figure 274. *Filter Response and Order Modification*

5. The bill of materials (BOM table), as shown in **Figure 275**, provides details about the part number, manufacturer, and price for reference.

Bill of Materials

Part ▲	Manufacturer	Part Number	Price	Value	Footprint	Top Vie	Edit
A1	Texas Instruments	LMV711M6 (Single de...	$0.60 Per Channel:$0.60	N/A	14.0 mm²		Select Alternate Part
C1	MuRata	GRM2195C1H912JA0...	$0.06	9.100nF	6.75 mm²		Select Alternate Part
C2	MuRata	GRM3195C1H333JA0...	$0.10	33.000n	10.920000		Select Alternate Part
R1	Panasonic	ERJ-6GEYJ113V	$0.01	11.000K	6.75 mm²		Select Alternate Part
R2	Panasonic	ERJ-6GEYJ113V	$0.01	11.000K	6.75 mm²		Select Alternate Part
R3	Panasonic	ERJ-6GEYJ562V	$0.01	5.600KΩ	6.75 mm²		Select Alternate Part

Figure 275. *BOM Table for the Reference Design*

As shown in **Figure 276**, change the filter topology type to MFB (Multiple Feedback) and click "Update".

1. A filter in the MFB topology uses an inverting input. Therefore, for single-supply op amps, V_{CM} must be provided at the non-inverting input to raise the signal by one level.
2. All single-supply op amp circuits must be carefully analyzed to determine whether the input and output voltages meet the supply rail requirements. If necessary, a common-mode voltage V_{CM}, which is obtained through resistance division, should be applied to the non-inverting input.

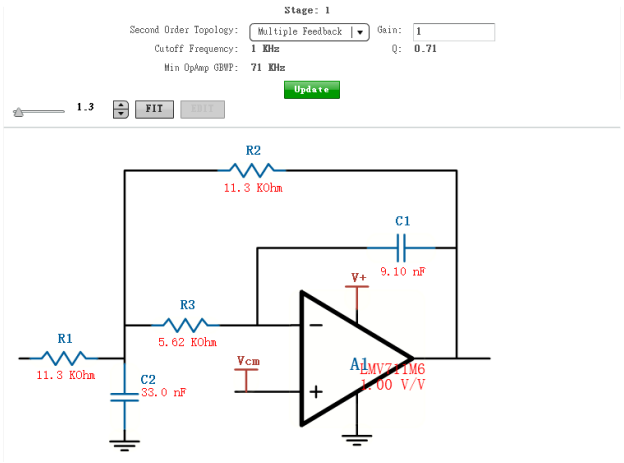


Figure 276. *Second-Order Active Filter in the MFB Topology*

High-Frequency Feedthrough in Sallen-Key Filters

When deriving the amplitude-frequency and phase-frequency characteristics of active filters, op amps are typically treated as ideal amplifiers. When considering op amp's bandwidth, filters in different topologies exhibit distinct characteristics.

Figure 277 shows TINA simulated schematics for a second-order active low-pass filter using the same op amp OPA347 in Sallen-Key and MFB topologies.

1. The cutoff frequency of both filters is 660Hz based on parameters of inductor and capacitor in **Figure 277**.

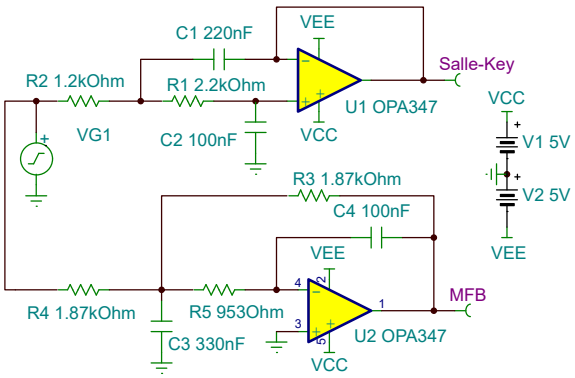


Figure 277. *TINA Simulation of Active Filters*

2. Simulate the AC characteristics of the circuit shown in **Figure 277** and set the AC transfer characteristics as shown in **Figure 278**, and observe the amplitude-frequency characteristics (amplitude).

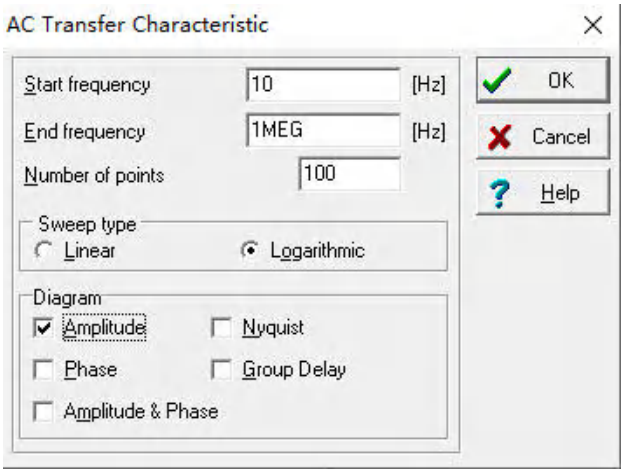


Figure 278. *Parameter Settings of AC Transfer Characteristic*

3. Among the AC transfer characteristics shown in **Figure 279**, within the low frequency band (below 18.22kHz), the amplitude-frequency characteristics of the Sallen-Key and MFB are almost identical. However, as the frequency continues to rise, the low-pass filter employing the Sallen-Key topology exhibits an inverse behavior: its gain increases with higher frequencies, thereby adopting a high-pass characteristic.

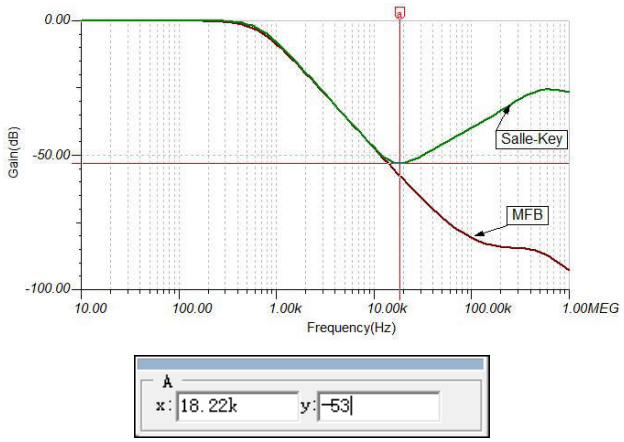


Figure 279. *Amplitude-Frequency Characteristic Simulation of the OPA347 Active Filter*

The amplitude-frequency characteristics with an inflection point shown in **Figure 279** indicates that the low-pass filter employing the Sallen-Key topology exhibits high-frequency feedthrough at the high-frequency end.

1. Referring to **Figure 277**, the Sallen-Key has two output channels, an op amp output and a capacitor C_1 output.
2. When the frequency is high enough, C_1 can be considered to be short-circuited to the signal, while the op amp, constrained by its bandwidth limitations, is "open-circuited" to the signal. Consequently, the output signal is predominantly supplied by C_1 channel, ultimately manifesting as a high-pass characteristic.

This high-frequency feedthrough phenomenon renders the Sallen-Key low-pass filter ineffective against signals at "particularly" high frequencies. Simulate the transient behavior of the circuit shown in **Figure 277**.

1. The signal generator is set for a 24kHz square wave signal with a 50% duty cycle and a +2V amplitude.

2. According to theoretical calculations, the output of the MFB filter should be a negative voltage with –1V magnitude.**Figure 280** The theoretical calculation is well verified, and the output voltage fluctuates only slightly.
3. Theoretically, the Sallen-Key filter output should be a positive voltage with an amplitude of 1V. However, it is indicated in **Figure 280** that the low-pass filter barely filters the high-frequency components of the square wave signal (rising and falling edges).

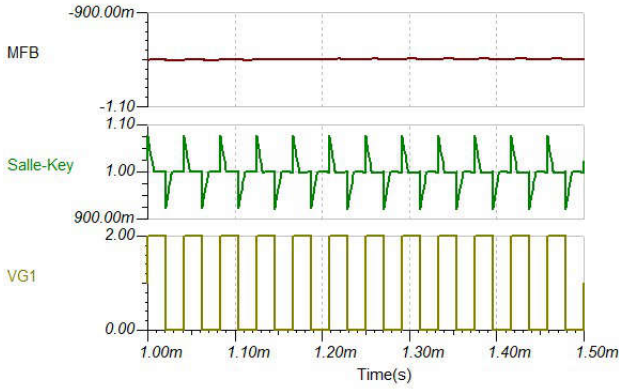


Figure 280. *Simulated Transient Waveforms for High-Frequency Feedthrough*

Impacts of Op Amp's Bandwidth on Filters

The high-frequency feedthrough of Sallen-Key filters shows that the op amp's bandwidth may influence the performance of filters. In this section, we will use TINA simulations to analyze how the op amp's bandwidth affects filters in various topologies.

For comparison, we select the "affordable op amp" LM324 with a unit-gain bandwidth of only 1.2MHz and the wideband op amp OPA842 with a unit-gain bandwidth of 400MHz.

1. As shown in **Figure 281**, we first compare the amplitude-frequency characteristics of the second-order active low-pass filters constructed from these two op amps using the Sallen-Key topology.

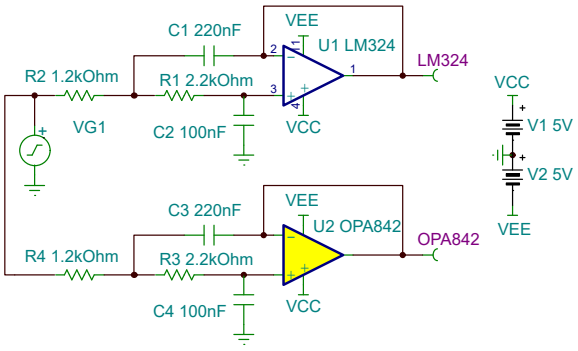


Figure 281. *Simulated Schematic for Op Amps with Different Bandwidths Using the Sallen-Key Topology*

2. According to the amplitude-frequency characteristics shown in **Figure 282**, in the low-frequency band (below 10kHz), the low-pass filters composed of the two op amps show no difference, with their curves completely overlapping.
3. At high frequencies, the differences between the two begin to emerge. The corner frequency of the LM324 filter is only 11.54kHz, while that of the OPA842 filter reaches 180kHz.

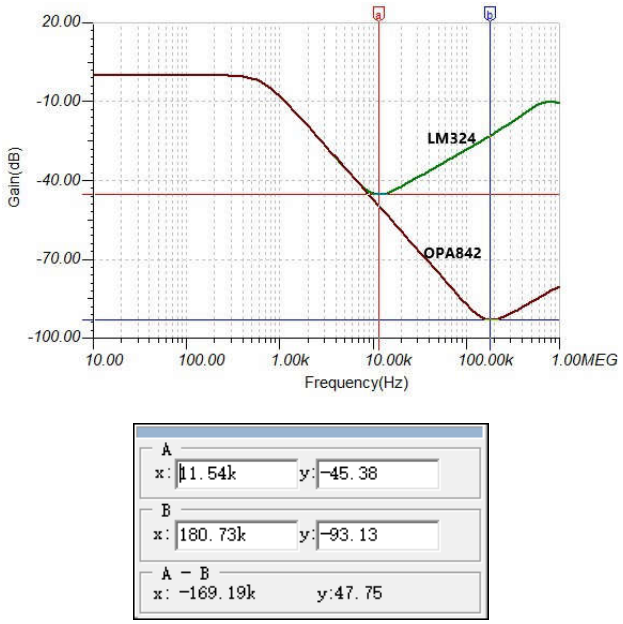


Figure 282. *Amplitude-Frequency Characteristic Comparison Using the Sallen-Key Topology*

4. As shown in **Figure 283**, we then compare the amplitude-frequency characteristics of the second-order active low-pass filters constructed from the two op amps using the MFB topology.

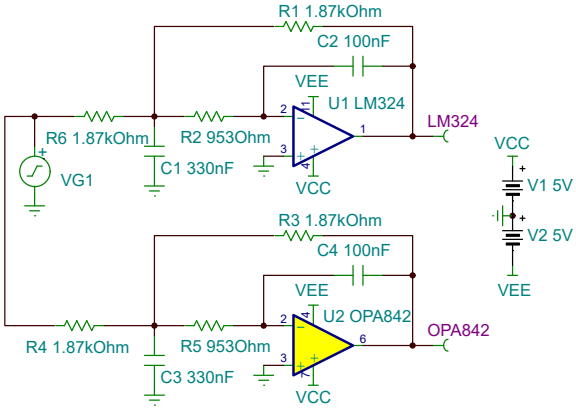


Figure 283. *Simulated Schematic for Op Amps with Different Bandwidths Using the MFB Topology*

5. According to the amplitude-frequency characteristics shown in **Figure 284**, at frequencies below 100kHz, the amplitude-frequency characteristic curves of the two low-pass filters composed of the two op amps are essentially the same.

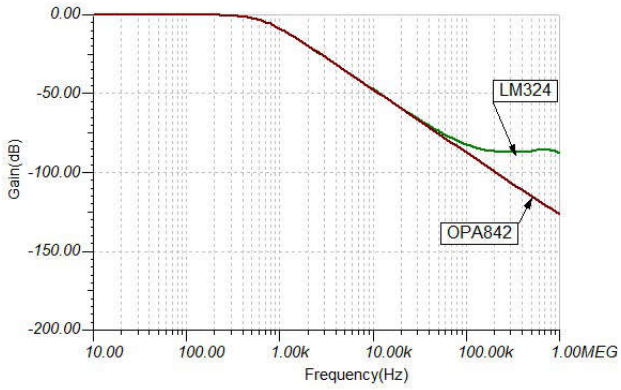


Figure 284. *Amplitude-Frequency Characteristic Comparison Using the Sallen-Key Topology*

The above simulation analysis indicates that the MFB topology has much lower bandwidth requirements for op amps than the Sallen-Key topology. Therefore, the MFB topology is more commonly used. TI's application report ZHCA035 provides detailed explanations of application scenarios for the MFB and Sallen-Key topologies, as well as instructions for FilterPro, another filter design software from TI.

Power Supply Management

Power supply is an extensive subject that covers a vast amount of content. Previous teaching experience has shown that a superficial explanation of main circuit principles yields minimal results. Students can easily find various power supply main circuits online, and there is little room for creativity in main circuit topologies themselves. However, they often know very little about the detailed design and use of power supplies. Therefore, it is aimed in this chapter to prioritize depth over breadth. Only the simplest types of power supply circuits are selected for in-depth explanation, covering the following three parts:

1. Power MOSFET switch.
2. Chopper circuits.
3. Bridge circuits.

- Power MOSFET Switch
- Chopper Circuits
- Bridge Circuits
- Driver Isolation

Power MOSFET Switch

In power supply circuits ranging from low to medium power, the power MOSFET demonstrates the most outstanding performance as switching elements. This section will cover the operating principles, key performance parameters, and drive methods of power MOSFET.

Operating Principle of Power MOSFET

To increase the conductive cross-section, the power MOSFET employs the vertical conductive structure illustrated in **Figure 285**.

1. Taking a N-type transistor as an example: a P-type zone is doped onto the upper layer of the N-type semiconductor substrate material. The control gate (conductive metal) is separated from the P-zone by a silicon dioxide insulating layer.
2. The metal conductors shown in the thick black lines are connected to the control gate, the P-doping zone, and the N-substrate zone to form the Gate (G), Source (S) and Drain (D) of MOSFET.

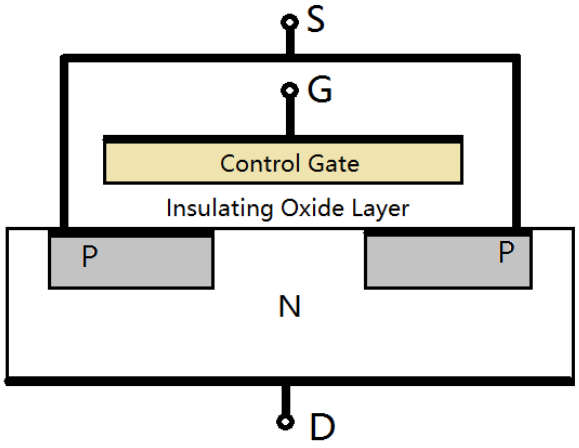


Figure 285. *Schematic for Power Field-Effect Transistors*

Referring to **Figure 285**, the operating principle of a power MOSFET is described as follows:

1. When no voltage is applied between the gate G and source S, current cannot flow from the drain D to the source S (the PN junction is reverse-biased and cut off), known as the off state.
2. At any time, current can flow from S to D (PN junction forward-biased), so the power MOSFET naturally has a parasitic diode, and the N-type power MOSFET symbol is shown in **Figure 286**.

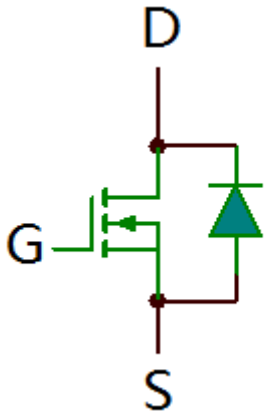


Figure 286. *MOSFET Symbol with Parasitic Diode*

3. Upon applying a forward voltage between G and S, an electric field forms between them, generating N-type inversion layer as indicated by the small white square, as shown in **Figure 287**.

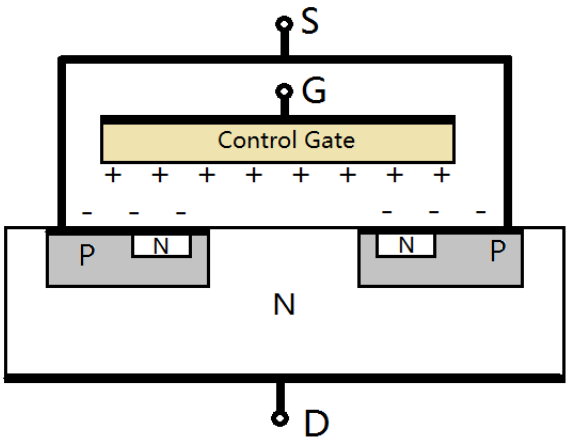


Figure 287. *Creating Inverse Layer*

4. Continuing to increase U_{GS}, when the GS voltage becomes sufficiently high, the N-type inversion layer penetrates the P-type semiconductor zone and connects with the substrate N-type semiconductor, forming a continuous path, enabling conduction between the drain (D) and source (S).

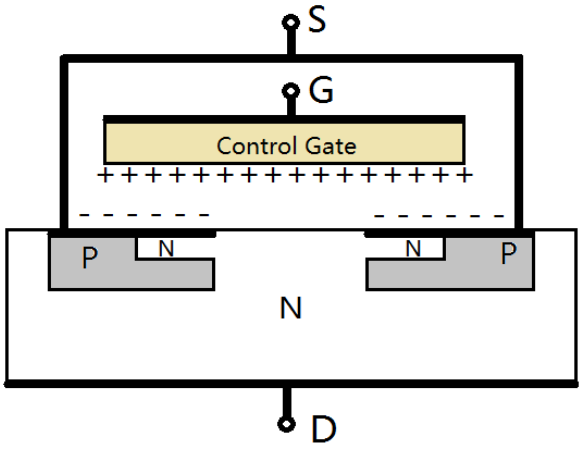


Figure 288. *Forming Conductive Channel*

If it is a P-type MOS transistor, the entire situation is reversed. Applying reverse voltage between G and S enables conduction from S to D (S→D), while conduction from D to S (D→S) is always possible (due to the parasitic diode).

On-Resistance

As described in the section with **Figure 285**, the current conduction principle from D to S relies solely on N-type semiconductor conductivity, thus exhibiting resistive conduction characteristics. This differs from the conductance modulation effect observed in bipolar junction transistors with a 0.7V conduction voltage drop.

Figure 289 shows the low RDS family MOSFET switches from TI. RDS ≤ 1.7mΩ was chosen, yielding 5 products with breakdown voltages ranging from 25V to 40V.

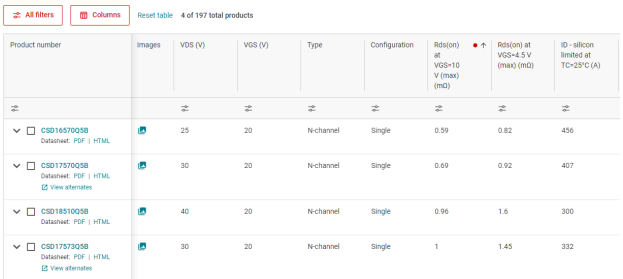


Figure 289. *Low RDS Series MOSFET Switches*

Due to the extremely low on-resistance RDS achievable at low breakdown voltages (mΩ range as indicated in **Figure 289**), this type of MOSFET is particularly well-suited for low-voltage and low-power circuits.

Rated Voltage

The rated voltage of a MOSFET refers to its breakdown voltage UDS. High breakdown voltage indicates high RDS (high conduction loss), while low breakdown voltage indicates low RDS.

1. The on-resistance R_{DS} is determined by the conductor's cross-sectional area and thickness, following the conductivity rule of conductors.
2. Increasing the thickness leads to a higher breakdown voltage, but there is a trade-off: thicker semiconductor material also indicates an increase in the on-resistance R_{DS} between the drain (D) and source (S).

3. Considering both breakdown voltage and on-resistance, the use of MOSFETs in high-voltage applications (e.g., mains electricity) requires careful trade-offs.

Generally, MOSFETs are available in variants designed for low-voltage applications (20-60 volts), as well as those rated up to 500 volts for mains voltage level applications. **Table 5** shows some MOSFET models from International Rectifier (IR) rated from 80V to 300V, focusing on the correlation between breakdown voltage (VBRDSS) and on-resistance (RDS).

Table 5. Specifications of Some MOSFETs from IR

Part	VBRDSS (V)	RDS(on) Max 10V (mOhms)
IRF3000	300	400.0
IRF7453	250	230.0
IRF7464	200	730.0
IRF7492	200	79.0
IRF7450	200	170.0
IRF7465	150	280.0
IRF7451	150	90.0
IRF7494	150	44.0
IRF7490	100	39.0
IRF7452	100	60.0
IRF7473	100	26.0
IRF7474	100	63.0
IRF7495	100	22.0
IRF7488	80	29.0
IRF7493	80	15.0

As shown in **Table 5**, the basic rule is that the higher the breakdown voltage, the higher the on-resistance. For MOSFETs with the same breakdown voltage, their on-resistance, as well as their price, can vary by several times, depending on the process and design.

Rated Current

The rated current of a MOSFET is closely related to the on-resistance RDS. It can be inferred that the dissipation power of a MOSFET in a certain package and under a specific heat dissipation condition is fixed. The larger the on-resistance is, the smaller the rated current will be.

Table 6 is the on-resistance (RDS) vs. rated current (ID) table for some MOSFET models in the TO220 package from International Rectifier (IR).

Table 6. Specifications of MOSFET Variants in the TO220 Package from IR

Part	RDS(on) Max 10V (mΩ)	ID @ TA = 25C (A)	P = I*I*R (W)
IRF3000	400.0	1.6	1.024
IRF7453	230.0	2.2	1.1132
IRF7464	730.0	1.2	1.0512
IRF7492	79.0	3.7	1.08151
IRF7450	170.0	2.5	1.0625
IRF7465	280.0	1.9	1.0108
IRF7451	90.0	3.6	1.1664
IRF7494	44.0	5.2	1.18976
IRF7490	39.0	5.4	1.13724

Table 6. Specifications of MOSFET Variants in the TO220 Package from IR (continued)

Part	RDS(on) Max 10V (mΩ)	ID @ TA = 25C (A)	P = I*I*R (W)
IRF7452	60.0	4.5	1.215
IRF7473	26.0	6.9	1.23786
IRF7474	63.0	4.5	1.27575
IRF7495	22.0	7.3	1.17238
IRF7488	29.0	6.3	1.15101
IRF7493	15.0	9.2	1.2696

A simple calculation using P = I*I*R on the values shown in **Table 6** reveals that the TO220 package offers a dissipation power of approximately 1W. If the drain current ID doubles, the on-resistance RDS must decrease by a factor of four.

Unlike instantaneously breaking down a device by voltage, over-current damage to a device is actually a process of thermal accumulation. In this case, a large instantaneous current (pulsed) does not necessarily damage the device. Therefore, MOSFETs also have a specification of pulsed drain current IDM/IPEAK, generally reaching 5-10 times the ID ratings. For the pulse duration, refer to the specific chip datasheet. The current ratings for a family of MOSFETs from TI are shown in **Figure 290**, where Id Max refers to the typical rated current (continuous), and ID/IPEAK refers to the pulsed current rating.

	CSD17307Q5A	CSD17301Q5A	CSD17302Q5A	CSD17303Q5	CSD17304Q3
VDS (V)	30	30	30	30	30
Logic Level	Yes	Yes	Yes	Yes	Yes
Rds(on) Max @ VGS=4.5V (mOhms)	12.1	3	9	2.6	8.8
ID / IPEAK (Max) (A)	92	181	104	200	88
Id Max@TC=25°C (A)	14	28	16	32	15

Figure 290. *Rated Current of a Family of MOSFETs from TI*

Switching Time

For semiconductor switches, the switching time is a critical parameter, in addition to those that are paramount to all electronic components, such as rated voltage/current. A shorter switching time means that the switching frequency can be very high, allowing for a lower capacity of energy storage components in the circuit, such as inductors and capacitors, as well as a significant reduction in the volume of transformers. High-frequency operation is a major trend in the development of power supply technologies.

1. The roles of inductors and capacitors in a circuit are fundamentally related to their inductive reactance and capacitive reactance, both of which are directly related to frequency.
2. A transformer is akin to a temporary storage reservoir that absorbs and releases energy. Its magnetic core needs to be capable of storing energy for half a cycle; otherwise, it may magnetically saturate. The higher the frequency is, the faster the reservoir "turns over", and a low capacity will be sufficient to meet the energy absorbing and releasing demands.

The switching process of MOSFETs can be simulated using TINA, as shown in **Figure 291**:

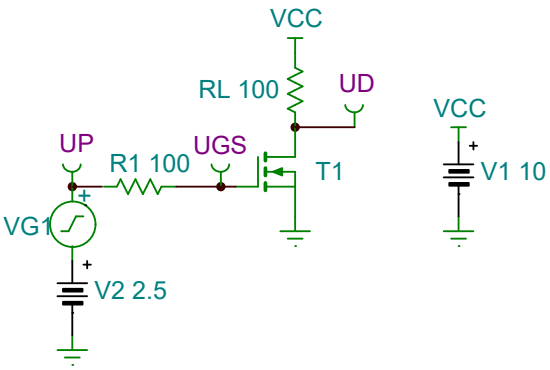
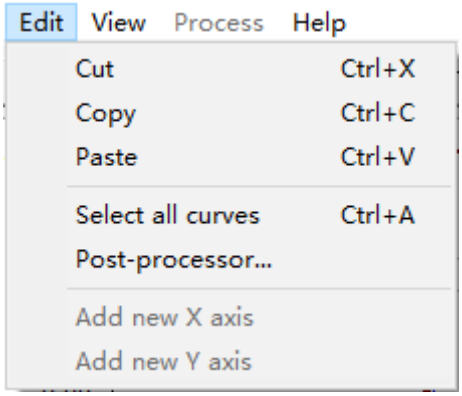


Figure 291. *TINA Simulation of MOSFET Switching Characteristic*

1. The signal generator VG1 is configured as a 500kHz square wave with a 2.5V amplitude. After a 2.5V DC supply voltage V_2 is superimposed, the total drive signal U_P is a 5V square wave pulse (as the U_P waveform shows in **Figure 293**).
2. R_1, the equivalent impedance of the signal generator, is used for the simulation of the control signal's drive capability. The smaller R_1 is, the stronger the drive capability will be.
3. Due to the presence of parasitic capacitances at the gate/source/drain, the U_{GS} waveform is no longer a perfect square wave, but exhibits a slow rise and fall, as the U_{GS} waveform shows in **Figure 293**.
4. U_D represents the drain voltage. I_D can be calculated using the formula $(V_{CC} - U_D)/R_L$.

Simulate the transients in the circuit shown in **Figure 291** using TINA, with the simulation start/stop period set to 1.5μs-4μs. According to **Figure 292**, click “Edit” → “Post-processor” in the simulated waveform window to open the post-processing window, and add the calculation formula for I_D in the “Create” bar: " $(10 - U_D(t))/100$ ". Click “Line Edit” to create the I_D curve.



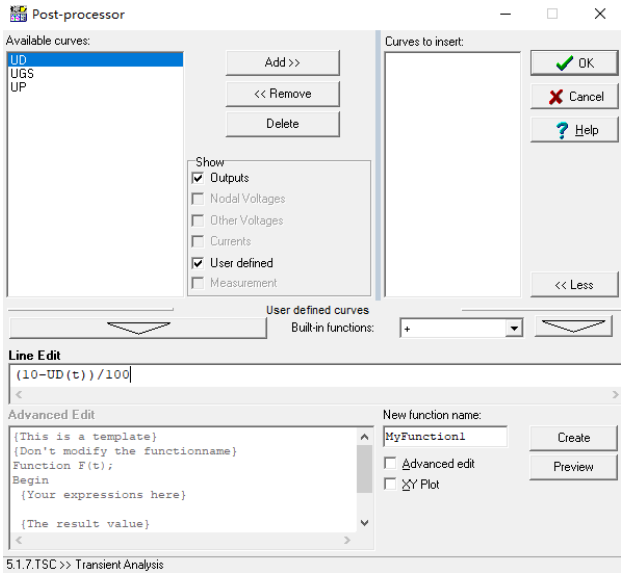


Figure 292. *Adding ID Curve in the "Post-Processing" Window*

Figure 293 shows the simulation of the MOSFET switching process after the ID curve is added. The on-time (ton) of the MOSFET consists of the turn-on delay time (td(on)) and the rise time (tr), while the off-time (toff) consists of the turn-off delay time (td(off)) and the fall time (tf). In **Figure 293**, 6 time points from t0 to t5 are marked with dotted lines, and each period represents a different switching process.

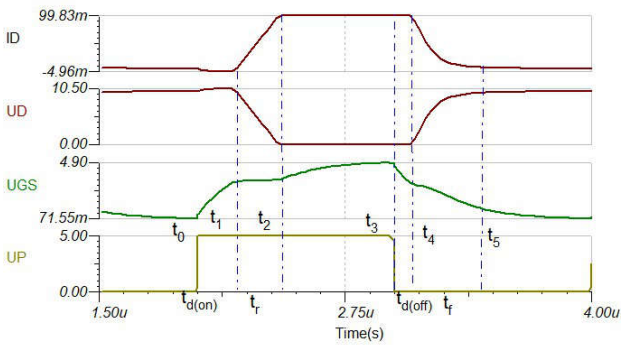


Figure 293. *Simulation of MOSFET Switching Process*

1. At t_0, the drive level is asserted high with the intention of turning on the MOSFET. However, the gate voltage U_{GS} can only rise slowly due to the presence of the equivalent capacitance at the gate. The MOSFET will not be turned on before U_{GS} reaches its threshold $U_{GS(TH)}$ (high U_D, low I_D).
2. At t_1, the voltage U_{GS} reaches its threshold, and the MOSFET begins to conduct. The time period from t_0 to t_1 is called the turn-on delay time $t_{d(on)}$, representing the delay from the switch "being turned on" until it "enters the on-state". From t_1, U_D gradually decreases while I_D gradually increases due to the equivalent capacitance between the drain and source.
3. At t_2, U_D reaches its minimum while I_D reaches its maximum. The MOSFET completes its turn-on process. The period from t_1 to t_2 is called the rise time t_r and represents the time required for the current I_D to rise to its maximum. It should be noted that within the t_r period, the voltage U_{GS} remains constant due to the "Miller effect" of the junction

capacitance, which is known as the "Miller plateau". After t_2, the voltage U_{GS} gradually rises to the maximum drive voltage.

4. At t_3, the drive level is asserted low with the intention of turning off the MOSFET. Similarly, due to the presence of the equivalent capacitance at the gate, U_{GS} can only decrease slowly. The MOSFET's on-state will not change before U_{GS} drops to its threshold $U_{GS(TH)}$.
5. At t_4, the voltage U_{GS} drops to its threshold, and the MOSFET starts the turn-off process. The time period from t_3 to t_4 is called the turn-on delay time $t_{d(off)}$, representing the delay from the switch "being turned off" until it "enters the off-state".
6. At t_5, U_D reaches its maximum, and I_D reaches its minimum. The MOSFET completes its turn-off process. The period from t_4 to t_5 is called the fall time t_f, representing the time required for the current I_D to fall to its minimum.

As described in the datasheet for MOSFETs, the quality of the parameters shown in **Figure 294** determines the switching speed. Obviously, the smaller the gate charge is, the higher the switching speed can be.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_D = 11A		4	5.2	nC
Q_{gd}	Gate Charge Gate to Drain			1		nC
Q_{gs}	Gate Charge Gate to Source			1.3		nC
$Q_{g(th)}$	Gate Charge at Vth			0.65		nC
Q_{oss}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		7.3		nC

Figure 294. *Gate Charge Parameters of a MOSFET*

MOSFET Driver

MOSFET driver falls into the realm of power technology. Novices often fall into two extremes:

1. It is taken for granted that the MOSFET is in the switching state, and the switching waveform is perfectly consistent with the control signal.
2. Regardless of the circumstances, always opt for the most expensive and top-tier dedicated driver chips to drive MOSFET.

The simplest method to verify whether any power electronic switch has sufficient drive capability is to construct a test circuit as shown in **Figure 295**, using an oscilloscope to observe whether the UGS and ID waveforms align perfectly. How much current is enough to drive a MOSFET? This is related not only to the MOSFET itself, but also to the switching frequency of the circuit.

1. As shown in **Figure 295**, at 1MHz switching frequency and 200Ω drive internal resistance, the drain current I_D begins to drop before it rises to its maximum value. The switch never reaches full conduction (I_D should close to 100mA when fully being turned on).

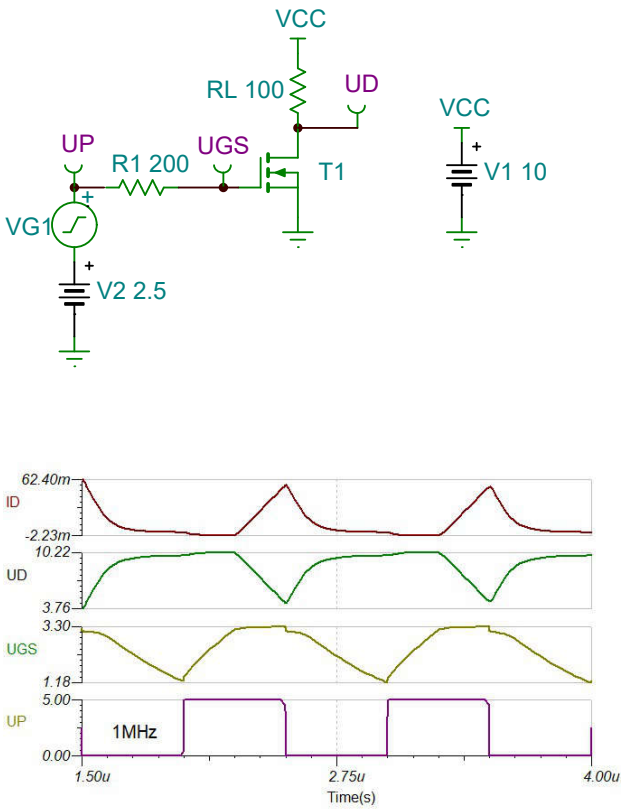
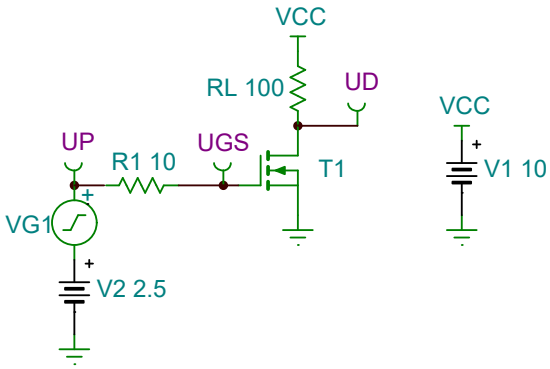


Figure 295. *High-Frequency and High-Internal-Resistance Driver Simulation*

2. As shown in **Figure 296**, the switching frequency is still 1MHz, but the drive internal resistance is reduced to 10Ω and the drain current I_D is basically kept as a square wave. However, it has been seen that the proportion of I_D turn-off "trailing" current duration in the cycle is quite significant, which means that even if the drive current is extremely high, there is still an upper limit to the switching frequency.



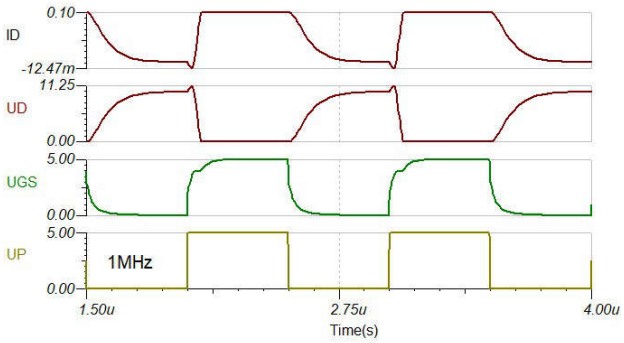


Figure 296. *High-Frequency and Low Internal-Resistance Drive Simulation*

3. As shown in **Figure 297**, the switching frequency is reduced to 100kHz, the drive internal resistance is reverted to 200Ω, and the drain current I_D basically maintains a good square wave. If other factors such as switching losses and delayed response are disregarded, such a drive is also considered acceptable. Note that U_{GS} waveform is not a perfect square wave. It exhibits not only rising and falling slopes but also a clearly visible Miller platform.

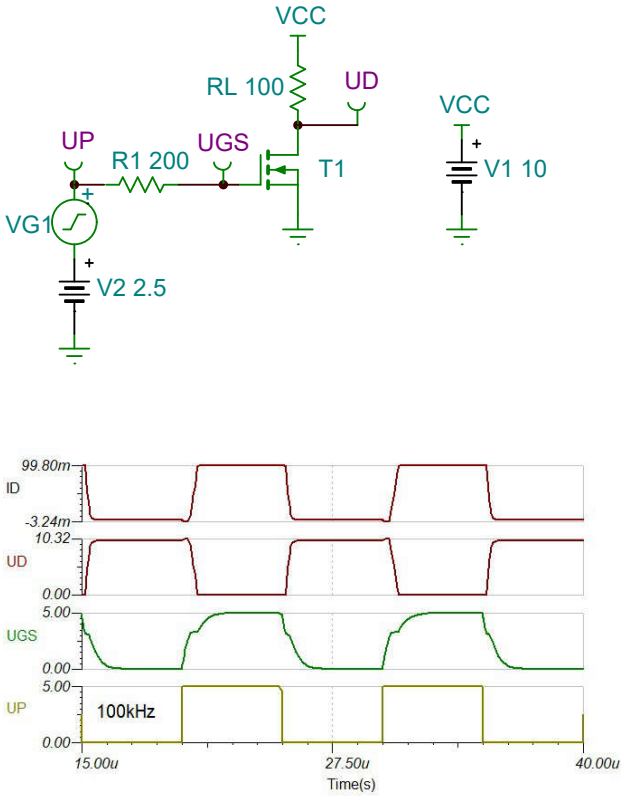


Figure 297. *Low-Frequency and High-Internal-Resistance Driver Simulation*

Is it the case that the greater the gate driver current, the better, that is, the lower the internal resistance of the driver circuit, the better? This can also be problematic. As shown in **Figure 298**, a quantitative simulation of the driver circuit is performed:

1. V_{G1} shows a 2.5V square wave with 500kHz amplitude, and it, together with the 2.5V DC voltage V_2, forms the square wave driver circuit.

2. R_1 represents the internal resistance of the driver circuit, L_1 represents the lead parasitic inductance, and C_1 emulates the gate capacitance of MOSFET.
3. The start and stop time of the simulated transient waveform in **Figure 298** is set between 1.5μs and 4μs, which shows that the gate voltage U_{GS} has a significant oscillation.
4. The hazard from oscillation can be fatal, as MOSFET is no longer operating in either fully ON or OFF state, but will repeatedly enter a high-resistance conduction state, which in turn leads to burnout due to high power loss and overheating.

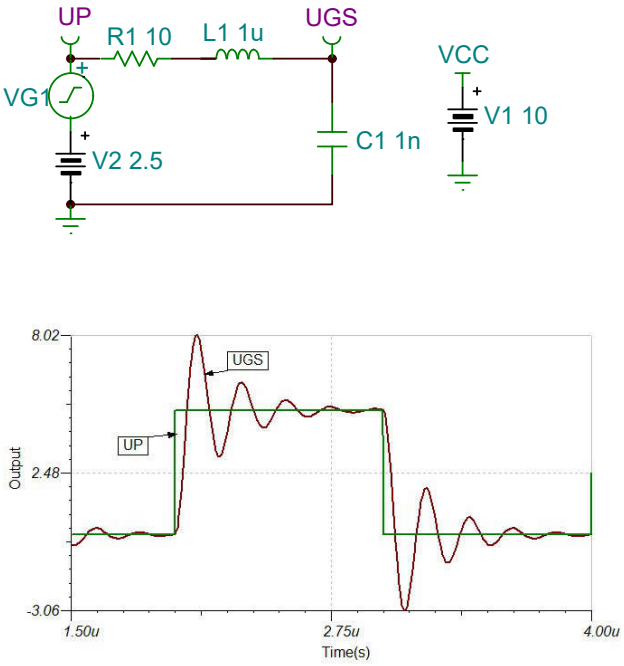
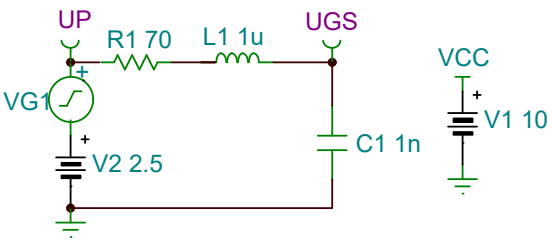


Figure 298. *Simulation of an Underdamped Oscillation in a Gate Driver Circuit*

The cause of oscillation is quite straightforward, that is, underdamped oscillation in RLC circuit.

1. The conductor inductance must be present, so the gate driver circuit is actually a RLC circuit.
2. Theoretical calculations show that when $R < 2\sqrt{\frac{L}{C}}$, it is called as underdamping, and oscillations will inevitably occur. Armed with this theoretical understanding, the solution is straightforward to make $R \geq 2\sqrt{\frac{L}{C}}$ and then eliminate the gate oscillation.
3. As shown in **Figure 299**, after changing R_1 to 70Ω, the oscillation disappears.



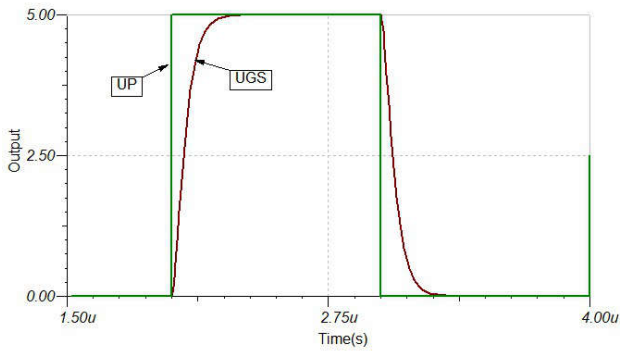


Figure 299. *Simulation of Overdamping in a Gate Driver Circuit*

4. Increasing the resistance will weaken the drive capability (current), so a good driver circuit should first minimize the lead parasitic inductance. When inductance cannot be further reduced, the expedient of adding resistors is employed as a stopgap measure.

The concept of damping is also prevalent in real life: Let's take a few examples to help understand the principle of damped oscillation:

1. In air or water, a pulled pendulum will definitely swing past the lowest point and generate oscillation. But what if the pendulum is placed in extremely viscous oil? Will it still oscillate? This is overdamping.
2. If we simply attach a spring to the door as a door closer, when releasing the door to close, it will inevitably slam heavily against the frame. This is known as the underdamped oscillation. A well-designed door closer should operate at a state of critical damping. It will neither slam against the door frame due to "underdamping" nor take an excessively long time to close, as if it were moving through extremely viscous oil.

Finally, it is crucial to emphasize that MOSFET gate driver voltage typically operates within a range of ±15V. Voltage levels that are either too high or too low are unacceptable.

1. The gate driver voltage must be sufficient to fully turn on MOSFET. Otherwise, MOSFET will act as a resistor with high resistance, and its power loss and heat will burn out MOSFET in a short period of time.
2. A negative voltage provided by the gate driver facilitates the rapid turn-off of MOSFET. However, neither the positive nor the negative driving voltage shall exceed ±20V limit; otherwise, the silicon dioxide insulating layer between the gate and the source will break down.

Synchronous Rectification

While it is quite easy to accept the use of MOSFETs as switches, diodes also function as switches in power electronics circuits. A conducting diode behaves as a closed switch, and a non-conducting diode acts as an open switch.

1. The voltage drop across a conducting diode is the primary source of loss in the low-voltage power supply circuit. Therefore, we generally use Schottky diodes with a lower voltage drop (about 0.5 V).
2. The loss from a Schottky diode is also unacceptable when the power supply circuit's output voltage is very low, such as 2.5V or 1.8V.

The method of using MOSFETs as diodes is called synchronous rectification. Which of the two equivalents shown in **Figure 300** is correct?

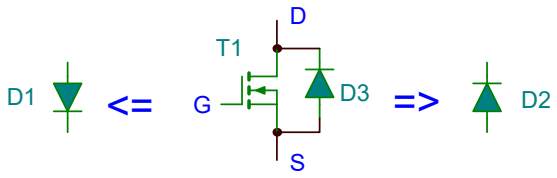


Figure 300. *Equivalent Circuits of Synchronous Rectifying MOSFET*

1. The MOSFET itself has a parasitic diode D3, so its current flows from D (Drain) to S (Source) in typical applications.
2. In typical applications where the current flows from D to S, when the MOSFET is used as a diode, its orientation should be as shown in D1. But in that case, due to the presence of the parasitic diode D3, the MOSFET would conduct bidirectionally, being equivalent to a conductor.
3. The correct solution is to place the MOSFET in the orientation as shown in D2. When D3 "is about to" conduct, a GS control voltage is applied, forcing the current to flow from S to D. Since the voltage drop between S and D is extremely small (because R_{DS} is extremely small), D3 will not conduct, and the equivalent diode of the MOSFET will also exhibit an extremely small voltage drop.

The analysis of **Figure 300** reveals that "synchronous control" of the MOSFET's GS terminal is required to achieve a "micro-voltage-drop" diode (otherwise, the diode would conduct bidirectionally). This is why the aforementioned circuit is called a synchronous rectifier.

Chopper Circuits

The apparatus that converts parameters such as voltage and frequency of a power supply is called the converter. To convert the voltage of AC power, we can easily think of using a transformer. But what should be used when we need to convert the voltage of DC power or the frequency of AC power?

1. Even before the advent of power electronic switches, there was a demand for "power conversion". At that time, "power conversion" was achieved through the combination of an electric motor and a generator. This combination is known as a converter set. For example, to convert DC power to AC power, one can use a DC motor driven by DC power to drive an alternator. Any power supply can be converted to another type of power supply through the combination of a motor and a generator.
2. Although the converter sets were "versatile" and "robust", their drawbacks were obvious - their mechanical devices are inefficient and noisy. After the advent of power electronic switches, the power converter fully entered an era of "static conversion" (in contrast to converter sets). The chopper circuit, as the simplest type of static converter, established the dominant position of switching power supplies.

Buck Chopper Circuit

Imagine an occasion where a room only needs 1kW heating power, yet only a 2kW electric heater is available. Could one achieve the effect of a 1kW heater by installing a switch to intermittently turn it on and off at several-minute intervals? This is one of the most modest models in the chopper circuit, as shown in **Figure 301**.

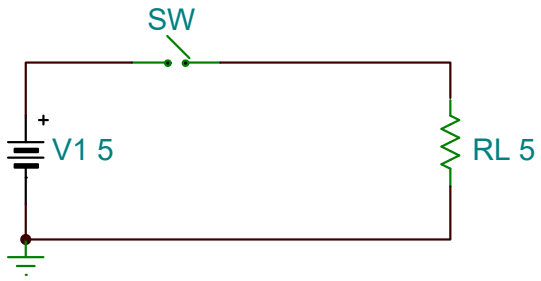


Figure 301. *The Simplest Switching Chopper Circuit*

A "hysteresis effect" load like a heater can tolerate intermittent current supply, but most loads, such as electric lamps, circuits like **Figure 301** cannot be used. How can current be made continuous? Among 3 common passive electronic components, the function of inductance is to ensure current continuity.

1. As shown in **Figure 302**, connecting the inductance L in series at the load terminal guarantees continuous current flow through the load.

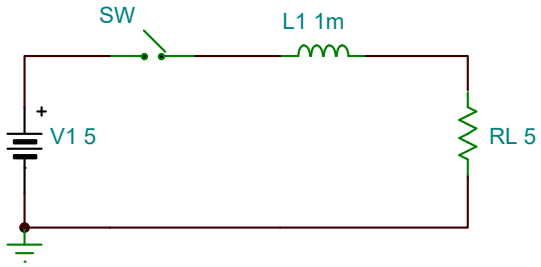


Figure 302. *Chopper Circuit with Series Load and Inductor*

2. In the circuit shown in **Figure 303**, when SW switch is open, to satisfy the requirement that the inductor current must remain continuous, the inductor generates a high voltage until it breaks down SW switch. Therefore, an inductive circuit needs to provide an additional path for the discharge of the inductor current. D_1 diode as shown in **Figure 303** acts as a continuous inductor current, becoming a freewheeling diode.

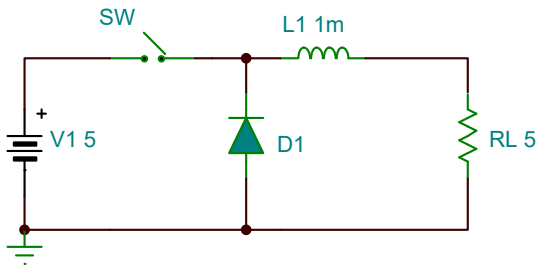


Figure 303. *Chopper Circuit with Freewheeling Diode*

3. In the main circuit of power electronics, the diode is also a type of switch (its conduction voltage drop can generally be neglected). All the methods for analyzing switches are the same: a conducting switch is equivalent to a conductor, while a disconnected switch is treated as if the component were removed. Thus, analysis of **Figure 303** schematic becomes an examination of whether the diode is equivalent to a conductor.
4. Refer to **Figure 303**. When SW switch is closed, diode D_1 is exposed to reverse voltage, so D_1 is removed. The equivalent circuit at this point is shown in **Figure 304**. The power supply V_1 powers the load R_L through the inductor L_1 and the current ramps up.

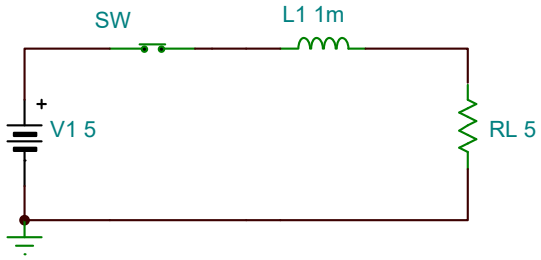


Figure 304. *Equivalent Circuit When the Switch is Closed*

5. Refer to **Figure 303**. When SW is off, SW is removed and D_1 is turned on, which is equivalent to a conductor. The equivalent circuit is shown in **Figure 305**. The current on L_1 is gradually reduced and the current energy is derived from the magnetic field energy stored by the inductor. And D_1 guarantees that the inductor current forms a loop.

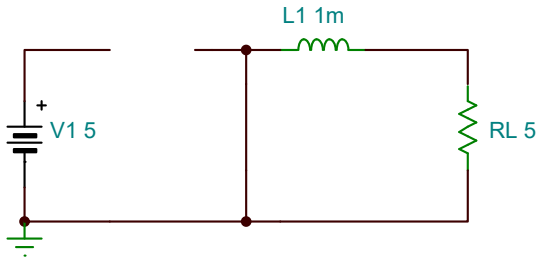


Figure 305. *Equivalent Circuit When the Switch is Open*

6. In all circuits where the output is a voltage source, the bulk capacitors are connected in parallel at the load terminals to ensure the effect approximates that of a voltage source as closely as possible. As shown in **Figure 306**, the output filter capacitor C_1 is added and the mechanical switch SW is replaced with MOSFET switch T_1, which constitutes the main circuit of a complete Buck chopper circuit.

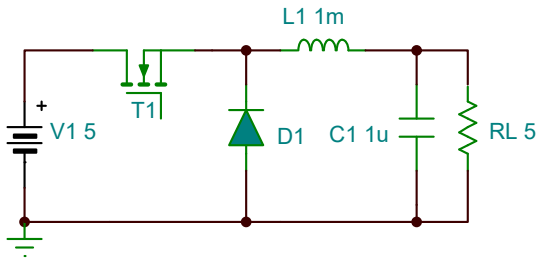


Figure 306. *Complete Main Buck Chopper Circuit*

When the inductor current is continuous in a chopper circuit, there is a simplified method for calculating output voltage:

1. The average current through the capacitor in steady state is zero. If charging exceeds discharging within a cycle, the voltage across the capacitor will rise, which is not a steady state; if discharging exceeds charging within a cycle, the voltage across the capacitor will fall, which is also not a steady state.
2. What is really useful for chopper circuit calculations is actually another conclusion: The average voltage across the inductor is zero in steady state. To make this "conclusion" more palatable, the capacitor was cited earlier as an example, as the characteristics of inductors and capacitors are perfectly symmetrical. If the average voltage across the inductor is not zero, the inductor current rises or falls, which is not a steady state.
3. By calculating the voltage U_{L_ON} across the inductor when the switch is closed and the voltage U_{L_OFF} across the inductor when the switch is open, the output voltage can be readily determined.

Assuming a well-designed chopper circuit with a small ripple voltage, the output voltage UO is essentially constant voltage:

1. When the switch is closed, the voltage U_{L_ON} on the inductor, referring to the reference voltage direction shown in **Figure 307**, is:

$$U_{L\_ON} = E - U_O \tag{124}$$

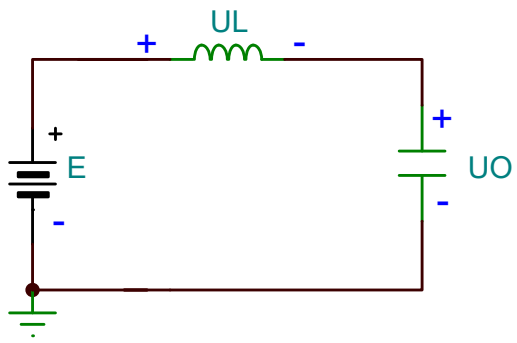


Figure 307. *Inductor Equivalent Circuit When the Buck Circuit Switch is Closed*

2. When the switch is open, the voltage U_{L_OFF} on the inductor, referring to the reference voltage direction shown in **Figure 308**, is:

$$U_{L\_OFF} = -U_O \text{ (5.2)} \quad (125)$$

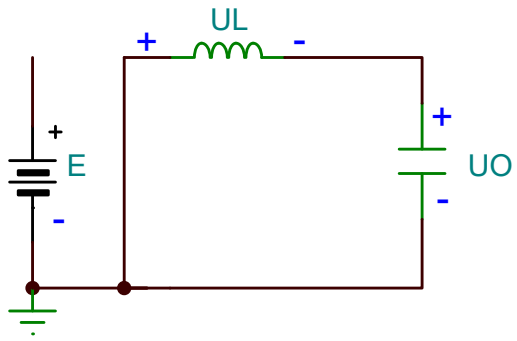


Figure 308. *Inductor Equivalent Circuit When the Buck Circuit Switch is open*

3. Based on the characteristic that the average voltage across the inductor is zero during steady state, **Equation 126** can be deduced, where D denotes the duty cycle. It can be seen from **Equation 128** that Buck circuit is a step-down circuit with the output voltage proportional to the duty cycle of the switch (when the inductor current is continuous).

$$U_{L\_ON} \times T_{ON} + U_{L\_OFF} \times T_{OFF} = 0 \quad (126)$$

$$(E - U_O) \times T_{ON} + (-U_O) \times T_{OFF} = 0 \quad (127)$$

$$U_O = \frac{T_{ON}}{T_{ON} + T_{OFF}} E = DE \quad (128)$$

4. If the inductor L current is discontinuous, T_{OFF} period needs to be analyzed in two segments. During the period T_{OFF1} when current flows through the inductor, the inductor voltage is –Uo. During the period T_{OFF2} when no current flows

through the inductor, the inductor voltage is 0 (at this time the load is powered by the filter capacitor). As derived from Equation 5.5, the output voltage U_O can be higher.

$$U_{L\_ON} \times T_{ON} + U_{L\_OFF} \times T_{OFF1} + 0 \times T_{OFF2} = 0 \quad (129)$$

$$(E - U_O) \times T_{ON} + (-U_O) \times T_{OFF1} = 0 \quad (130)$$

$$U_O = \frac{T_{ON}}{T_{ON} + T_{OFF1}} E > \frac{T_{ON}}{T_{ON} + T_{OFF1} + T_{OFF2}} E = DE \ (5.5) \quad (131)$$

Although the straightforward derivation of the output voltage formula **Equation 131** does not involve the specific values of L, C, and f (switching frequency), in actual Buck circuits, L, C, and f are not arbitrarily selected. The TINA simulated circuit shown in **Figure 309** will quantitatively analyze the impact of component parameters on the Buck circuit.

1. For simplicity, time switch SW1 is used to simulate MOSFET switching, the duty cycle of the time switch is set to 0.6, and the specific switching frequency is set according to simulation requirements.
2. The filter capacitor C_O is connected in series with resistor R_{CS} to simulate the equivalent series resistance of the capacitor. Although TINA allows setting the parameters of equivalent series resistance of the capacitor, directly connecting a resistor in series provides a more intuitive simulation approach.

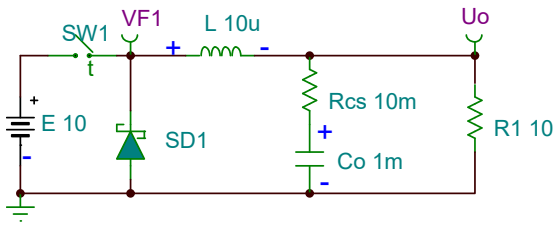


Figure 309. *TINA Simulation of Buck Circuit*

First, simulate the effect of equivalent series resistance RCS of the filter capacitor on the output voltage ripple.

1. The switching frequency remains at 1MHz while monitoring the diode cathode voltage V_{F1} and the output voltage U_O.
2. If the voltage on VF1 shows a perfect square wave, this indicates that the inductor current is continuous. When SW1 is closed, V_{F1} voltage must be 10V. However, when SW1 is disconnected, V_{F1} voltage will remain close to 0V (ignoring the diode voltage drop of S_{D1}) only if the inductor current is continuous.
3. As shown in **Figure 310**, V_{F1} voltage shows a perfect square wave, so the inductor current is continuous. Taking the value of R_{CS} to be 100mΩ, it can be seen that the ripple voltage of U_O is obvious. Further analysis shows that U_O output increases when SW1 is closed; U_O output decreases and presents in a sawtooth shape when SW1 is off. The source of ripple voltage is the voltage drop of sawtooth ripple current on R_{CS}.

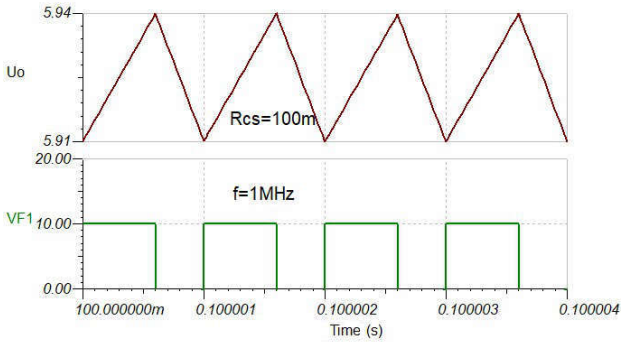


Figure 310. *Output Ripple with 100mΩ Equivalent Series Resistance*

4. As shown in **Figure 311**, no other parameters change, R_{CS} will be 10mΩ and the ripple voltage will be significantly reduced. The above analysis demonstrates that the effectiveness of DC power supply filter capacitors is not solely determined by their capacitance value, but is directly related to their equivalent series resistance. For capacitors in the same type, the higher capacitance value, the lower equivalent series resistance. The equivalent series resistance of tantalum capacitor in the same capacitance is significantly smaller than that of aluminum electrolytic capacitor, which is the root cause of good filtering effect of tantalum capacitor.

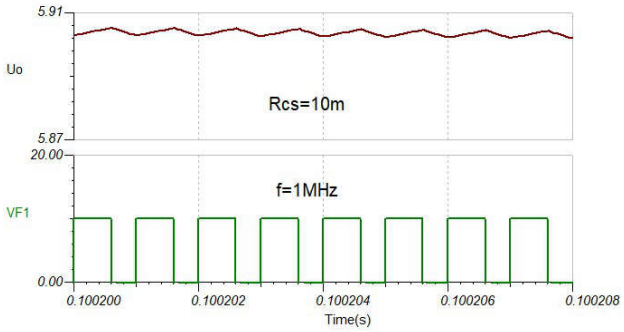


Figure 311. *Output Ripple with 10mΩ Equivalent Series Resistance*

In either **Figure 310** or **Figure 311**, the waveform of VF1 remains a perfect square wave, indicating that inductor current is continuous and an output voltage value closes to the theoretical value of 6V. Let's discuss the scenario where inductor current is discontinuous.

1. As shown in **Figure 312**, the switching frequency is reduced to 100kHz, and the waveform of VF1 is no longer a perfect square wave, which indicates the discontinuity of the inductor current.
2. While R_{CS} is taken to be 10mΩ, the ripple voltage is comparable to that observed with **Figure 310**: 100mΩ. This occurs because the switching frequency has been reduced by a tenfold (10), prolonging the duration of current fluctuations and increasing the peak value of ripple current. Consequently, the ripple voltage also increases, broadly adhering to a tenfold relationship.
3. The output voltage U_O reaches 7.1V, which is higher than the theoretical value 6V when the inductor current is continuous, consistent with the preceding analysis.
4. In **Figure 312**, during the hiccup period in the inductor current, the voltage V_{F1} rings, with a trend to be equal to U_O. When the inductor current no longer changes, U_L voltage is zero and V_{F1} voltage is equal to U_O.

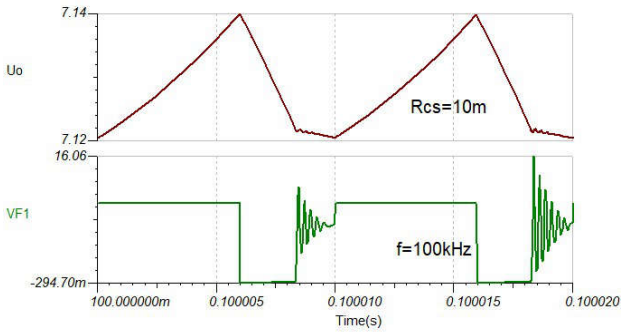


Figure 312. *Simulated Transient Waveforms at 100kHz Switching Frequency*

5. As shown in **Figure 313**, the switching frequency is reduced further and the inductor current hiccups for a longer time. This more clearly demonstrates that U_O output voltage reaches 9V, deviating further from the "theoretical value" of 6V. During the current hiccup period, the voltage V_{F1} remains at 9V after experiencing ringing until SW1 is closed again, clamping the voltage to the input voltage of 10V.

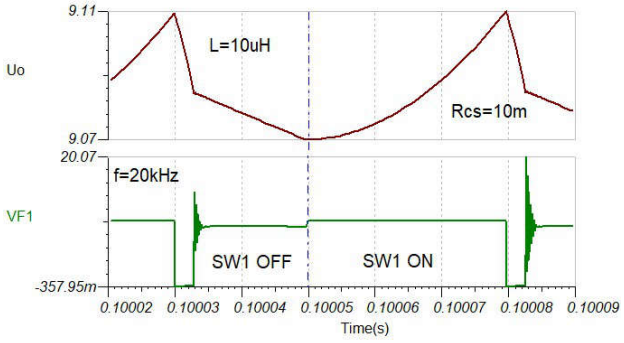


Figure 313. *Simulated Transient Waveform at 20kHz Switching Frequency*

Figure 312 and **Figure 313** demonstrate that the switching frequency influences whether the inductor current remains continuous. This occurs because the decay rate of the inductor current is constant with fixed values for the inductor, filter capacitor and load. A higher switching frequency results in a shorter SW1 off-time, making it more difficult for the inductor current to decay to zero, thereby maintaining current continuity. The following simulation will achieve continuous inductor current by modifying the inductance L.

1. As shown in **Figure 314**, increase inductance L to 1mH while maintaining 20kHz switching frequency.
2. The inductor current decay equation is shown in **Equation 132**. The higher the inductance, the smaller the current decay rate. Therefore, the inductor current can be continuous by increasing the inductance even if the switching frequency is not high.

$$u_L = L\frac{di}{dt} \Rightarrow \frac{di}{dt} = \frac{u_L}{L} = \frac{-u_O}{L} \quad (5.6) \tag{132}$$

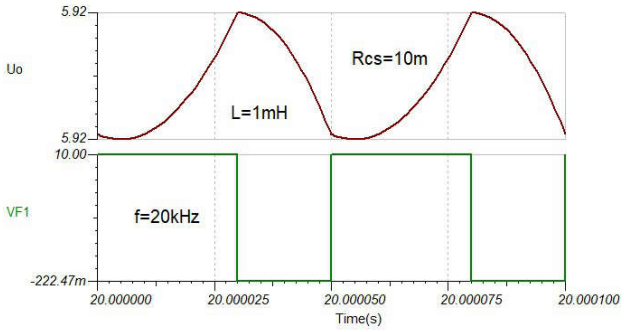


Figure 314. *Simulated Transient Waveforms at 1mH Inductance*

To summarize the discussion above: While we generally expect the inductor current to be continuous, factors such as inductance value, filter capacitance, switching frequency, and even load conditions influence whether the inductor current remains continuous.

1. The larger the inductance value, the slower the current decays and the easier the current is to be continuous.
2. The higher the switching frequency, the shorter the T_{OFF} absolute time and the easier the current is to be continuous.
3. The heavier the load (the smaller the resistance value), the larger the initial value of inductor current and the easier the current is to be continuous. Imagine an extreme scenario where if the load is open-circuited, the inductor current will be zero even when the switch is closed, let alone when it is open. This conclusion is left for the reader to simulate independently.

Charge Pump Circuits

Although the input-output voltage relationship of the Buck circuit is derived through extensive quantitative calculations, the principle behind the Buck chopper circuit is not difficult to grasp - it essentially involves the power supply alternating between providing power and resting. Before introducing a boost circuit, take a look at the principles for the charge pump circuit and get some inspiration.

A brainteaser can illustrate what a charge pump is. The topic is how to get 10V with 1 5V battery and 2 capacitors. The solution involves connecting the two capacitors in series and charging them sequentially from the same battery to achieve 10V.

As shown in **Figure 315**, the charge pump can be simulated with TINA, and power supply V1 charges C1 and C2 in time by time-switching.

1. To simplify drive control, the simulation employs time switches SW_1~SW_4 to manage charging. SW_1 and SW_2 are set of switches that charge C_2; SW_3 and SW_4 are set of switches that charge C_1.

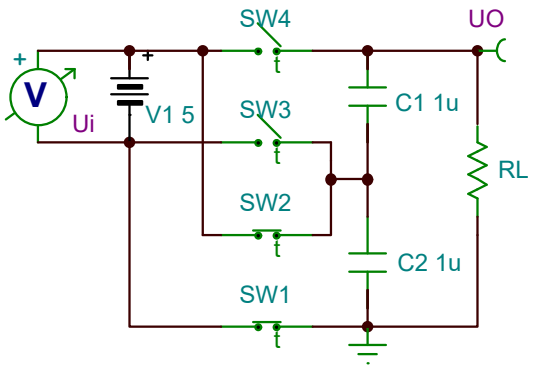


Figure 315. *Charge Pump Boost Circuit*

2. The timing control switch parameters are set as shown in **Figure 316**, with a control period of 200ns and two sets of switches turning on in complementary 90ns with a 10ns "dead time".

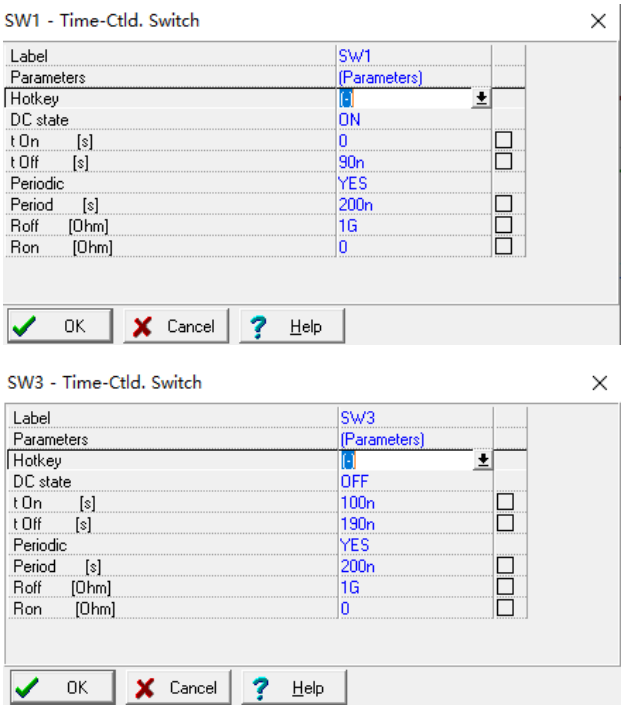


Figure 316. *Time Switch Settings Parameters*

3. Both capacitors are charged from a 5V power supply. Regardless of load effects, it would result in each capacitor charging to 5V, yielding an output voltage U_O of 10V. However, the load discharges the capacitors, producing a sawtooth discharge curve. **Figure 317** shows the actual output voltage U_O waveforms with a 10Ω load and a 1Ω load, where the heavier the load, the more visible the sawtooth, the worse the "constant voltage" effect.

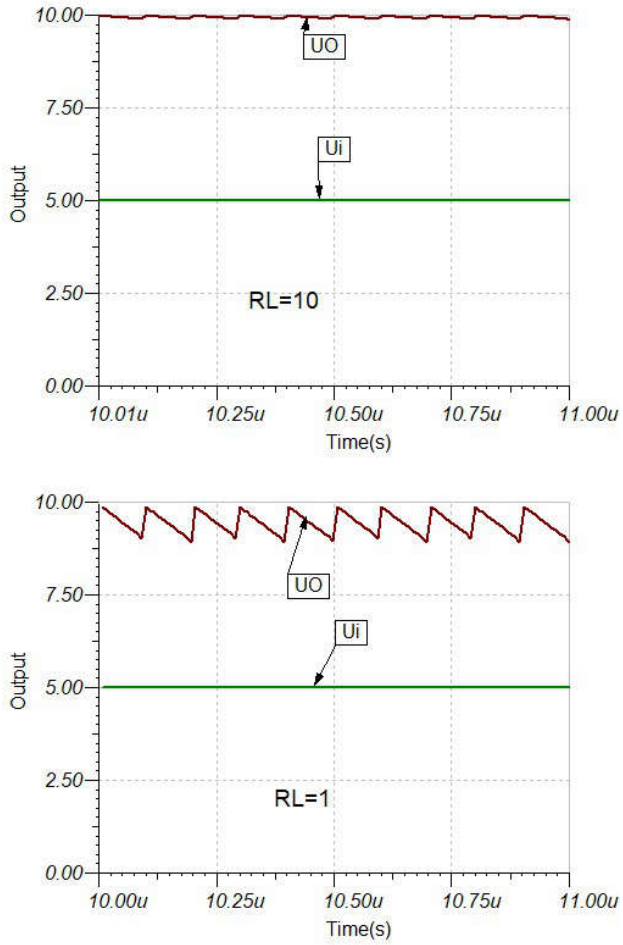


Figure 317. *Output Waveforms at Different Loads*

By increasing the number of switches and capacitors, it is straightforward to achieve voltage outputs 3 times or more the original value. Negative voltages can also be obtained, as demonstrated in **Figure 318**.

1. The settings parameters for each time switch in **Figure 318** are the same as shown in **Figure 316**. SW1 and SW2 charge capacitor C_{fly} with a left-positive and right-negative voltage, while SW3 and SW4 carry the charge of C_{fly} to C_1 to form a bottom-positive and top-negative voltage U_O.

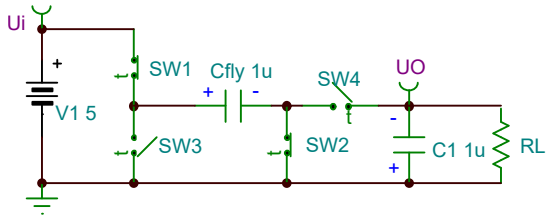


Figure 318. *Reverse Voltage Type Charge Pump Circuit*

2. The output of a charge pump circuit must not be connected to an excessively heavy load; typically, the output current of integrated charge pump power supply chips remains below 100mA. **Figure 319** shows the waveforms of the output voltage U_O at different loads of the reverse voltage type charge pump circuit.

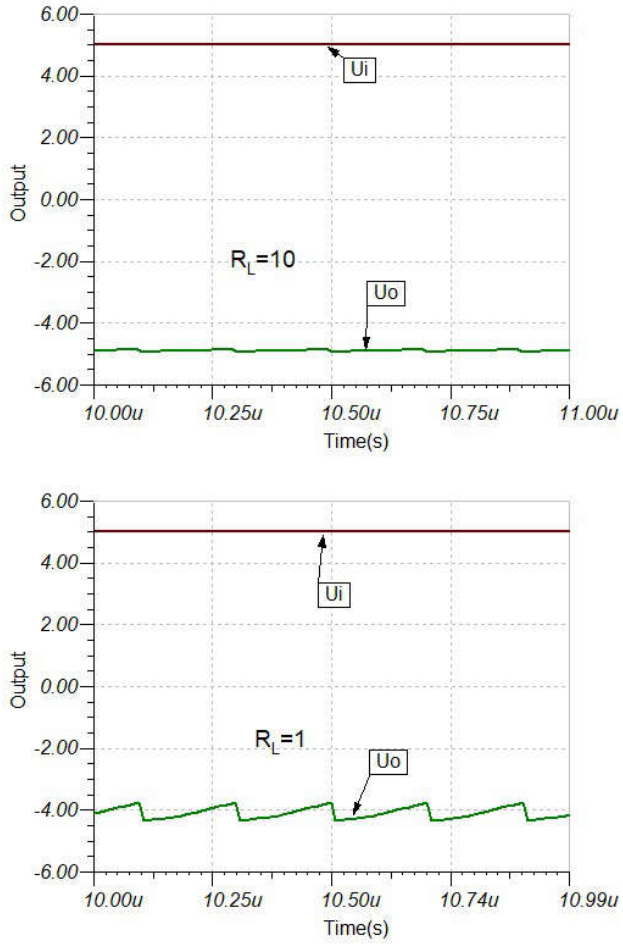


Figure 319. *Reverse Voltage Charge Pump Output Waveforms at Different Loads*

Although the principle for charge pump circuit may seem simple, the numerous switches involved complicate drive implementation (high-side drive issues will be addressed in the following section). Consequently, they are typically employed only within integrated power supply chips.

Boost Chopper Circuit

The capacitor within the charge pump provides a valuable insight that a capacitor can sustain voltage after only a brief charging period. The circuit shown in **Figure 320** is one of the fundamental schematic that make up the Boost chopper circuit: the peak voltage sample-and-hold circuit.

1. As shown in **Figure 320**, the capacitor is charged by a diode with square wave, sine wave, triangle wave. Regardless of the power supply waveform, there is always a voltage peak on the capacitor.

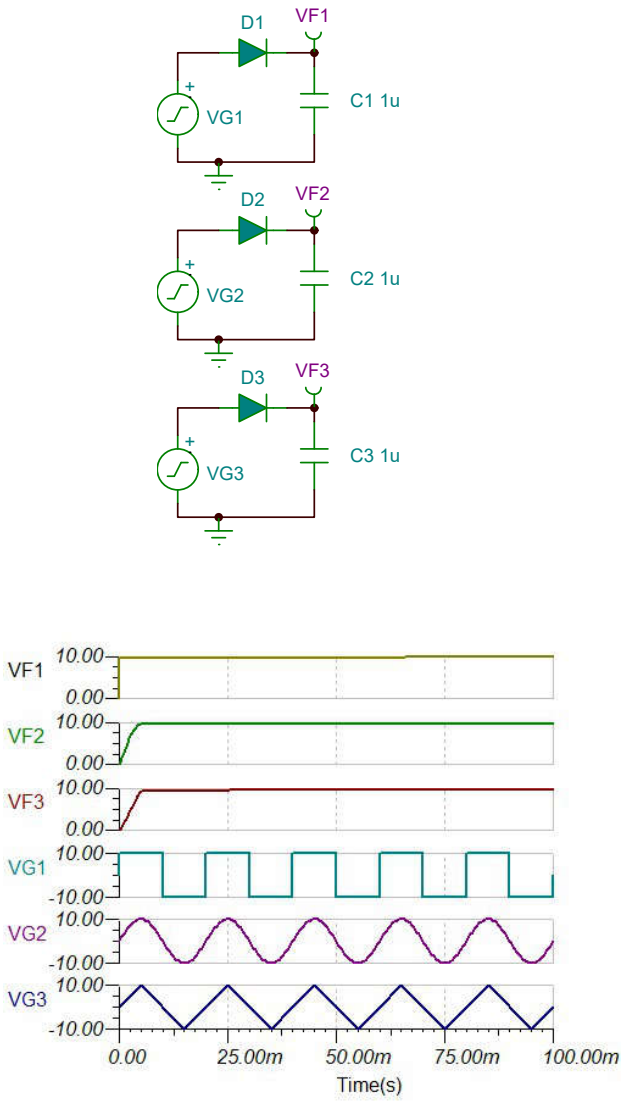


Figure 320. *Peak Voltage Hold Circuit*

2. As shown in **Figure 321**, this depicts the behavior of the peak voltage hold circuit when loaded. The heavier the load, the faster the voltage decays. To achieve effective peak voltage hold, the time constant of RC circuit must be substantially greater than the repetition period of the input signal.

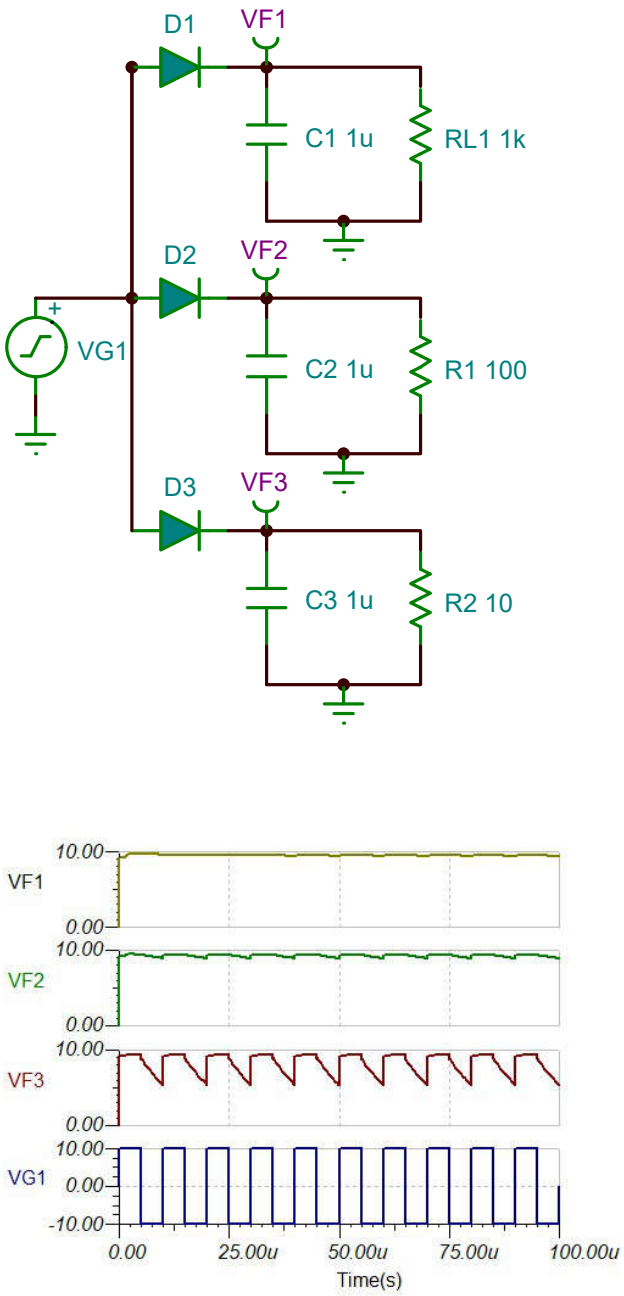


Figure 321. *Impact of Load on Peak Voltage Hold Circuit*

For Boost circuit, once the peak voltage hold circuit is established, the next step is to get the high voltage for a short time. Of the three basic components, resistors can only divide voltage (buck), and the characteristic of the capacitor is to maintain the voltage, and only the inductor can generate high voltage. Examples of high voltages generated by the inductors are frequently encountered in daily life, such as electrical sparks generated by switches, plugs, and so on.

1. As shown in **Figure 322**, when switch SW1 is closed, current flows through the inductor L_1. When SW1 is opened, the inductor current abruptly drops to zero, which is not allowed. A voltage on L_1 in the same direction as V_1 is generated, attempting to maintain the current unchanged. If SW1 is a semiconductor switch, it will be easily broken down. If SW1 is a mechanical switch, the high voltage on L_1 will ionize the air, thereby generating an electric spark.

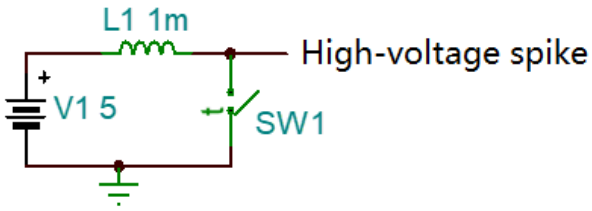


Figure 322. *Circuit for Generating High Voltage Using Inductance*

2. An electric spark is usually harmful and the temperature of the spark is sufficient to melt the metal contacts locally. However, if the high-voltage component of the inductor **Figure 322** is extracted with a "peak voltage hold circuit" (**Figure 321**), it becomes a Boost chopper circuit as shown in **Figure 323**.

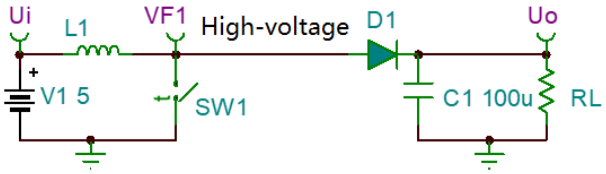


Figure 323. *Boost Chopper Circuit*

By utilizing the characteristic that the average voltage across the inductor terminal is zero during steady-state operation, the relationship between the input and output voltages of a Boost circuit can likewise be readily derived.

1. When the switch is closed, the Boost equivalent circuit is shown in **Figure 324** (Note the positive direction of each voltage). The voltage across the inductor during this phase is expressed as:

$$u_{L\_ON} = U_I \quad (5.7) \tag{133}$$

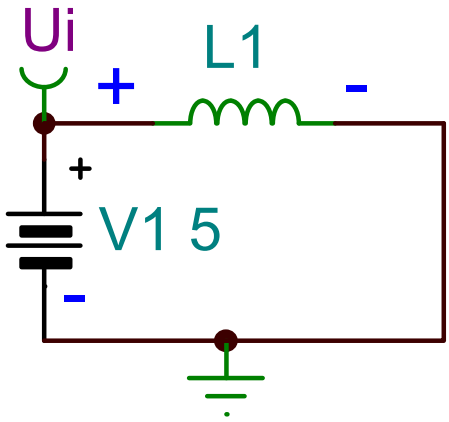


Figure 324. *Boost Equivalent Circuit When the Switch Is Closed*

2. The diode conduction voltage drop is generally ignored when analyzing the power electronics circuits principle. Thus, when the switch is turned off, the Boost equivalent circuit is shown in **Figure 324**. The voltage across the inductor during this phase is expressed as:

$$u_{LOFF} = U_I - U_O \tag{134}$$

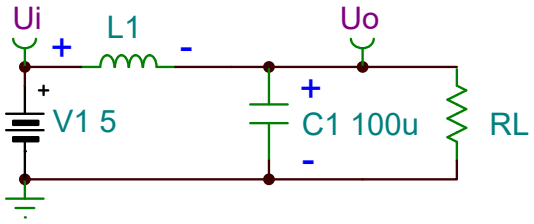


Figure 325. *Boost Equivalent Circuit When Switch Is Opened*

3. Given that the average voltage across the inductor terminal is zero, it yields **Equation 137**, and D in the equation is the duty cycle. Since D is less than or equal to 1, the Boost circuit is a step-up circuit. The larger the duty cycle, the higher the output voltage.

$$u_{LON} \times T_{ON} + u_{LOFF} \times T_{OFF} = 0 \tag{135}$$

$$U_I \times T_{ON} + (U_I - U_O) \times T_{OFF} = 0 \tag{136}$$

$$U_O = \frac{T_{ON} + T_{OFF}}{T_{OFF}} \times U_I = \frac{1}{1 - D} \times U_I \tag{137}$$

It is not possible to design and use the Boost circuit properly by merely understanding **Equation 137**. The transient behavior of the **Figure 325** Boost circuit shall be simulated below, considering aspects such as load conditions, inductance magnitude, and switching frequency. The simulation time interval is set to 1s or later, displaying waveforms after the circuit has fully stabilized.

High inductance and light load. Similar to a Buck circuit, a high inductance always guarantees continuous inductor current. **Figure 326** shows a transient simulation of the Boost circuit with a 1mH inductance, 1kΩ load, switching at 50kHz, and 60% duty cycle.

1. When the inductor L_1 current is continuous, the voltage waveform V_{F1} of the switch SW1 will be a square wave. When the switch is closed, V_{F1} voltage is zero; when the switch is turned off, the diode D_1 turns on and V_{F1} voltage will be higher than U_O voltage by one diode voltage drop. **Figure 326** when the switch is turned off, V_{F1} voltage is 12.54V and it is about 0.6V above the 11.95V U_O voltage, which is exactly the voltage drop in D_1 diode.
2. When SW1 is closed, the inductor L_1 stores energy, the load is supplied by C_1 and the voltage drops; when SW1 is opened, the inductor L_1 supplies the stored energy to the load and charges C_1, and U_O voltage rises; the ripple of U_O is very small (Approximately $2mV_{pp}$) because the load is very light (R_L is 1kΩ). The effect of C_1 equivalent series resistance on output ripple can be simulated and analyzed by yourself.

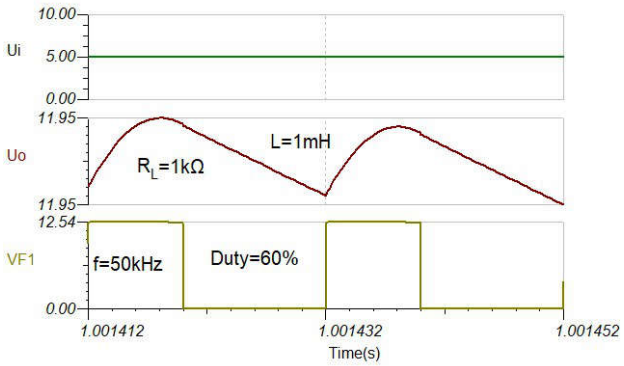


Figure 326. *Transient Simulation of a Boost Circuit with High Inductance and Light Load*

3. The theoretical value of the output voltage, calculated as shown in **Equation 138**, is 12.5V, and the difference is mainly caused by the voltage drop of the diode D_1. During the derivation of the formula **Equation 138**, D_1 was treated as a conductor without voltage drop when turning on. Considering a 0.6V voltage drop on D_1 (regular diode), the corrected U_O theoretical value is 11.9V, closely matching the simulation value.

$$U_O = \frac{1}{1-D} \times U_I = \frac{1}{1-0.6} \times 5 = 12.5V \tag{138}$$

As shown in **Figure 327**, those are the simulated transient waveforms under conditions of high inductance and heavy load. The output voltage exhibits significant ripple (approximately 1.5Vpp).

1. While the inductor current is continuous, the current at the load terminal of the Boost circuit (including filter capacitor and load) is discontinuous. Consequently, when the inductor ceases to supply the load, the load current is entirely sourced from the filter capacitor.
2. The load condition seriously affects the ripple of the output voltage, simply the heavier the load, the larger the ripple.

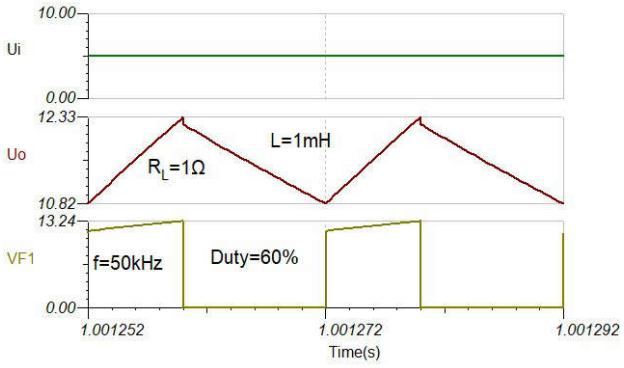


Figure 327. *Transient Simulation of a Boost Circuit with High Inductance and Heavy Load*

3. As shown in **Figure 328**, increasing the output filter capacitor C_1 will reduce the output voltage ripple. In general, the larger the RC time constant, the smaller the ripple voltage.

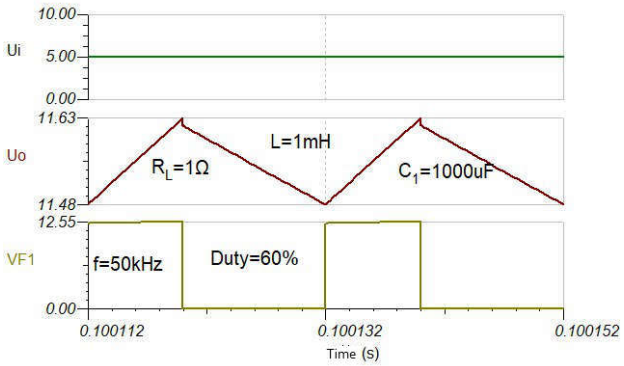


Figure 328. *Transient Simulation of a Boost Circuit with High Capacitance and Heavy Load*

The magnitude of inductance does not affect ripple. As shown in **Figure 329**, the inductance is reduced to 10uH, the capacitor C1 is remained at 100μF, and the ripple is similar to the one at 1mH inductance (approximately 1.5V).

1. When analyzing the cause of this phenomenon, one only needs to consider the period after switch SW1 closes. At this stage, the circuit operates purely as a RC discharge circuit, independent of inductance L. RC time constant determines the rate at which U_O decays. The duration for which SW1 remains closed corresponds to a proportional voltage drop in U_O.
2. The inductance acts upon the "RC load" during the turn-off phase of SW1. At steady state, the voltage U_O discharged from the capacitor is precisely recharged by the inductor. Therefore, once the discharge curve's "shape" is established, the charging curve's "shape" follows suit. Consequently, the magnitude of sawtooth ripple bears little relation to the inductance.

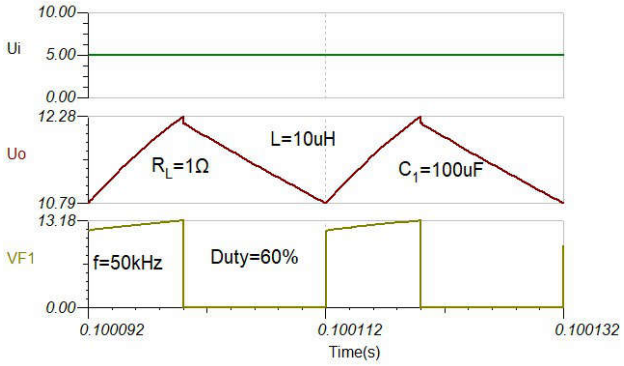


Figure 329. *Transient Simulation of a Boost Circuit with Low Inductance and Heavy Load*

The preceding analysis assumes that continuous inductor current is achievable with either high inductance or heavy load. Under light loads, insufficient inductance readily causes discontinuous inductor current. As shown in **Figure 330**, the load is 1kΩ and the inductance is reduced to 10μH.

1. First, it can be observed that the voltage of V_{F1} does not always "follow" the change of U_O during the turn-off phase. When diode D does not turn on, V_{F1} voltage will be indeterminate (after oscillation, closing to V_1).

2. The output voltage of U_O is much higher than the theoretical value of 11.9V. Similar to the process of derivation when the inductor current is discontinuous in the Buck circuit, T_{OFF} will consist of two periods, T_{OFF1} (inductance current present) and T_{OFF2} (inductance current absent). Equation 5.9 is corrected to be **Equation 139**.

$$U_O = \frac{T_{ON} + T_{OFF1}}{T_{OFF1}} \times U_I = \left(1 + \frac{T_{ON}}{T_{OFF1}}\right) \times U_I \tag{139}$$

3. Based on the estimated reading on **Figure 330**, T_{ON} time is about 7 times that of T_{OFF1}, so the output voltage, based on formula 5.11, should be 40V, which also roughly matches the simulation results (the difference stems from the **Equation 139** oscillation voltage which neglects V_{F1}).
4. Under no-load condition, T_{OFF2} will be significantly longer than T_{OFF1}, and U_O will create unintentional high-voltage, potentially causing breakdown of low-voltage-rated devices such as filter capacitors. Therefore, the Boost circuit must not operate under no-load conditions; it shall be connected to at least a high-resistance "dummy load".

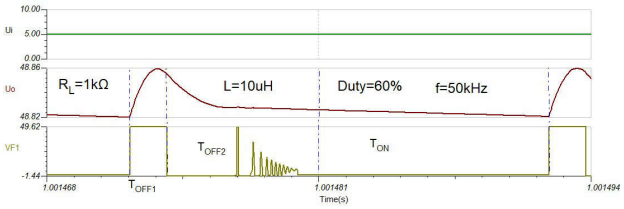


Figure 330. *Transient Simulation of a Boost Circuit with Low Inductance and Light Load*

Since inductive reactance and capacitive reactance are the fundamental physical quantities at work in the circuit, increasing the switching frequency invariably resolves the issue of limited component values (insufficient inductance or capacitance). As shown in **Figure 331**, by raising the switching frequency to 2MHz, the output voltage ripple remains exceptionally low despite the inductance L being merely 10μH and the filter capacitance C1 only being 100μF, with the inductor current remaining continuous.

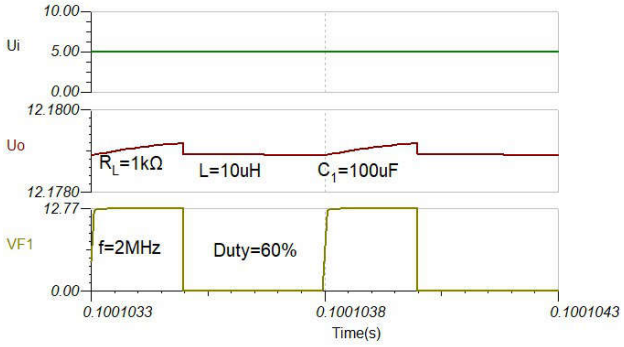


Figure 331. *Transient Simulation of a Boost Circuit with High-Frequency, Small Inductance and Light Load*

Buck-Boost Chopper Circuits

After studying the buck circuits and the boost circuits, it is time to move on to the buck-boost circuits. You might have such an idea: Wouldn't a circuit that cascades a Buck circuit and a Boost circuit be able to both step down and step up the voltage? While the Buck-Boost circuit is named so, attempting to deduce how to simplify the cascading of a Buck

circuit and a Boost circuit into a Buck-Boost circuit would be misleading. A Buck-Boost circuit is actually developed solely based on a Boost circuit and has nothing to do with the Buck circuit.

In the analysis of Boost circuit principles, the high-voltage generation circuit and peak voltage hold circuit, as shown in **Figure 332**, are used.

1. When switch SW1 is open, the voltage direction of U_L helps V_1 sustain the current, so it is the same as the direction of V_1. In other words, the voltage drawn from points A and B must be stepped up (higher than V_1). By connecting points A and B with points E and F, respectively, a Boost circuit is naturally formed.

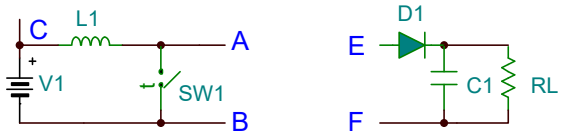


Figure 332. *High-Voltage Generation Circuit and Peak Voltage Hold Circuit*

2. If we do not extract voltage from points A and B but directly take the voltage across the inductor, it may not necessarily be a boost circuit. As shown in **Figure 333**, place the peak voltage hold circuit vertically, intending to connect points C to E and points A to F.

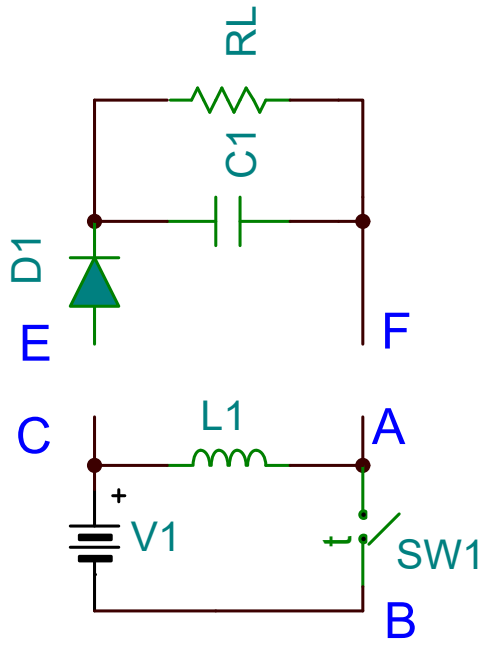


Figure 333. *Buck-Boost Circuit Prototype 1*

3. Further analysis reveals that when SW1 is open, the inductor current flows from C to A. If connected as shown in **Figure 333**, diode D_1 would block the inductor from charging C_1. Therefore, the orientation of the peak voltage hold circuit should be mirrored, as shown in **Figure 334**.

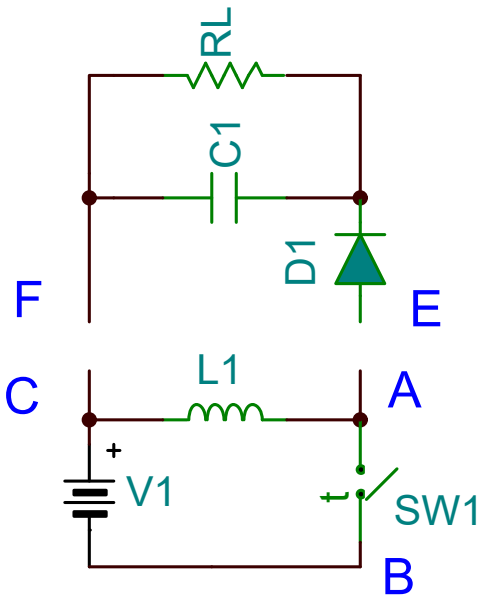


Figure 334. *Buck-Boost Circuit Prototype 2*

4. Connect points F to C and points A to E in the circuit shown in **Figure 334**, and "lay it flat" to obtain the circuit shown in **Figure 335**.

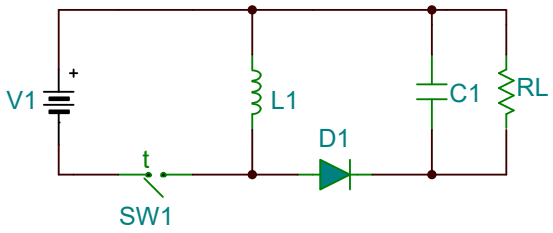


Figure 335. *Buck-Boost Circuit Prototype 3*

5. To enable the input and output voltages to share a "common ground", some adjustments are made to the circuit shown in **Figure 335** by moving both SW1 and D_1 to the upper part. It makes no difference for switch SW1 whether it controls the cathode or the anode of the power supply. However, when diode D_1 is moved to the upper part, its orientation should be adjusted accordingly.

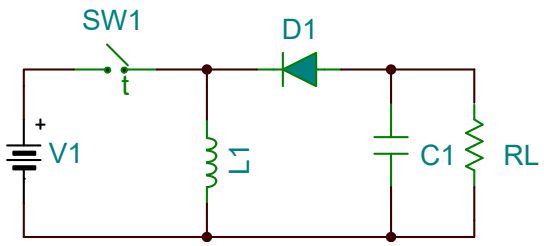


Figure 336. *Buck-Boost Circuit Prototype 4*

After annotating the input and output voltages and the ground, we eventually obtain the Buck-Boost circuit shown in **Figure 337**. It is in doubt whether this circuit can truly step the voltage up or down. Based on the positive direction shown in **Figure 337**, the expression for the voltage across the inductor can be given. By calculating the inductor voltage, the relationship between the input and output voltages can be determined.

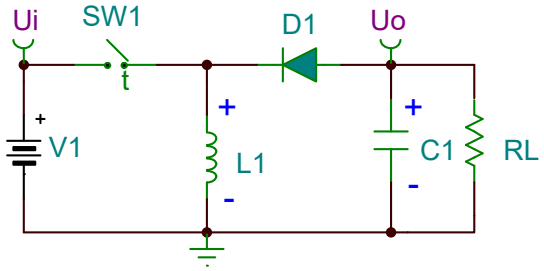


Figure 337. *Buck-Boost Circuit*

1. When the switch is closed, the equivalent circuit of the Buck-Boost circuit is as shown in **Figure 338**, and the expression for the inductor voltage is:

$$u_{LON} = U_I \tag{140}$$

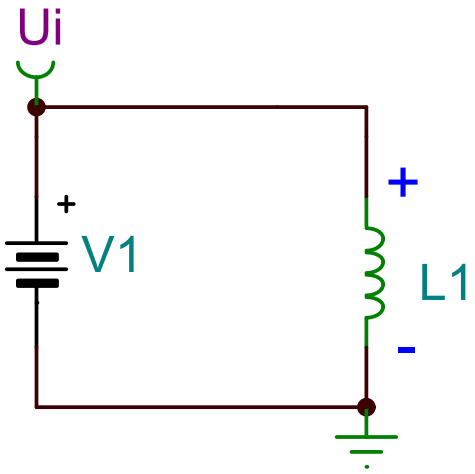


Figure 338. *Buck-Boost Circuit Equivalent Circuit When the Switch is Closed*

2. When the switch is open, the equivalent circuit of the Buck-Boost circuit is as shown in **Figure 339**, and the expression for the inductor voltage is:

$$u_{LOFF} = U_O \tag{141}$$

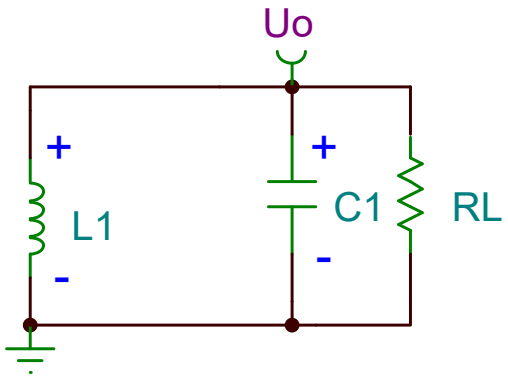


Figure 339. *Buck-Boost Circuit Equivalent Circuit When the Switch is Closed*

3. Based on the fact that the voltage across the inductor averages zero when the steady-state current is continuous, **Equation 144** can be obtained. The output voltage is determined by the on-off time ratio of the switch. It may be stepped up or down and is a negative output.

$$u_{LON} \times T_{ON} + u_{LOFF} \times T_{OFF} = 0 \tag{142}$$

$$U_I \times T_{ON} + U_O \times T_{OFF} = 0 \tag{143}$$

$$U_O = -\frac{T_{ON}}{T_{OFF}} \times U_I \tag{144}$$

Just now, we theoretically verified the characteristics of the Buck-Boost circuit through calculation, and we can also explain it qualitatively.

1. **Equation 139** for the output voltage in the Boost circuit can be transformed into **Equation 145**, which consists of two parts: U_I and U_L. The voltage for the Buck-Boost circuit is taken from U_L, so U_O in the Buck-Boost circuit should be given by **Equation 145**.

$$U_O = \frac{T_{ON} + T_{OFF}}{T_{OFF}} \times U_I = U_I + \frac{T_{ON}}{T_{OFF}} U_I \tag{145}$$

2. Analysis of the circuit shown in **Figure 339** reveals that after the switch is turned off, the current through inductor L should flow from top to bottom, which corresponds to charging the filter capacitor with a positive voltage at the bottom and a negative voltage at the top. Therefore, it's not surprising that the output voltage U_O is negative.

The Buck-Boost voltage circuit is developed based on the Boost circuit, so it cannot operate under no-load conditions, either. By referring to the analysis methods used for Buck and Boost circuits, you may independently conduct your own discussion and study on inductance, switching frequency, filter capacitance, and load conditions using TINA simulation.

Cuk Chopper Circuit

In power supply circuit design, the continuity of input and output currents serves as an indicator for assessing circuit quality. If the input current is continuous, it implies the power factor at UI terminal is relatively high and the harmonic interference to the upper-level power supply is low; while continuous output current indicates low output ripple and stable voltage at UO terminal.

1. The output current of the Buck circuit is continuous, but the input current is discontinuous. When the load terminal is directly connected in series with the inductor and the inductor current has no other branches, it implies that input current is continuous.
2. The input current to the Boost circuit is continuous, but the output current is discontinuous. When U_I terminal is directly connected in series with the inductor and the inductor current has no other branch, it implies that input current is continuous.
3. In Buck-Boost circuits, neither the input nor output current is continuous.

There is a type of chopper circuit that can achieve continuous input and output currents simultaneously, and it is the legendary Cuk circuit. Let's now attempt to "reconstruct" the design process of Cuk circuit.

1. The input current of the Boost circuit is continuous, so the input part of the Cuk circuit should resemble the circuit shown in **Figure 340** (the input part of Boost).

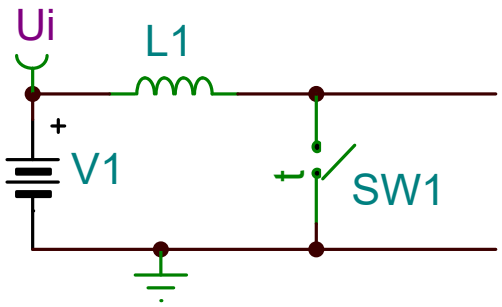


Figure 340. *Chopper Circuit Unit with Continuous Input Current*

2. The output current of the Buck circuit is continuous, so the output part of the Cuk circuit should resemble the circuit shown in **Figure 341** (the output part of buck). Judging by the diode orientation, the positive-voltage output is shown on the left and the negative-voltage output on the right in **Figure 341**, that is, the Cuk circuit can be either positive-voltage output or reverse-voltage output.

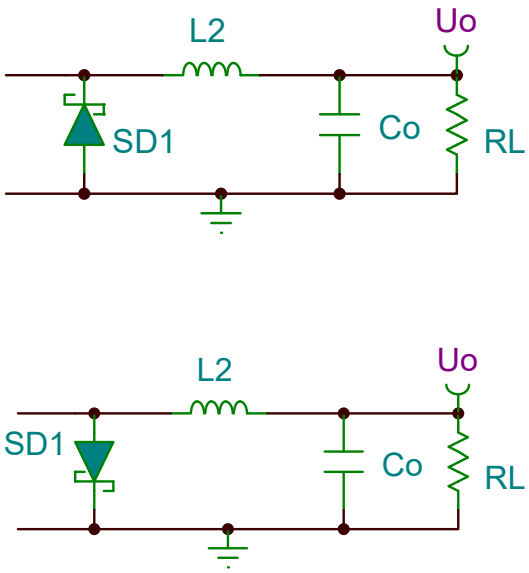


Figure 341. *Chopper Circuit Unit with Continuous Output Current*

Assuming the Cuk circuit operates with a positive output voltage, combining **Figure 340** and **Figure 341**, with a simple conductor connection between inductors L1 and L2, it will yield the **Figure 342** circuit.

1. A little analysis of **Figure 342** may reveal the problem. Since the average voltage on inductors L_1 and L_2 is zero in steady state, a direct conductor connection would imply that the input voltage U_I equals the output voltage U_O. Such a circuit lacks any voltage transformation capability and is clearly impractical. A potential difference must exist between L_1 and L_2.

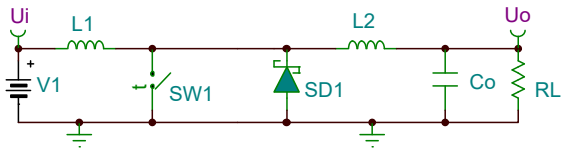


Figure 342. *Cuk Circuit Prototype 1*

2. Of the three basic components, the inductor acts as a conductor, and the resistor contributes directly to the power dissipation, and only the capacitor can create a voltage difference between the input and the output.

Assuming the Cuk circuit operates with a positive output voltage, connecting circuits in **Figure 340** and **Figure 341** using capacitors yields the Cuk circuit prototype shown in **Figure 343**.

1. By analyzing **Figure 343**, when the switch SW1 is closed and opened, the current direction on C_1 must alternate left and right (or vice versa). Otherwise, the voltage on C_1 could not remain stable under unidirectional current.
2. When the SW1 switch is closed, L_1 current must flows from left to right. Consequently, when the switch is open, L_1 current continues to flow from left to right. Similarly, the current on C_1 flows from left to right when the switch is open. Therefore, when the switch is closed, C_1 current should flow from right to left. The current mesh formed by C_1, SW1 and S_{D1} will be short-circuited if a counterclockwise current flows through it, so the circuit shown in **Figure 343** also has problems.

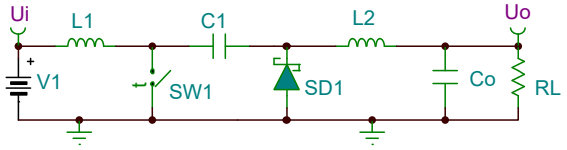


Figure 343. *Cuk Circuit Prototype 2*

At present, we can only assume the Cuk circuit operates with negative voltage output. By combining **Figure 340** with **Figure 341**, it yields the circuit shown in **Figure 344**, that is, Cuk circuit. When analyzing the working principle of a complex power electronic circuit, always keep in mind the rule that a closed switch acts as a conductor, while an open switch can be erased.

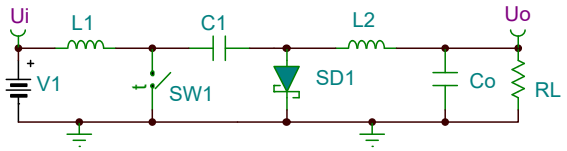


Figure 344. *Cuk Circuit*

1. When SW1 switch is closed, SW1 is replaced with a conductor, S_{D1} is erased, and the equivalent circuit of Cuk circuit is shown in **Figure 345**. V_1 and L_1 form a voltage loop, and the actual current must be clockwise; C_1, L_2,

and the load (C_O and R_L) form another voltage loop, and the actual current must be counterclockwise (the reason is analyzed in the **Figure 345** circuit, and C_1 current must be counterclockwise at this time).

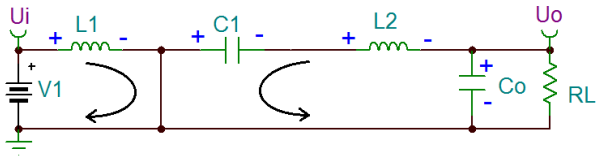


Figure 345. *Cuk Circuit Equivalent Circuit When the Switch is Closed*

2. When the switch is closed, the voltages across L_1 and L_2 can be expressed separately as **Equation 146** based on the positive directions for each component's voltage as indicated in **Figure 345**. Note that, compared with the three circuits introduced earlier, the calculation of the Cuk circuit involves one additional voltage equation for the inductor and one more unknown quantity for the capacitor voltage.

$$\begin{cases} u_{L1ON} = U_I \\ u_{L2ON} = -u_{C1} - U_O \end{cases} \tag{146}$$

3. When SW1 switch is open, SW1 is erased and S_{D1} is replaced with a conductor, the equivalent circuit of Cuk circuit is shown in **Figure 346**. V_1, L_1, and C_1 form one voltage loop, and the actual current must be clockwise (L_1 current direction does not change); L_2 and the load (C_O and R_L) form another voltage loop and the actual current direction must be counterclockwise (L_2 current direction does not change).

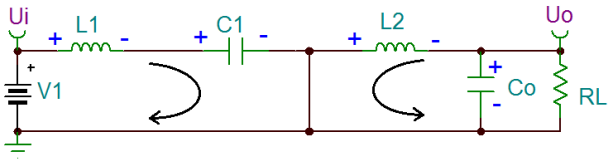


Figure 346. *Cuk Circuit Equivalent Circuit When the Switch is Open*

4. When the switch is open, the voltages across L1 and L2 can be expressed separately as **Figure 346** based on the positive directions for each component's voltage as indicated in **Equation 147**.

$$\begin{cases} u_{L1OFF} = U_I - u_{C1} \\ u_{L2OFF} = -U_O \end{cases} \tag{147}$$

5. By calculating the average voltages across L1 and L2 respectively, a system of linear equations with two variables will be obtained. Solve this system to derive **Equation 150**. The findings demonstrate that the Cuk circuit functions as a negative voltage output circuit, capable of both step-up and step-down conversion.

$$\begin{cases} u_{L1ON} \times T_{ON} + u_{L1OFF} \times T_{OFF} = 0 \\ u_{L2ON} \times T_{ON} + u_{L2OFF} \times T_{OFF} = 0 \end{cases} \tag{148}$$

$$\begin{cases} U_I \times T_{ON} + (U_I - u_{C1}) \times T_{OFF} = 0 \\ (-u_C - U_O) \times T_{ON} + (-U_O) \times T_{OFF} = 0 \end{cases} \tag{149}$$

$$\begin{cases} U_O = -\frac{T_{ON}}{T_{OFF}} \times U_I \\ u_C = \left(1 + \frac{T_{ON}}{T_{OFF}}\right) \times U_I \end{cases} \quad (150)$$

Readers may independently investigate simulations concerning inductance values, switching frequency, filter capacitance, and load conditions within the Cuk circuit using TINA simulation software. It is worth mentioning that Cuk circuit is theoretically perfect, but the parameters are difficult to set due to the complexity of the circuit. The most common chopper circuits are Buck, Boost and Buck-Boost.

Sepic and Zeta Chopper Circuit

The Cuk circuit features reverse-voltage output. As previously analyzed, achieving continuous input and output currents is challenging with forward-voltage output. Sepic and Zeta topologies within the basic chopper circuit can provide forward-voltage output, though only one current can be guaranteed continuous. Sepic circuit maintains continuous input current, while Zeta circuit maintains continuous output current.

Drawing upon the negative experience with Buck-Boost circuits, the unit with discontinuous input current are illustrated as shown in **Figure 347**; the unit with discontinuous output current are illustrated as shown in **Figure 348**, where the left side indicates negative output voltage and the right side indicates positive output voltage.

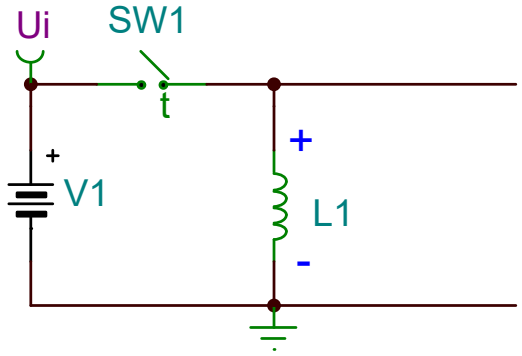
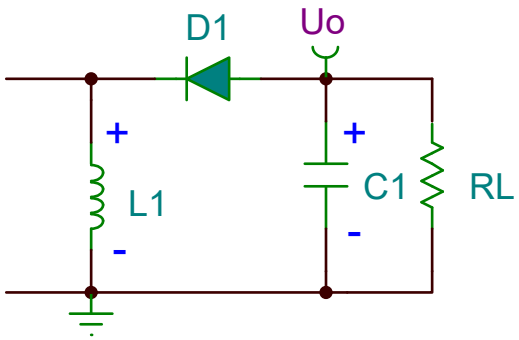


Figure 347. *Chopper Circuit Unit with Discontinuous Input Current*



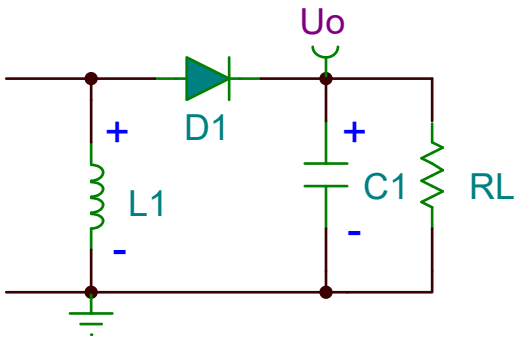


Figure 348. *Chopper Circuit Unit with Discontinuous Output Current*

Connecting the unit with discontinuous input current in **Figure 340** to the unit with continuous output current in **Figure 348** via capacitors forms a Sepic circuit, as shown in **Figure 349**. By setting up the system of equations for L1 and L2 voltages, as in the Cuk circuit, the output voltage UO of the Sepic circuit can be calculated. It differs from the Cuk circuit's UO expression only in sign, and this book shall not derive it further.

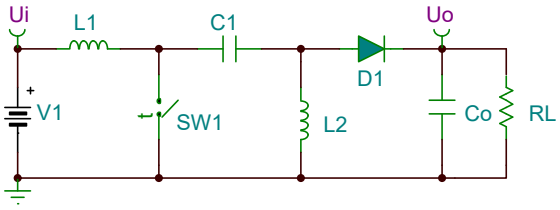


Figure 349. *Sepic Circuit*

Connecting the unit with discontinuous input current in **Figure 341** to the unit with continuous output current in **Figure 347** via capacitors forms a Zeta circuit, as shown in **Figure 350**. Zeta circuit output voltage UO expression is the same as that of Sepic circuit and it is no longer derived in this book.

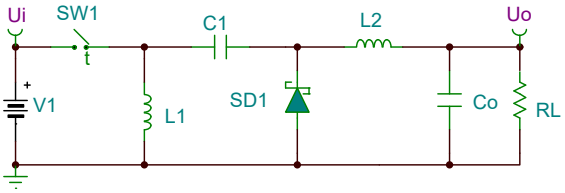


Figure 350. *Zeta Circuit*

Current Reversible Chopper Circuit

As we mentioned earlier, we discussed how the Buck-Boost circuit is somewhat misleadingly named, as it does not truly derive from combining Buck and Boost circuits. Indeed, another chopper circuit genuinely combines the principles of both Buck and Boost, yet it bears the name "current reversible chopper circuit".

The circuit shown in **Figure 351** is a current reversible chopper circuit, which is typically loaded with a DC motor or power supply. Since a rotating DC motor can be seen as a power supply, the battery is always used in the following circuit instead of the motor symbol.

1. For a current reversible chopper circuit, V_1 voltage is high and V_2 voltage is low, but which is the power supply and which is the load depends on the situation, which is why the current reversible chopper circuit name comes from.
2. If V2 is an actual battery, this circuit can either charge V2 after V1 steps down the voltage, or charge V1 after V2 steps up the voltage.
3. If V2 is a DC motor, this circuit can implement a circuit where power V1 drives V2 motor, or V2 motor can decelerate and feed energy back into power V1.

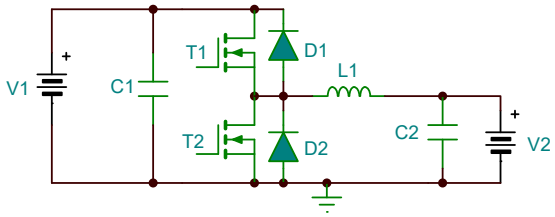


Figure 351. *Current Reversible Chopper Circuit*

The schematic for the current reversible chopper circuit as shown in Figure 1 can be analyzed simply as follows:

1. D1 and D2 are the parasitic diodes of field-effect transistors T1 and T2. Even without controlling the conduction of T1 and T2, these two diodes will still operate "automatically".
2. If we completely abandon control T2 and erase T2 (D2 reserved), the circuit would form a conventional buck chopper circuit. The current through L1 would flow from left to right, though the inductor current may be continuous or discontinuous.
3. If we completely abandon control T1 and erase T1 (D1 reserved), the circuit would form a conventional boost chopper circuit. The current through L1 would flow from left to right, though the inductor current may be continuous or discontinuous.
4. In practice, we can also enable complementary conduction of T1 and T2. Consequently, during one cycle, the circuit will operate in Buck mode for part of the time and in Boost mode for the remainder.

Below, we simulate the three operating modes mentioned above. First, we simplify the circuit and set specific parameters to obtain the circuit shown in **Figure 352**.

1. Replace the MOSFET switches represented by T1 and T2 with time-controlled switches to simplify the control circuit.
2. Add a current probe AM1 at inductor L1 to analyze the circuit operation. (Note: In practical switching power supply design, employing a high bandwidth oscilloscope current probe to directly observe current signals would prove immensely beneficial. Unfortunately, however, the high bandwidth current probe price was at least 10,000 Yuan, which is rare for students to see in the general lab of the school.)
3. Change diode to fast recovery diode 1N4148 (default diode variant is 1N1183).
4. The filter capacitors C1 and C2 are changed to 10μF.

5. V1 is set to 10V and V2 is set to 5V with 10Ω internal resistors R1 and R2 each.

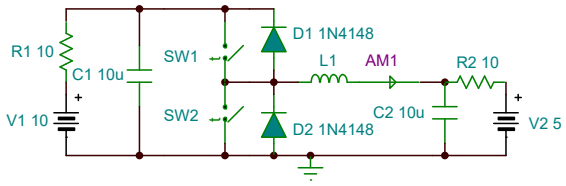


Figure 352. *Simulated Circuit for Current Reversible Chopper Circuit Operating States*

Using the time switch parameters shown in **Figure 353**, set the switching period to 50 microseconds, the duty cycle of SW1 to 50%, and SW2 to remain open. This configuration yields a pure Buck circuit control mode. The transient simulation period was set to 1ms-1.1ms to obtain the inductor current waveform shown in **Figure 354**.

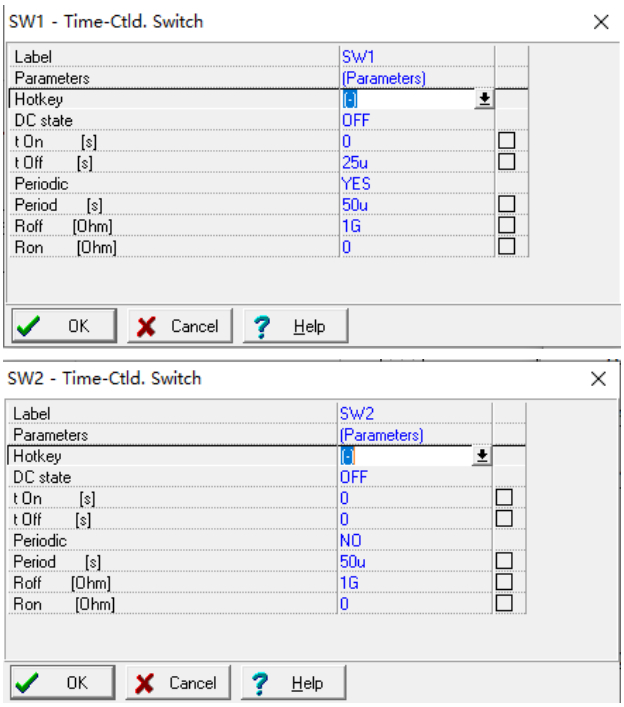


Figure 353. *Time-Controlled Switch Settings for the Buck Operation in Reversible Current Chopper Circuit*

1. From 1ms to 1.025ms, this is the switch SW1 turn-off period, at which point the inductor current rises approximately linearly and the current path is V1 → SW1 → L1 → Load → GND, meeting the Buck circuit operating characteristics.
2. From 1.025ms to 1.05ms, this is the switch SW1 turn-off period. The simulation results show that the inductor current has hiccup. The inductor current in the first half drops approximately linearly, and the current path is D2 → L1 → Load → GND. After the current drops to 0 in the second half, the current remains at zero, since D2 cannot conduct in the reverse direction. These meet the Buck circuit operating characteristics.

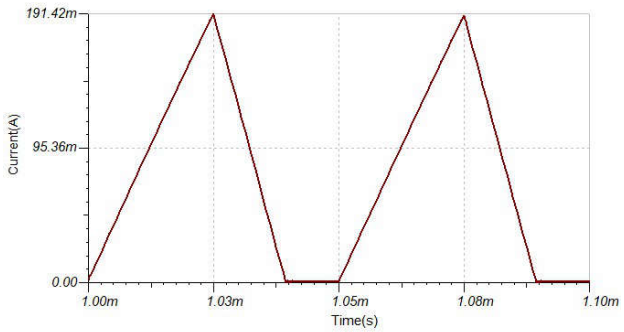


Figure 354. *Inductor Current Waveform during Buck Operation in the Current Reversible Chopper Circuit*

Why did we replace the default regular rectifier diode 1N1183 diode with the fast recovery diode 1N4148 earlier? If the **Figure 355** circuit is simulated with the same parameters as before, the resulting current waveform would look like **Figure 356**. Have you noticed that the inductor current has reversed ever so slightly! Please analyze the cause yourself. You may refer to the preceding material.

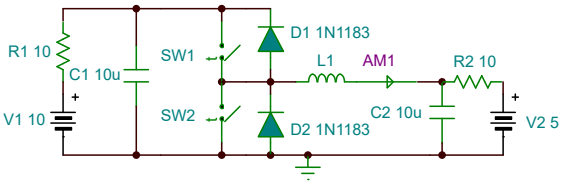


Figure 355. *Simulated Circuit for Current Reversible Chopper Circuit Operating States Using Regular Diodes*

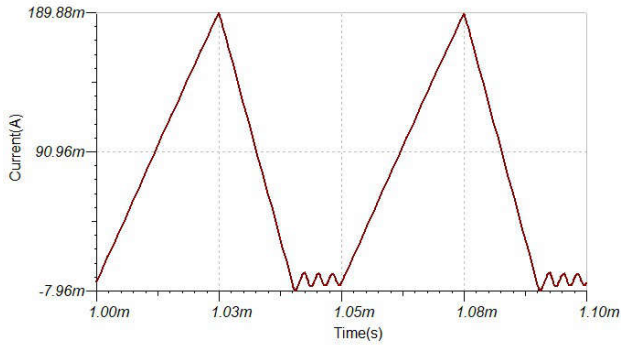


Figure 356. *Inductor Current Waveform during Buck Operation in the Current Reversible Chopper Circuit Using Regular Diode*

Swapping the settings of SW1 and SW2 results in pure Boost circuit control. The transient simulation period is also set to 1ms-1.1ms to get the inductor current waveform shown in **Figure 357**. The inductor current is also hiccup, and the analysis process is similar to Buck. It will not be elaborated upon here.

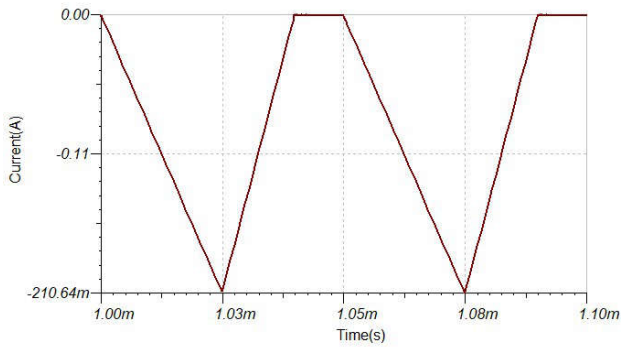


Figure 357. *Inductor Current Waveform during Boost Operation in the Current Reversible Chopper Circuit*

With the time switch parameters shown in **Figure 358**, SW1 and SW2 turn on in a complementary manner, and thus this gives "current reversible" control mode. The transient simulation period is set to 1ms-1.1ms, and changing the coordinate limits to symmetric (–130mA to 130mA) to yield the inductor current waveform depicted in **Figure 359**.

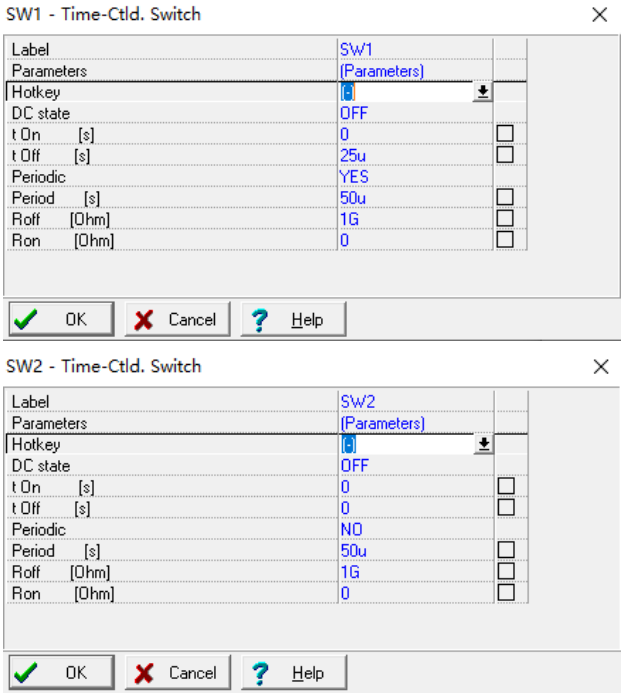


Figure 358. *Time-Controlled Switch Settings for the "Current Reversible" Operating State in the Reversible Current Chopper Circuit*

1. Since the SW1 and SW2 switches are complementary conducting, there is no problem with diode reverse current flow, so the inductor current is continuous.
2. The interval from 1.0000mS to 1.0250mS sees SW1 conducting, but the operational state comprises two distinct phases. From 1.0000mS to 1.0125mS, the current flows in the direction V2 → L1 → SW1 → V1 → GND, gradually decreasing to zero, and the circuit operates as a boost circuit with V2 as the power supply and V1 as the load. From 1.0125mS to 1.0250mS, the current flows in the direction V1 → SW1 → L1 → V2 → GND, gradually increasing, and the circuit operates as a buck circuit with V1 as the power supply and V2 as the load.
3. The interval from 1.0250mS to 1.0500mS sees SW2 conducting, but the operational state comprises two distinct phases. From 1.0250mS to 1.0375mS, the current flows in the direction SW2 → L1 → V2 → GND, gradually

decreasing to zero, and the circuit operates as a buck circuit with V1 as the power supply and V2 as the load. From 1.0375mS to 1.0500mS, the current flows in the direction V2 → L1 → SW2 → GND, gradually increasing, and the circuit operates as a boost circuit with V2 as the power supply and V1 as the load.

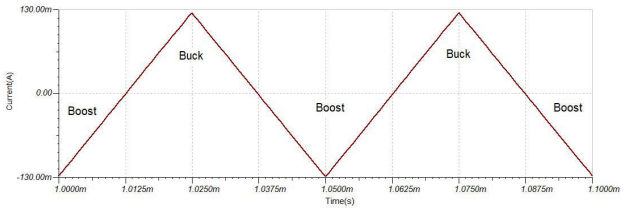


Figure 359. *Inductor Current Waveform during the Operating Status of "Reversible Current" in the Reversible Current Chopper Circuit*

The parameter settings for **Figure 358** is just an explanation of the principle. In practice, we will not set the duty cycle of SW1 and SW2 to 50% as this would result in a seesaw effect where the current oscillates, causing the two batteries to engage in a futile cycle of mutual charging and discharging. Changing the duty cycle to get the operating state of the actual current reversible chopper circuit.

1. Setting SW1 duty cycle to 75% and SW2 duty cycle to complementary conduction to 25%, the current simulation results are shown in **Figure 360**. In Buck mode, the current never drops to zero, so the circuit consistently operates as a Buck. Theoretically, D2's freewheeling function alone suffices at this point. The conduction of SW2 effectively achieves "synchronous rectification", reducing conduction voltage drop and minimizing losses.

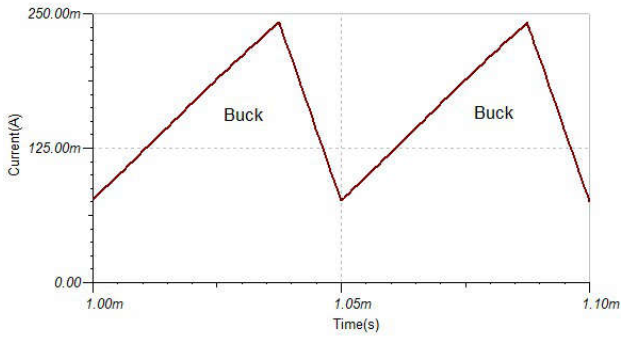


Figure 360. *Simulated Current Waveform of Current Reversible Chopper Circuit at 75% Duty Cycle*

2. Setting SW1 duty cycle to 60% and SW2 duty cycle to complementary conduction to 40%, the current simulation results are shown in **Figure 361**. At this point, the circuit works primarily in the Buck state and, in a few cases, in the Boost state. Overall, it can be considered that V1 charges V2. Similarly, the switches perform complementary conduction and the diode is actually shorted out, achieving the effect of "synchronous rectification".

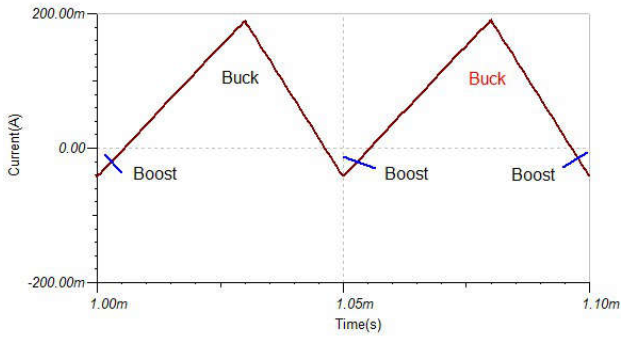


Figure 361. *Simulated Current Waveform of Current Reversible Chopper Circuit at 60% Duty Cycle*

3. Setting SW1 duty cycle to 40% and SW2 duty cycle to complementary conduction to 60%, the current simulation results are shown in **Figure 362**. At this point, the circuit works mainly in Boost state, and a few times in Buck state. Overall, it can be considered that V2 charges V1. Similarly, the switches perform complementary conduction, achieving the effect of "synchronous rectification".

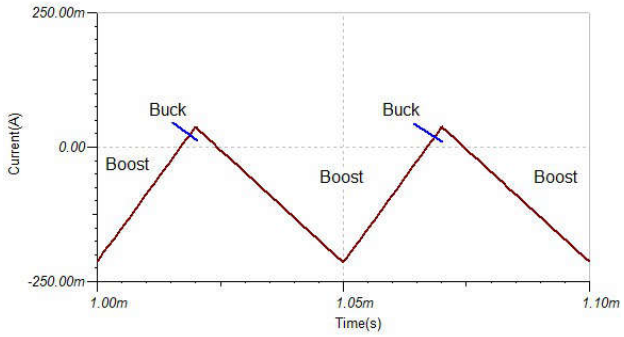


Figure 362. *Simulated Current Waveform of Current Reversible Chopper Circuit at 25% Duty Cycle*

4. Setting SW1 duty cycle to 25% and SW2 duty cycle to complementary conduction to 75%, the current simulation results are shown in **Figure 363**. At this point, the circuit is fully operational in Boost state and V1 is charged after V2 boost.

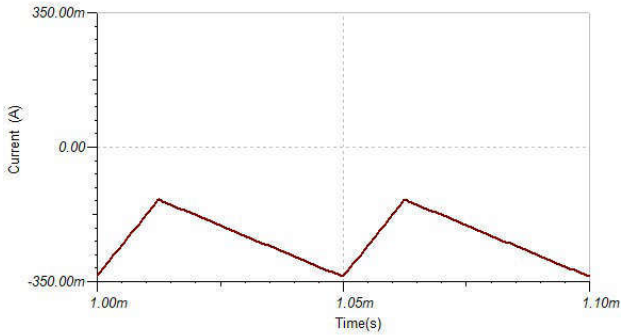


Figure 363. *Simulated Current Waveform of Current Reversible Chopper Circuit at 25% Duty Cycle*

5. Note that under "current-reversible" control, the diode may be bidirectionally conductive. Therefore, complementary conduction of SW1 and SW2 achieves the effect of synchronous rectification. Other circuits, such as pure Buck

circuits, are not as easy to implement synchronous rectification, and SW2 must be turned off when freewheeling current drops to zero, requiring significantly more complex control.

Bridge Circuits

The chopper circuits introduced earlier (excluding the current reversible chopper circuit) all adhere to using only one switch. This is because power electronic switches are not only relatively expensive (compared to other components in the circuit), but also difficult to manage (requiring drive control). If you pay for large-value inductors and capacitors, it is merely a matter of spending more money; they can be used once installed.

However, when the load requires the voltage and current directions to be reversed, a multi-switch bridge power supply circuit is necessary.

Full-Bridge Circuit

The full-bridge circuit, also known as the H-bridge circuit, is widely applied due to its fundamental ability to apply both positive and negative voltages (currents) to a load.

1. When used to drive a DC motor, it is possible to reverse the rotation direction of the motor and control the speed by adjusting the duty cycle of the switches.
2. When used to drive a loudspeaker, it is an efficient Class D power amplifier.

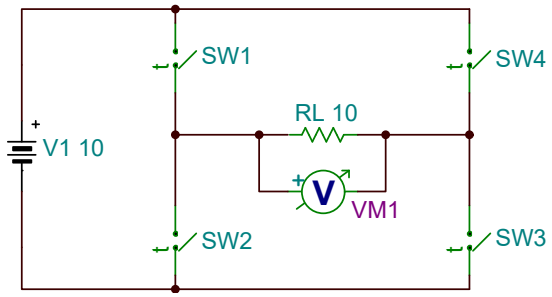


Figure 364. *Full-Bridge Circuit*

3. As shown in **Figure 364**, the diagonal switches operate alternately to output AC power. In this case, the full-bridge circuit is an inverter circuit, which converts DC power into AC power. If the duty cycle of the switches varies in a sinusoidal pattern, the output can be equivalent to sinusoidal AC power.

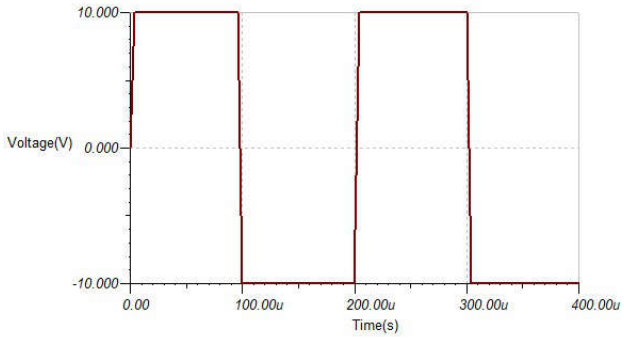


Figure 365. *Transient Simulation of the Full-Bridge Circuit in Inverter Mode*

4. The two switches in the same arm (for example, SW1 and SW2) cannot conduct simultaneously; otherwise, the power supply will be short-circuited. Since there is a delay for a power semiconductor switch from receiving a control signal until it is actually turned off, the control signals for SW1 and SW2 must allow for a period of time to ensure that both switches are turned off. This minimum required time is known as the dead time. The required dead time varies for different types of switches, and the off-time of a MOSFET switch ranges from microseconds to tens of microseconds.

Half-Bridge Circuit

The principle of the full-bridge circuit is well understood, but sometimes we do not need 4 switches to realize the inverter circuit. As shown in **Figure 366**, replacing two switches in the H-bridge with 2 bulk capacitors forms a half-bridge circuit.

1. Given the substantial capacitance values of C_1 and C_2, their voltage can be considered virtually constant over one cycle. It is calculated based on V_1 voltage of 10V, and the voltages on C_1 and C_2 should remain at 5V.

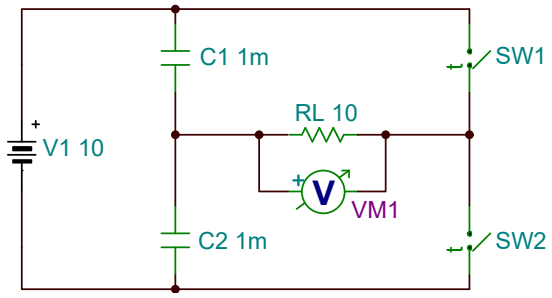


Figure 366. *Half-Bridge Circuit*

2. When turning on SW1 (SW2 open), R_L is connected in parallel with C_1 and loaded with a 5V voltage (positive at the right, negative at the left); when turning on SW2 (SW1 open), R_L is connected in parallel with C_2 and loaded with 5V voltage (positive at the left, negative at the right); the AC voltage developed on the load R_L, is shown in **Figure 367**. Note that the output voltage of the half-bridge circuit is only half that of the full-bridge circuit.

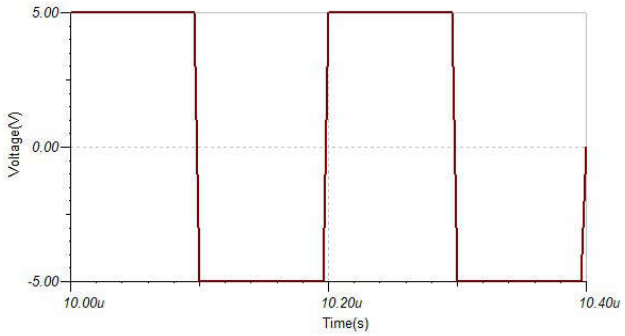


Figure 367. *Transient Simulation of the Half-Bridge Inverter Circuit*

3. Half-bridge circuits, like full-bridge circuits, can be controlled using SPWM with varying duty cycles to generate a sinusoidal voltage output. Unlike the full-bridge circuit, the two switches of the half-bridge circuit must operate symmetrically and complement each other, otherwise the voltages on C_1 and C_2 will no longer be balanced and the circuit will operate in a completely different state. Readers may simulate this by themselves.

Driver Isolation

The drive circuit for power semiconductor switches primarily serves two functions. We have already discussed one of these functions: the drive circuit must provide sufficient power to rapidly turn the switch on and off. The other function of the driver circuit - isolation - will be explained in this section, including why isolation is needed and how it is achieved.

Floating Driver Level

By analyzing the floating driver level in bridge circuits, this section will help you understand why it is required to isolate the driver. As shown in **Figure 368**, all switches in the full-bridge circuit are replaced with practical N-channel enhancement MOSFET, with the DC voltage PVCC set to 100V.

1. It is easy to drive T_2 and T_3 by applying a control voltage of a few volts to points E and F. Therefore, T_2 and T_3 constitute the low-side arm.
2. To drive T_1, a voltage of a few volts must be applied between points A and C. Let's temporarily set it to 5V. T_4 is similar to T_1, so only T_1 will be discussed below.
3. Assuming the switches' characteristics are identical, the voltage at point C will be 50V (T_1 and T_2 have equal insulation resistances and each bears half of the voltage) when none of the four switches conduct. This means that the drive voltage at point A needs to be 55V.
4. When T_1 turns on, the voltage at point C will rise to 100V. At this point, the drive voltage at point A must reach 105V. It will be difficult to drive the MOSFETs in the high-side arm due to the floating voltage at point C.

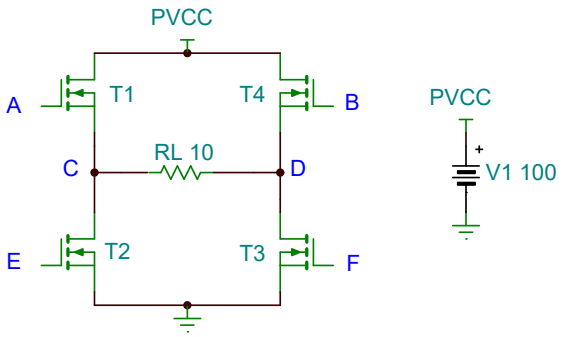


Figure 368. *Full-Bridge Circuit Formed by N-Channel MOSFETs*

To handle floating levels similar to those occurring at the switches in the high-side arm, there are several drive schemes as follows:

1. For high-voltage, high-power supplies, or in situations where cost is not a concern, pulse transformer isolation or optocoupler isolation schemes can be used.
2. The principle of pulse transformers is not complicated, but pulse transformers are not readily available as off-the-shelf products and require custom manufacturing. Due to the involvement of complex knowledge, such as the selection of magnetic components and the calculation of the turns ratio, and given the space constraints, this book will not cover this topic at all.

3. The principle of optocoupler isolation is also quite simple. It is important to emphasize that true optocoupler isolation requires operating power from an isolated power supply. Refer to the design principle of isolation amplifier power supplies.
4. Two low-cost solutions, bootstrap boost drive and P-type transistor drive, are more widely used in low- to medium-power circuits. These will be explained in the following sections.

Bootstrap Boost Driver

When a power supply circuit incorporates two switches that form high-side and low-side bridge arms and achieve control through their alternative conduction, a cleverly designed bootstrap boost driver chip can be used, such as the UCC27200A driver chip from TI, as shown in **Figure 369**.

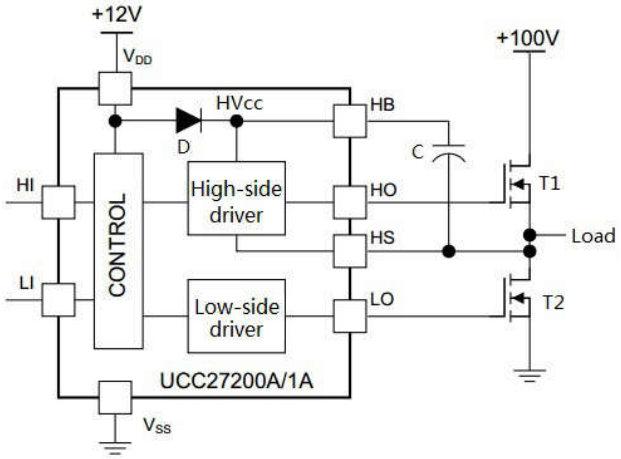


Figure 369. *Simplified Schematic Block for the UCC27200A Bootstrap Boost Driver*

1. T_1 and T_2 form a half-bridge pair. T_2, as the low-side arm, can be driven effortlessly. The source of T_1 is connected to the HS pin of the chip. As T_2 turns on and off, the V_{HS} level will fluctuate, making it difficult to drive the transistor T_1.
2. Inside the chip, the low-side driver unit is directly powered by the 12V control power supply V_{DD}, while the power supply HVcc for the high-side driver unit is provided by the bootstrap boost capacitor C, with its "ground" reference being V_{HS}.
3. Since the level of capacitor C floats with the source of T_1 (V_{HS}), the level of the driving signal HO output by the high-side driver unit also automatically varies, thereby solving the T_1 driving problem. This is why the bootstrap boost driver is named so.

How is it ensured that capacitor C always has a charge? The answer lies in the charge loop VDD → D → C → T2 → GND.

1. When T2 conducts, the voltage V_{HS} drops to 0, allowing capacitor C to be charged to 12V by V_{DD}.
2. When T2 is off, the voltage V_{HS} rises, causing H_{VCC} to rise synchronously. Since diode D is reverse-biased and cut off, capacitor C will not leak to V_{DD}, making the voltage across itself remain at 12V.
3. Since the energy stored in capacitor C is always limited and will be consumed by the high-side driver circuit, the low-side switch T_2 needs to periodically conduct (incidentally) to recharge C. Also, during the initial startup of the circuit, T_2 must be turned on first (to charge capacitor C) before T_1 can be controlled.

In the "current reversible" operating state of the current reversible chopper circuit discussed in the book, as the two switches conduct in a complementary manner, a bootstrap boost driver chip can be used for driving. Common bootstrap boost driver chips also include the IR2110 from IR. It primarily differs from the UCC27200A in that its bootstrap boost diode D is not integrated inside the chip. Therefore, it is necessary to select a fast recovery diode.

P-Type Transistor Driver

For low power switching circuits that do not satisfy the bootstrap boost drive principle, such as Buck chopper circuit shown in **Figure 370**, the source potential VF1 of T1 is floating and has a hard-to-drive problem. At this time, employing excessive isolation measures like optocouplers or pulse transformers in such cases would be neither economical nor reasonable.

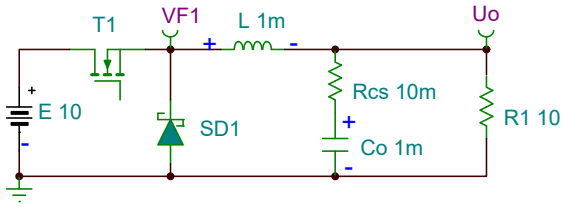


Figure 370. *Switch of Buck Circuit*

A straightforward solution employs P-type power electronic switch to solve the voltage floating issue. Replace high-side bridge arm switches of the bridge circuit with a PMOS transistor as shown in **Figure 371**.

1. For T_1 and T_4, the switch turns on when the gate voltage is below P_{VCC}; the switch turns off when the gate voltage is equal to P_{VCC}. The control voltage required for the gate is no longer floating.

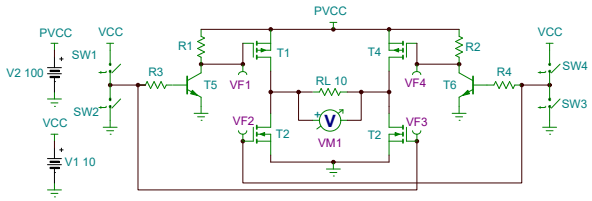


Figure 371. *PMOS Driver Circuit*

2. The inverter circuit, composed of bipolar junction transistors (or field-effect transistors) T_5 and T_6, can convert the gate control voltage of T_1 and T_4 into low-voltage control. Note that T_5 and T_6 need to be bipolar junction transistors or field-effect transistors with high voltage resistance.
3. **Figure 372** shows the simulated transient waveforms, observing the gate control voltage waveforms of 4 MOSFET switches.

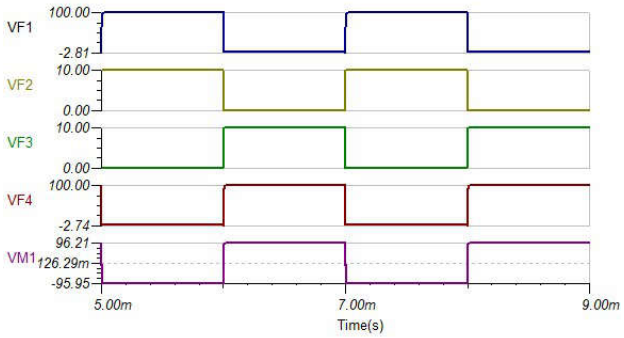


Figure 372. *Transient Simulation of the H-Bridge Circuit Formed by PMOS*

To speed up the turn-off, the actual PMOS driver additionally uses switching transistors to replace resistors R1 and R2 so as to speed up the charging process of the gate capacitor. The driver circuit shown in **Figure 372** is feasible for low-speed applications and as a theoretical illustration.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025