

LMK6B 9.3fs Ultra-Low Jitter, High-performance Differential Oscillator

1 Features

- Industry's lowest jitter:
 - 9.3fs typical differential RMS jitter at 625MHz HS-LVDS with 4MHz 1st order high-pass filter (12kHz to 20MHz)
 - 19.7fs typical differential RMS jitter at 312.5MHz AC-LVPECL with 4MHz 1st order high-pass filter (12kHz to 20MHz)
 - 16fs typical RMS jitter at 2500MHz AC-LVPECL output (12kHz to 20MHz)
 - 18fs typical, 35fs max RMS jitter at 625MHz AC-LVPECL output (12kHz to 20MHz)
 - 28fs typical RMS jitter at 312.5MHz AC-LVPECL output (12kHz to 20MHz)
- Exceptional PSRR performance (ripple frequencies > 10kHz, 50mV supply ripple, 0.1μF decoupling capacitor):
 - < -95dBc spurs for 156.25MHz LP-HCSL
 - < -80dBc spurs for 312.5MHz LVDS
- Output frequency:
 - Initial frequency offerings: 100, 125, 156.25, 312.5, 625, 1250, 2500MHz, and others
 - Preview, contact TI: 322.265625, 390.625, 425, 496, 603.2291, 804.305467, 2343.75, 2400, 2412.91636, 2457.6, 2480, 2550, 2578.125MHz
 - Other fixed frequencies on request
- Supports PCIe Gen 1 to Gen 7
- Output formats:
 - LVDS, HS-LVDS, AC-LVPECL, Custom Swing: 50MHz to 2500MHz
 - LP-HCSL: 50MHz to 625MHz
- ±25ppm total frequency stability (inclusive of all factors with 10-year aging at 25°C board temperature)
 - ±7ppm temperature variation (-40°C to 105°C)
- Preview, contact TI: ±20ppm total frequency stability (inclusive of all factors with 10-year aging at 85°C board temperature)
- 91mA maximum current consumption (AC-LVPECL, Custom Swing, LVDS, HS-LVDS)
- 85mA maximum current consumption (LP-HCSL)
- 2.5V / 3.3V power supply (2.375V through 3.465V)
- Industry standard 6-pin package:
 - 2.0mm × 1.6mm (wettable flank)
 - Preview, contact TI: 2.5mm × 2.0mm, 3.2mm × 2.5mm
- 40°C to 105°C PCB temperature

2 Applications

- Optical transceiver module
- Switch, router, optical
- NIC, SmartNIC
- 112G / 224G / 448G PAM-4 Ethernet clocking

3 Description

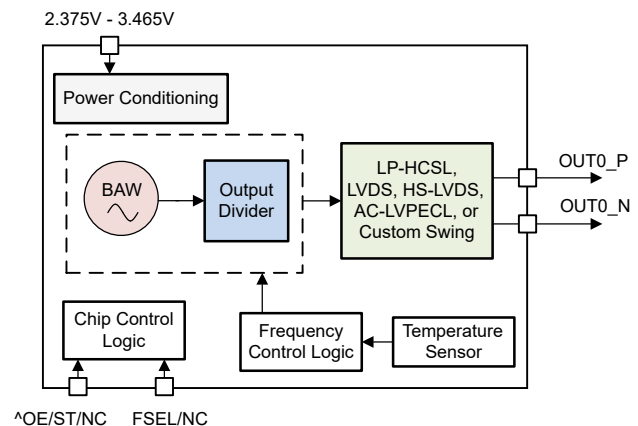
The LMK6Bx device is an ultra-low jitter, fixed frequency oscillator achieving 9.3fs at 625MHz. This device incorporates the [BAW](#) as the resonator source. The device is factory programmed per specific operation mode, including frequency, output type, function pin, and frequency stability.

The high-performance clocking, mechanical stability, flexibility, and small package options for this device are designed for reference and core clocks in high-speed SerDes used in telecommunications, data and enterprise network, and industrial applications.

Table 3-1. Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LMK6B	DLE (VSON, 6) ⁽³⁾	3.2mm×2.5mm
	DLF (VSON, 6) ⁽³⁾	2.5mm×2.0mm
	DLR (VSON, 6)	2.0mm×1.6mm

- (1) See also, [Mechanical, Packaging, and Orderable Information](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.
 (3) Preview, contact TI



LMK6Bx Simplified Block Diagram

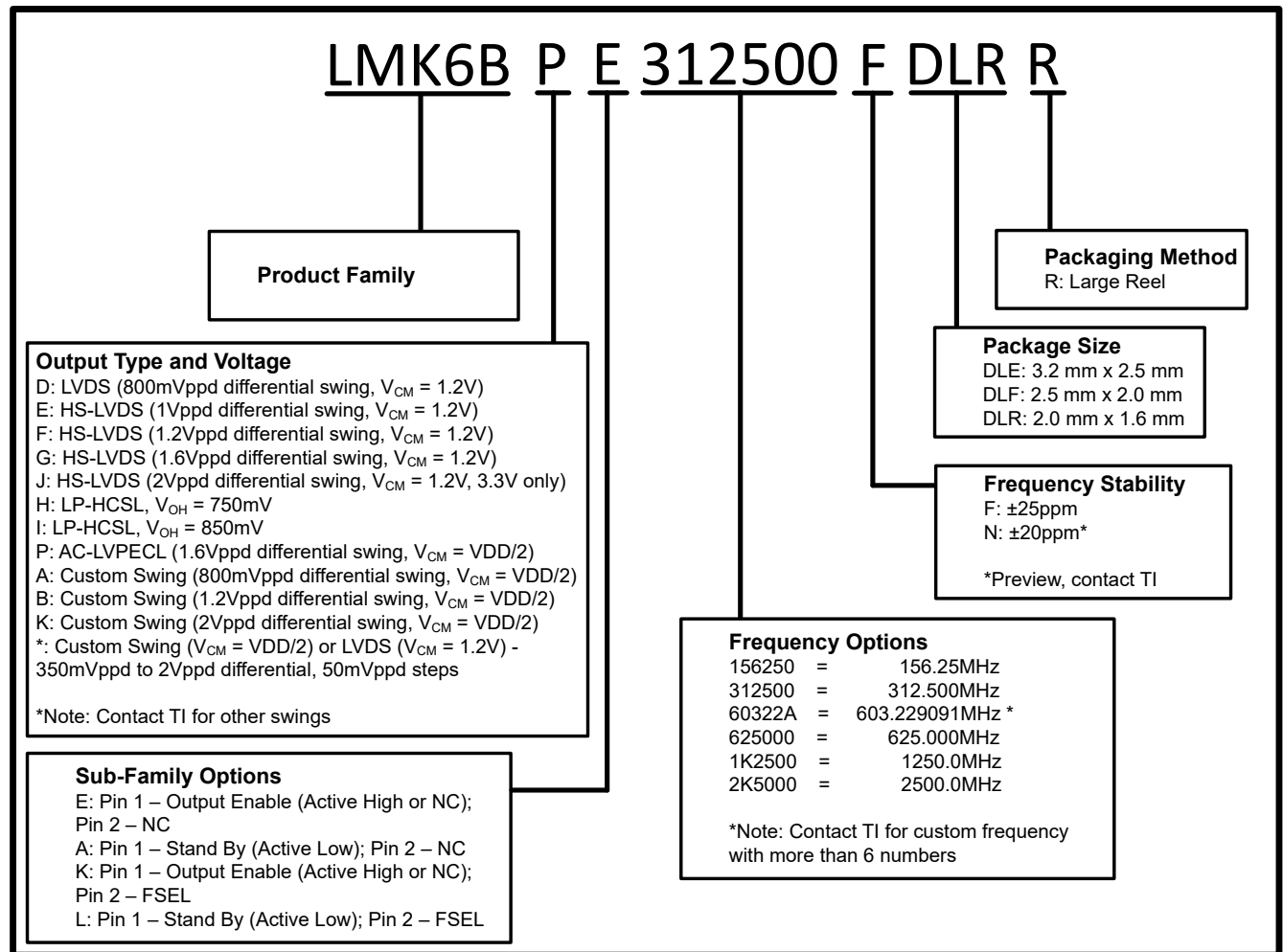


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4 Device Comparison

Use [Figure 4-1](#) to understand the device nomenclature of the LMK6Bx orderable options



ADVANCE INFORMATION

Figure 4-1. Part Number Guide: LMK6Bx

5 Pin Configuration and Functions

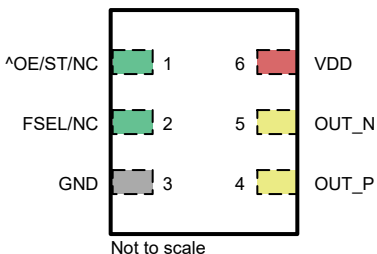


Figure 5-1. LMK6Bx DLE, DLF, and DLR 6-Pin (Top View)

Legend	
Input	Power
Ground	Output

Table 5-1. LMK6Bx Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
[^] OE/ST/NC ⁽²⁾	1	I / NC	Output Enable (OE), Stand By (ST), or No Connect (NC). For OE and ST: - Low: Output inactive - High/Floating: Output active Internal pull-up of 150kΩ. See Section 8.3.3 for more details.
^{^v} FSEL/NC ^{(2) (3)}	2	I / NC	Output Frequency Select (FSEL) pin, or No Connect (NC). For FSEL, - Low: $F_{OUT}/4$ - Floating: F_{OUT} - High: $F_{OUT}/2$ F_{OUT} is the output frequency set by the OPN. See Section 4 for more details. Internal pullup resistor of 200kΩ and internal pulldown resistor of 200kΩ. See Section 8.3.3 for more details.
GND	3	G	Device ground.
OUT_P	4	O	Positive differential output clock.
OUT_N	5	O	Negative differential output clock.
VDD	6	P	Device power supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) Pins with a "[^]" prefix have an internal pullup resistor.

(3) Pins with a "^v" prefix have an internal pulldown resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDD	Device Supply Voltage ⁽²⁾	−0.3	3.7	V
EN	Logic Input Voltage	−0.3	VDD + 0.3	V
OUTP, OUTN	Clock Output Voltage ⁽³⁾	−0.3	VDD + 0.3	V
T _J	Junction Temperature		140	°C
T _{STG}	Storage Temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) For all devices with Recommended Operating Voltage of 2.5 V +/- 5% and 3.3 V +/- 5%
- (3) For all differential output types.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Environmental Compliance

		VALUE	UNIT
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
	MIL-STD-883F, Method 2007, Condition A	20	g
Moisture Sensitivity Level (MSL)		MSL1	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Device Supply Voltage ⁽¹⁾	2.375	2.5, 3.3	3.465	V
T _A	Ambient temperature	−40		105	°C
T _{PCB}	PCB temperature (measured below package)	−40		105	°C
T _J	Junction temperature	−40		125	°C
t _{RAMP}	VDD power-up ramp time ^{(1) (2)}	0.1		100	ms

- (1) For all devices with Recommended Operating Voltage of 2.5V ±5% and 3.3V + 5% to -10%
- (2) VDD power-up ramp time is defined as minimum time taken for power supply to exceed 95% of nominal VDD. Monotonic power supply ramp is assumed. In case of erratic or non-monotonic power supply ramp, enable the output stage by controlling OE and EN pin.

6.5 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
DLR (VSON)	6	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
DLF (VSON)	6	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
DLE (VSON)	6	TBD	TBD	TBD	TBD	TBD	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.6 Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.3V +5%/-10%, 2.5V ±5%. Typical values are at V_{DD} = 3.3V, T_{PCB} = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Tolerance						
F _T	Total frequency stability (OPN 14 th character: option F)	Inclusive of: solder shift, initial tolerance, variation over -40°C to 105°C, variation over rated supply voltage range, and 10 year aging at 25°C.	-25		25	ppm
F _{AGE_1yr}	Frequency stability due to 1 year aging	1 year aging at 25°C (±25ppm)				ppm
F _{AGE_10yr}	Frequency stability change due to aging (included in total frequency stability)	10 year aging at 25°C (±25ppm)				ppm
F _{TEMP}	Frequency stability due to temperature (included in total frequency stability)	Over Recommended Operating Condition, dT/dt < 10°K/min	-7		+7	ppm
F _{HYS}	Frequency stability due to hysteresis (included in total frequency stability)					ppm
Current Consumption Characteristics						
I _{DD}	Device Power Consumption (LVDS, Excluding load current)	50MHz, 2.5V				mA
		50MHz, 3.3V				mA
		100MHz, 2.5V				mA
		100MHz, 3.3V				mA
		125MHz, 2.5V				mA
		125MHz, 3.3V				mA
		156.25MHz, 2.5V		70		mA
		156.25MHz, 3.3V		72		mA
		312.5MHz, 2.5V		70		mA
		312.5MHz, 3.3V		74		mA
		625MHz, 2.5V		68		mA
		625MHz, 3.3V		72		mA
		603.229091MHz, 2.5V				mA
		603.229091MHz, 3.3V				mA
		1250MHz, 2.5V		70		mA
		1250MHz, 3.3V		72		mA
		2500MHz, 2.5V		65		mA
		2500MHz, 3.3V		68		mA

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device Power Consumption (HS-LVDS and AC-LVPECL, Excluding load current)	50MHz, 2.5V		70		mA
		50MHz, 3.3V		74		mA
		100MHz, 2.5V		75		mA
		100MHz, 3.3V		80		mA
		125MHz, 2.5V		70		mA
		125MHz, 3.3V		75		mA
		156.25MHz, 2.5V		71		mA
		156.25MHz, 3.3V		75		mA
		312.5MHz, 2.5V		74		mA
		312.5MHz, 3.3V		78		mA
		500MHz, 2.5V		79		mA
		500MHz, 3.3V		84		mA
		625MHz, 2.5V		77		mA
		625MHz, 3.3V		82		mA
		603.229091MHz, 2.5V				mA
		603.229091MHz, 3.3V				mA
		1250MHz, 2.5V		72		mA
		1250MHz, 3.3V		76		mA
		2500MHz, 2.5V		69		mA
		2500MHz, 3.3V		73		mA
I_{DD}	Device Power Consumption (LP-HCSL, Excluding load current)	50MHz, 2.5V		63		mA
		50MHz, 3.3V		66		mA
		100MHz, 2.5V		70		mA
		100MHz, 3.3V		72		mA
		125MHz, 2.5V		65		mA
		125MHz, 3.3V		67		mA
		156.25MHz, 2.5V		66		mA
		156.25MHz, 3.3V		68		mA
		312.5MHz, 2.5V		70		mA
		312.5MHz, 3.3V		72		mA
		500MHz, 2.5V		75		mA
		500MHz, 3.3V		77		mA
		603.229091MHz, 2.5V				mA
		603.229091MHz, 3.3V				mA
		625MHz, 2.5V		72		mA
		625MHz, 3.3V		74		mA

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device Power Consumption (2Vppd, Excluding load current)	50MHz, 2.5V				mA
		50MHz, 3.3V				mA
		100MHz, 2.5V				mA
		100MHz, 3.3V				mA
		125MHz, 2.5V				mA
		125MHz, 3.3V				mA
		156.25MHz, 2.5V		73		mA
		156.25MHz, 3.3V		76		mA
		312.5MHz, 2.5V		77		mA
		312.5MHz, 3.3V		81		mA
		625MHz, 2.5V		74		mA
		625MHz, 3.3V		78		mA
		603.229091MHz, 2.5V				mA
		603.229091MHz, 3.3V				mA
		1250MHz, 2.5V		75		mA
		1250MHz, 3.3V		79		mA
		2500MHz, 2.5V		70		mA
		2500MHz, 3.3V		74		mA
$I_{DD-STBY}$	Device Stand By current	ST (Stand By) = GND, 2.5V				mA
		ST (Stand By) = GND, 3.3V		2.3		mA
I_{DD-OD}	Device current with output disabled (625MHz)	OE = GND, HS-LVDS and AC-LVPECL mode, VDD = 2.5V		54		mA
		OE = GND, HS-LVDS and AC-LVPECL mode, VDD = 3.3 V		56		mA
		OE = GND, LVDS mode, VDD = 2.5V		54		mA
		OE = GND, LVDS mode, VDD = 3.3 V		56		mA
		OE = GND, LP-HCSL mode, VDD = 2.5V		59		mA
		OE = GND, LP-HCSL mode, VDD = 3.3 V		61		mA
		OE = GND, Highest Swing (2Vppd), VDD = 2.5V				mA
		OE = GND, Highest Swing (2Vppd), VDD = 3.3 V				mA

LVDS Output Characteristics

F_{out}	Output Frequency		50		2500	MHz
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, VDD = 3.3V, 625MHz	350	400		mVpp
		AC coupled, VDD = 2.5V, 625MHz	300	350		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, VDD = 3.3V, 1250MHz	350	400		mVpp
		AC coupled, VDD = 2.5V, 1250MHz	300	350		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, VDD = 3.3V, 2500MHz	350	400		mVpp
		AC coupled, VDD = 2.5V, 2500MHz	300	350		mVpp
$V_{OD,DIFF}$	Differential Output peak-peak swing ⁽²⁾			$2 \times V_{OD} $		mVppd
V_{OS}	Output Common-Mode Voltage	VDD = 3.3 V	TBD	1.2	TBD	V
		VDD = 2.5 V	TBD	1.2	TBD	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5 V/ 3.3 V		65		ps
ODC	Output Duty Cycle	VDD = 2.5 V/ 3.3V, measured between 50% points on the waveform	45	50	55	%

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM-IM}	Common Mode Imbalance	Measured at $C_L = 100$ pF on Common Mode Node	-150		150	mV
HS-LVDS Output Characteristics						
F_{out}	Output Frequency		50		2500	MHz
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 625MHz	400		1000	mVpp
		AC coupled, $V_{DD} = 2.5V$, 625MHz	350		800	mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 1250MHz	400		1000	mVpp
		AC coupled, $V_{DD} = 2.5V$, 1250MHz	350		800	mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 2500MHz	400		1000	mVpp
		AC coupled, $V_{DD} = 2.5V$, 2500MHz	350		800	mVpp
$V_{OD,DIFF}$	Differential Output peak-peak swing ⁽²⁾		$2 \times V_{OD} $			mVppd
V_{OS}	Output Common-Mode Voltage	$V_{DD} = 3.3$ V	TBD	1.2	TBD	V
V_{OS}	Output Common-Mode Voltage	$V_{DD} = 2.5$ V	TBD	1.2	TBD	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, $V_{DD} = 2.5$ V/ 3.3 V		65		ps
ODC	Output Duty Cycle	$V_{DD} = 2.5$ V/ $3.3V$, measured between 50% points on the waveform, divider set to bypass, 2,3,4,5,6,8, and other odd divides	48	50	52	%
ODC	Output Duty Cycle	$V_{DD} = 2.5$ V/ $3.3V$, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at $C_L = 100$ pF on Common Mode Node	-150		150	mV
AC-LVPECL Output Characteristics						
F_{out}	Output Frequency		50		2500	MHz
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 156.25MHz	700	800		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 2.5V$, 156.25MHz	600	700		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 625MHz	700	800		mVpp
		AC coupled, $V_{DD} = 2.5V$, 625MHz	600	700		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 1250MHz	700	800		mVpp
		AC coupled, $V_{DD} = 2.5V$, 1250MHz	600	700		mVpp
V_{OD}	Output Voltage Swing ($V_{OH} - V_{OL}$)	AC coupled, $V_{DD} = 3.3V$, 2500MHz	700	800		mVpp
		AC coupled, $V_{DD} = 2.5V$, 2500MHz	600	700		mVpp
$V_{OD,DIFF}$	Differential Output peak-peak swing ⁽²⁾		$2 \times V_{OD} $			mVppd
V_{OS}	Output Common-Mode Voltage	$V_{DD} = 3.3$ V	TBD	$V_{DD}/2$	TBD	V
		$V_{DD} = 2.5$ V	TBD	$V_{DD}/2$	TBD	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, $V_{DD} = 2.5$ V/ 3.3 V		65		ps
ODC	Output Duty Cycle	$V_{DD} = 2.5$ V/ $3.3V$, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at $C_L = 100$ pF on Common Mode Node	-150		150	mV
Custom Swing Output Characteristics						
F_{out}	Output Frequency		50		2500	MHz
$V_{OD,range}$	Custom Voltage Swing ($V_{OH} - V_{OL}$) range	AC coupled, $V_{DD} = 3.3V$, 156.25MHz	175		1000	mVpp
$V_{OD,range}$	Custom Voltage Swing ($V_{OH} - V_{OL}$) range	AC coupled, $V_{DD} = 2.5V$, 156.25MHz	175		750	mVpp

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD,range}$	Custom Voltage Swing ($V_{OH} - V_{OL}$) range	AC coupled, $V_{DD} = 3.3V$, 625MHz	175		1000	mVpp
		AC coupled, $V_{DD} = 2.5V$, 625MHz	175		750	mVpp
$V_{OD,step}$	Output Voltage Swing ($V_{OH} - V_{OL}$) step size	AC coupled, 1250MHz		25		mVpp
$V_{OD,DIFF}$	Differential Output peak-peak swing ⁽²⁾			$2 \times V_{OD} $		mVppd
V_{OS}	Output Common-Mode Voltage	$V_{DD} = 3.3V$	TBD	$V_{DD}/2$	TBD	V
		$V_{DD} = 2.5V$	TBD	$V_{DD}/2$	TBD	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, $V_{DD} = 2.5V/3.3V$		65		ps
ODC	Output Duty Cycle	$V_{DD} = 2.5V/3.3V$, measured between 50% points on the waveform	45	50	55	%
V_{CM-IM}	Common Mode Imbalance	Measured at $C_L = 100pF$ on Common Mode Node	-150		150	mV
LP-HCSL Output characteristics						
F_{out}	Output Frequency		50		625	MHz
V_{OH}	Output High Voltage (OPN 6 th character: option H)	DC coupled, 2pF load, $V_{DD} = 2.5V/3.3V$	650	750	850	mV
	Output High Voltage (OPN 6 th character: option I)	DC coupled, 2pF load, $V_{DD} = 2.5V/3.3V$	750	850	950	mV
V_{OL}	Output Low Voltage	DC coupled, 2pF load, $V_{DD} = 2.5V/3.3V$	-150	0	150	mV
$V_{overshoot}$	Overshoot voltage	$V_{max} - V_{OH}$			150	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing ⁽²⁾			$2 \times V_{OH} - V_{OL} $		mVppd
V_{cross}	Absolute Crossing Point Voltage ⁽³⁾	$V_{DD} = 3.3V/2.5V$, $f_{out} = 100MHz$, PCIe test load, 15 dB loss at 4 GHz, $f_{out} = 100MHz$, $Z_{diff} = 100\Omega$	0.28	0.35	0.48	V
$V_{cross-delta}$	Absolute Crossing Point Voltage variation	$V_{DD} = 3.3V/2.5V$, $f_{out} = 100MHz$, PCIe test load, 15 dB loss at 4 GHz, $f_{out} = 100MHz$, $Z_{diff} = 100\Omega$			TBD	mV
dV/dt	Output Slew Rate	50 ohms to ground; DC coupled load; measured slew rate in $\pm 150mV$ from Center, programmable. ⁽¹⁾	2		12	V/ns
$\Delta dV/dt$	Output Slew Rate variation				20	%
ODC	Output Duty Cycle		45	50	55	%
$ V_{RB} $	Absolute value of ring back voltage	PCIe test load, 15 dB loss at 4 GHz, $f_{out} = 100MHz$, $Z_{diff} = 100\Omega$	100			mV
t_{stable}	Time before V_{RB} is allowed	PCIe test load, 15 dB loss at 4 GHz, $f_{out} = 100MHz$, $Z_{diff} = 100\Omega$	500			ps
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$		180		ps
Z_{DIFF}	Differential output DC impedance	$V_{DD} = 3.3V$		100		Ω
Z_{SE}	Single-ended output DC impedance	$V_{DD} = 3.3V$		50		Ω
Pin 1 Input Characteristics (OE/ST)						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.3			V
I_{IL}	Input Low Current	OE = GND	-40			μA
I_{IH}	Input High Current	OE = VDD			40	μA
C_{IN}	Input Capacitance			2		pF
Pin 2 Input Characteristics (FSEL)						
V_{IL}	Input Low Voltage, FSEL				$0.2 \times V_{DD}$	V

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{MID}	Input Middle Voltage, FSEL		0.4×VDD – 0.6×VDD			V
V _{IH}	Input High Voltage, FSEL		0.8×VDD			V
I _{IL}	Input Low Current	OE = GND	–40			μA
I _{IH}	Input High Current	OE = VDD	40			μA
C _{IN}	Input Capacitance		2			pF
PSRR Characteristics						
PSRR _{50mV} , 0.1μF	Spur induced by 50mV power supply ripple at 156.25MHz LP-HCSL output, 0.1μF decoupling capacitor	Sine wave at 10kHz	–95			dBc
		Sine wave at 100kHz	–108			dBc
		Sine wave at 200kHz	–153			dBc
		Sine wave at 500kHz	–158			dBc
		Sine wave at 1MHz	–158			dBc
		Sine wave at 2MHz	–160			dBc
		Sine wave at 5MHz	–161			dBc
PSRR _{50mV}	Spur induced by 50mV power supply ripple at 156.25MHz LP-HCSL output, no power supply decoupling capacitor	Sine wave at 10kHz	–97			dBc
		Sine wave at 100kHz	–99			dBc
		Sine wave at 200kHz	–100			dBc
		Sine wave at 500kHz	–99			dBc
		Sine wave at 1MHz	–95			dBc
		Sine wave at 2MHz	–90			dBc
		Sine wave at 5MHz	–96			dBc
PSRR _{50mV} , 0.1μF	Spur induced by 50mV power supply ripple at 312.5MHz LVDS output, 0.1μF decoupling capacitor	Sine wave at 10MHz	–156			dBc
		Sine wave at 10kHz	–80			dBc
		Sine wave at 100kHz	–83			dBc
		Sine wave at 200kHz	–88			dBc
		Sine wave at 500kHz	–96			dBc
		Sine wave at 1MHz	–101			dBc
		Sine wave at 2MHz	–106			dBc
PSRR _{50mV}	Spur induced by 50mV power supply ripple at 312.5MHz LVDS output, no power supply decoupling capacitor	Sine wave at 4.9MHz	–160			dBc
		Sine wave at 10kHz	–81			dBc
		Sine wave at 100kHz	–74			dBc
		Sine wave at 200kHz	–74			dBc
		Sine wave at 500kHz	–74			dBc
		Sine wave at 1MHz	–74			dBc
		Sine wave at 2MHz	–75			dBc
PSRR _{JITTER}	Jitter sensitivity to power supply ripple	Sine wave at 5MHz	–75			dBc
		Sine wave at 10MHz	–134			dBc
		100kHz sine wave ripple, 3.3 V Supply				fs/mV
Power-On Characteristics						
t _{START_UP}	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification; Tested with a VDD supply ramp time of around 200 μs	2			ms
t _{ST-EN}	Chip enable time	Time elapsed from standby (ST = V _{IH}) until output is enabled and output is within specification	2			ms

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ST-DIS}	Chip disable time	Time elapsed from standby ($ST = V_{IL}$) until chip is in standby mode				
t_{OE-EN}	Output enable time	Time elapsed from $OE = V_{IH}$ until output is enabled and output is within specification			25	μs
t_{OE-DIS}	Output disable Time	Time elapsed from $OE = V_{IL}$ until output is disabled			1	μs
LVDS - Clock Output Jitter						
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 4MHz 1 st order high-pass filter		47.6		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$		58		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-112		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-137		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-157		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-161		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 4MHz 1 st order high-pass filter		26.3		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$		36		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-106		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-131		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-152		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-159		dBc/Hz
PN_{10M}	Phase Noise at 10MHz			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 4MHz 1 st order high-pass filter		11.6		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$		25		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-91		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-122		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-146		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-161		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-162		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$, 4MHz 1 st order high-pass filter		7.8		fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$		22		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-89		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-116		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-141		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-156		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-159		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$, 4MHz 1 st order high-pass filter		4.7		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$		21		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-82		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-110		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-134		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-153		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-159		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-159		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 100MHz$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 125MHz$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 603.229091MHz$				fs
HS-LVDS - Clock Output Jitter						
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 1.2Vppd, 4MHz 1 st order high-pass filter		40.2		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 1.2Vppd		50		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-112		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-137		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-157		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-163		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 1.2Vppd, 4MHz 1 st order high-pass filter		25.1		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 1.2Vppd		35		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-106		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-130		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-152		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-159		dBc/Hz
PN_{10M}	Phase Noise at 10MHz			-162		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-163		dBc/Hz

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 625MHz, 1.2Vppd, 4MHz 1 st order high-pass filter		9.3		fs
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 625MHz, 1.2Vppd		20		fs
PN ₁₀₀	Phase Noise at 100Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-100		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-125		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-147		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-164		dBc/Hz
PN _{100M}	Phase Noise at 100MHz Offset			-163		dBc/Hz
R _{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 1250MHz, 1.2Vppd, 4MHz 1 st order high-pass filter		6.9		fs
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 1250MHz, 1.2Vppd		19		fs
PN ₁₀₀	Phase Noise at 100 Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-94		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-119		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-141		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-157		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN _{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
R _{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 2500MHz, 1.2Vppd, 4MHz 1 st order high-pass filter		3.8		fs
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 2500MHz, 1.2Vppd		17		fs
PN ₁₀₀	Phase Noise at 100 Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-88		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-112		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-135		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-153		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN _{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
AC-LVPECL - Clock Output Jitter						
R _{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 156.25MHz, 4MHz 1 st order high-pass filter		31		fs
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 156.25MHz		45		fs
PN ₁₀₀	Phase Noise at 100Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-106		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-138		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-158		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-164		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-165		dBc/Hz
R _{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 312.5MHz, 4MHz 1 st order high-pass filter		19.7		fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$		28		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-100		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-132		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-153		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-164		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-165		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 4MHz 1 st order high-pass filter		9.6		fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$		18		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-94		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-126		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-148		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-165		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-164		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$, 4MHz 1 st order high-pass filter				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$		17		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-88		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-120		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-142		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-156		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$, 4MHz 1 st order high-pass filter				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$		16		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-81		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-114		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-136		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-152		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 100MHz$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 125MHz$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 603.229091MHz$				fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Custom Swing - Clock Output Jitter						
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 800mVppd swing, 4MHz 1 st order high-pass filter				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 800mVppd swing		58		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-104		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-138		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-157		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-162		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 800mVppd swing, 4MHz 1 st order high-pass filter				fs
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 800mVppd swing		35		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-131		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-152		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-160		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-162		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 800mVppd swing, 4MHz 1 st order high-pass filter				fs
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 800mVppd swing		20		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-91		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-126		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-148		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-160		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-162		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$, 800mVppd swing, 4MHz 1 st order high-pass filter				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$, 800mVppd swing		18		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-85		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-119		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-142		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-157		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-160		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$, 800mVppd swing, 4MHz 1 st order high-pass filter				fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 2500MHz$, 800mVppd swing		16		fs
PN_{100}	Phase Noise at 100 Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-79		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-114		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-136		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-153		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-159		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-160		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 2000mVppd swing, 4MHz 1 st order high-pass filter				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 2000mVppd swing		39		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-103		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-137		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-159		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-165		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-166		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 2000mVppd swing, 4MHz 1 st order high-pass filter				fs
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 2000mVppd swing		22		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-131		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-154		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-165		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-167		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-167		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 2000mVppd swing, 4MHz 1 st order high-pass filter				fs
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 2000mVppd swing		19		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-91		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-126		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-148		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-163		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-165		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-164		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 1250MHz$, 2000mVppd swing, 4MHz 1 st order high-pass filter				fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 1250MHz, 2000mVppd swing		17		fs
PN ₁₀₀	Phase Noise at 100 Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-86		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-119		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-142		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-156		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN _{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
R _{J_HP} F	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 2500MHz, 2000mVppd swing, 4MHz 1 st order high-pass filter				fs
R _J	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 2500MHz, 2000mVppd swing		16		fs
PN ₁₀₀	Phase Noise at 100 Hz Offset					dBc/Hz
PN _{1k}	Phase Noise at 1kHz Offset			-79		dBc/Hz
PN _{10k}	Phase Noise at 10kHz Offset			-113		dBc/Hz
PN _{100k}	Phase Noise at 100kHz Offset			-136		dBc/Hz
PN _{1M}	Phase Noise at 1MHz Offset			-153		dBc/Hz
PN _{10M}	Phase Noise at 10MHz Offset			-161		dBc/Hz
PN _{100M}	Phase Noise at 100MHz Offset			-161		dBc/Hz
LP-HCSL - Clock output jitter						
J _{PCle1-cc}	PCle Gen 1 Common Clock jitter (jitter limit = 86ps)	F _{out} = 100MHz, V _{OH} = 850mV				ps
J _{PCle1-SRNS}	PCle Gen 1 SRNS jitter					ps
J _{PCle2-cc}	PCle Gen 2 Common Clock jitter (jitter limit = 3ps)					ps
J _{PCle2-SRNS}	PCle Gen 2 SRNS jitter					ps
J _{PCle3-cc}	PCle Gen 3 Common Clock jitter (jitter limit = 1ps)					ps
J _{PCle3-SRNS}	PCle Gen 3 SRNS jitter					ps
J _{PCle4-cc}	PCle Gen 4 Common Clock jitter (jitter limit = 500fs)					ps
J _{PCle4-SRNS}	PCle Gen 4 SRNS jitter					ps
J _{PCle5-cc}	PCle Gen 5 Common Clock jitter (jitter limit = 150fs)					ps
J _{PCle5-SRNS}	PCle Gen 5 SRNS jitter					ps
J _{PCle6-cc}	PCle Gen 6 Common Clock jitter (jitter limit = 100fs)					ps
J _{PCle6-SRNS}	PCle Gen 6 SRNS jitter					ps
J _{PCle6-cc}	PCle Gen 7 Common Clock jitter (jitter limit = 69fs)					ps
J _{PCle6-SRNS}	PCle Gen 7 SRNS jitter					ps
R _{J_HP} F	RMS Jitter (Integration BW: 12kHz to 20MHz)	F _{out} = 100MHz, 4MHz 1 st order high-pass filter, V _{OH} = 850mV				fs

Unless otherwise specified: $V_{DD} = 3.3V \pm 5\%/-10\%$, $2.5V \pm 5\%$. Typical values are at $V_{DD} = 3.3V$, $T_{PCB} = 25^{\circ}C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 100MHz$, $V_{OH} = 850mV$		59		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-116		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-142		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-163		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-168		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-169		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, 4MHz 1 st order high-pass filter, $V_{OH} = 850mV$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 156.25MHz$, $V_{OH} = 850mV$		43		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-112		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-139		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-160		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-166		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-168		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, 4MHz 1 st order high-pass filter, $V_{OH} = 850mV$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 312.5MHz$, $V_{OH} = 850mV$		34		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-98		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-131		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-154		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-165		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-167		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-166		dBc/Hz
R_{J_HPF}	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, 4MHz 1 st order high-pass filter, $V_{OH} = 850mV$				fs
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 625MHz$, $V_{OH} = 850mV$		34		fs
PN_{100}	Phase Noise at 100Hz Offset					dBc/Hz
PN_{1k}	Phase Noise at 1kHz Offset			-97		dBc/Hz
PN_{10k}	Phase Noise at 10kHz Offset			-127		dBc/Hz
PN_{100k}	Phase Noise at 100kHz Offset			-148		dBc/Hz
PN_{1M}	Phase Noise at 1MHz Offset			-160		dBc/Hz
PN_{10M}	Phase Noise at 10MHz Offset			-162		dBc/Hz
PN_{100M}	Phase Noise at 100MHz Offset			-162		dBc/Hz
R_J	RMS Jitter (Integration BW: 12kHz to 20MHz)	$F_{out} = 125MHz$, $V_{OH} = 850mV$				fs
$R_{JITT,RMS}$	RMS period jitter	$F_{out} = 156.25MHz$, $V_{OH} = 850mV$				fs
$R_{JITT,PK}$	Peak-to-peak period jitter	$F_{out} = 156.25MHz$, $V_{OH} = 850mV$				fs

- (1) Parameter is specified by design, not characterized or tested in production.
- (2) See *Differential Voltage Measurement Terminology* section for definition of $V_{OD,DIFF}$ voltages

- (3) V_{CROSS} is single-ended voltage when $\text{CLKOUTx_P} = \text{CLKOUTx_N}$ with respect to system ground. Only valid on rising edge of CLKOUTx_P , when CLKOUTx_N is rising.

6.7 Timing Diagrams

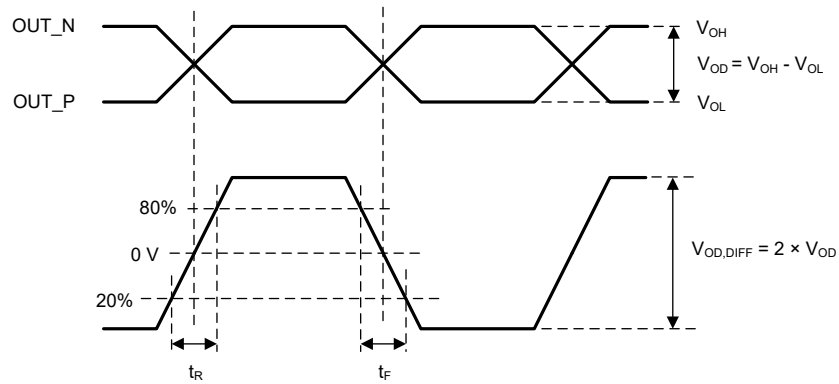


Figure 6-1. Differential Output Voltage Swing and Rise/Fall Time Definitions

6.8 Typical Characteristics

Typical values at 25°C.

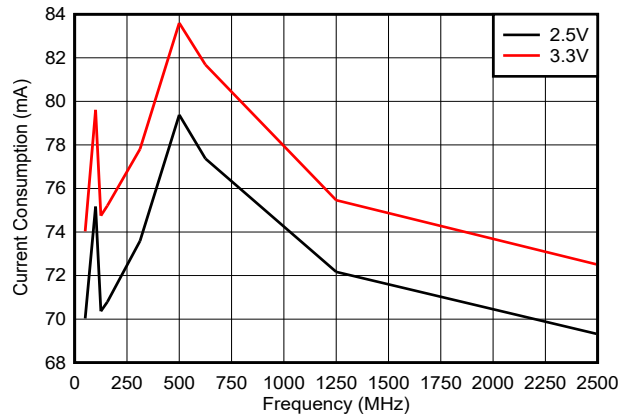


Figure 6-2. AC-LVPECL Current Consumption Across Frequency and Supply Voltage

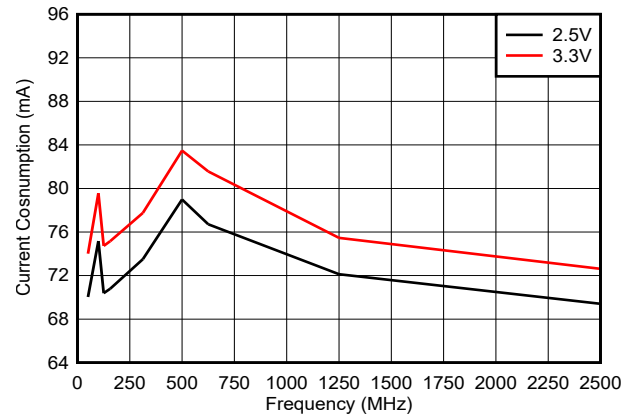


Figure 6-3. LVDS Current Consumption Across Frequency and Supply Voltage

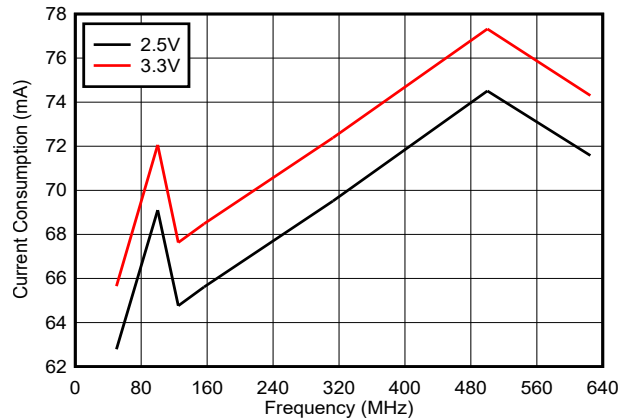


Figure 6-4. LP-HCSL ($V_{OH} = 850\text{mV}$) Current Consumption Across Frequency and Supply Voltage

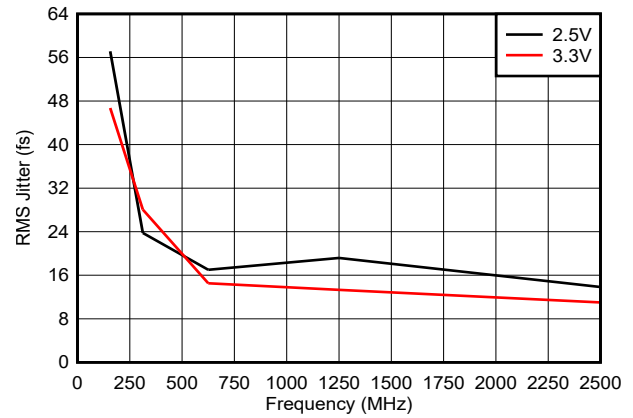


Figure 6-5. AC-LVPECL RMS Jitter (12kHz to 20MHz) Across Frequency and Supply Voltage

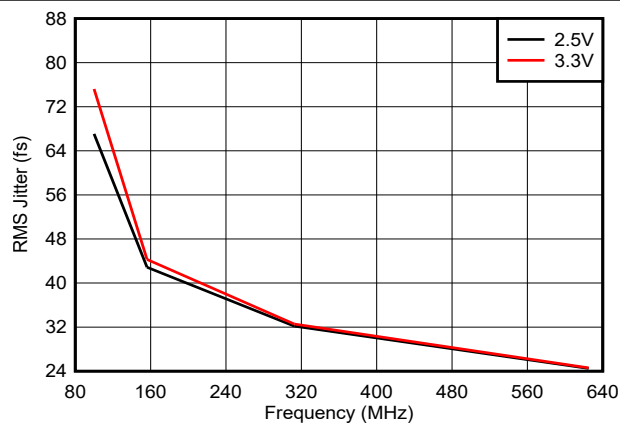


Figure 6-6. LP-HCSL ($V_{OH} = 850\text{mV}$) RMS Jitter vs. Frequency and Supply Voltage

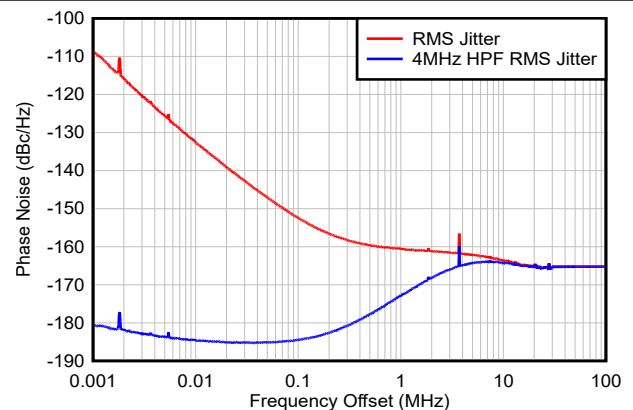


Figure 6-7. AC-LVPECL 312.5MHz Phase Noise Curve at 3.3V

7 Parameter Measurement Information

7.1 Device Output Configurations

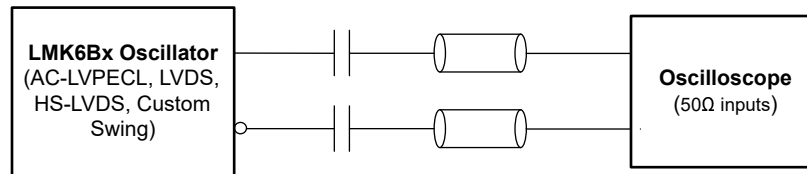


Figure 7-1. LMK6Bx Output Test Configuration for AC-LVPECL, LVDS, and Custom Swing Output Types

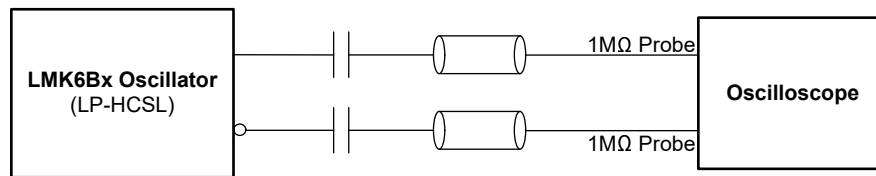


Figure 7-2. LMK6Bx Output Test Configuration for LP-HCSL Output Type

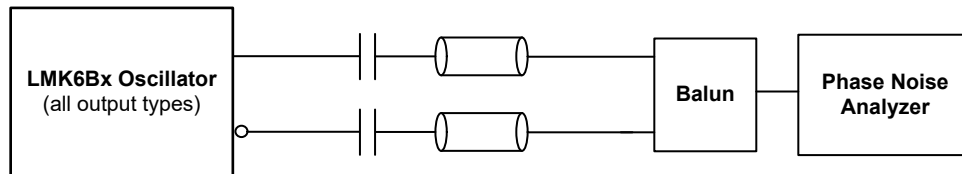


Figure 7-3. LMK6Bx Output Phase Noise Configuration for All Output Types

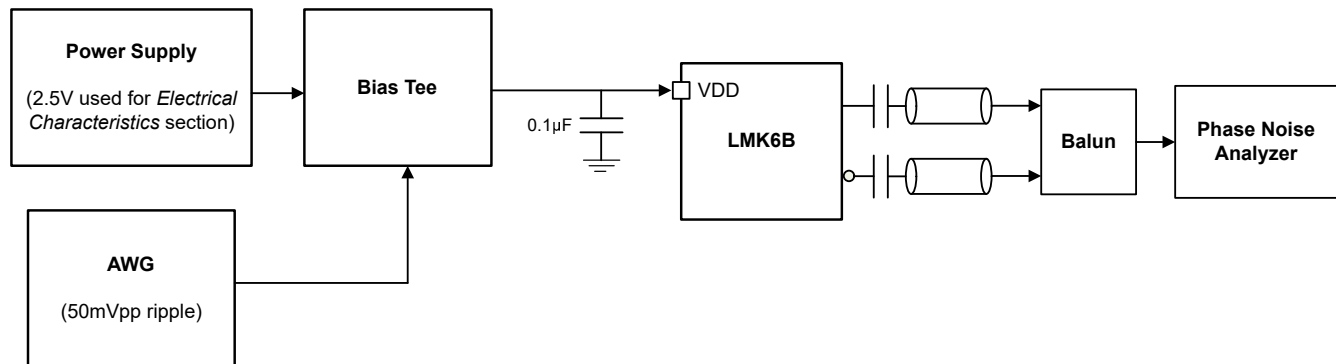


Figure 7-4. LMK6Bx PSRR Configuration

8 Detailed Description

8.1 Overview

The LMK6Bx is a fixed-frequency, factory-programmed BAW-based oscillator that can provide ultra-low jitter for differential outputs.

8.2 Functional Block Diagram

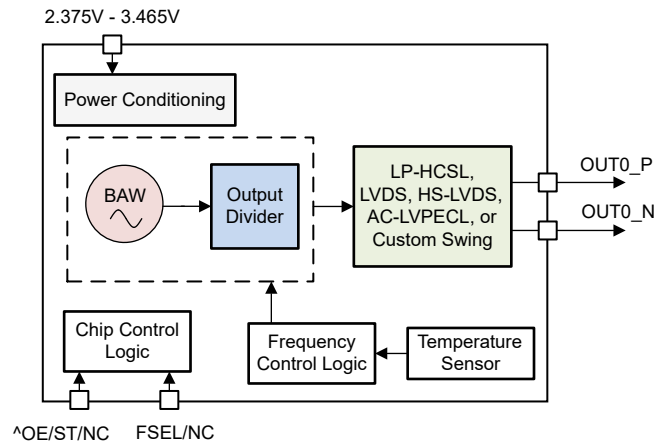


Figure 8-1. Functional Block Diagram

8.3 Features Description

8.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by adsorption of surface contaminants and can be directly placed in the non-hermetic plastic package with a small standard oscillator footprint of the oscillator IC. Refer to the [BAW webpage](#) for more details on TI's BAW technology.

8.3.2 Device Block-Level Description

The LMK6Bx contains a BAW oscillator, an integer divider, and an output driver, which together generate a factory-programmed output frequency. Temperature variations of oscillation frequency are continuously monitored by an internal precision temperature sensor and provided as input to the frequency control logic block as seen on [LMK6Bx Functional Block Diagram](#). Using this frequency control logic block, frequency corrections are performed internally for maintaining the output frequency within $\pm 25\text{ppm}$ or $\pm 20\text{ppm}$ across temperature range and aging for 10 years. The output driver is capable of providing differential AC-LVPECL, LVDS, HS-LVDS, LP-HCSL, and Custom Swing output formats. The device contains internal LDOs which reduces the power supply noise, resulting in low noise clock output, and exceptional PSRR performance as seen on [Electrical Characteristics](#).

8.3.3 Function Pins

Pins 1 and 2 on the LMK6Bx serve multiple functions as defined by the OPN (refer to [Section 4](#) for more information). Configurations include Output Enable (OE) and Stand By (ST) on pin 1, and Output Frequency Select (FSEL) on pin 2. FSEL divides the frequency defined in the OPN by 2 or 4, providing 3 different frequencies from one OPN. FSEL is further described in [Table 8-1](#). OE and ST are Active High by default. Contact TI for Active Low options.

Pin 1 is driven internally with a 150kΩ pullup resistor. Pin 2 is driven internally with a 200kΩ pullup and 200kΩ pulldown resistors. Both pin 1 and 2 can have an external pullup or pulldown resistor between 0Ω to 10kΩ each.

Table 8-1. Function Pin Descriptions for LMK6Bx

ORDERABLE OPTION	PIN NO.	PIN DESCRIPTION	OUTPUT FUNCTION
E	Pin 1	Output Enable (Active High) or No Connect	HIGH or No Connect : Output active at specified frequency LOW : Output disabled, high impedance; current consumption is given by I_{DD-OD}
	Pin 2	No Connect	N/A
A	Pin 1	Standby (Active Low) or No Connect	HIGH or No Connect : Output active at specified frequency LOW : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$
	Pin 2	No Connect	N/A
K	Pin 1	Output Enable (Active High) or No Connect	HIGH or No Connect : Output active at specified frequency LOW : Output disabled, high impedance; current consumption is given by I_{DD-OD}
	Pin 2	FSEL ⁽¹⁾	HIGH : Output active at $F_{OUT}/2$ FLOATING : Output active at F_{OUT} LOW : Output active at $F_{OUT}/4$
L	Pin 1	Standby (Active Low) or No Connect	HIGH or No Connect : Output active at specified frequency LOW : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$
	Pin 2	FSEL ⁽¹⁾	HIGH : Output active at $F_{OUT}/2$ FLOATING : Output active at F_{OUT} LOW : Output active at $F_{OUT}/4$

(1) F_{OUT} is the output frequency defined in the OPN (refer to [Section 4](#)).

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of *Electrical Characteristics*. The return time to the active output clock, or t_{ST-EN} corresponds to the same as the initial start-up time, or t_{START_UP} .

8.3.4 Output Terminations

The LMK6Bx has different output types: AC-LVPECL, LVDS, HS-LVDS, LP-HCSL, and Custom Swing. HS-LVDS and Custom Swing have different swing and common mode options. LP-HCSL output type has different V_{OH} options. For more information refer to [Section 4](#).

The multi-mode driver can create an output with a common mode set to $V_{DD}/2$ or 1.2V and a customizable swing from 350mVppd to 2Vppd. For the Custom Swing output type, the $V_{CM} = V_{DD}/2$ and the swing can be set from 350mVppd to 2Vppd for 3.3V supply and 350mVppd to 1.5Vppd for 2.5V supply. AC-LVPECL output type uses this driver to generate a 1.6Vppd with a $V_{CM} = V_{DD}/2$ for either 2.5V or 3.3V. The multi-mode driver can also generate an LVDS-like (including HS-LVDS) output, which has a 1.2V common mode and a customizable swing from 350mVppd to 2Vppd for a 3.3V supply and 350mVppd to 1.6Vppd for a 2.5V supply. By default, the LVDS driver comes with a 800mVppd swing.

To maximize the performance of the oscillator, use the Custom Swing multi-mode driver or AC-LVPECL. Better performance is achieved with a higher swing, so order the highest swing the receiver can handle.

No changes are required to replace an LVDS oscillator with the LMK6Bx. If replacing an LVDS oscillator for an AC-coupled applications and maximum performance is required, use the Custom Swing or AC-LVPECL output type and order the highest swing option the receiver can handle. No changes are required when replacing an LVDS oscillator with the Custom Swing or AC-LVPECL driver for AC-coupled applications. To replace an LVPECL oscillator refer to [Section 9.3.1](#). Termination schemes for AC-LVPECL, LVDS, HS-LVDS, and Custom Swing are shown in [Figure 8-2](#).

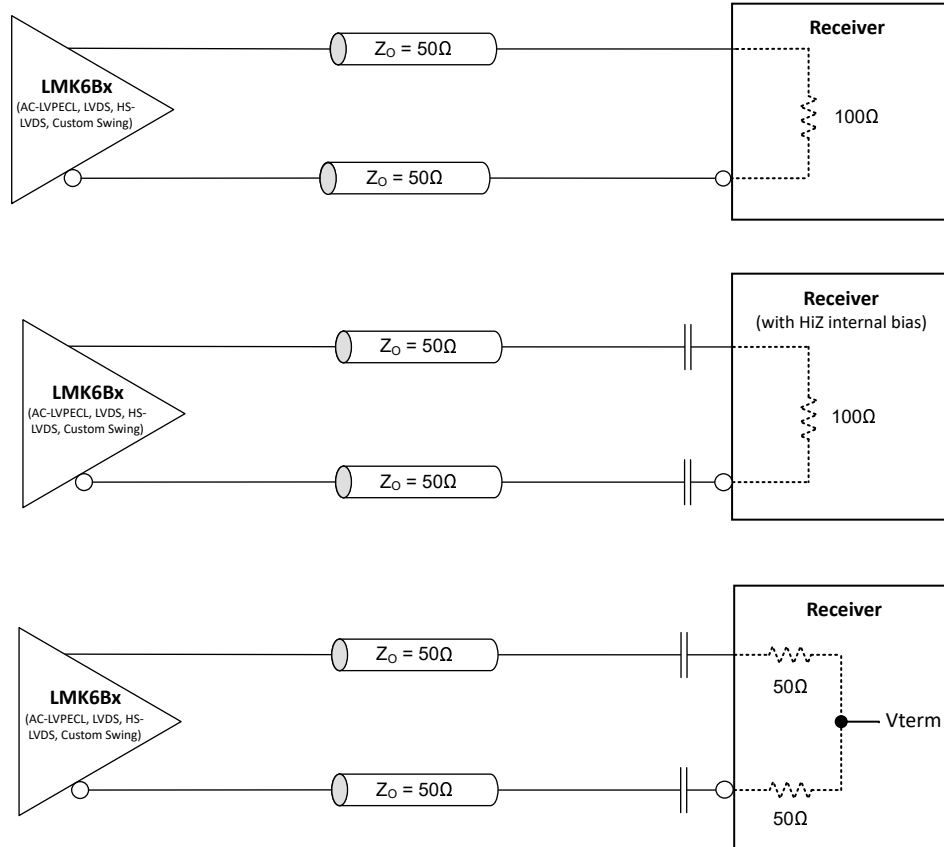


Figure 8-2. AC-LVPECL, LVDS, HS-LVDS, and Custom Swing Output Terminations

The LP-HCSL output driver can have a V_{OH} of 850mV or 750mV typical. No external termination is required as shown in [Figure 8-3](#). No changes are required to replace a LP-HCSL oscillator with the LMK6Bx. To replace a HCSL oscillator with the LMK6Bx, refer to [Section 9.3.2](#).

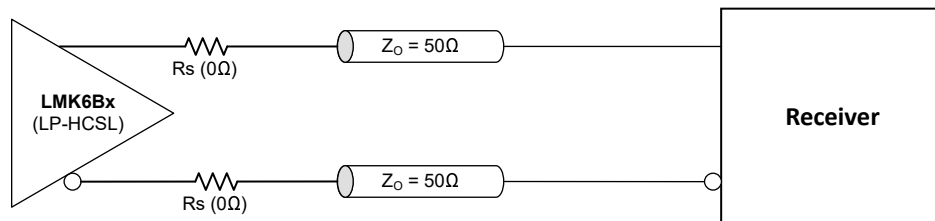


Figure 8-3. LP-HCSL Output Termination

To drive TI clock buffers with the LMK6Bx, refer to [Clocking TI Clock Buffers with the LMK6Bx](#) application note.

8.4 Device Functional Modes

The fixed-frequency, factory-programmed LMK6Bx can have different configurations based on the OPN as shown on [Section 4](#). The function pins, pins 1 or 2, can be set to output enable, standby, frequency select, or no connect. Frequency select divides the frequency defined in the OPN by 2 or 4, providing 3 different frequencies from one OPN. For more details, refer to [Section 8.3.3](#).

The LMK6Bx can also come in different output types with different swings and common modes (AC-LVPECL, LVDS, HS-LVDS, and Custom Swing) and LP-HCSL output type with different V_{OH} options as shown on [Section 4](#). For more details, refer to [Section 8.3.4](#).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK6Bx is an ultra-low jitter, fixed-frequency, factory-programmed, differential BAW oscillator that can be used as a reference clock for several applications. The device supports any output frequency between 50MHz to 2500MHz for the AC-LVPECL, LVDS, HS-LVDS, and Custom Swing output types and 50MHz to 625MHz for the LP-HCSL output type. The LMK6Bx supports 2.375V to 3.465V supply rails (nominal 2.5V and 3.3V).

9.2 Typical Application

Figure 9-1 shows an example of a typical application. The LMK6Bx oscillator is the reference clock for a DSP used in optical transceiver modules.

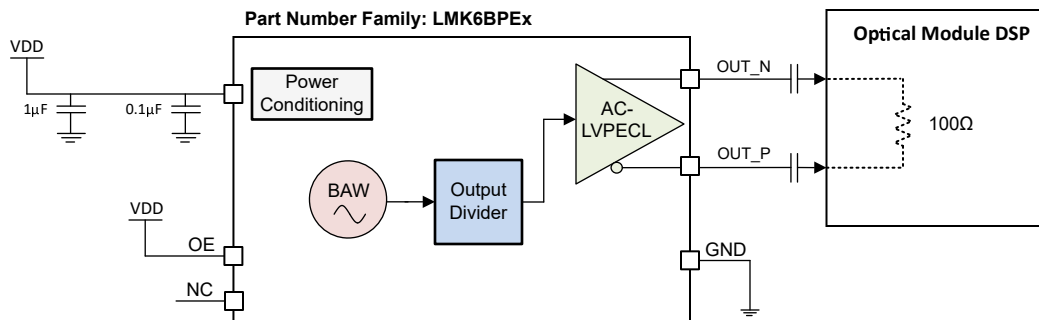


Figure 9-1. LMK6Bx Used as Reference Clock for a DSP of an Optical Transceiver Module

For a layout example of the LMK6Bx and bypass capacitor and AC-coupling capacitor value recommendations, refer to [Section 9.5.2](#). See [Section 8.3.4](#) for output type termination and biasing. Refer to the [The LMK6B: Revolutionizing Optical Module Performance with Industry-Leading Ultra-Low Jitter BAW Oscillators](#) application note to understand the benefits of the LMK6Bx for optical transceivers module applications.

9.2.1 Design Requirements

The LMK6Bx is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in [Section 8.3.4](#) and see [Section 8.3.3](#) to understand pin 1 and 2 function. Order the part number based on [Section 4](#) as per your requirements. Also, make sure to follow [Section 9.4](#) and [Section 9.5.1](#) to maximize the performance of the LMK6Bx.

9.2.2 Detailed Design Procedure

When designing with the LMK6Bx, the first step is to select the correct configuration based on your requirements. The OPN selected determines the output type, pins 1 and 2 functions, output frequency, frequency stability, and package type. Refer to [Section 4](#) for more details.

The LMK6Bx differential oscillator has AC-LVPECL, LVDS, HS-LVDS, LP-HCSL, and Custom Swing output type options. Use the proper AC or DC termination based on the application requirement as shown in [Section 8.3.4](#). The LMK6Bx has output enable, standby, or frequency select options for pins 1 and 2. Refer to [Section 8.3.3](#) for more information on each pin and function. The LMK6Bx has integrated LDOs and excellent PSRR performance as shown in *Electrical Characteristics*. Add a 0.1µF and 1µF to the VDD pin to achieve best performance. Follow [Section 9.4](#) for more power supply pin recommendations and [Section 9.5](#) for best board layout practices when designing with the LMK6Bx.

9.2.3 Clocking TI Clock Buffers with the LMK6Bx

The LMK6Bx can be used as the reference to TI clock buffers to create several ultra-low jitter clocks. The LMK6Bx and the LMKDB1x achieve 42.4fs of jitter at 312.5MHz and the LMK6Bx and the LMK1Dx achieve 19.8fs of jitter at 625MHz (12kHz to 20MHz bandwidth). More information can be found in [Clocking TI Clock Buffers With the LMK6Bx](#) application note.

9.2.4 Application Curves

9.2.4.1 LVDS Phase Noise Curves

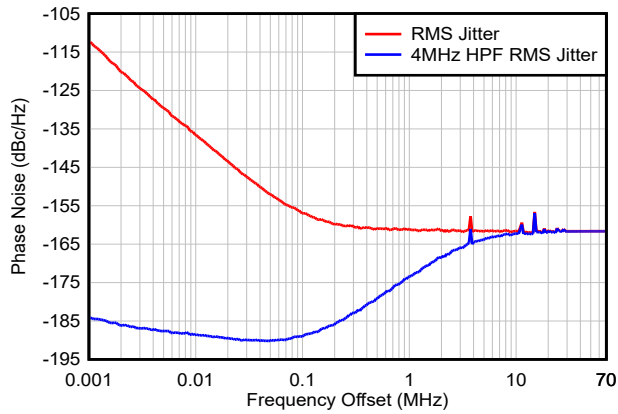


Figure 9-2. 156.25MHz LVDS, 25°C, 3.3V, 47.3fs RMS jitter and 39.2fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

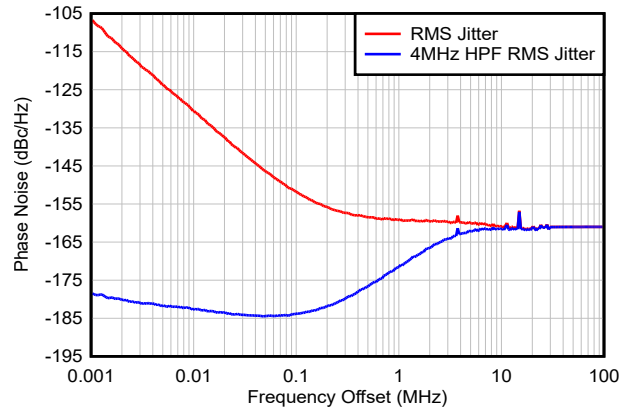


Figure 9-3. 312.5MHz LVDS, 25°C, 3.3V, 38.7fs RMS Jitter and 29.3fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

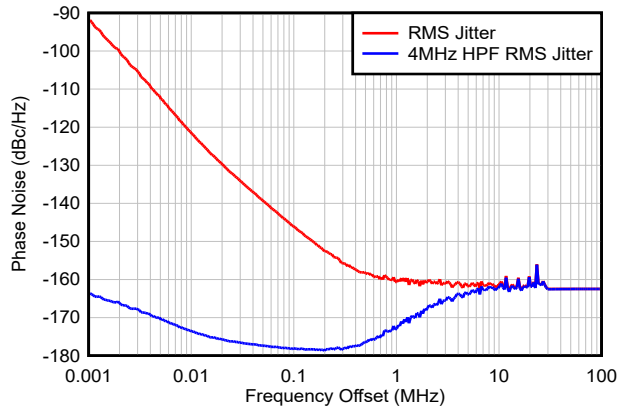


Figure 9-4. 625MHz LVDS, 25°C, 3.3V, 19.3fs RMS Jitter and 11.3fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

9.2.4.2 AC-LVPECL Phase Noise Curves

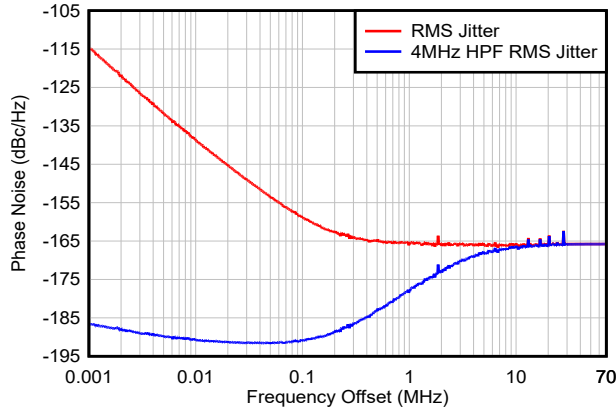


Figure 9-5. 156.25MHz, AC-LVPECL, 25°C, 3.3V, 38.5fs RMS Jitter and 31.0fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

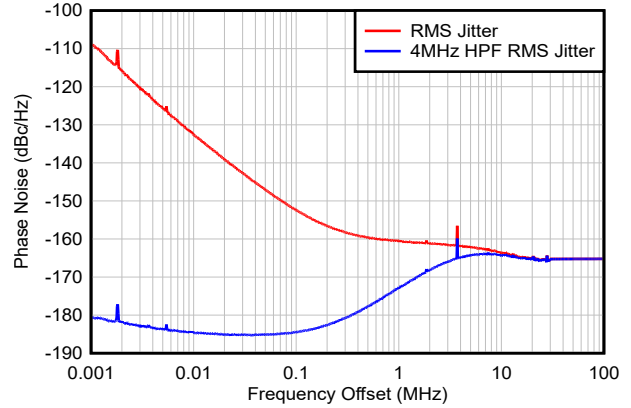


Figure 9-6. 312.5MHz AC-LVPECL, 25°C, 3.3V, 28.2fs RMS Jitter and 19.7fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

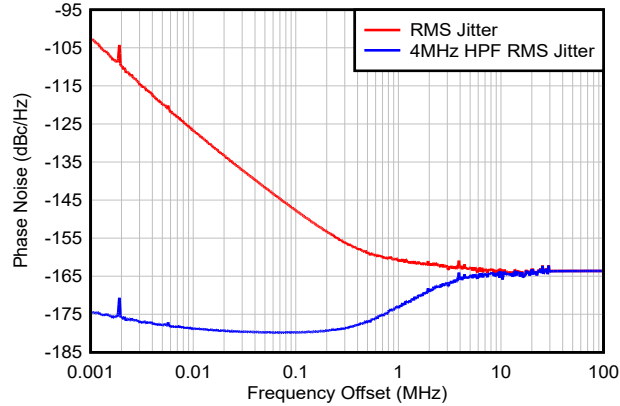


Figure 9-7. 625MHz AC-LVPECL, 25°C, 3.3V, 18.1fs RMS Jitter and 9.6fs 4MHz HPF RMS Jitter (12kHz to 20MHz)

9.2.4.3 LP-HCSL Phase Noise Curves

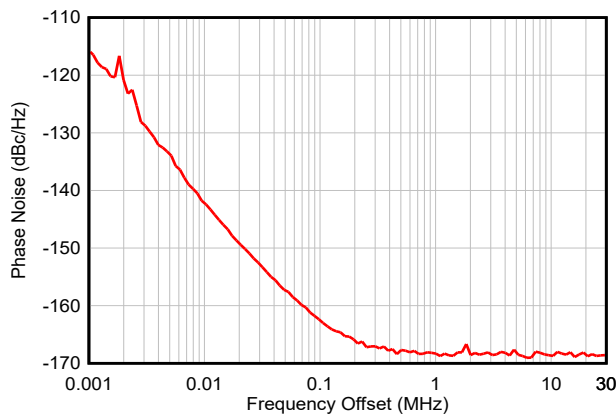


Figure 9-8. 100MHz LP-HCSL, 25°C, 3.3V, 54.4fs RMS Jitter (12kHz to 20MHz)

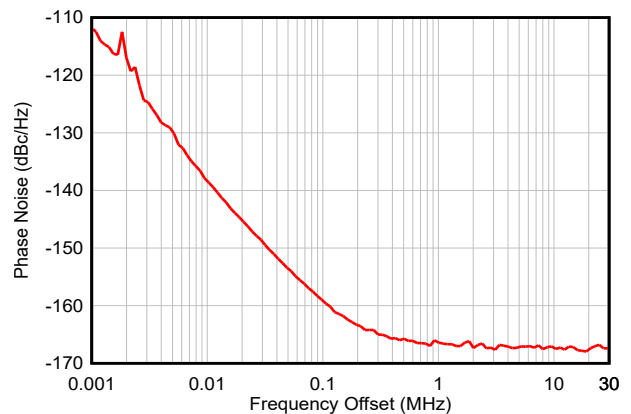


Figure 9-9. 156.25MHz LP-HCSL, 25°C, 3.3V, 38.3fs RMS Jitter (12kHz to 20MHz)

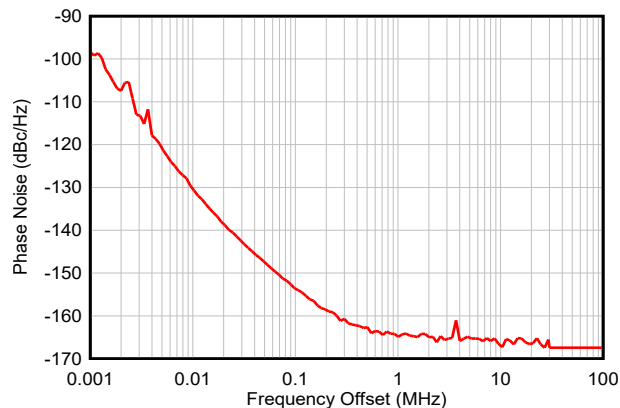


Figure 9-10. 312.5MHz LP-HCSL, 25°C, 3.3V, 27.1fs RMS Jitter (12kHz to 20MHz)

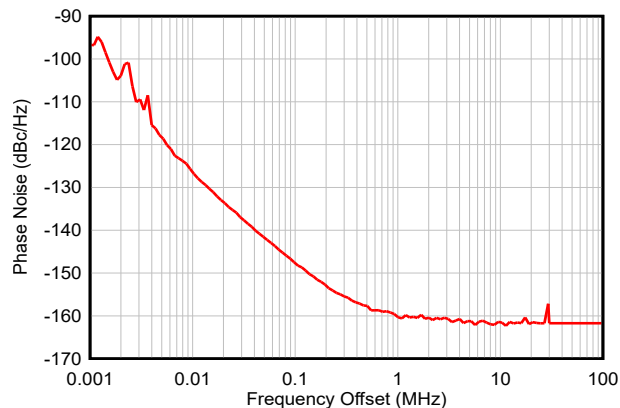


Figure 9-11. 625MHz LP-HCSL, 25°C, 3.3V, 22.9fs RMS Jitter (12kHz to 20MHz)

9.3 Replacing Competitor Oscillators with the LMK6Bx

9.3.1 Replacing a LVPECL oscillator with the LMK6Bx

To replace a LVPECL oscillator with the LMK6Bx for a AC-coupled applications,

1. The receiver must have a 100Ω internal termination (if not, one needs to be placed externally).
2. Use the LMK6Bx AC-LVPECL output type.
3. Depopulate any emitter resistors as shown in Figure 9-12.

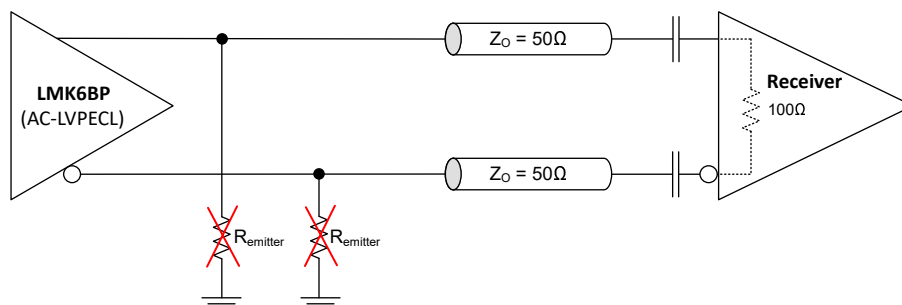


Figure 9-12. Replacing a LVPECL oscillator with the LMK6Bx

9.3.2 Replacing a HCSL OSC With the LMK6Bx

If using the LMK6Bx to replace a HCSL oscillator, follow these steps:

1. Use the LMK6Bx LP-HCSL output type.
2. Depopulate any 50Ω resistors to GND as shown in Figure 9-13.
3. Replace any series resistors with 0Ω as shown in Figure 9-13.

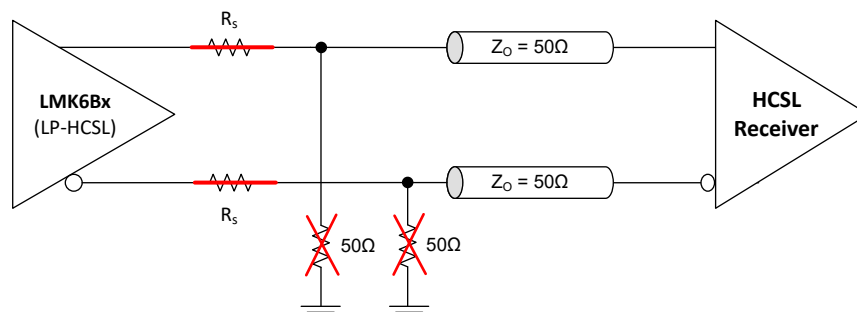


Figure 9-13. Replacing an HCSL Oscillator With the LMK6Bx

9.4 Power Supply Recommendations

For the best electrical performance of the LMK6Bx, TI recommends using 0.1μF and 1μF capacitor on the device power supply bypass network. Place these capacitors as close as possible to the supply pins. TI also recommends using component side mounting of the power supply bypass capacitors and use 0201 body size for the 0.1μF capacitor and 0603 body size for the 1μF capacitor to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

9.5 Layout

9.5.1 Layout Guidelines

The LMK6Bx can operate up to 2500MHz. To optimize the oscillator's performance, make sure to follow industry-standard high-speed layout guidelines as explained in [High-Speed Layout Guidelines](#). To summarize,

- Minimize long stubs that create antenna effects and deteriorate output performance.
- Impedance match the differential output traces to 50Ω single-ended or 100Ω differential to eliminate reflections.
- Make the output traces as short as possible and of equal length to achieve maximum performance.

[Section 9.5.1.1](#) discusses on providing thermal reliability for good thermal and electrical performance. [Section 9.5.1.2](#) discusses how to maintain signal integrity of the entire system by implementing a good solder reflow profile.

9.5.1.1 Providing Thermal Reliability

The LMK6Bx is a high-performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

[Equation 1](#) describes the relationship between the PCB temperature around the LMK6Bx and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- T_B : PCB temperature around the LMK6Bx
- T_J : Junction temperature of LMK6Bx
- Ψ_{JB} : Junction-to-board thermal resistance parameter of LMK6Bx (refer to the *Thermal Information* tables in the [Section 6](#) section for this information)
- P : On-chip power dissipation of LMK6Bx

9.5.1.2 Recommended Solder Reflow Profile

TI recommends following the recommendations provided by the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing the LMK6Bx with the lowest peak temperature possible is preferable while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile depends on several factors including maximum peak temperature as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, solder manufacture recommended profile, and capability of the reflow equipment as confirmed by the SMT assembly operation.

9.5.2 Layout Example

Figure 9-14 through Figure 9-18 show the printed circuit board (PCB) layout examples as done on the evaluation module (EVM) for the LMK6BEVM.

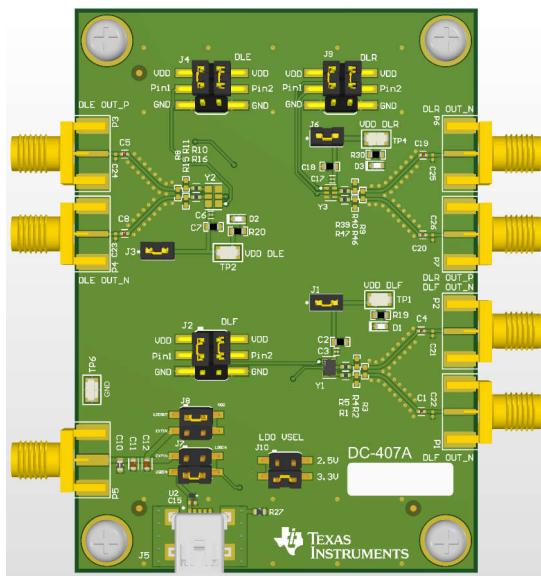


Figure 9-14. PCB Layout Example From LMK6BEVM

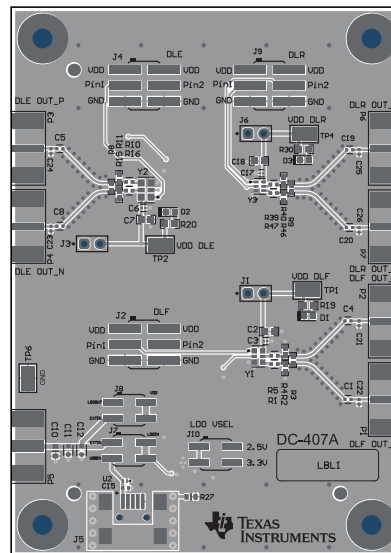


Figure 9-15. PCB Layout Example From LMK6BEVM - Top Layer

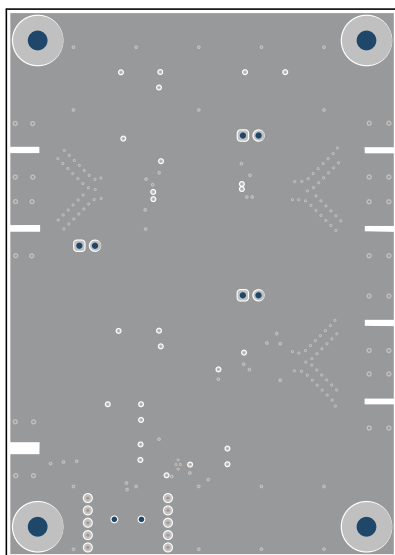


Figure 9-16. PCB Layout Example From LMK6BEVM - Ground Layer

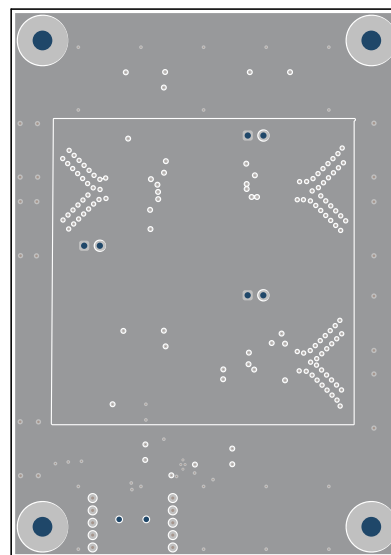


Figure 9-17. PCB Layout Example From LMK6BEVM - Power Layer

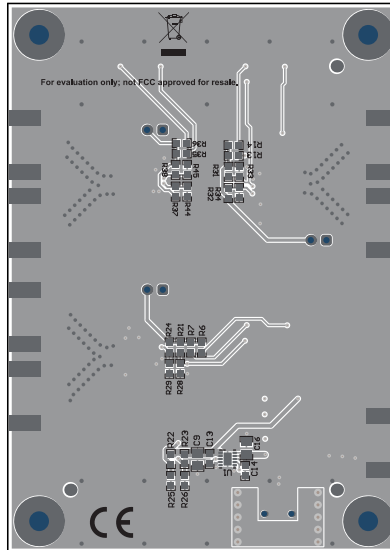


Figure 9-18. PCB Layout Example From LMK6BEVM - Bottom Layer

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMK6BEVM User's Guide](#)
- Texas Instruments, [The LMK6B: Revolutionizing Optical Module Performance with Industry-Leading Ultra-Low Jitter BAW Oscillators](#), application note
- Texas Instruments, [Clocking TI Clock Buffers With the LMK6Bx](#), application note
- Texas Instruments, [Standalone BAW Oscillators Advantages Over Quartz Oscillators](#), application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

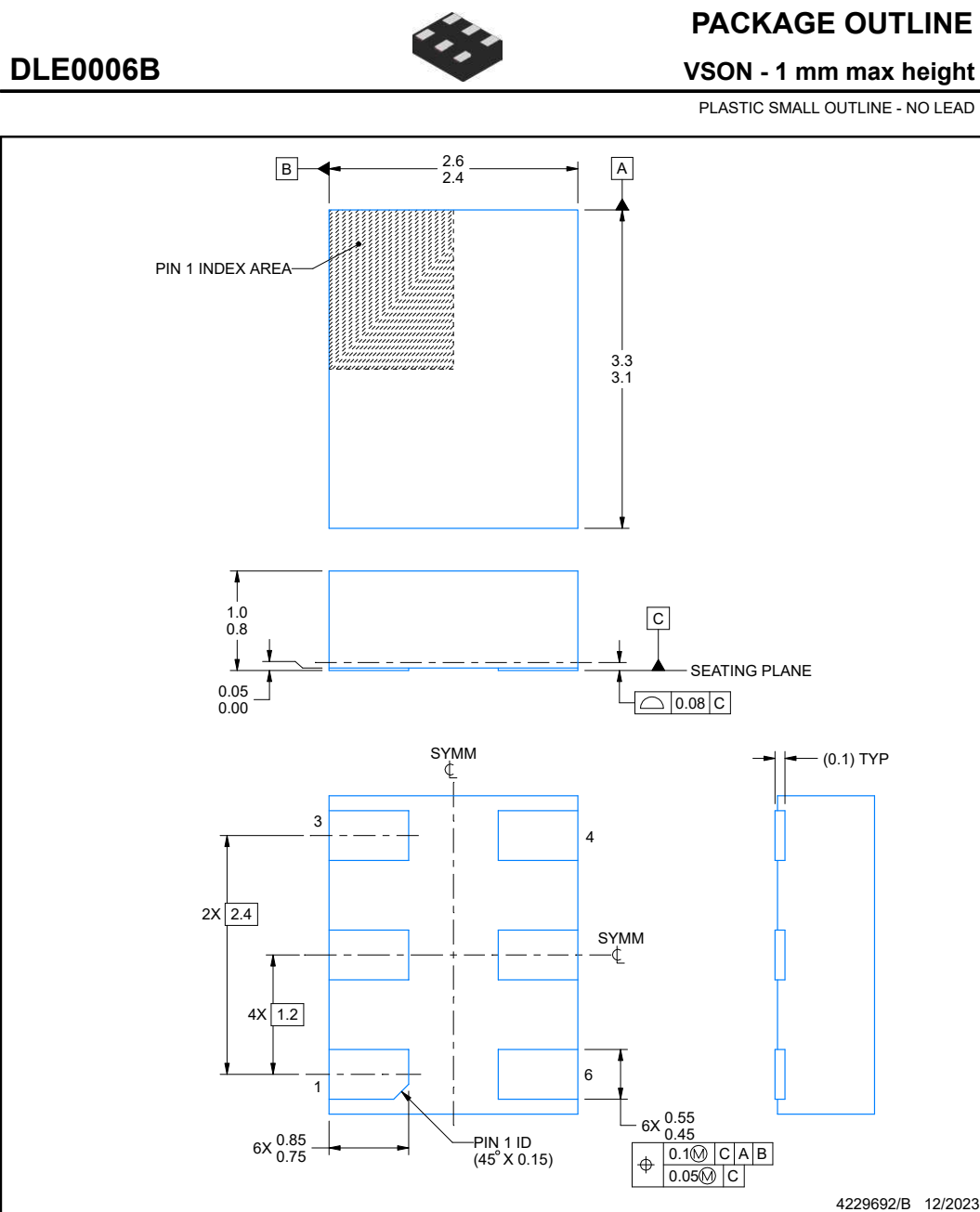
DATE	REVISION	NOTES
March 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

ADVANCE INFORMATION



NOTES:

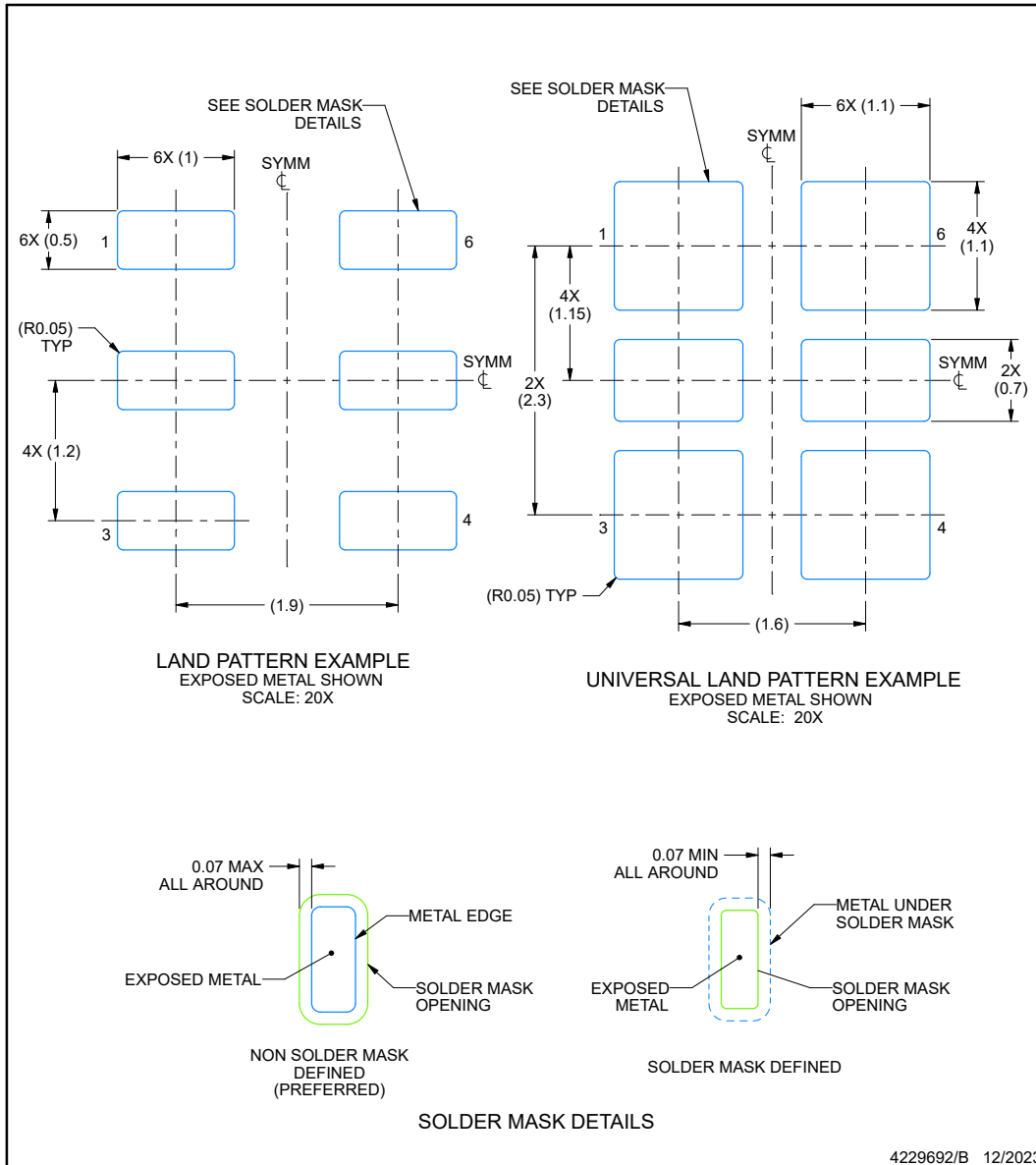
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DLE0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

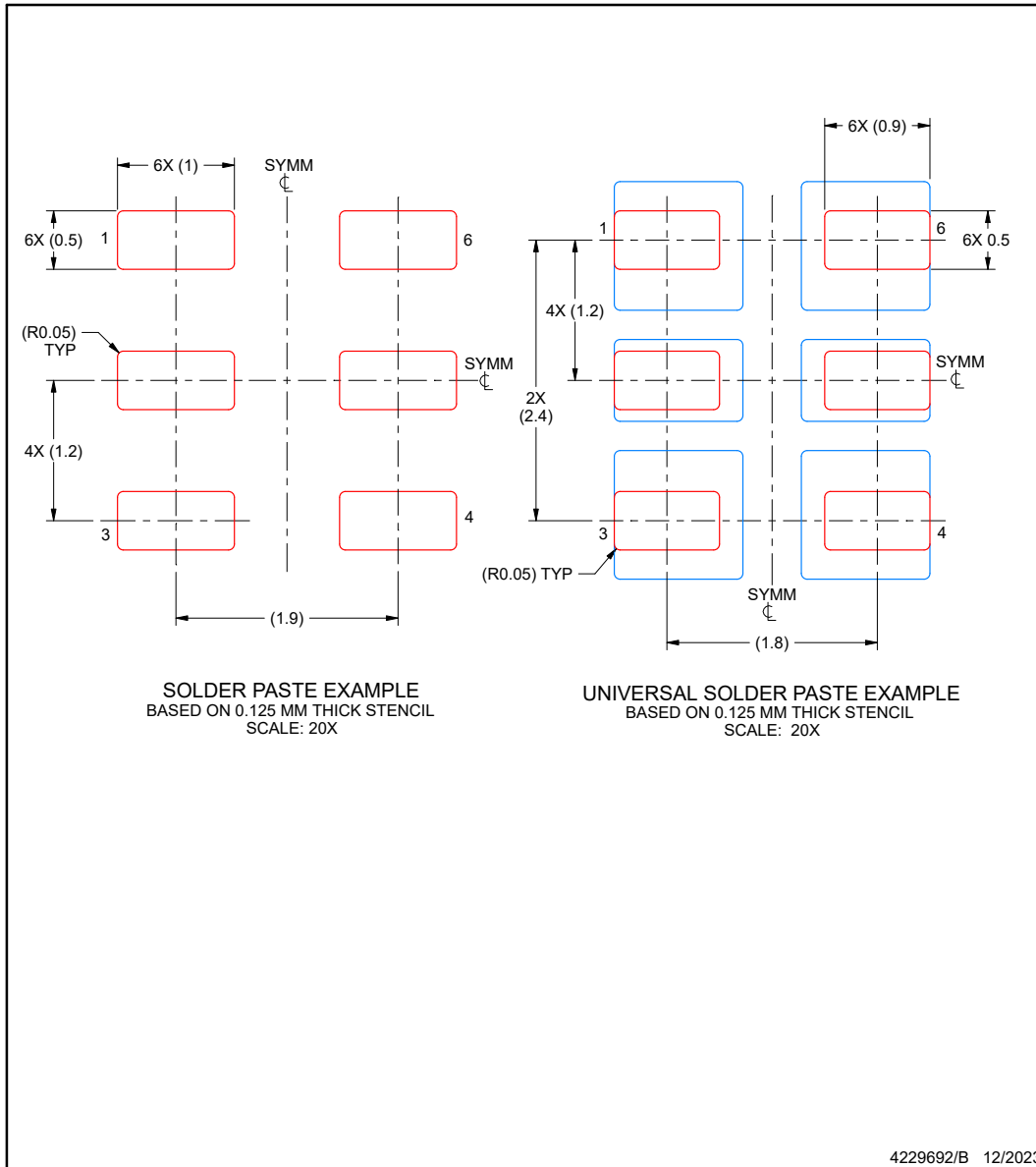


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN**DLE0006B****VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

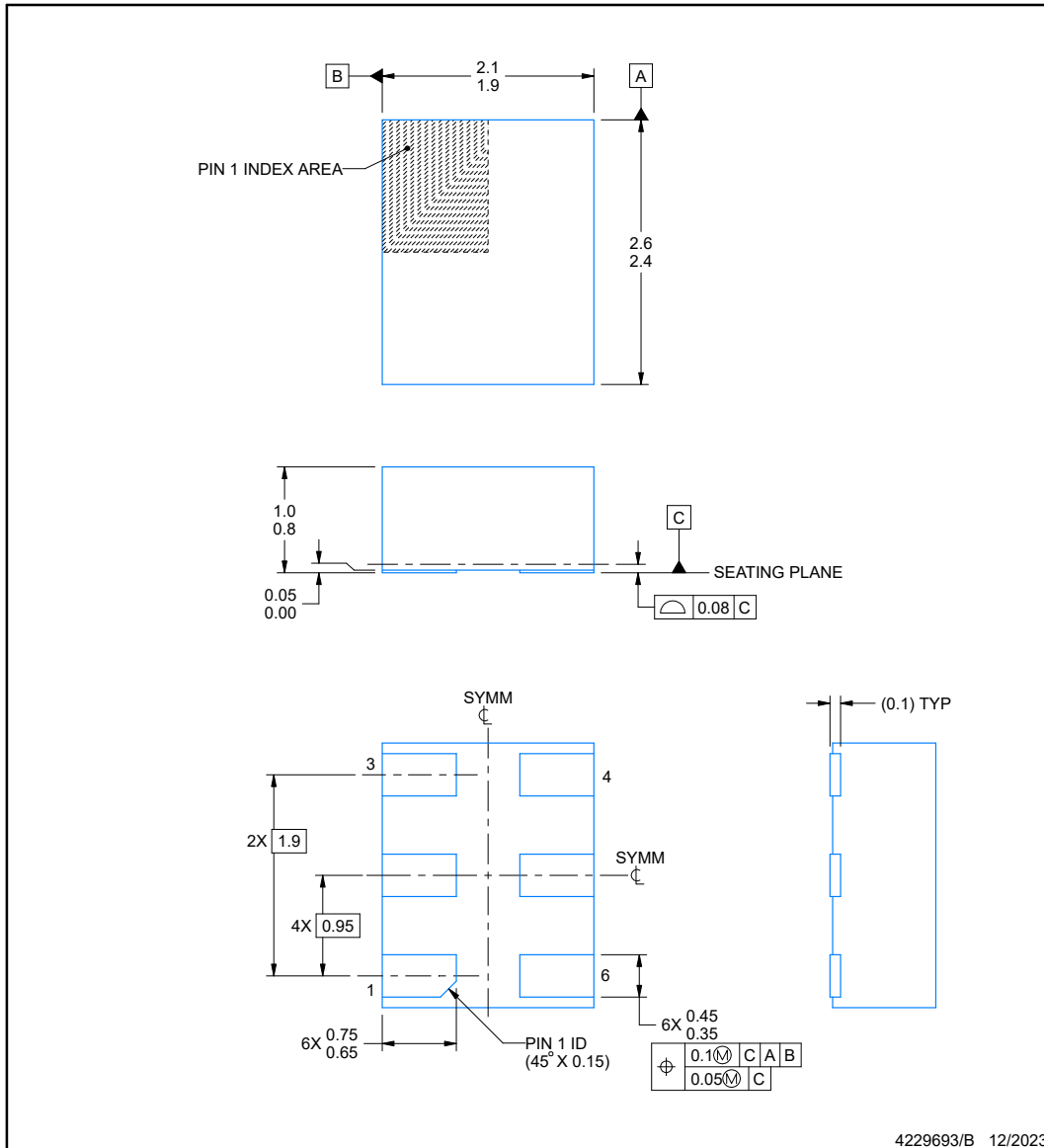
DLF0006B



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

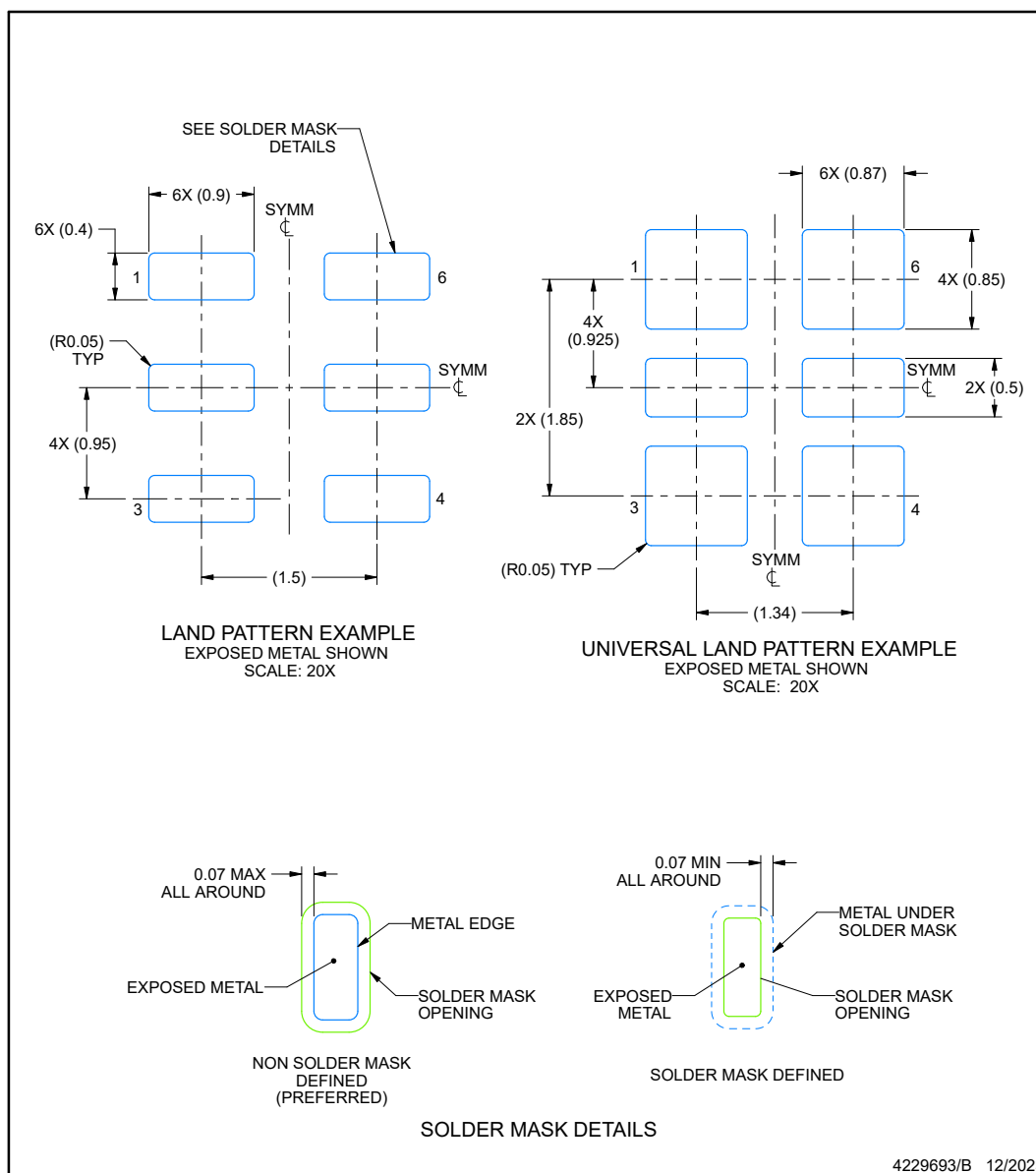
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DLF0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

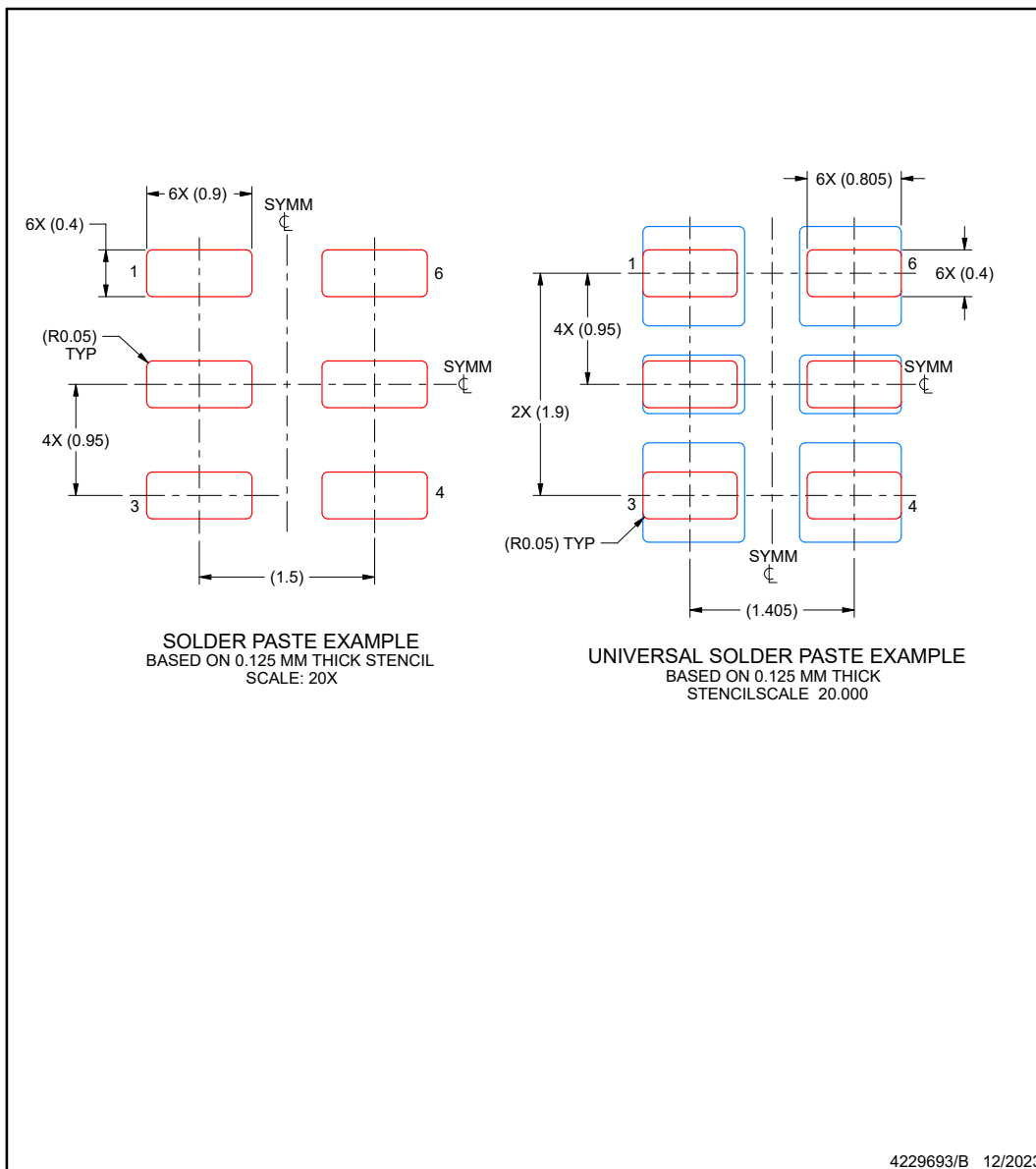
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DLF0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

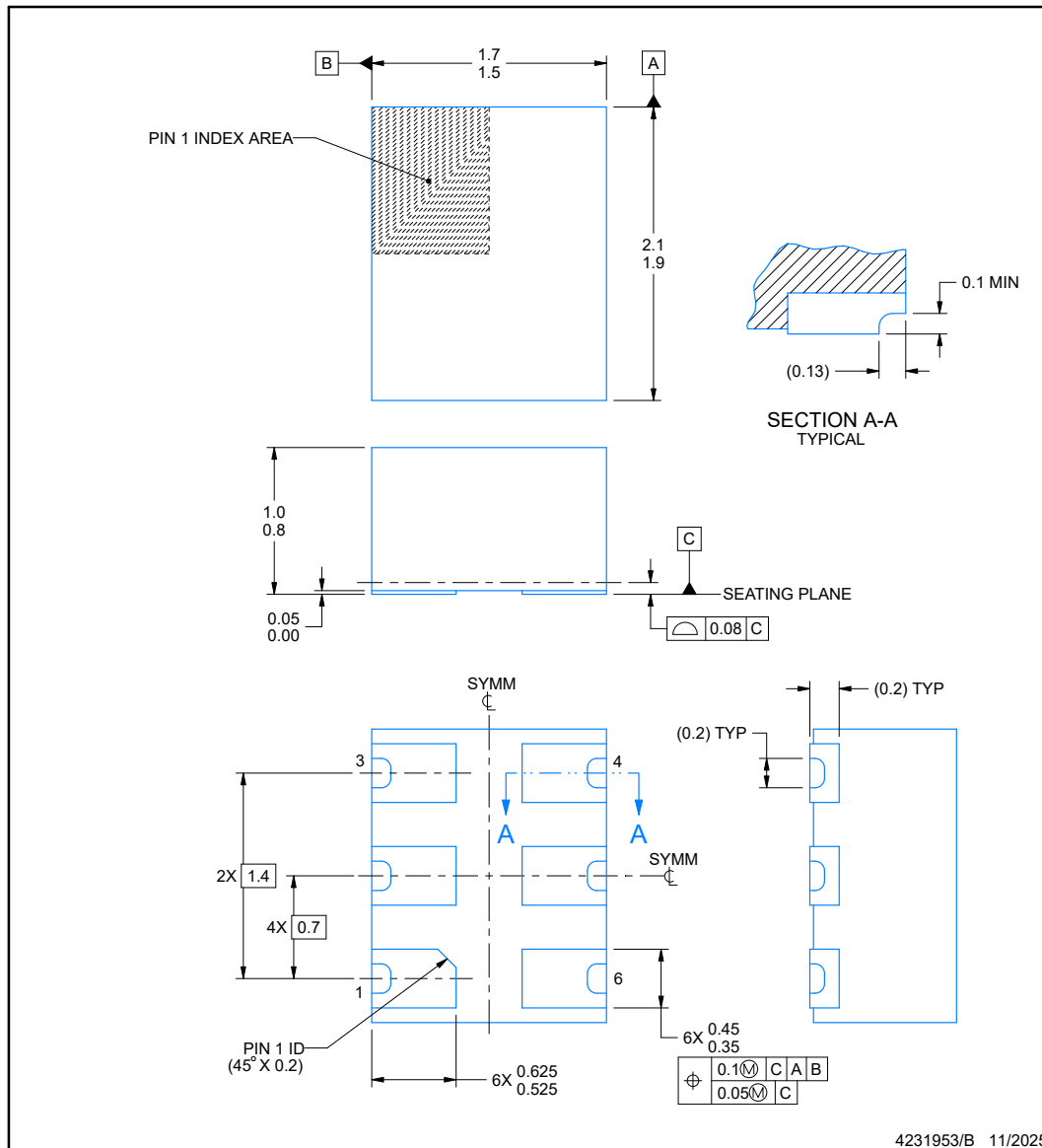


NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


DLR0006B
PACKAGE OUTLINE
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


NOTES:

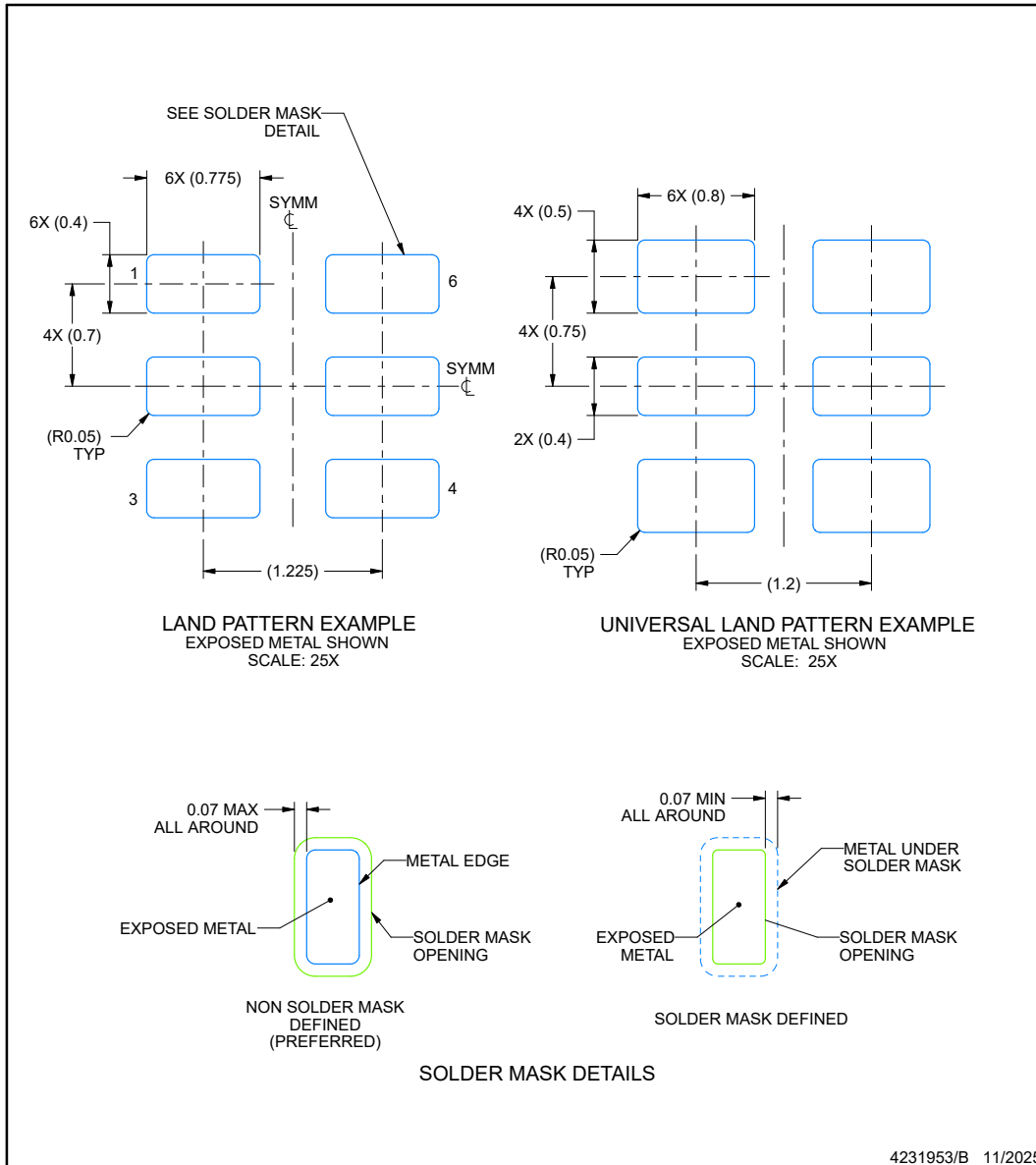
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DLR0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

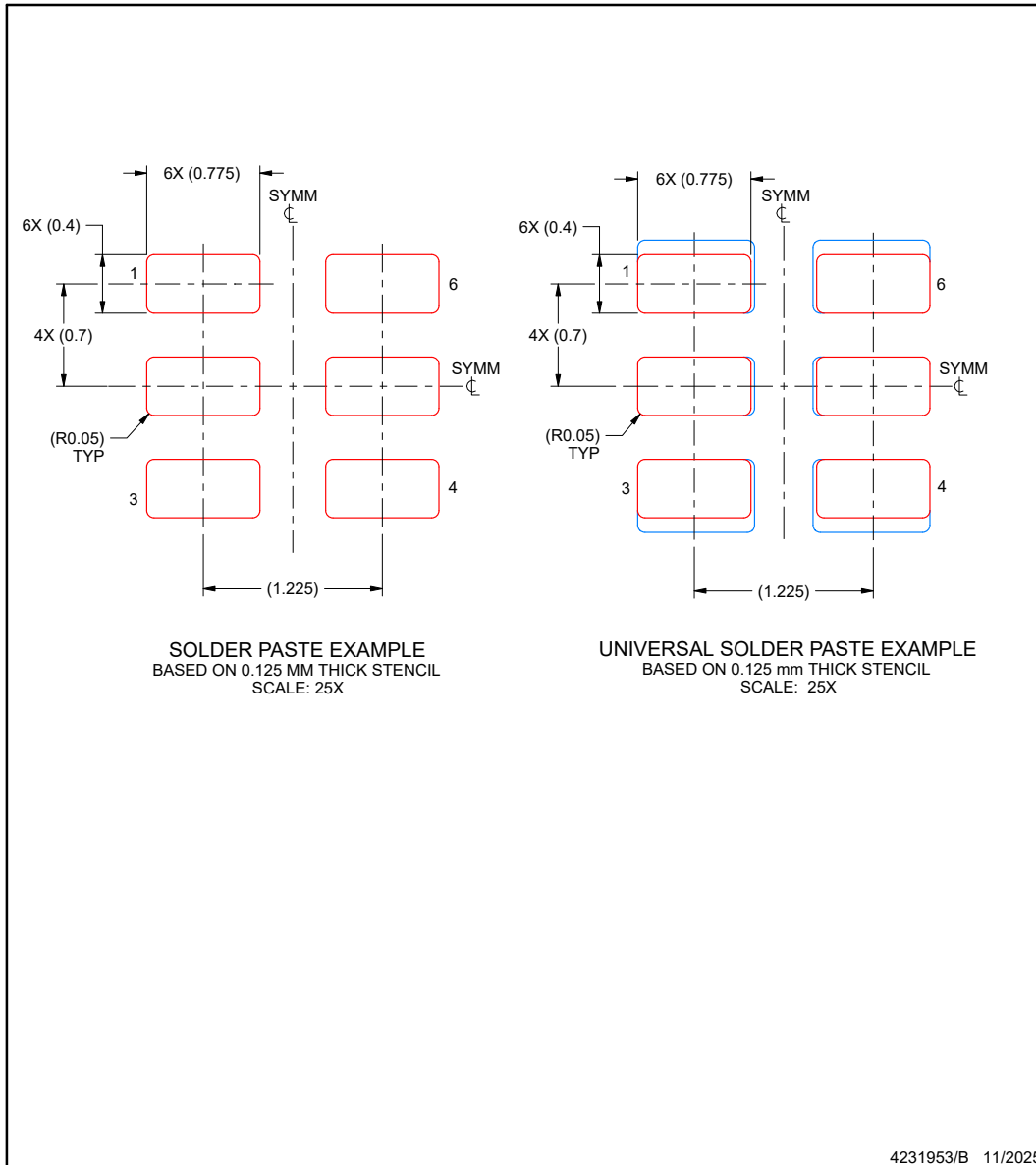
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DLR0006B

VSON - 1 mm max height

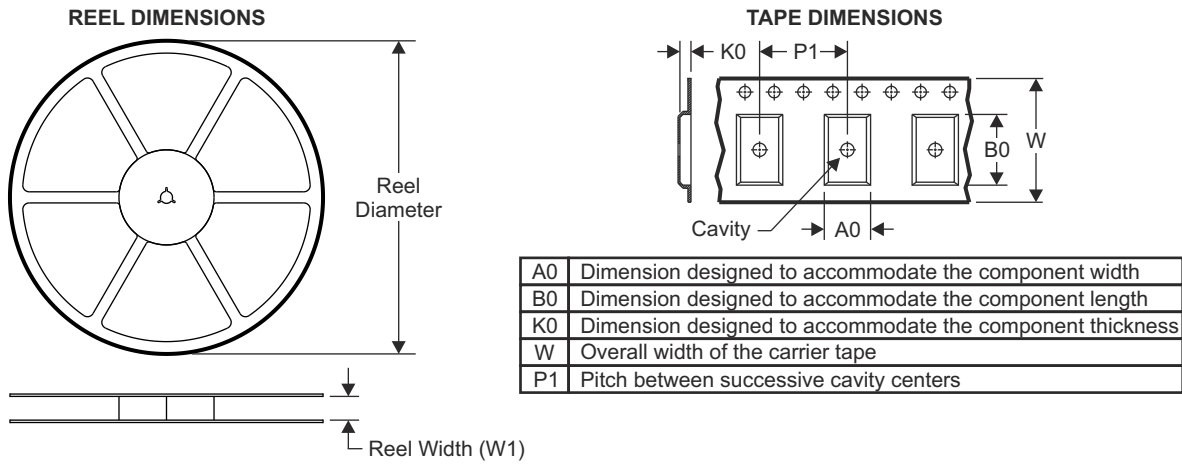
PLASTIC SMALL OUTLINE - NO LEAD



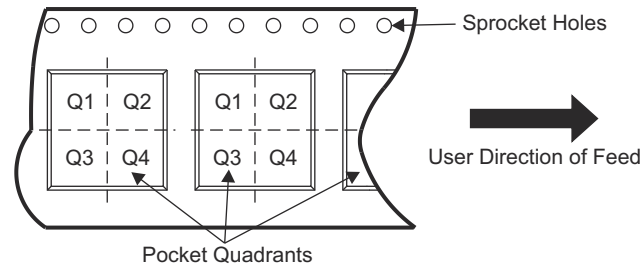
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.2 Tape and Reel Information

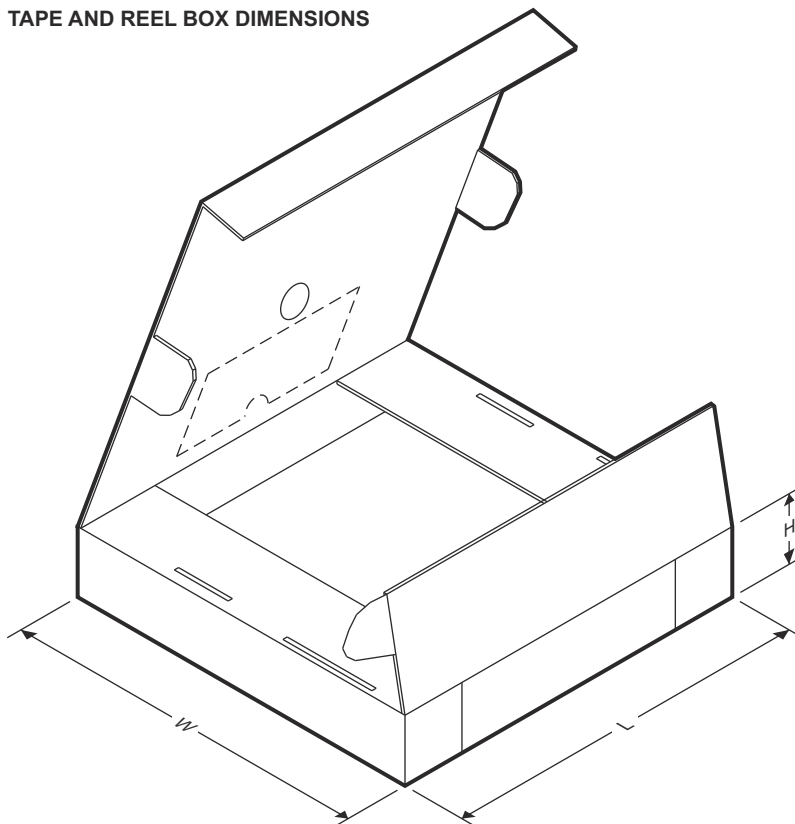


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLMK6BPK62500FDLR R	VSON	DLR	6	3000	180	8.4	1.85	2.3	1.16	4	8	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLMK6BPK62500FDLRR	VSON	DLR	6	3000	182	182	20

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLMK6BPK62500FDLRR	Active	Preproduction	VSON (DLR) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 105	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025