User's Guide

LMX2820 Register Map

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1 LMX2820 Register Map

Table 1-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. Device Registers

Offset	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1		Go
0x2	R2		Go
0x3	R3		Go
0x4	R4		Go
0x5	R5		Go
0x6	R6		Go
0x7	R7		Go
0x8	R8		Go
0x9	R9		Go
0xA	R10		Go
0xB	R11		Go
0xC	R12		Go
0xD	R13		Go
0xE	R14		Go
0xF	R15		Go
0x10	R16		Go
0x11	R17		Go
0x12	R18		Go
0x13	R19		Go
0x14	R20		Go
0x15	R21		Go
0x16	R22		Go
0x17	R23		Go
0x18	R24		Go
0x19	R25		Go
0x1A	R26		Go
0x1B	R27		Go
0x1C	R28		Go
0x1D	R29		Go
0x1E	R30		Go
0x1F	R31		Go
0x20	R32		Go
0x21	R33		Go
0x22	R34		Go
0x23	R35		Go
0x24	R36		Go
0x25	R37		Go
0x26	R38		Go
0x27	R39		Go
0x28	R40		Go
0x29	R41		Go
0x2A	R42		Go

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Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x2B	R43		Go
0x2C	R44		Go
0x2D	R45		Go
0x2E	R46		Go
0x2F	R47		Go
0x30	R48		Go
0x31	R49		Go
0x32	R50		Go
0x33	R51		Go
0x34	R52		Go
0x35	R53		Go
0x36	R54		Go
0x37	R55		Go
0x38	R56		Go
0x39	R57		Go
0x3A	R58		Go
0x3B	R59		Go
0x3C	R60		Go
0x3D	R61		Go
0x3E	R62		Go
0x3F	R63		Go
0x40	R64		Go
0x41	R65		Go
0x42	R66		Go
0x43	R67		Go
0x44	R68		Go
0x45	R69		Go
0x46	R70		Go
0x47	R71		Go
0x48	R72		Go
0x49	R73		Go
0x4A	R74		Go
0x4B	R75		Go
0x4C	R76		Go
0x4D	R77		Go
0x4E	R78		Go
0x4F	R79		Go
0x50	R80		Go
0x51	R81		Go
0x52	R82		Go
0x53	R83		Go
0x54	R84		Go
0x55	R85		Go
0x56	R86		Go
0x57	R87		Go
0x58	R88		Go
0x59	R89		Go

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Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x5A	R90		Go
0x5B	R91		Go
0x5C	R92		Go
0x5D	R93		Go
0x5E	R94		Go
0x5F	R95		Go
0x60	R96		Go
0x61	R97		Go
0x62	R98		Go
0x63	R99		Go
0x64	R100		Go
0x65	R101		Go
0x66	R102		Go
0x67	R103		Go
0x68	R104		Go
0x69	R105		Go
0x6A	R106		Go
0x6B	R107		Go
0x6C	R108		Go
0x6D	R109		Go
0x6E	R110		Go
0x6F	R111		Go
0x70	R112		Go
0x71	R113		Go
0x72	R114		Go
0x73	R115		Go
0x74	R116		Go
0x75	R117		Go
0x76	R118		Go
0x77	R119		Go
0x78	R120		Go
0x79	R121		Go
0x7A	R122		Go

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1.1 R0 Register (Offset = 0x0) [reset = 0x4070]

R0 is shown in Table 1-3.

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Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0x1	Program 0x1 to this field.
13	INSTCAL_SKIP_ACAL	R/W	0x0	Disable this bit when doing instant calibration. When not using instant calibration, it is recommended to enable it for faster VCO Calibration.
12-11	RESERVED	R/W	0x0	Program 0x0 to this field.
10-9	FCAL_HPFD_ADJ	R/W	0x0	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0x0 = $f_{PD} \leq 100$ MHz 0x1 = 100 MHz < $f_{PD} \leq 150$ MHz 0x2 = 150 MHz < $f_{PD} \leq 200$ MHz 0x3 = $f_{PD} > 200$ MHz
8-7	FCAL_LPFD_ADJ	R/W	0x0	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0x0 = $f_{PD} \geq 10$ MHz 0x1 = 10 MHz > $f_{PD} \geq 5$ MHz 0x2 = 5 MHz > $f_{PD} \geq 2.5$ MHz 0x3 = $f_{PD} < 2.5$ MHz
6	DBLR_CAL_EN	R/W	0x1	Enables VCO doubler calibration. 0x0 = Disabled 0x1 = Enabled
5	RESERVED	R/W	0x1	Program 0x1 to this field.
4	FCAL_EN	R/W	0x1	Enables and activates VCO calibration. Writing register R0 with this bit set to a 1 enables and triggers VCO calibration. 0x0 = Disabled 0x1 = Enabled
3-2	RESERVED	R/W	0x0	Program 0x0 to this field.
1	RESET	R/W	0x0	Resets all registers to silicon default values. This bit is self-clearing. 0x0 = Normal operation 0x1 = Reset
0	POWERDOWN	R/W	0x0	Powers down the device. 0x0 = Normal operation 0x1 = Power down

1.2 R1 Register (Offset = 0x1) [reset = 0x57A0]

R1 is shown in Table 1-4.

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Table 1-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PHASE_SYNC_EN	R/W	0x0	Enables phase synchronization. A Low-High-Low pulse is required at the PSYNC pin to trigger synchronization.Enable SYSREF requires PHASE_SYNC_EN = 1. 0x0 = Normal operation 0x1 = Phase synchronization enabled
14-6	RESERVED	R/W	0x15E	Program 0x15E to this field.
5	LD_VTUNE_EN	R/W	0x1	Selects lock detect type. VCOCal lock detect asserts a HIGH output after the VCO has finished calibration and the LD_DLY timeout counter is finished. VCOCal and Vtune lock detect asserts a HIGH output when VCOCal lock detect would assert a signal and the tuning voltage to the VCO is within acceptable limits. 0x0 = VCOCal lock detect 0x1 = VCOCal and Vtune lock detect
4-2	RESERVED	R/W	0x0	Program 0x0 to this field.
1	INSTCAL_DBLR_EN	R/W	0x0	Sets this bit to 1 if VCO doubler is engaged. 0x0 = Normal operation 0x1 = VCO doubler is engaged
0	INSTCAL_EN	R/W	0x0	Enables instant calibration. 0x0 = Disabled 0x1 = Enabled

1.3 R2 Register (Offset = 0x2) [reset = 0xB3E8]

R2 is shown in Table 1-5.

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Table 1-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x1	Program 0x1 to this field.
14-12	CAL_CLK_DIV	R/W	0x3	Divides down the state machine clock (fsm) during VCO calibration. Maximum fsm is 200 MHz. fsm = f_{OSCIN} / ($2^{CAL_CLK_DIV}$). 0x0 = f_{OSCIN} ≤ 200 MHz 0x1 = f_{OSCIN} ≤ 400 MHz 0x2 = f_{OSCIN} ≤ 800 MHz 0x3 = All other f_{OSCIN} values All other values are reserved
11-1	INSTCAL_DLY	R/W	0x1F4	Sets the wait time for instant calibration. INSTCAL_DLY = T x f_{OSCIN} / ($2^{CAL_CLK_DIV}$). T = 2.5 x $C_{BIASVCO}$ / 4.7 µF. $C_{BIASVCO}$ is the bypass capacitor at pin 3.
0	QUICK_RECAL_EN	R/W	0x0	Starts VCO calibration with the current VCO_SEL, VCO_CAPCTRL and VCO_DACISET values. 0x0 = Disabled 0x1 = Enabled

1.4 R3 Register (Offset = 0x3) [reset = 0x41]

R3 is shown in Table 1-6.

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Table 1-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x41	Program 0x41 to this field.

1.5 R4 Register (Offset = 0x4) [reset = 0x4204]

R4 is shown in Table 1-7.

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Table 1-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x4204	Program 0x4204 to this field.

1.6 R5 Register (Offset = 0x5) [reset = 0x3832]

R5 is shown in Table 1-8.

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Table 1-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x3832	Program 0x32 to this field.

1.7 R6 Register (Offset = 0x6) [reset = 0xA43]

R6 is shown in Table 1-9.

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Table 1-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	ACAL_CMP_DLY	R/W	0xA	VCO amplitude calibration delay. Lowering this value can speed up calibration time. If too low, phase noise may not be optimal due to insufficient time to reach final calibrated amplitude. Delay time = ACAL_CMP_DLY x 2 x state machine clock cycle.
7-0	RESERVED	R/W	0x43	Program 0x43 to this field.

1.8 R7 Register (Offset = 0x7) [reset = 0xC8]

R7 is shown in Table 1-10.

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Table 1-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xC8	Program 0x0 to this field.

1.9 R8 Register (Offset = 0x8) [reset = 0xC802]

R8 is shown in Table 1-11.

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Table 1-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xC802	Program 0xC802 to this field.

1.10 R9 Register (Offset = 0x9) [reset = 0x5]

R9 is shown in Table 1-12.

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Table 1-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x5	Program 0x5 to this field.

1.11 R10 Register (Offset = 0xA) [reset = 0x0]

R10 is shown in Table 1-13.

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Table 1-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0x0	Program 0x0 to this field.
12	PFD_DLY_MANUAL	R/W	0x0	Enables manual PFD_DLY adjustment. 0x0 = Disabled 0x1 = Enabled
11	VCO_DACISET_FORCE	R/W	0x0	Forces the VCO to use the current setting specified by VCO_DACISET. Useful for full-assisted VCO calibration and debugging purposes. 0x0 = Disabled 0x1 = Enabled
10-8	RESERVED	R/W	0x0	Program 0x0 to this field.
7	VCO_CAPCTRL_FORCE	R/W	0x0	Forces the VCO to use the sub-band specified by VCO_CAPCTRL. Useful for full-assisted VCO calibration and debugging purposes. 0x0 = Disabled 0x1 = Enabled
6-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.12 R11 Register (Offset = 0xB) [reset = 0x603]

R11 is shown in Table 1-14.

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Table 1-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0x30	Program 0x30 to this field.
4	OSC_2X	R/W	0x0	Enables reference input doubler. 0x0 = Disabled 0x1 = Enabled
3-0	RESERVED	R/W	0x3	Program 0x2 to this field.

1.13 R12 Register (Offset = 0xC) [reset = 0x408]

R12 is shown in Table 1-15.

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Table 1-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0x0	Program 0x0 to this field.

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Table 1-15. R12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	MULT	R/W	0x1	Sets reference path frequency multiplier value. 0x1 = Bypassed 0x3 = x3 0x4 = x4 0x5 = x5 0x6 = x6 0x7 = x7 All other values are reserved
9-0	RESERVED	R/W	0x8	Program 0x8 to this field.

1.14 R13 Register (Offset = 0xD) [reset = 0x38]

R13 is shown in Table 1-16.

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Table 1-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0x0	Program 0x0 to this field.
12-5	PLL_R	R/W	0x1	Sets reference path Post-R divider value.
4-0	RESERVED	R/W	0x18	Program 0x18 to this field.

1.15 R14 Register (Offset = 0xE) [reset = 0x3001]

R14 is shown in Table 1-17.

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Table 1-17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x3	Program 0x3 to this field.
11-0	PLL_R_PRE	R/W	0x1	Sets reference path Pre-R divider value.

1.16 R15 Register (Offset = 0xF) [reset = 0x2001]

R15 is shown in Table 1-18.

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Table 1-18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x2	Program 0x2 to this field.
11	PFD_POL	R/W	0x0	Sets the polarity of phase detector. Internal VCO operation requires negative Vtune with non-inverting loop filter. 0x0 = Negative Vtune 0x1 = Positive Vtune
10-9	PFD_SINGLE	R/W	0x0	Uses single PFD when PFDIN input is enabled. The actual charge pump current is equal to half the current setting made in CPG. 0x0 = Normal operation 0x1 = Not used 0x2 = Not used 0x3 = Single PFD

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Table 1-18. R15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	RESERVED	R/W	0x1	Program 0x1 to this field.

1.17 R16 Register (Offset = 0x10) [reset = 0x271C]

R16 is shown in Table 1-19.

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Table 1-19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0x138	Program 0xB8 to this field.
4-1	CPG	R/W	0xE	Sets charge pump gain value. 0x0 = Tri-state 0x1 = 1.4 mA 0x4 = 5.6 mA 0x5 = 7 mA 0x6 = 11.2 mA 0x7 = 12.6 mA 0x8 = 2.8 mA 0x9 = 4.2 mA 0x12 = 8.4 mA 0x13 = 9.8 mA 0x14 = 14 mA 0x15 = 15.4 mA All other values are reserved
0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.18 R17 Register (Offset = 0x11) [reset = 0x1440]

R17 is shown in Table 1-20.

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Table 1-20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	RESERVED	R/W	0x0	Program 0x0 to this field.
6	LD_TYPE	R/W	0x1	Defines lock detect monitor type. One-Shot detects lock only after the VCO calibrates and the LD_DLY timeout counter is finished. Continuous lock detect checks for lock all the time, including when the input reference is removed. 0x0 = One-Shot 0x1 = Continuous
15-7	RESERVED	R/W	0x28	Program 0x2B to this field.

1.19 R18 Register (Offset = 0x12) [reset = 0x3E8]

R18 is shown in Table 1-21.

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Table 1-21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LD_DLY	R/W	0x3E8	Lock detect assertion delay. This is the delay that is added after the VCO calibration is completed before indicating lock. This delay is only applied if LD_VTUNE_EN = 1. Delay time = LD_DLY / f_{PD}.

1.20 R19 Register (Offset = 0x13) [reset = 0x2120]

R19 is shown in Table 1-22.

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Table 1-22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0x109	Program 0x109 to this field.
4-3	TEMPSENSE_EN	R/W	0x0	Enables temperature sensor. 0x0 = Disabled 0x1 = Reserved 0x2 = Reserved 0x3 = Enabled
2-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.21 R20 Register (Offset = 0x14) [reset = 0x272C]

R20 is shown in Table 1-23.

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Table 1-23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0x13	Program 0x13 to this field.
8-0	VCO_DACISET	R/W	0x12C	User specified start VCO current setting for calibration. Unless QUICK_RECAL_EN = 1, VCO calibration will always start with the VCO current setting that is specified in this field.

1.22 R21 Register (Offset = 0x15) [reset = 0x1C64]

R21 is shown in Table 1-24.

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Table 1-24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1C64	Program 0x1C64 to this field.

1.23 R22 Register (Offset = 0x16) [reset = 0xE2BF]

R22 is shown in Table 1-25.

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Table 1-25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	VCO_SEL	R/W	0x7	User specified start VCO core for calibration. Unless QUICK_RECAL_EN = 1, VCO calibration will always start with the VCO core that is specified in this field. 0x0 = Reserved 0x1 = VCO1 0x2 = VCO2 ... 0x6 = VCO6 0x7 = VCO7
12-8	RESERVED	R/W	0x2	Program 0x2 to this field.
7-0	VCO_CAPCTRL	R/W	0xBF	User specified start VCO sub-band for calibration. Valid values are 191 to 0, where the higher number represents a lower frequency band. Unless QUICK_RECAL_EN = 1, VCO calibration will always start with the VCO sub-band that is specified in this field.

1.24 R23 Register (Offset = 0x17) [reset = 0x1102]

R23 is shown in Table 1-26.

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Table 1-26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0x881	Program 0x881 to this field.
0	VCO_SEL_FORCE	R/W	0x0	Forces the VCO to use the core specified by VCO_SEL. Useful for full-assisted VCO calibration and debugging purposes. 0x0 = Disabled 0x1 = Enabled

1.25 R24 Register (Offset = 0x18) [reset = 0xE34]

R24 is shown in Table 1-27.

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Table 1-27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xE34	Program 0xE34 to this field.

1.26 R25 Register (Offset = 0x19) [reset = 0x624]

R25 is shown in Table 1-28.

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Table 1-28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x624	Program 0x624 to this field.

1.27 R26 Register (Offset = 0x1A) [reset = 0xDB0]

R26 is shown in Table 1-29.

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Table 1-29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xDB0	Program 0xDB0 to this field.

1.28 R27 Register (Offset = 0x1B) [reset = 0x8001]

R27 is shown in Table 1-30.

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Table 1-30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x8001	Program 0x8001 to this field.

1.29 R28 Register (Offset = 0x1C) [reset = 0x639]

R28 is shown in Table 1-31.

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Table 1-31. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x639	Program 0x639 to this field.

1.30 R29 Register (Offset = 0x1D) [reset = 0x318C]

R29 is shown in Table 1-32.

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Table 1-32. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x318C	Program 0x318C to this field.

1.31 R30 Register (Offset = 0x1E) [reset = 0xB18C]

R30 is shown in Table 1-33.

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Table 1-33. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xB18C	Program 0xB18C to this field.

1.32 R31 Register (Offset = 0x1F) [reset = 0x401]

R31 is shown in Table 1-34.

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Table 1-34. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x401	Program 0x401 to this field.

1.33 R32 Register (Offset = 0x20) [reset = 0x1001]

R32 is shown in Table 1-35.

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Table 1-35. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x1	Program 0x1 to this field.

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Table 1-35. R32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	CHDIVB	R/W	0x0	Sets divider value for RFOUTB. 0x0 = Divide by 2 0x1 = Divide by 4 0x2 = Divide by 8 0x3 = Divide by 16 0x4 = Divide by 32 0x5 = Divide by 64 0x6 = Divide by 128 0x7 = Reserved
8-6	CHDIVA	R/W	0x0	Sets divider value for RFOUTA. 0x0 = Divide by 2 0x1 = Divide by 4 0x2 = Divide by 8 0x3 = Divide by 16 0x4 = Divide by 32 0x5 = Divide by 64 0x6 = Divide by 128 0x7 = Reserved
5-0	RESERVED	R/W	0x1	Program 0x1 to this field.

1.34 R33 Register (Offset = 0x21) [reset = 0x0]

R33 is shown in Table 1-36.

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Table 1-36. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.35 R34 Register (Offset = 0x22) [reset = 0x10]

R34 is shown in Table 1-37.

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Table 1-37. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Program 0x0 to this field.
11	LOOPBACK_EN	R/W	0x0	Enables loop back mode. In this mode, both RFIN input path and internal VCO are active, the synthesizer will try to lock to the internal VCO. EXTVCO_EN must be set to 0 in this mode. 0x0 = Disabled 0x1 = Enabled
10-5	RESERVED	R/W	0x0	Program 0x0 to this field.
4	EXTVCO_DIV	R/W	0x1	Sets external VCO input divider value. 0x0 = Divide by 2 0x1 = Bypassed
3-1	RESERVED	R/W	0x0	Program 0x0 to this field.

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Table 1-37. R34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EXTVCO_EN	R/W	0x0	Enables external VCO mode. Set this bit to 1 will enables RFIN input path but disables internal VCO, the synthesizer will try to lock to an external source appear at RFIN pin. In loop back mode, this bit has to be set to 0, RFIN input path will be enabled by the LOOPBACK_EN bit. 0x0 = Disabled 0x1 = Enabled

1.36 R35 Register (Offset = 0x23) [reset = 0x3100]

R35 is shown in Table 1-38.

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Table 1-38. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0x1	Program 0x1 to this field.
12	MASH_RESET_N	R/W	0x1	Resets the MASH (active LOW). 0x0 = Reset 0x1 = Normal operation
11-9	RESERVED	R/W	0x0	Program 0x0 to this field.
8-7	MASH_ORDER	R/W	0x2	Sets the MASH order. 0x0 = Integer mode 0x1 = First order 0x2 = Second order 0x3 = Third order
6	MASHSEED_EN	R/W	0x0	Enables MASHSEED for phase adjustment. 0x0 = Disabled 0x1 = Enabled
5-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.37 R36 Register (Offset = 0x24) [reset = 0x38]

R36 is shown in Table 1-39.

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Table 1-39. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Program 0x0 to this field.
14-0	PLL_N	R/W	0x38	Sets N divider value (integer portion).

1.38 R37 Register (Offset = 0x25) [reset = 0x500]

R37 is shown in Table 1-40.

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Table 1-40. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Program 0x0 to this field.

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Table 1-40. R37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-9	PFD_DLY	R/W	0x2	Sets N divider delay time in phase detector. Effective only when PFD_DLY_MANUAL = 1. 0x0 = Reserved All other values must be set in accordance to the N divider value
8-0	RESERVED	R/W	0x100	Program 0x100 to this field.

1.39 R38 Register (Offset = 0x26) [reset = 0x0]

R38 is shown in Table 1-41.

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Table 1-41. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN[31:16]	R/W	0x0	Sets the upper 16 bits of fractional denominator (DEN).

1.40 R39 Register (Offset = 0x27) [reset = 0x3E8]

R39 is shown in Table 1-42.

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Table 1-42. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN[15:0]	R/W	0x3E8	Sets the lower 16 bits of fractional denominator (DEN).

1.41 R40 Register (Offset = 0x28) [reset = 0x0]

R40 is shown in Table 1-43.

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Table 1-43. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[31:16]	R/W	0x0	Sets the upper 16 bits of MASH_SEED.

1.42 R41 Register (Offset = 0x29) [reset = 0x0]

R41 is shown in Table 1-44.

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Table 1-44. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[15:0]	R/W	0x0	Sets the lower 16 bits of MASH SEED.

1.43 R42 Register (Offset = 0x2A) [reset = 0x0]

R42 is shown in Table 1-45.

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Table 1-45. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM[31:16]	R/W	0x0	Sets the upper 16 bits of fractional numerator (NUM).

1.44 R43 Register (Offset = 0x2B) [reset = 0x0]

R43 is shown in Table 1-46.

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Table 1-46. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM[15:0]	R/W	0x0	Sets the lower 16 bits of fractional numerator (NUM).

1.45 R44 Register (Offset = 0x2C) [reset = 0x0]

R44 is shown in Table 1-47.

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Table 1-47. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	INSTCAL_PLL_NUM[31:16]	R/W	0x0	Sets the upper 16 bits of INSTCAL_PLL_NUM. INSTCAL_PLL_NUM = 2^{32} x (PLL_NUM / PLL_DEN).

1.46 R45 Register (Offset = 0x2D) [reset = 0x0]

R45 is shown in Table 1-48.

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Table 1-48. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	INSTCAL_PLL_NUM[15:0]	R/W	0x0	Sets the lower 16 bits of INSTCAL_PLL_NUM. INSTCAL_PLL_NUM = 2^{32} x (PLL_NUM / PLL_DEN).

1.47 R46 Register (Offset = 0x2E) [reset = 0x300]

R46 is shown in Table 1-49.

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Table 1-49. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x300	Program 0x300 to this field.

1.48 R47 Register (Offset = 0x2F) [reset = 0x300]

R47 is shown in Table 1-50.

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Table 1-50. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x300	Program 0x300 to this field.

1.49 R48 Register (Offset = 0x30) [reset = 0x4180]

R48 is shown in Table 1-51.

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Table 1-51. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x4180	Program 0x4180 to this field.

1.50 R49 Register (Offset = 0x31) [reset = 0x0]

R49 is shown in Table 1-52.

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Table 1-52. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.51 R50 Register (Offset = 0x32) [reset = 0x80]

R50 is shown in Table 1-53.

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Table 1-53. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x80	Program 0x80 to this field.

1.52 R51 Register (Offset = 0x33) [reset = 0x203F]

R51 is shown in Table 1-54.

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Table 1-54. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x203F	Program 0x203F to this field.

1.53 R52 Register (Offset = 0x34) [reset = 0x0]

R52 is shown in Table 1-55.

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Table 1-55. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.54 R53 Register (Offset = 0x35) [reset = 0x0]

R53 is shown in Table 1-56.

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Table 1-56. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.55 R54 Register (Offset = 0x36) [reset = 0x0]

R54 is shown in Table 1-57.

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Table 1-57. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.56 R55 Register (Offset = 0x37) [reset = 0x2]

R55 is shown in Table 1-58.

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Table 1-58. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x2	Program 0x2 to this field.

1.57 R56 Register (Offset = 0x38) [reset = 0x1]

R56 is shown in Table 1-59.

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Table 1-59. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0x0	Program 0x0 to this field.
5-0	EXTPFD_DIV	R/W	0x1	Sets external PFD input divider value. Set this field to 0 is not allowed. A value of 1 means bypassed.

1.58 R57 Register (Offset = 0x39) [reset = 0x1]

R57 is shown in Table 1-60.

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Table 1-60. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0x0	Program 0x0 to this field.
0	PFD_SEL	R/W	0x1	Enables PFDIN input. When using PFDIN input, the charge pump has to be set to single PFD by setting PFD_SINGLE = 0x3. 0x0 = Enabled 0x1 = Disabled

1.59 R58 Register (Offset = 0x3A) [reset = 0x0]

R58 is shown in Table 1-61.

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Table 1-61. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.60 R59 Register (Offset = 0x3B) [reset = 0x1388]

R59 is shown in Table 1-62.

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Table 1-62. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1388	Program 0x1388 to this field.

1.61 R60 Register (Offset = 0x3C) [reset = 0x1F4]

R60 is shown in Table 1-63.

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Table 1-63. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1F4	Program 0x1F4 to this field.

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1.62 R61 Register (Offset = 0x3D) [reset = 0x3E8]

R61 is shown in Table 1-64.

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Table 1-64. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x3E8	Program 0x3E8 to this field.

1.63 R62 Register (Offset = 0x3E) [reset = 0x0]

R62 is shown in Table 1-65.

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Table 1-65. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[31:16]	R/W	0x0	Sets the upper 16 bits of MASH reset delay. This is the delay that is necessary after the MASH engine is reset during phase synchronization when PLL_NUM is not equal to zero. The delay time must be set to greater than the lock time of the PLL. Delay time = MASH_RST_COUNT x ($2^{CAL_CLK_DIV}$) / f_{OSCIN}. This field can be set to 0 when PLL_NUM = 0.

1.64 R63 Register (Offset = 0x3F) [reset = 0xC350]

R63 is shown in Table 1-66.

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Table 1-66. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[15:0]	R/W	0xC350	Sets the lower 16 bits of MASH reset delay.

1.65 R64 Register (Offset = 0x40) [reset = 0x4080]

R64 is shown in Table 1-67.

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Table 1-67. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0x10	Program 0x10 to this field.
9-8	SYSREF_INP_FMT	R/W	0x0	Sets SRREQ pin input format. 0x0 = CMOS input at SRREQ_P pin, 1.8-V to 3.3-V logic 0x1 = AC-couple CMOS input at SRREQ_P pin 0x2 = AC-coupled differential LVDS input, requires external 100-Ω differential termination 0x3 = DC-coupled differential LVDS input, requires external 100-Ω differential termination
7-5	SYSREF_DIV_PRE	R/W	0x4	This divider is used to get the frequency input to SYSREF_DIV within acceptable limits. 0x1 = Divide by 2 0x2 = Divide by 4 0x4 = Divide by 8 All other values are reserved

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Table 1-67. R64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SYSREF_REPEAT_NS	R/W	0x0	Enables asynchronous SYSREF repeater mode. In this mode, the SYSREF signal coming from the SRREQ pin will be passed through to the SROUT pin without reclocking. 0x0 = If SYSREF_REPEAT = 1 0x1 = Enabled
3	SYSREF_PULSE	R/W	0x0	Defines SYSREF master mode. In continuous mode, SYSREF pulses are generated continuously. Pulsed mode allows multiple pulses (as determined by SYSREF_PULSE_CNT) to be sent out whenever the SRREQ pins go HIGH. 0x0 = Continuous mode 0x1 = Pulsed mode
2	SYSREF_EN	R/W	0x0	Enables SYSREF mode. 0x0 = Disabled 0x1 = Enabled
1	SYSREF_REPEAT	R/W	0x0	Defines SYSREF mode. In master mode, SYSREF pulses are generated internally. In repeater mode, SYSREF pulses are generated in response to the SRREQ pins. 0x0 = Master mode 0x1 = Repeater mode
0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.66 R65 Register (Offset = 0x41) [reset = 0x1]

R65 is shown in Table 1-68.

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Table 1-68. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	0x0	Program 0x0 to this field.
10-0	SYSREF_DIV	R/W	0x1	This divider further divides the output frequency for the SYSREF.

1.67 R66 Register (Offset = 0x42) [reset = 0x3F]

R66 is shown in Table 1-69.

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Table 1-69. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Program 0x0 to this field.
11-6	JESD_DAC2_CTRL	R/W	0x0	Programmable delay adjustment for SYSREF mode.
5-0	JESD_DAC1_CTRL	R/W	0x3F	Programmable delay adjustment for SYSREF mode.

1.68 R67 Register (Offset = 0x43) [reset = 0x0]

R67 is shown in Table 1-70.

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Table 1-70. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SYSREF_PULSE_CNT	R/W	0x0	Defines how many pulses are sent in SYSREF pulsed mode.

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Table 1-70. R67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	JESD_DAC4_CTRL	R/W	0x0	Programmable delay adjustment for SYSREF mode.
5-0	JESD_DAC3_CTRL	R/W	0x0	Programmable delay adjustment for SYSREF mode.

1.69 R68 Register (Offset = 0x44) [reset = 0x0]

R68 is shown in Table 1-71.

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Table 1-71. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0x0	Program 0x0 to this field.
5	INPIN_IGNORE	R/W	0x0	Disables PSYNC pin. Keep this bit equals 1 unless phase sync is required. 0x0 = Enables pin 0x1 = Disables pin
4-1	RESERVED	R/W	0x0	Program 0x0 to this field.
0	PSYNC_INP_FMT	R/W	0x0	Sets PSYNC pin input format. 0x0 = CMOS input, 1.8-V to 3.3-V logic 0x1 = AC-coupled differential LVDS input, requires external 100-Ω differential termination

1.70 R69 Register (Offset = 0x45) [reset = 0x11]

R69 is shown in Table 1-72.

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Table 1-72. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0x0	Program 0x0 to this field.
4	SROUT_PD	R/W	0x1	Powerdowns SYSREF output buffer. 0x0 = Normal operation 0x1 = Power down
3-0	RESERVED	R/W	0x1	Program 0x1 to this field.

1.71 R70 Register (Offset = 0x46) [reset = 0x1E]

R70 is shown in Table 1-73.

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Table 1-73. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0x0	Program 0x0 to this field.
7	DBLBUF_OUTMUX_EN	R/W	0x0	Enables double buffering for OUTA_MUX and OUTB_MUX. Changes of these registers will only be effective after R0 is programmed. 0x0 = Disabled 0x1 = Enabled

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Table 1-73. R70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DBLBUF_OUTBUF_EN	R/W	0x0	Enables double buffering for OUTA_PD and OUTB_PD. Changes of these registers will only be effective after R0 is programmed. 0x0 = Disabled 0x1 = Enabled
5	DBLBUF_CHDIV_EN	R/W	0x0	Enables double buffering for CHDIVA and CHDIVB. Changes of these registers will only be effective after R0 is programmed. 0x0 = Disabled 0x1 = Enabled
4	DBLBUF_PLL_EN	R/W	0x1	Enables double buffering for PLL_N, PLL_NUM, PLL_DEN, MULT, PLL_R, PLL_R_PRE, MASH_ORDER and PFD_DLY. Changes of these registers will only be effective after R0 is programmed. 0x0 = Disabled 0x1 = Enabled
3-0	RESERVED	R/W	0xE	Program 0xE to this field.

1.72 R71 Register (Offset = 0x47) [reset = 0x0]

R71 is shown in Table 1-74.

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Table 1-74. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.73 R72 Register (Offset = 0x48) [reset = 0x0]

R72 is shown in Table 1-75.

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Table 1-75. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.74 R73 Register (Offset = 0x49) [reset = 0x0]

R73 is shown in Table 1-76.

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Table 1-76. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.75 R74 Register (Offset = 0x4A) [reset = 0x0]

R74 is shown in Table 1-77.

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Table 1-77. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	rb_LD	R	0x0	Reads back lock detect status. 0x0 = Unlocked 0x1 = Unlocked 0x2 = Locked 0x3 = Invalid
13	RESERVED	R	0x0	Not used. Read back only.
12-5	rb_VCO_CAPCTRL	R	0x0	Reads back the actual CAPCTRL value that the VCO calibration has chosen.
4-2	rb_VCO_SEL	R	0x0	Reads back the actual VCO that the VCO calibration has selected. 0x0 = Invalid 0x1 = VCO1 0x2 = VCO2 ... 0x6 = VCO6 0x7 = VCO7
1-0	RESERVED	R	0x0	Not used. Read back only.

1.76 R75 Register (Offset = 0x4B) [reset = 0x0]

R75 is shown in Table 1-78.

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Table 1-78. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Not used. Read back only.
8-0	rb_VCO_DACISET	R	0x0	Reads back the actual DACISET value that the VCO calibration has chosen.

1.77 R76 Register (Offset = 0x4C) [reset = 0x0]

R76 is shown in Table 1-79.

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Table 1-79. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Not used. Read back only.
10-0	rb_TEMP_SENS	R	0x0	Reads back temperature sensor code. Temperature in °C = 0.85 x code - 415. Resolution is 0.6°C per code. Measurement accuracy is ±5 degrees.

1.78 R77 Register (Offset = 0x4D) [reset = 0x56CC]

R77 is shown in Table 1-80.

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Table 1-80. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0x2B	Program 0x3 to this field.
8	PINMUTE_POL	R/W	0x0	Sets the polarity of mute control for MUTE pin. 0x0 = Active HIGH 0x1 = Active LOW

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Table 1-80. R77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0xCC	Program 0x8 to this field.

1.79 R78 Register (Offset = 0x4E) [reset = 0x1]

R78 is shown in Table 1-81.

Return to Summary Table.

Table 1-81. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0x0	Program 0x0 to this field.
4	OUTA_PD	R/W	0x0	Power downs RFOUTA. 0x0 = Normal operation 0x1 = Power down
3-2	RESERVED	R/W	0x0	Program 0x0 to this field.
1-0	OUTA_MUX	R/W	0x1	Selects the input source to RFOUTA. 0x0 = Channel divider 0x1 = VCO 0x2 = VCO doubler 0x3 = Reserved

1.80 R79 Register (Offset = 0x4F) [reset = 0x11E]

R79 is shown in Table 1-82.

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Table 1-82. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0x0	Program 0x0 to this field.
8	OUTB_PD	R/W	0x1	Power downs RFOUTB. 0x0 = Normal operation 0x1 = Power down
7-6	RESERVED	R/W	0x0	Program 0x0 to this field.
5-4	OUTB_MUX	R/W	0x1	Selects the input source to RFOUTB. 0x0 = Channel divider 0x1 = VCO 0x2 = VCO doubler 0x3 = Reserved
3-1	OUTA_PWR	R/W	0x7	Adjusts RFOUTA output power. Higher numbers give more output power.
0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.81 R80 Register (Offset = 0x50) [reset = 0x1C0]

R80 is shown in Table 1-83.

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Table 1-83. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0x0	Program 0x0 to this field.

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Table 1-83. R80 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-6	OUTB_PWR	R/W	0x7	Adjusts RFOUTB output power. Higher numbers give more output power.
5-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.82 R81 Register (Offset = 0x51) [reset = 0x0]

R81 is shown in Table 1-84.

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Table 1-84. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.83 R82 Register (Offset = 0x52) [reset = 0x0]

R82 is shown in Table 1-85.

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Table 1-85. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.84 R83 Register (Offset = 0x53) [reset = 0xF00]

R83 is shown in Table 1-86.

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Table 1-86. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xF00	Program 0xF00 to this field.

1.85 R84 Register (Offset = 0x54) [reset = 0x40]

R84 is shown in Table 1-87.

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Table 1-87. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x40	Program 0x40 to this field.

1.86 R85 Register (Offset = 0x55) [reset = 0x0]

R85 is shown in Table 1-88.

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Table 1-88. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.87 R86 Register (Offset = 0x56) [reset = 0x40]

R86 is shown in Table 1-89.

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Table 1-89. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x40	Program 0x40 to this field.

1.88 R87 Register (Offset = 0x57) [reset = 0xFF00]

R87 is shown in Table 1-90.

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Table 1-90. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xFF00	Program 0xFF00 to this field.

1.89 R88 Register (Offset = 0x58) [reset = 0x3FF]

R88 is shown in Table 1-91.

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Table 1-91. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x3FF	Program 0x3FF to this field.

1.90 R89 Register (Offset = 0x59) [reset = 0x0]

R89 is shown in Table 1-92.

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Table 1-92. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.91 R90 Register (Offset = 0x5A) [reset = 0x0]

R90 is shown in Table 1-93.

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Table 1-93. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.92 R91 Register (Offset = 0x5B) [reset = 0x0]

R91 is shown in Table 1-94.

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Table 1-94. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.93 R92 Register (Offset = 0x5C) [reset = 0x0]

R92 is shown in Table 1-95.

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Table 1-95. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.94 R93 Register (Offset = 0x5D) [reset = 0x1000]

R93 is shown in Table 1-96.

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Table 1-96. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1000	Program 0x1000 to this field.

1.95 R94 Register (Offset = 0x5E) [reset = 0x0]

R94 is shown in Table 1-97.

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Table 1-97. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.96 R95 Register (Offset = 0x5F) [reset = 0x0]

R95 is shown in Table 1-98.

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Table 1-98. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.97 R96 Register (Offset = 0x60) [reset = 0x17F8]

R96 is shown in Table 1-99.

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Table 1-99. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x17F8	Program 0x17F8 to this field.

1.98 R97 Register (Offset = 0x61) [reset = 0x0]

R97 is shown in Table 1-100.

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Table 1-100. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.99 R98 Register (Offset = 0x62) [reset = 0x1C80]

R98 is shown in Table 1-101.

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Table 1-101. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1C80	Program 0x1C80 to this field.

1.100 R99 Register (Offset = 0x63) [reset = 0x19B9]

R99 is shown in Table 1-102.

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Table 1-102. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x19B9	Program 0x19B9 to this field.

1.101 R100 Register (Offset = 0x64) [reset = 0x533]

R100 is shown in Table 1-103.

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Table 1-103. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x533	Program 0x533 to this field.

1.102 R101 Register (Offset = 0x65) [reset = 0x3E8]

R101 is shown in Table 1-104.

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Table 1-104. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x3E8	Program 0x3E8 to this field.

1.103 R102 Register (Offset = 0x66) [reset = 0x28]

R102 is shown in Table 1-105.

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Table 1-105. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x28	Program 0x28 to this field.

1.104 R103 Register (Offset = 0x67) [reset = 0x14]

R103 is shown in Table 1-106.

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Table 1-106. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x14	Program 0x14 to this field.

1.105 R104 Register (Offset = 0x68) [reset = 0x14]

R104 is shown in Table 1-107.

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Table 1-107. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x14	Program 0x14 to this field.

1.106 R105 Register (Offset = 0x69) [reset = 0xA]

R105 is shown in Table 1-108.

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Table 1-108. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xA	Program 0xA to this field.

1.107 R106 Register (Offset = 0x6A) [reset = 0x0]

R106 is shown in Table 1-109.

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Table 1-109. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.108 R107 Register (Offset = 0x6B) [reset = 0x0]

R107 is shown in Table 1-110.

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Table 1-110. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.109 R108 Register (Offset = 0x6C) [reset = 0x0]

R108 is shown in Table 1-111.

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Table 1-111. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.110 R109 Register (Offset = 0x6D) [reset = 0x0]

R109 is shown in Table 1-112.

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Table 1-112. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.111 R110 Register (Offset = 0x6E) [reset = 0x1F]

R110 is shown in Table 1-113.

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Table 1-113. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x1F	Program 0x1F to this field.

1.112 R111 Register (Offset = 0x6F) [reset = 0x0]

R111 is shown in Table 1-114.

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Table 1-114. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0x0	Program 0x0 to this field.

1.113 R112 Register (Offset = 0x70) [reset = 0xFFFF]

R112 is shown in Table 1-115.

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Table 1-115. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	0xFFFF	Program 0xFFFF to this field.

1.114 R113 Register (Offset = 0x71) [reset = 0x0]

R113 is shown in Table 1-116.

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Table 1-116. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.115 R114 Register (Offset = 0x72) [reset = 0x0]

R114 is shown in Table 1-117.

Return to Summary Table.

Table 1-117. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.116 R115 Register (Offset = 0x73) [reset = 0x0]

R115 is shown in Table 1-118.

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Table 1-118. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.117 R116 Register (Offset = 0x74) [reset = 0x0]

R116 is shown in Table 1-119.

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Table 1-119. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.118 R117 Register (Offset = 0x75) [reset = 0x0]

R117 is shown in Table 1-120.

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Table 1-120. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.119 R118 Register (Offset = 0x76) [reset = 0x0]

R118 is shown in Table 1-121.

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Table 1-121. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.120 R119 Register (Offset = 0x77) [reset = 0x0]

R119 is shown in Table 1-122.

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Table 1-122. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.121 R120 Register (Offset = 0x78) [reset = 0x0]

R120 is shown in Table 1-123.

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Table 1-123. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.122 R121 Register (Offset = 0x79) [reset = 0x0]

R121 is shown in Table 1-124.

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Table 1-124. R121 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

1.123 R122 Register (Offset = 0x7A) [reset = 0x0]

R122 is shown in Table 1-125.

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Table 1-125. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Not used. Read back only.

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (December 2020) **Page**

- INSTCAL_SKIP_ACAL is added in R0 7
- Description of PHASE_SYNC_EN is changed. R1[5] field name is changed to LD_VTUNE_EN 7
- Description of INSTCAL_DLY is changed 8
- R5 reset value is changed 9
- Removed LD_DLY in R7 9
- Changed the description of PFD_POL in R15 11
- The description of CPG and R16[15:5] are changed 12
- Added LD_TYPE in R17 12
- Added LD_DLY in R18 12
- R20 reset value is changed 13
- Added LOOPBACK_EN. The bit position of EXTVCO_DIV is changed. Description of EXTVCO_EN is changed 16
- Added MASH_RESET_N in R35 17
- R36 reset value is changed 17
- R37 reset value is changed 17
- R38 reset value is changed 18
- R39 reset value is changed 18
- R55 reset value is changed 20
- Description of PFD_SEL is changed 21
- Added MASH_RST_COUNT in R62 22
- Added MASH_RST_COUNT in R63 22
- Added SYSREF_INP_FMT and SYSREF_REPEAT_NS in R64 22
- Added INPIN_IGNORE and PSYNC_INP_FMT in R68 24
- Added DBLBUF_OUTMUX_EN, DBLBUF_OUTBUF_EN, DBLBUF_CHDIV_EN in R70. Field name of R70[4] is changed 24
- Description of rb_TEMP_SENS is changed 26
- Description of R77[7:0] is changed 26
- R96 reset value is changed 30
- R99 reset value is changed 31

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