EVM User's Guide: LMK3H2104EVM

LMK3H2104 Evaluation Module

Description

The LMK3H2104 Evaluation Module (LMK3H2104EVM) provides a complete clocking platform to evaluate the clock performance, pin configuration, software configuration, and features of the Texas Instruments LMK3H2104 Clock Generator with integrated BAW-based oscillator. The LMK3H2104 is a four-output clock generator with an integrated BAW resonator and fractional output dividers, eliminating the need for an external reference clock. The LMK3H2104 accepts up to one input clock, functioning as a buffer with divers, or as an I2C clock multiplexer. The EVM includes SMA connectors for all clock outputs for interfacing with 50Ω test equipment. The EVM can be configured through the onboard USB microcontroller (USB2ANY) using a PC with TI's TICS Pro 2 software. TICS Pro 2 can be used to program the LMK3H2104 registers for live configurations. The LMK3H2104 device has a preprogrammed startup configuration that cannot be overwritten.

Features

- PCIe Gen 1 to Gen 7 compliant clock generator
- External and USB power supply options
- Programmability through TICS Pro 2 software graphical user interface (GUI)
- On-board control of device GPIO pins.

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator

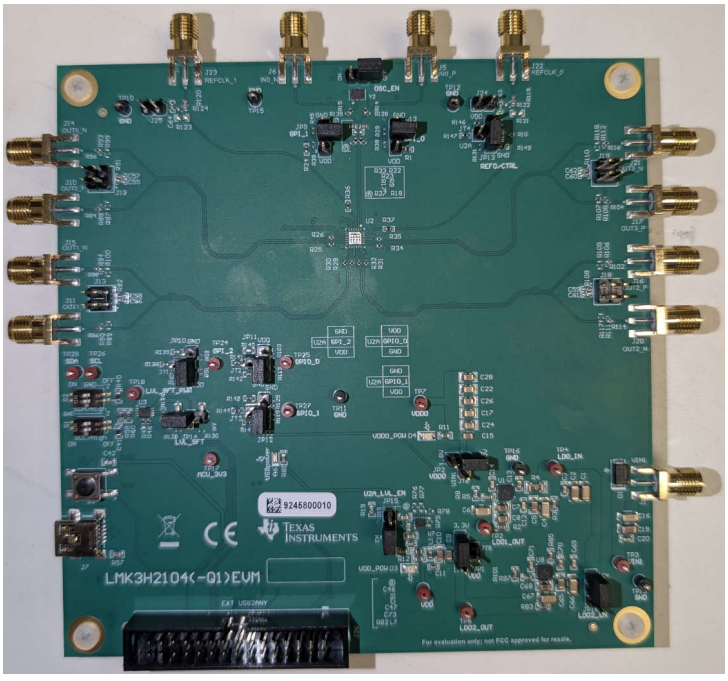


Figure 1-1. LMK3H2104 EVM Default Settings

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (USB2ANY) interface using a PC with TI's TICS Pro 2 Software GUI. TICS Pro 2 can also be used to import / export register data for flexible programming of the device. The input and outputs of the LMK3H2104 can be interfaced with external systems for evaluating compatibility and performance through coaxial cables. On-board LDOs provide an option for using the USB power supply to minimize the amount of external test equipment required.

1.2 Kit Contents

The LMK3H2104EVM box contains:

- One LMK3H2104EVM board (DC321B)
- 3-ft mini-USB cable (MPN 3021003-03)

1.3 Specification

Some of the key specifications for the LMK3H2104 device and EVM are noted in the table below.

Table 1-1. LMK3H2104 Key Parameters

Parameter	Value
Ambient Temperature	-40°C to 105°C
Power Supply	1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10%
Operating Frequency	LVCMOS: DC to 200MHz (38.15Hz to 200MHz from BAW)
	Differential: 2.5MHz to 400MHz
Output Format	LVCMOS, LP-HCSL, LVDS

1.4 Device Information

The LMK3H2104 is a high-performance PCIe compliant clock generator that supports PCIe Gen 1 to Gen 6. The LMK3H2104 can generate any frequency between 2.5MHz and 400MHz differential or any frequency up to 200MHz single-ended. The LMK3H2104 has fail-safe input pins, a flexible power-up sequence, individually controllable outputs through headers or USB2ANY control, and an I2C interface for configuration. The EVM has integrated LDOs for excellent power supply noise suppression with an operating supply voltage of 1.8V, 2.5V, or 3.3V.

2 Hardware

2.1 EVM Quick Start

Table 2-1 describes the default jumper configuration for the EVM to power the device from a USB supply using an on-board LDO. Configure the EVM as specified in the table for initial bring up.

Table 2-1. Jumper and Switch Configuration for Typical Operation

Category	Reference Designator	Position	Description
Power	JP1 + JT5	2 - JT5	All VDD_x driven by on-board 3.3V LDO
	JP2 + JT6	2 - JT6	All VDDO_x driven by on-board 3.3V LDO
	JP16	2-3	On-board 1.8V LDO disabled.
GPI / Input Clock Pins	JP20	1-2	On-board LMK6H oscillator disabled.
	JP8	Disconnected	Connects the GPI_0 pin to VDDD or GND, not connected by default.
	JP9	Disconnected	Connects the GPI_1 pin to VDDD or GND, not connected by default.
	JP10 + JT1	2-JT1	GPI_2 connected to GND.
I^2C Control Pins	JP14	1-2	I2C level shifter enabled.
	S1	No Connection	Close 1-4 to connect SCL/ OTP_SEL0 to VDD/USB2ANY. Close 2-3 to connect SCL/ OTP_SEL0 to GND.
	S2	No Connection	Close 1-4 to connect SDA/ OTP_SEL1 to VDD/USB2ANY. Close 2-3 to connect SDA/ OTP_SEL1 to GND.
GPIO Pins	JP11 + JT2	2-3	GPIO_0 connected to GND.
	JP12 + JT3	2-3	GPIO_1 connected to GND.
	JP13 + JT4	2-3	REF_0/CTRL pin connected to the USB2ANY.

2.1.1 Hardware Setup

Table 2-1 describes the default jumper configuration for the EVM. Be sure to set the jumpers as described for initial power-up using the USB supply.

To begin using the LMK3H2104EVM, follow the steps below.

1. Verify that the jumper configuration matches the default as shown in Figure 1-1 and Table 2-1.
2. Connect the USB cable to the USB port, J19.
3. (Optional) For I2C connection to the TICS Pro 2 GUI, connect pins 1 & 4 on both S1 and S2.

2.1.2 Software Setup

The TICS Pro 2 software allows for simplification of programming device registers. Use the TICS Pro 2 software to:

- View the live device settings,
- View the settings programmed on the four OTP pages, and
- Control the on-board GPIO pins and device registers for automated testing.

2.2 EVM Configuration

The LMK3H2104EVM can be configured for multiple modes using the on-board USB2ANY and either USB power or external supply power. The following sections describe the power, logic, clock input, and clock output interfaces on the EVM, as well as setup and configuration of these modes.

2.2.1 Device Operational Modes

The LMK3H2104 can be configured to start up on one of four OTP pages in OTP mode, or on OTP Page 0 in I^2C mode. If the REF_0/CTRL pin is pulled low at startup, the device loads OTP Page 0 in I^2C mode. If the REF0_CTRL pin is pulled high on startup, the device loads the OTP page selected by the OTP_SEL0 and OTP_SEL1 pins. In OTP mode, the I^2C interface is not available.

An LMK6H device is present on the board for driving IN_P and IN_P from a 100MHz HCSL PCIe-compatible reference. The LMK6H can be enabled or disabled using JP20.

2.2.2 Power Supply

The LMK3H2104 has multiple VDD and VDDO pins that operate from 1.8V ± 10% to 3.3V ± 10%. For both 1.8V and 3.3V operation, the on-board LDOs can be used to control the supply voltage. Alternatively, external power can be supplied through the VIN1 SMA connector. Table 2-2 describes the multiple power supply configurations.

Note

The initial version of the evaluation module (DC321B) is missing a connection between the BIAS pin of the 1.8V LDO (U8) and the 5V USB supply. A wire can be connected between R95 and Pin 1 of JP16 to allow for usage of the 1.8V LDO on this board revision.

Table 2-2. LMK3H2104EVM Power Configurations

Designator	Default Position	Description
JP1 + JT5	1-2	1-2: VDD_A and VDD_D powered by 3.3V LDO 2-3: VDD_A and VDD_D powered by 1.8V LDO 2-3: VDD_A and VDD_D powered by external supply
JP2 + JT6	1-2	1-2: All VDDO_x powered by 3.3V LDO 2-3: All VDDO_x powered by 1.8V LDO 2-3: All VDDO_x powered by external supply
JP16	2-3	1-2: 1.8V LDO is enabled 2-3: 1.8V LDO is disabled

2.2.3 Logic Inputs & Outputs

The General Purpose Input (GPI) and General Purpose Input/Output (GPIO) pins on the LMK3H2104 provide options for output enable / disable control, status signal output, and I^2C device address selection. Table 2-3 describes the default functions of each GPI and GPIO pin.

Table 2-3. LMK3H2104 GPI/GPIO Pin Functionality

Pin Name	OE_GROUP Function	Input Clock Function	Status Output Function
GPI_0	OE_GROUP_0	Pin not used for clock input	Pin not used for status output
GPI_1	OE_GROUP_1	Pin not used for clock input	Pin not used for status output
GPI_2	OE_GROUP_2	N/A	Pin not used for status output
GPIO_0	OE_GROUP_3	N/A	Pin not used for status output
GPIO_1	Pin not used for output enable control	N/A	CLK_READY status signal

Table 2-4 details the configuration options available for each GPI and GPIO pin. The REF_0/CTRL pin serves as an input at startup, determining if the device starts in I2C mode or OTP mode.

Table 2-4. LMK3H2104EVM GPI/GPIO Configurations

Pin Name	Reference Designator	Position	Description
GPI_0 [1]	JP8	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND
GPI_1 [2]	JP9	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND
GPI_2	JP10 + JT1	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND 2-JT1: Controlled by USB2ANY
GPIO_0	JP11 + JT2	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND 2-JT2: Controlled by USB2ANY
GPIO1	JP12 + JT3	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND 2-JT6: Controlled by USB2ANY
REF_0/CTRL	JP13 + JT4	1-2	1-2: Pulled to VDD_D 2-3: Pulled to GND 2-JT6: Controlled by USB2ANY

1. The GPI pins are hardware-configured as clock input pins by default. For using GPI_0, move the R9 resistor to the R18 footprint.
2. The GPI pins are hardware-configured as clock input pins by default. For using GPI_1, move the R17 resistor to the R27 footprint.

2.2.4 Configuring the Clock Outputs

The clock output pairs of the LMK3H2104 are routed via 50Ω single-ended traces to SMA ports (OUT[3:0]_P/OUT[3:0]_N, REF_0/CTRL, & REF_1). These outputs have series resistor (0Ω populated) options. The default output configuration for the LMK3H2104EVM is DC-coupled LP-HCSL for all differential outputs, with no LVCMOS outputs on REF_0/CTRL and REF_1. Each of the differential outputs can be configured for AC-LVDS, DC-LVDS, LP-HCSL, and LVCMOS output formats.

For 1.2V LVCMOS outputs, the logic high level is set by setting the OUTx_CMOS_1P2V_EN bit of the output channel to a '1'. When this bit is a 0, the logic high level of LVCMOS outputs is determined by the voltage on the VDDO supply for the output.

2.2.5 Using the USB Interface Connection

The on-board MSP430F5529 USB microcontroller (U6) provides an I2C host interface to the LMK3H2104 peripheral device. The device registers can be controlled via USB using the TICS Pro 2 software running on a host PC. J22 can be used with an external USB2ANY as an alternative to using the on-board USB2ANY.

If the USB2ANY firmware needs to be updated, the S3 button serves as the BSL connection. Press the S3 button to mimic pressing the BSL button of an external USB2ANY. Release the button after updating the firmware.

3 Software

3.1 Software Installation

The TICS Pro 2 software allows for simplification of programming device registers. The TICS Pro 2 software is available here. Note that the TICS Pro version 1.x software available on TI.com is **not** compatible with the LMK3H2104EVM.

3.2 Using TICS Pro 2 with the LMK3H2104EVM

The TICS Pro 2 profile for the LMK3H2104 can be accessed by performing the following steps:

1. Open the TICS Pro 2 software
2. Navigate to Select Device > Reference-less Clock Generators > LMK3H2104

3.2.1 Global Settings

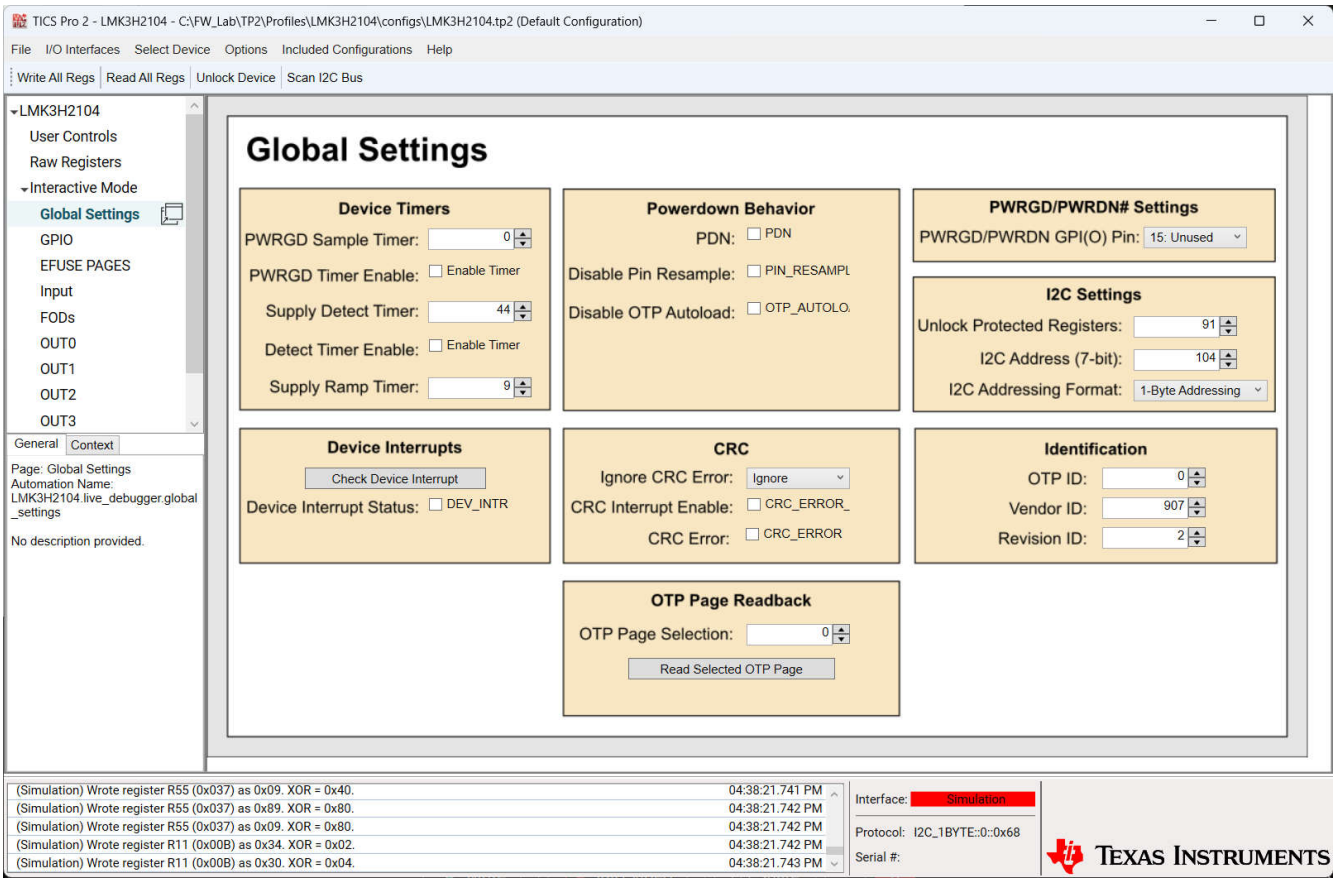


Figure 3-1. Global Settings Page

The *Global Settings* page allows for modification of device settings that impact general device behaviors not related to frequency generation. The sections are as follows:

- Device Timers, for viewing the device startup timing behavior,
- Powerdown Behavior, for both placing the device in low-power mode and controlling the behavior in low-power mode,
- PWRGD/PWRDN Settings, for controlling which pin is used as the PWRGD/PWRDN pin (if any),
- I2C settings, for configuring the I2C address and setting the register addressing format (1-Byte vs 2-Byte),
- Device Interrupts, for checking the global device interrupt status,
- CRC, for viewing the status of the CRC error, and the device behavior when there is a CRC error,
- Identification, for viewing the OTP, vendor, and device revision information, and
- OTP Page Readback, for reading back the settings of any one of the four OTP pages into the live registers. Note that this readback only works with a device connected.

3.2.2 GPIO Page

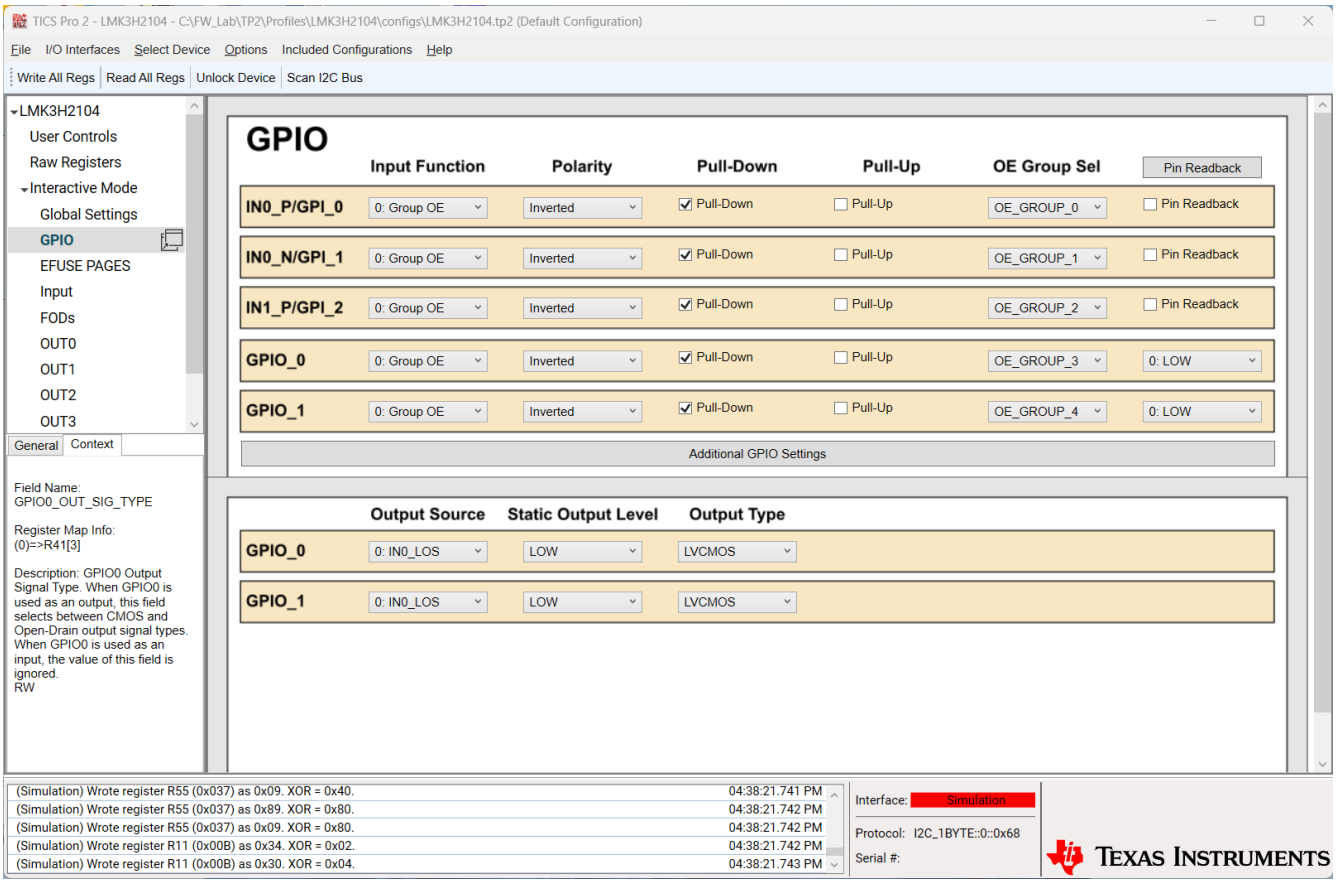


Figure 3-2. LMK3H2104 GPIO Page

The *GPIO* page contains the settings for configuring the GPI and GPIO pins of the LMK3H2104. If a GPI or GPIO pin is unused, that pin must be configured as a "General Purpose Input". Each GPI and GPIO pin has pull-down resistors that can be individually enabled or disabled. Readback of the pin state is available for each GPI and GPIO pin.

GPIO pins, when configured as a status output, can provide a loss of signal status for the input clock, or a clock ready signal when the device is ready to provide output clocks. Click the "Additional GPIO Settings" button to configure the status output source (status output behavior selected), static output level (GPO behavior selected), and the output type (LVCMOS or open-drain).

3.2.3 EFUSE Pages

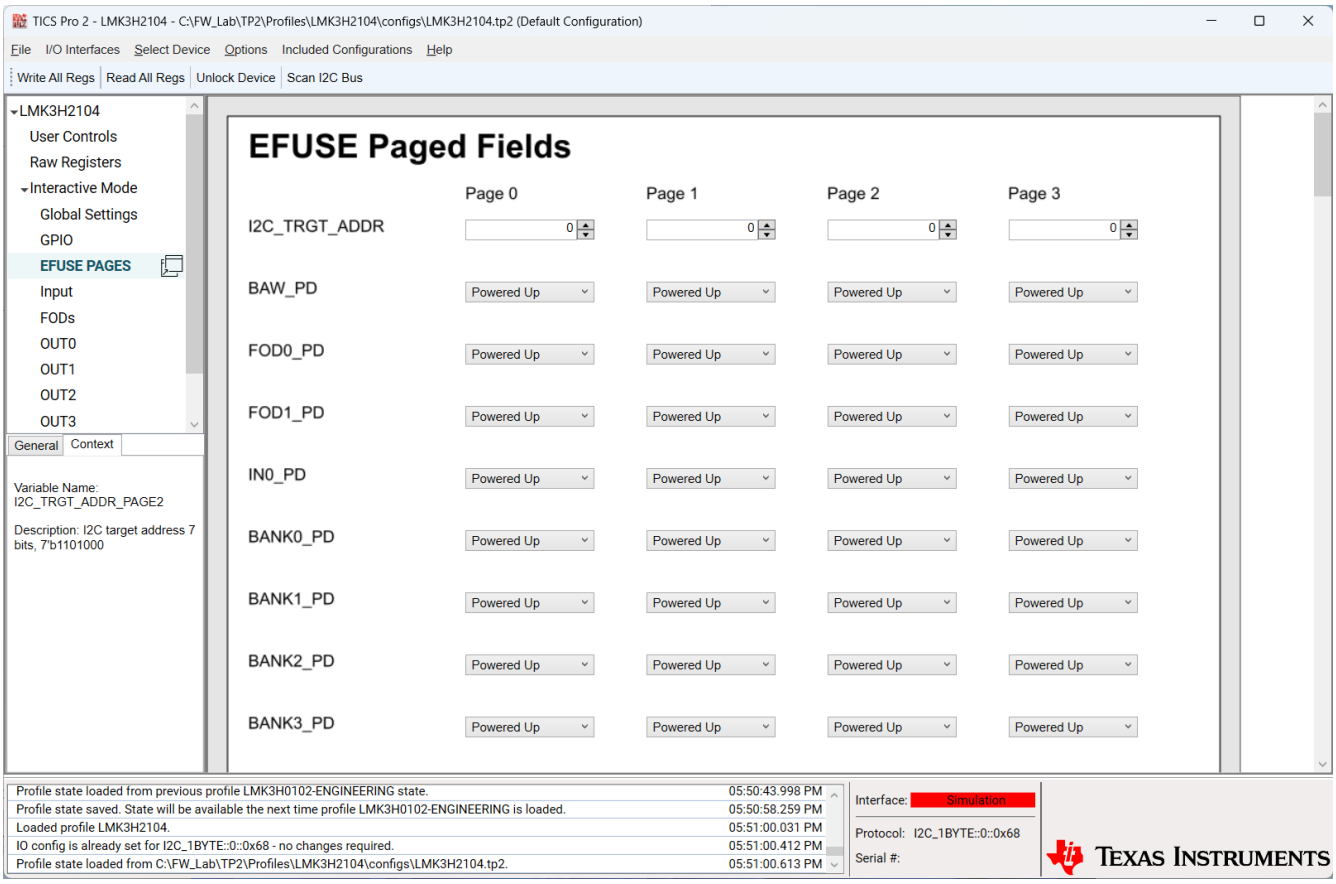


Figure 3-3. LMK3H2104 EFUSE Page

The *EFUSE Paged Fields* page allows for viewing the full contents of the device non-volatile memory. The "Read Selected OTP Page" button on the *Global Settings* page, in addition to writing the live registers, populates this page with the memory contents.

3.2.4 Input Page

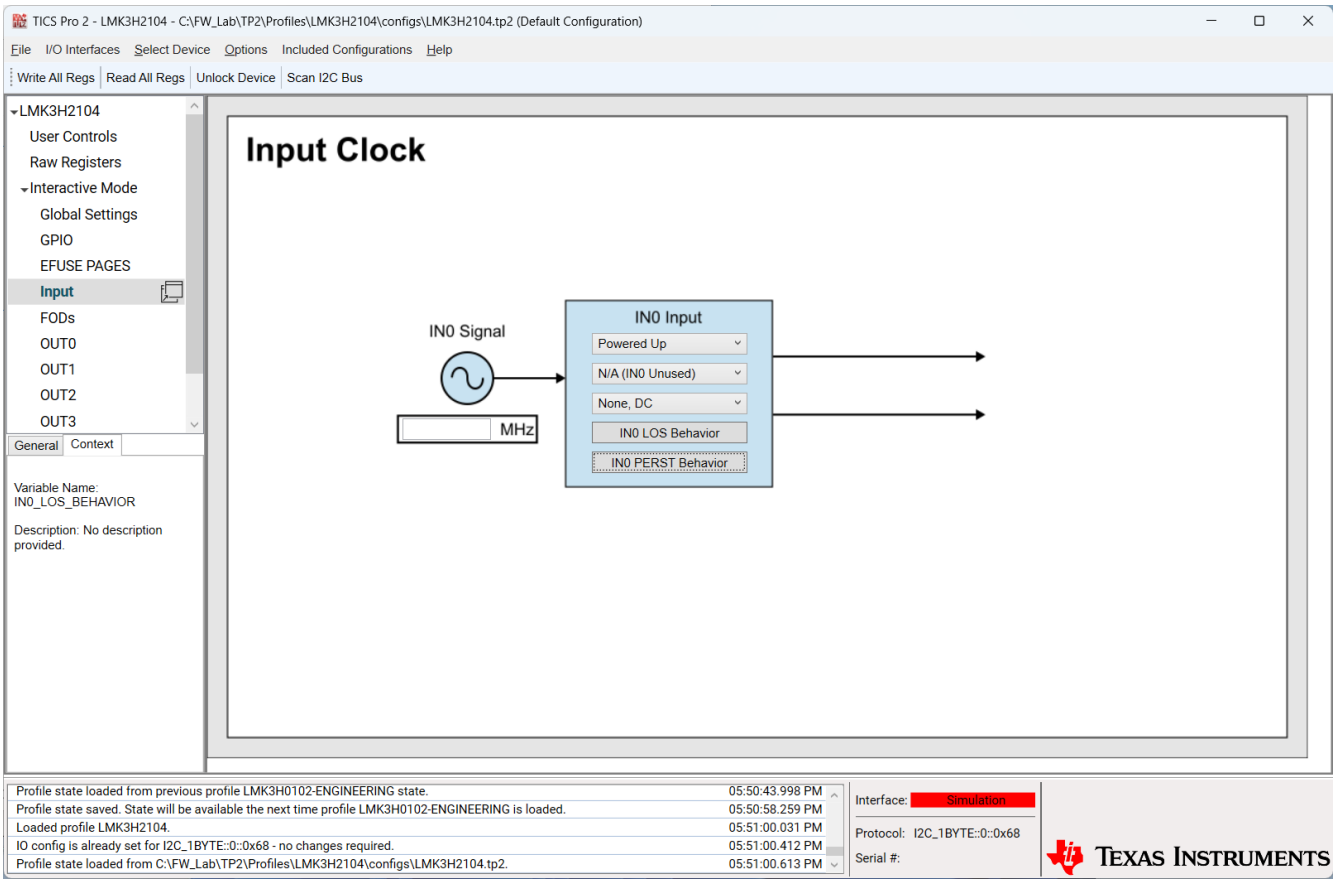


Figure 3-4. LMK3H2104 Input Page

The *Input Clock* page allows for modification of the LMK3H2104 input buffer. The input consists of the following fields:

- Input frequency: Used solely for calculation purposes on the output pages
- Input format: Disabled, IN0_P LVCMOS, IN0_N LVCMOS, or IN0 Differential
- Input termination: No termination, 100Ω differential termination (for LVDS), 100kΩ to an internal bias voltage, or 50Ω to GND (for HCSL)
- Loss of signal detection
- PCIe buffer mode configuration.

3.2.5 FODs Page

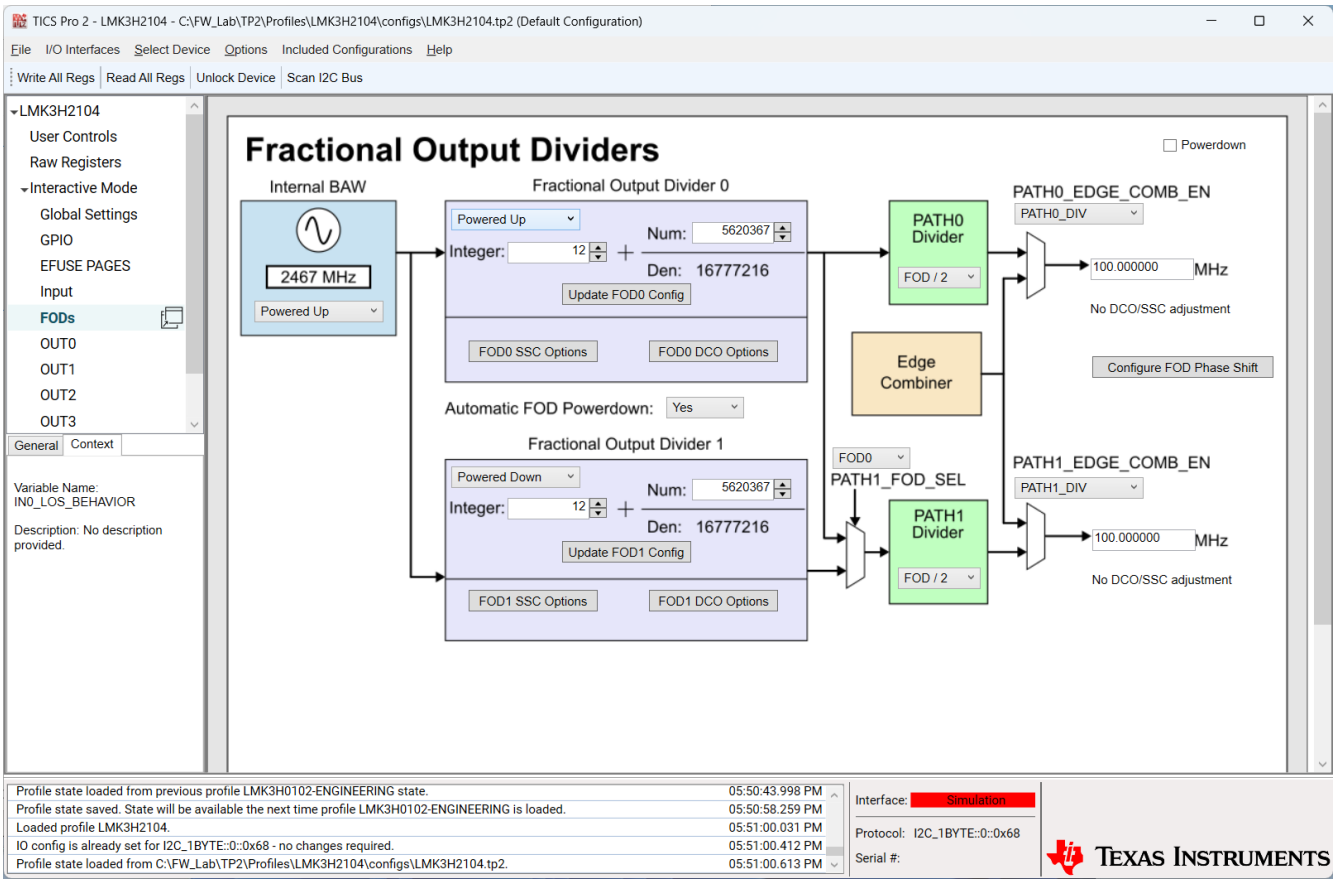


Figure 3-5. LMK3H2104 FODs Page

The *FODs* page allows for setting the FOD0 and FOD1 divider values. Each FOD has a path postdivider, allowing for the generation of frequencies between 2.5MHz and 200MHz after the postdivider. If the edge combiner is selected in place of the FOD postdivider, then frequencies between 200MHz and 400MHz can be generated. When either path selects the edge combiner, then the FOD1 divider values are ignored by the LMK3H2104, and both FODs use the FOD0 divider values.

The textbox to the right of each FOD path divider allows for automatic calculation of the FOD divider values. Users have the option to select from each possible combination of FOD frequency and path divider value for frequency generation. If the frequency cannot be generated, the box turns red, and an error message appears in the status bar. If the frequency requires usage of the edge combiner, or only has one FOD-divider combination for generating the frequency, then both frequency boxes are updated accordingly without the selection popup. If the FOD divider selection for the PATH1 frequency results in the same values as the FOD0 divider values, then FOD0 is automatically selected as the source for PATH1. Note that changing FOD1_PATH_SEL requires unlocking the device. This is done by writing 91d to the field "Unlock Protected Registers" on the *Global Settings* page.

FOD0 and FOD1 provide the option for Spread Spectrum Clocking (SSC). Four preconfigured SSC options are available, in addition to custom SSC options. The preconfigured SSC options are optimized for an FOD frequency of 200MHz. The custom SSC can be used with any FOD frequency. The GUI automatically calculates the values for the SSC_STEPS and SSC_STEP_SIZE fields when a value is entered for the SSC depth. Changing the modulation type between down-spread and center-spread also recalculates these values. If a preconfigured SSC option is used on FOD0, FOD1 must have a preconfigured SSC option selected even if SSC is not enabled on FOD1.

The GUI allows for adjustment of FOD values in terms of PPM adjustment. Once a PPM step is entered, the "Step DCO Up" and "Step DCO Down" buttons for each FOD increment or decrement the total PPM shift. The

PPM shift can be reset by toggling the Powerdown checkbox. If "Disable OTP Autoload"" is not selected on the *Global Settings* page, then the device registers are re-loaded from memory.

3.2.6 OUT0 Page

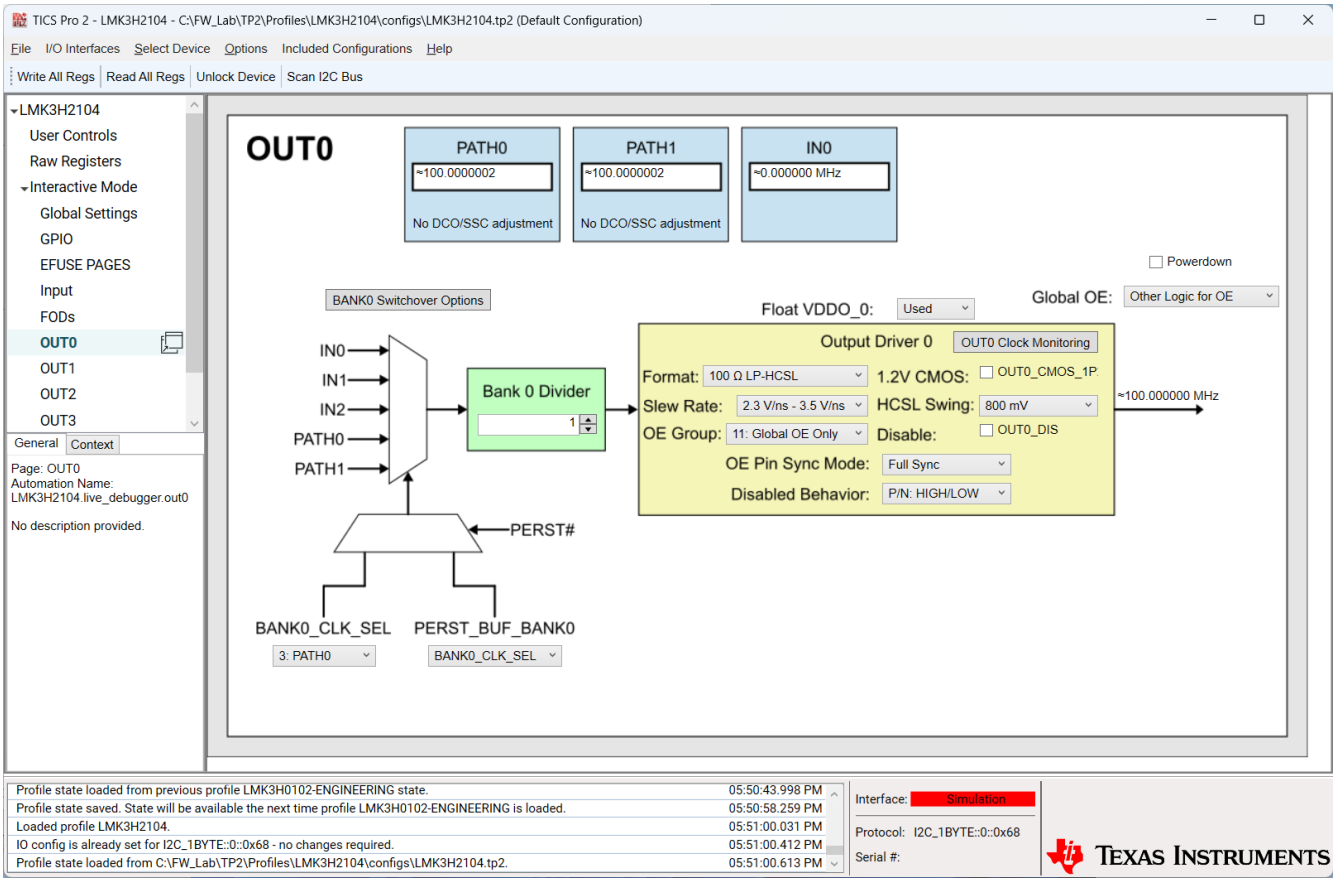


Figure 3-6. LMK3H2104 OUT0 Page

The *OUT0* page allows for configuration of OUT0. The GUI pages for OUT1, OUT2, and OUT3 function similarly to this page. This page allows for the configuration of the following options for OUT0:

- Float VDDO_x: Whether the device expects the supply for this bank to be floating or powered
- Bank divider: For OUT0 this allows for a maximum divide value of 65536 when selecting a divider value of 0, for all other outputs the maximum divider value is 16.
- Output format
- Slew rate (for differential output formats only)
- Output enable group
- 1.2V LVCMOS enable: When 1.2V LVCMOS is enabled, and the output format field selects an LVCMOS output type, the output is LVCMOS with a swing of 1.2V. Otherwise, the output format field selects the output format.
- LP-HCSL swing
- Output disable
- Output enable pin synchronization mode: Whether a group of clocks are phase-synchronized (Full Sync), if there are at least four output clock cycles between output enable assertion and the clock output (Self Sync), or is completely asynchronous (No Sync)
- Output disable behavior
- Switchover and clock monitoring features
- BANKx clock selection
- PCIe reset buffer mode behavior

3.2.7 REF0 Page

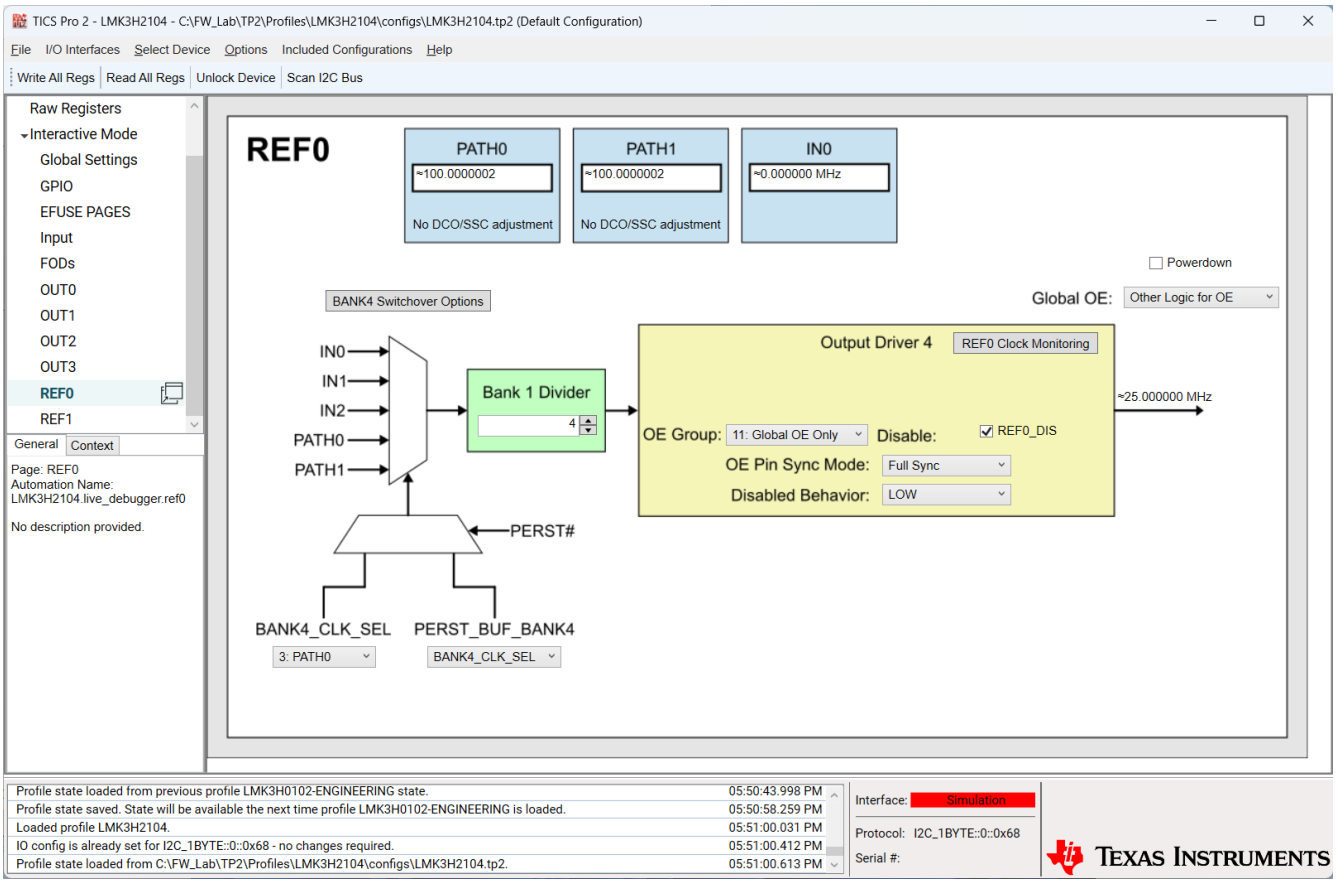


Figure 3-7. LMK3H2104 REF0 Page

The *REF0* page allows for configuration of REF0. The GUI page for REF1 functions similarly to this page. This page allows for the configuration of the following options for REF0:

- Bank divider: For OUT0 this allows for a maximum divide value of 65536 when selecting a divider value of 0, for all other outputs the maximum divider value is 16.
- Output enable group
- Output disable
- Output enable pin synchronization mode: Whether a group of clocks are phase-synchronized (Full Sync), if there are at least four output clock cycles between output enable assertion and the clock output (Self Sync), or is completely asynchronous (No Sync)
- Output disable behavior
- Switchover and clock monitoring features
- BANKx clock selection
- PCIe reset buffer mode behavior

4 Implementation Results

4.1 Evaluation Setup

For test measurements, the evaluation module is configured in one of two modes:

1. Operation from the onboard LDOs in BAW + FOD mode
2. Operation from the onboard LDOs in input buffer mode

Measurement data provided is reflective of device performance under typical conditions.

4.2 Performance Data and Results

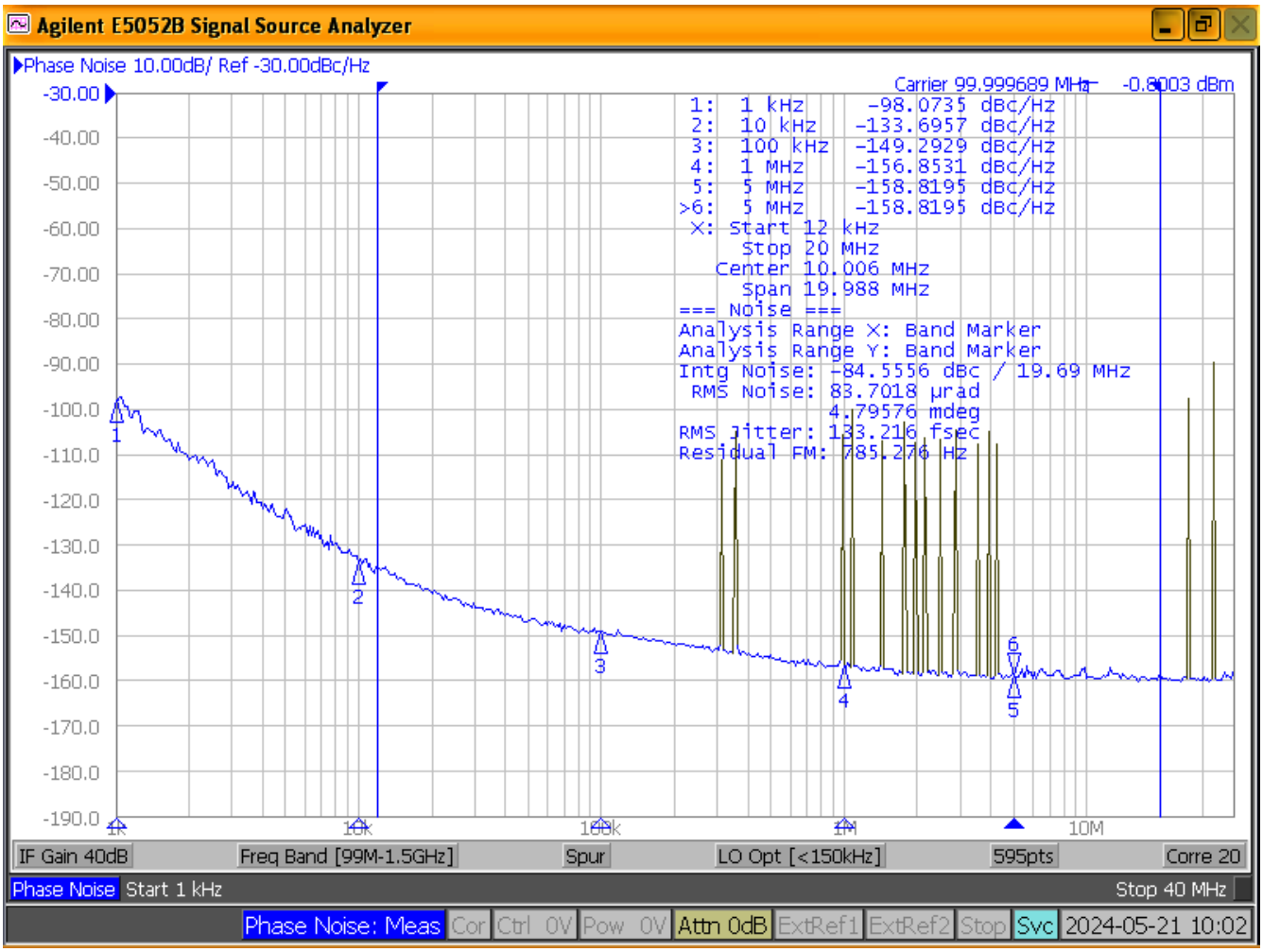


Figure 4-1. LMK3H2104EVM Typical Performance Using FOD0 Through PATH1, 100MHz

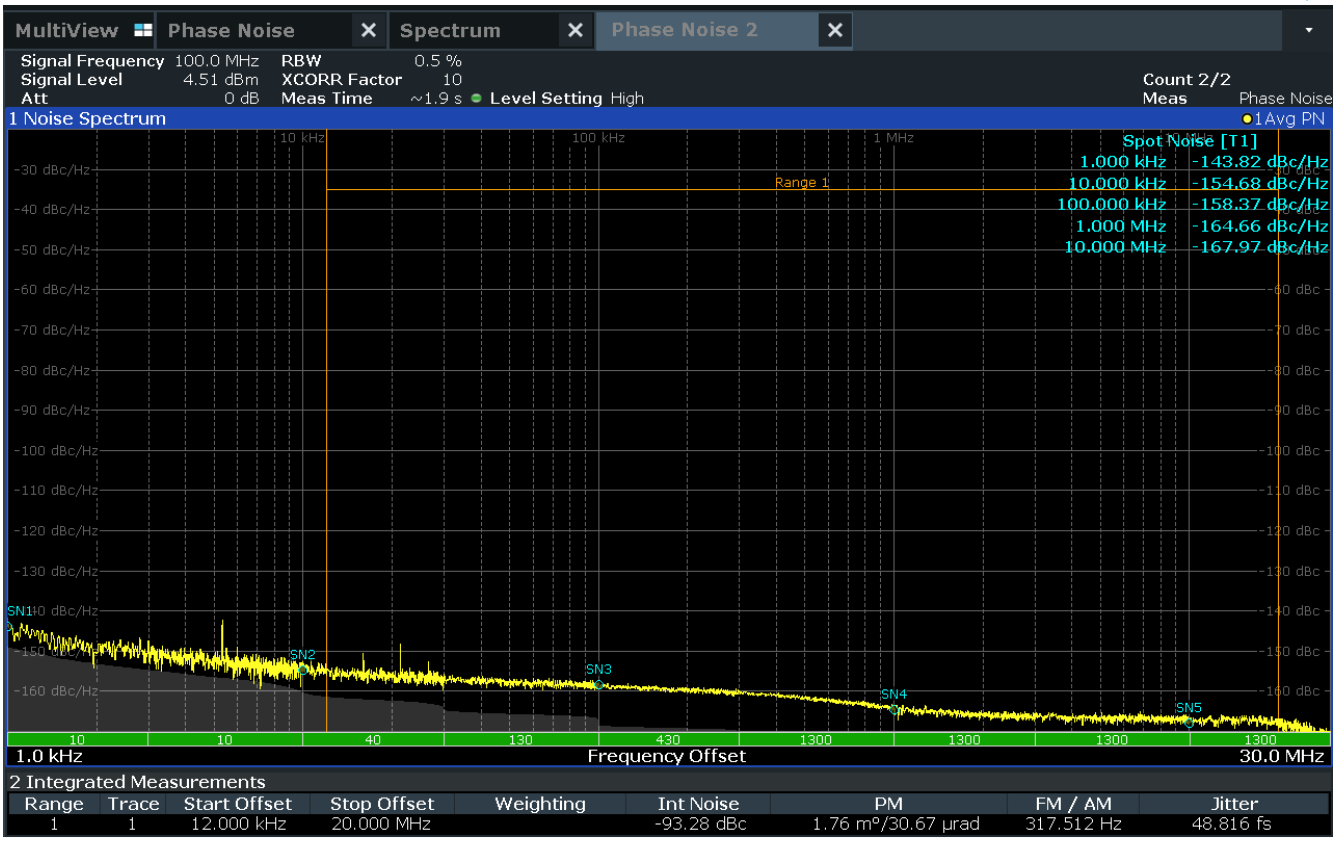


Figure 4-2. SMA100B 100MHz Input to LMK3H2104EVM for Buffer Mode Measurement

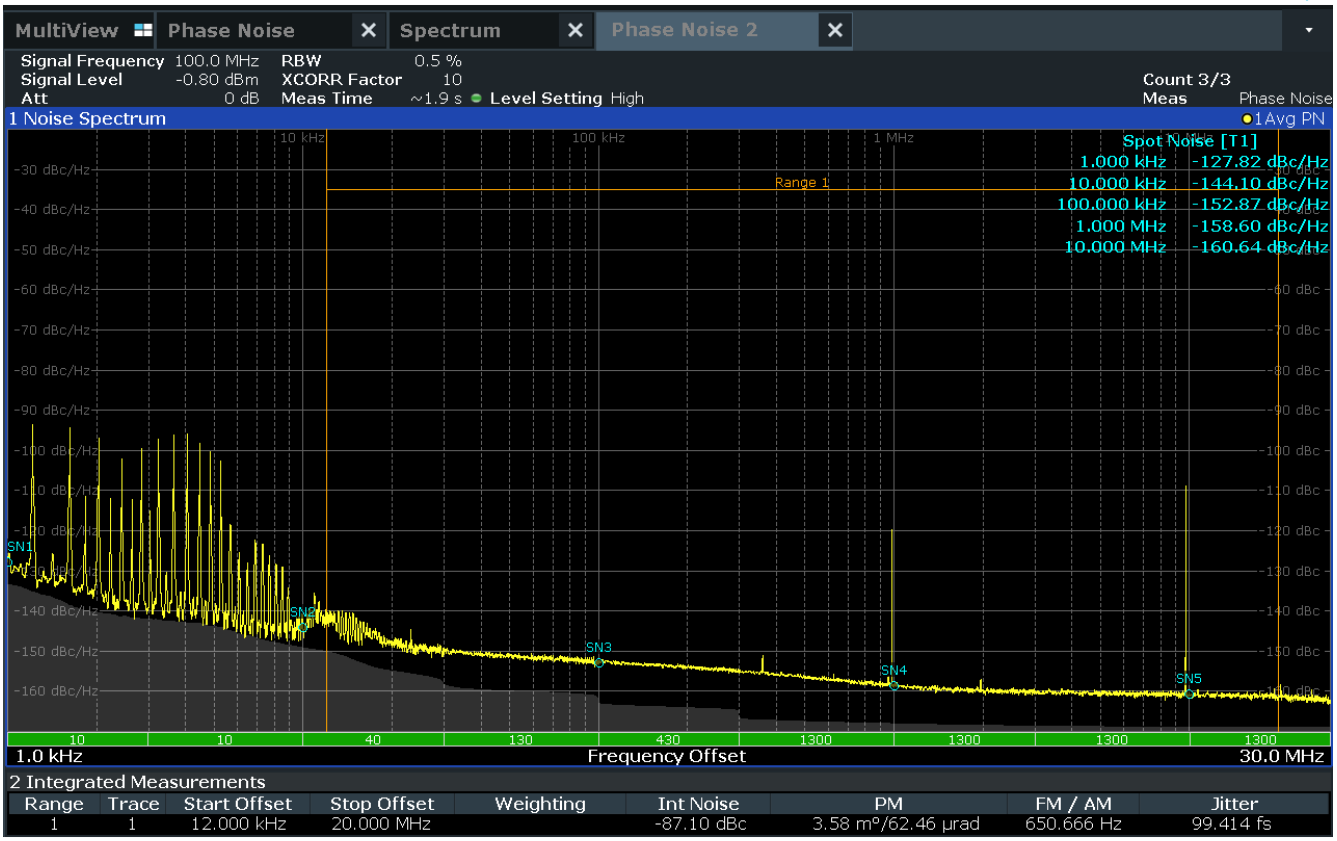


Figure 4-3. LMK3H2104 Typical Performance in Buffer Mode, SMA100B 100MHz Input

Figure 4-1 shows the typical performance of the LMK3H2104EVM when all outputs are 100MHz LP-HCSL using FOD0 routed through PATH1. TI has seen a small performance improvement when using PATH1 instead of PATH0 for the clock source, on the order of tens of femtoseconds.

Figure 4-3 shows the performance of the LMK3H2104EVM when used in buffer mode. Figure 4-2 shows the performance of the input provided to the evaluation module for buffer mode testing.

5 Hardware Design Files

5.1 Schematics

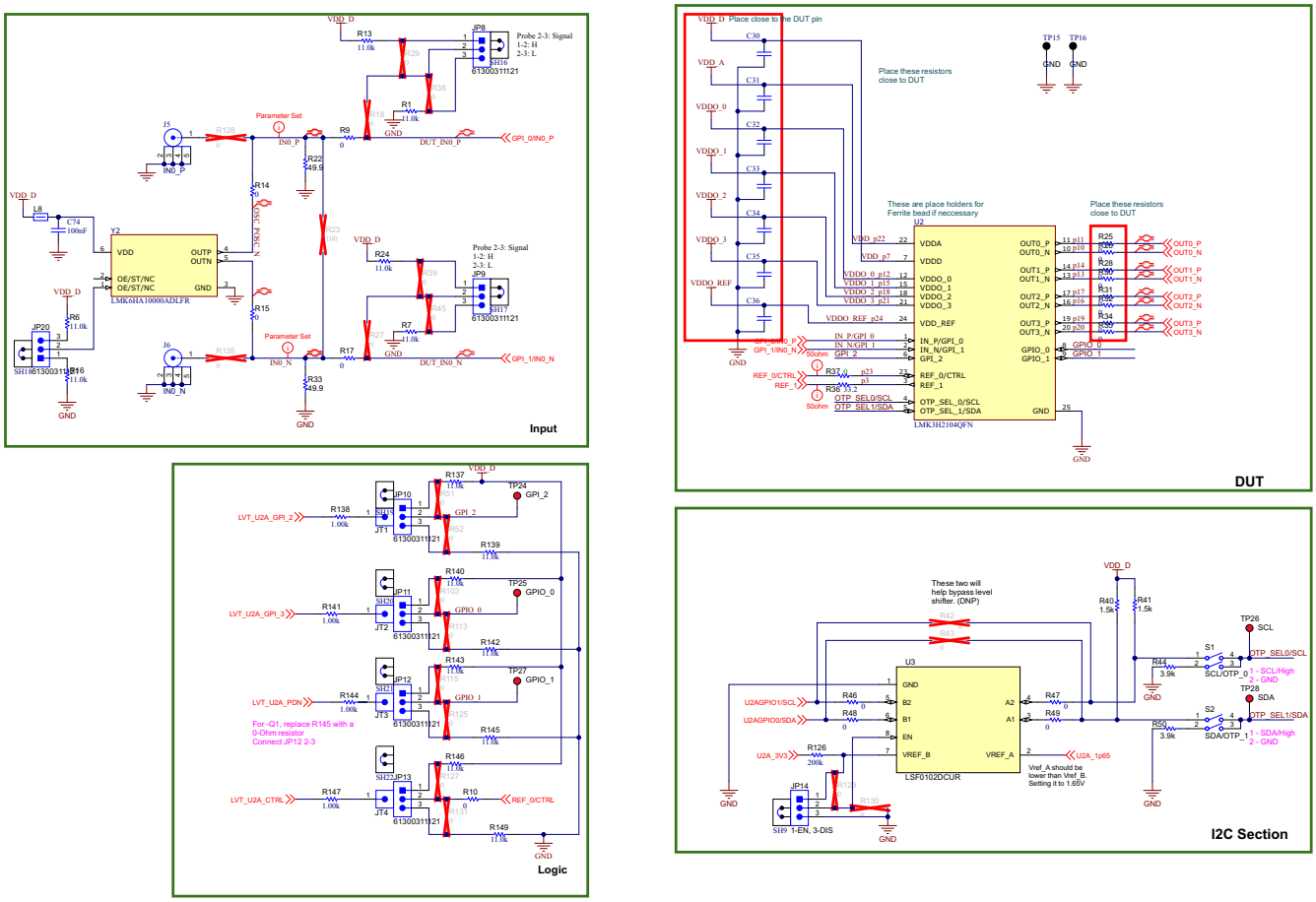


Figure 5-1. LMK3H2104EVM Device, Inputs, and GPI

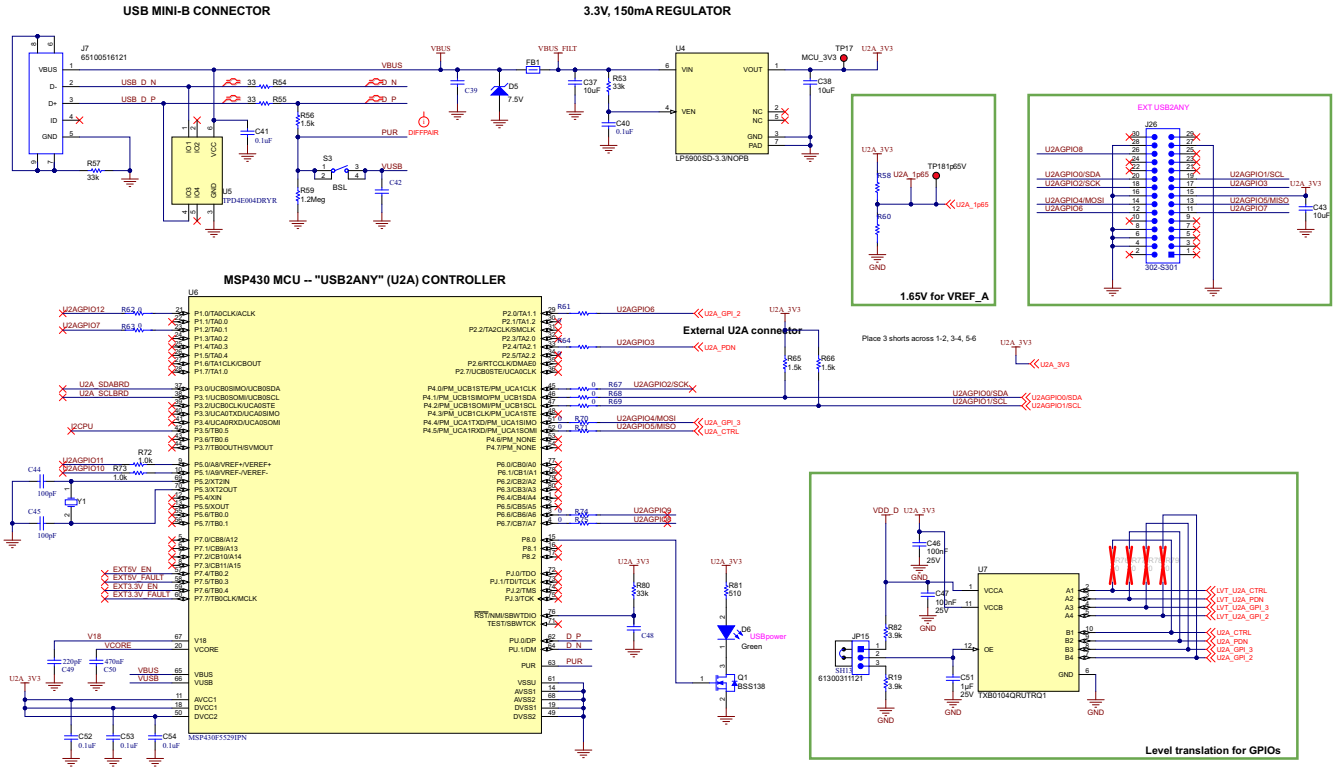


Figure 5-2. LMK3H2104EVM USB2ANY and USB Power

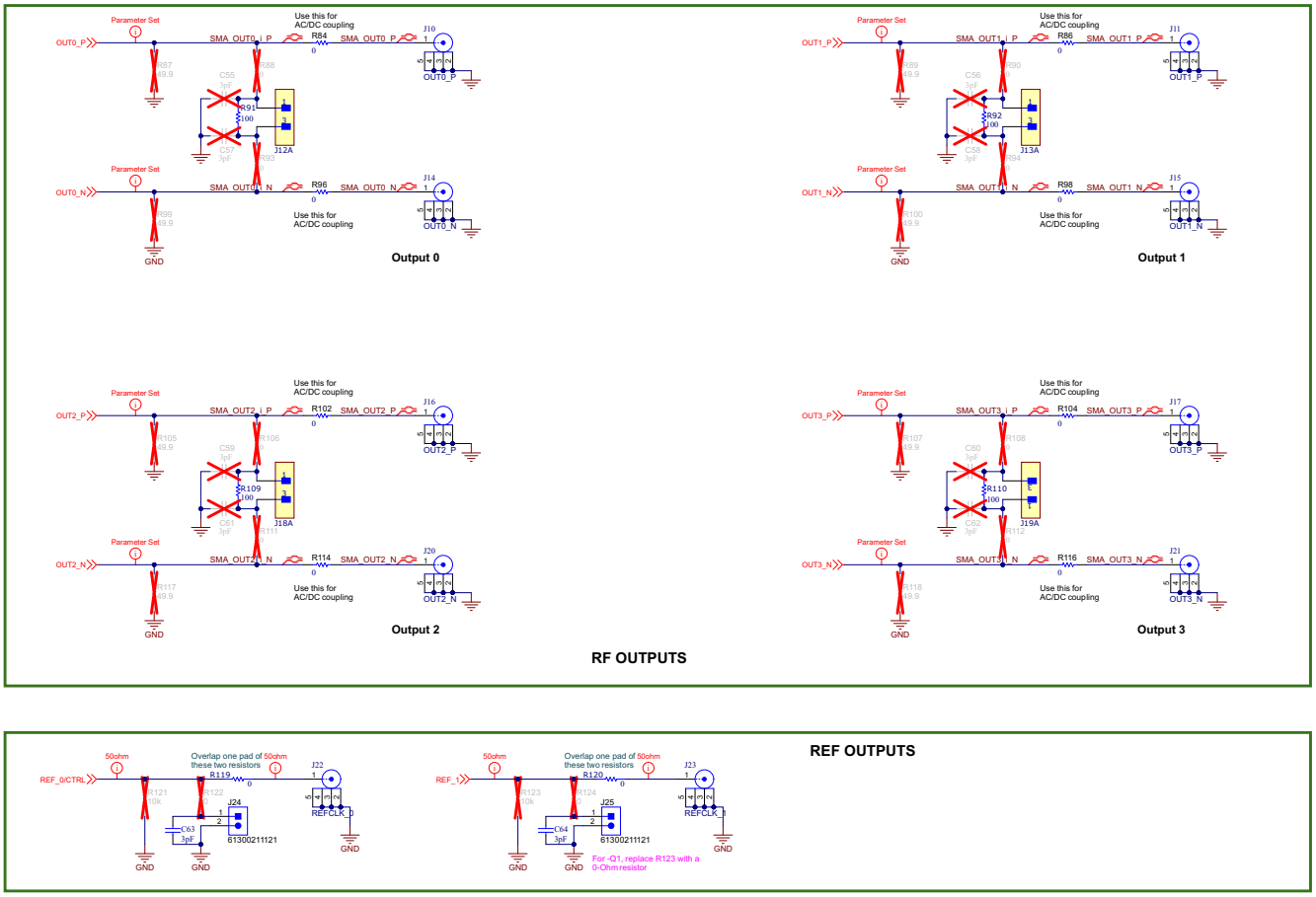


Figure 5-3. LMK3H2104EVM Outputs

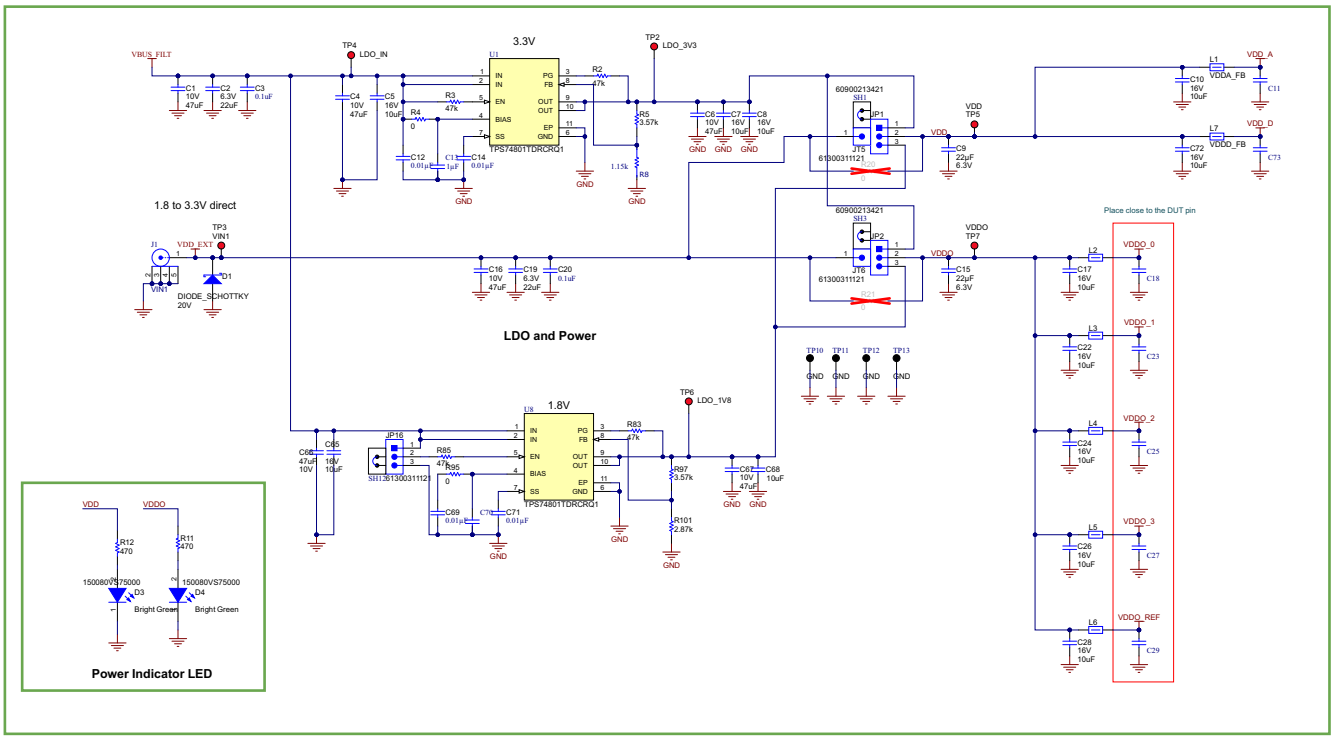


Figure 5-4. LMK3H2104EVM Power

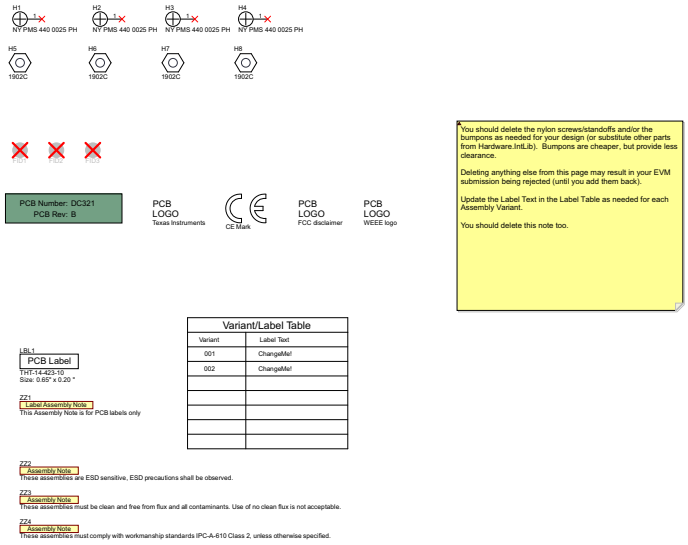


Figure 5-5. LMK3H2104EVM Hardware

5.2 EVM Layout

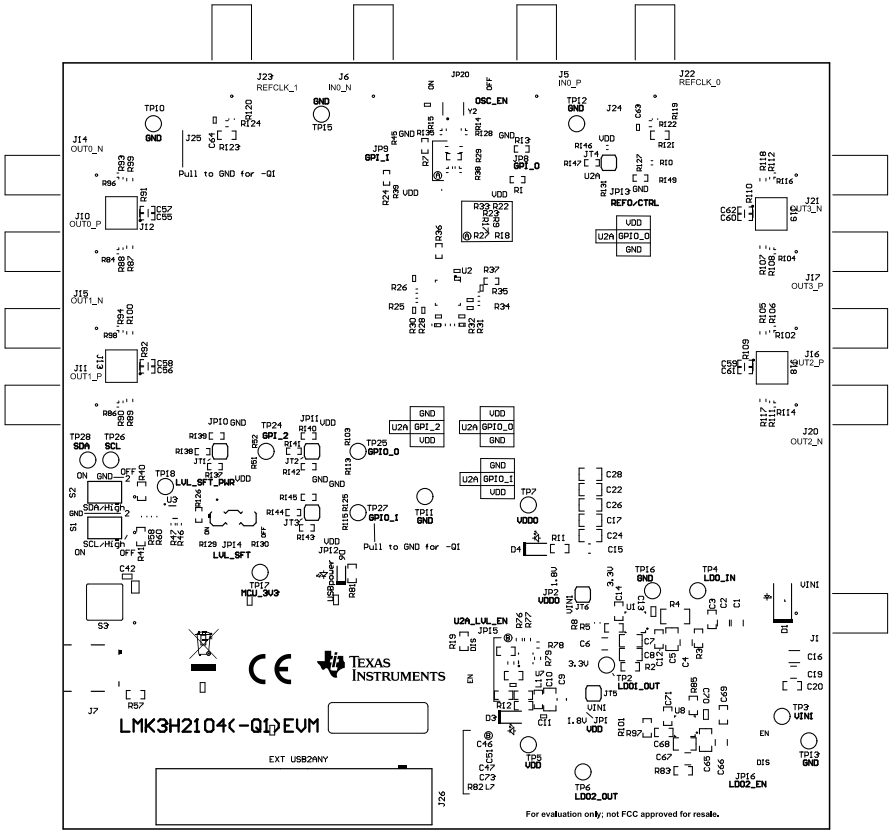


Figure 5-6. Top Overlay

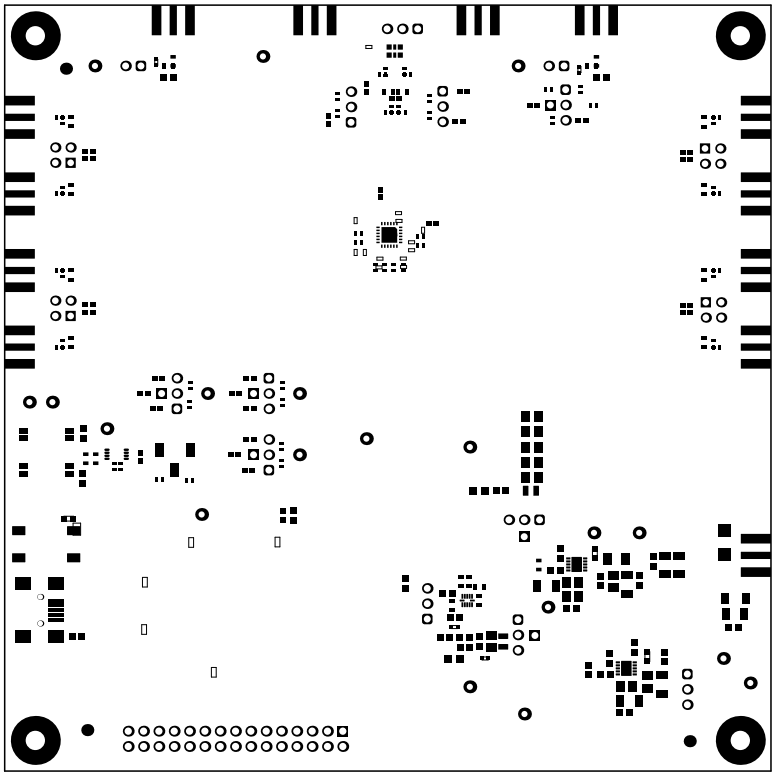


Figure 5-7. Top Solder Mask

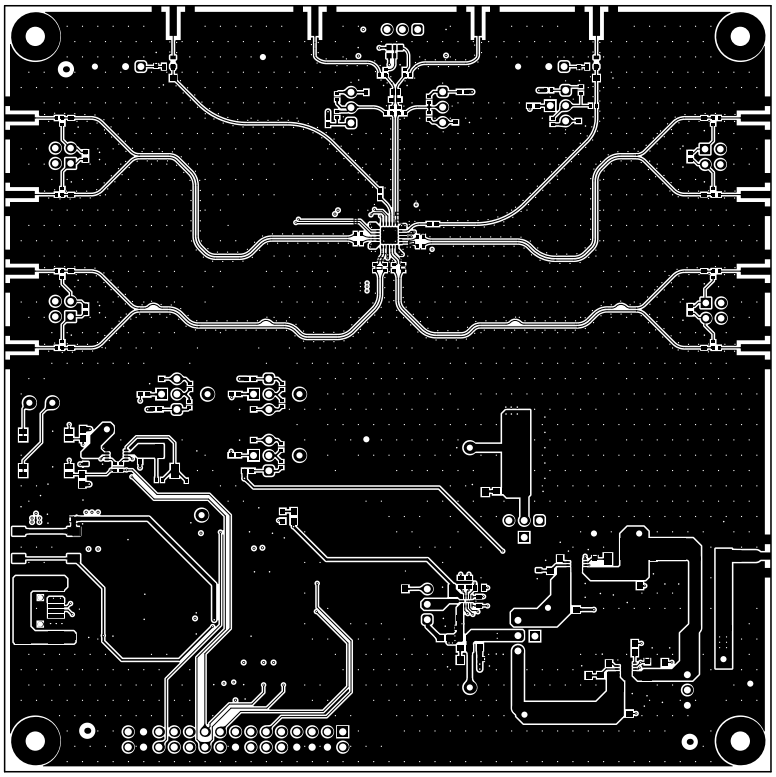


Figure 5-8. Top Layer

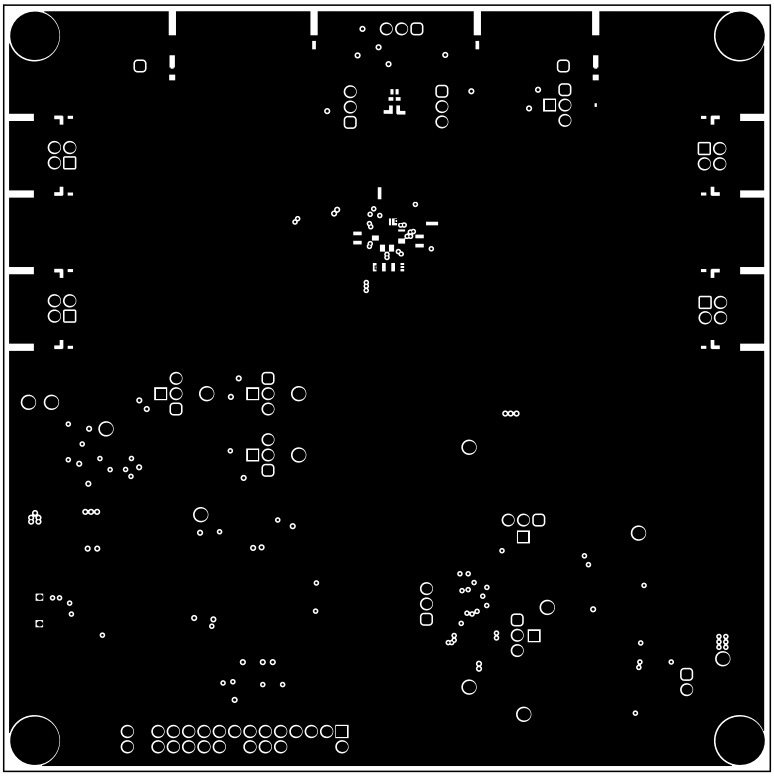


Figure 5-9. Signal Layer 1

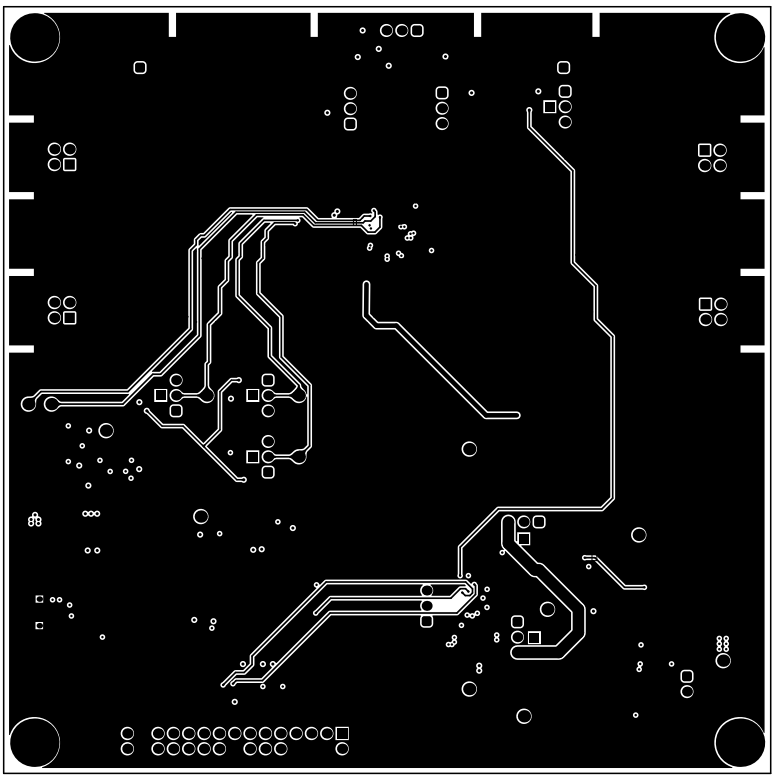


Figure 5-10. Signal Layer 2

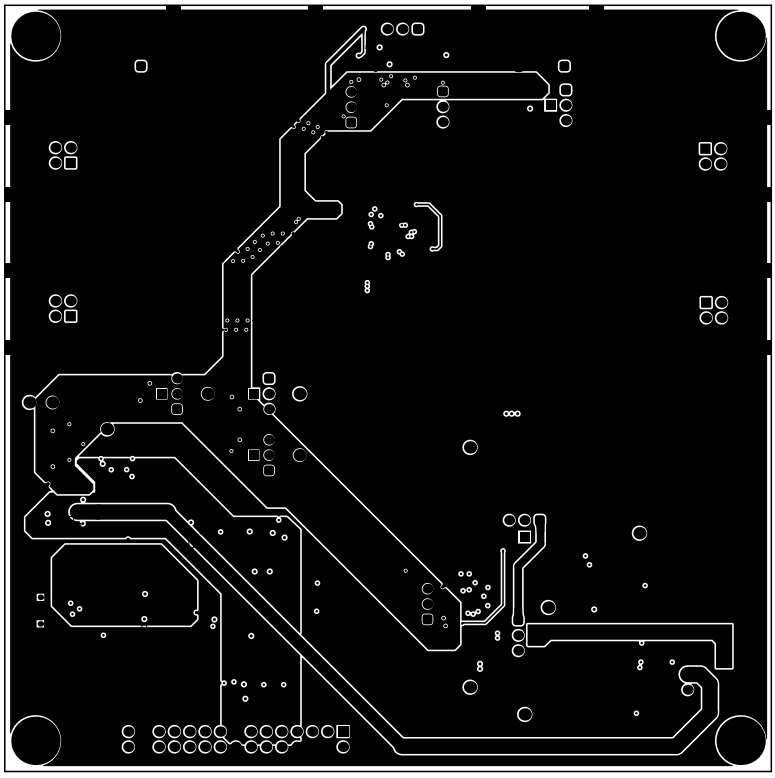


Figure 5-11. Signal Layer 3

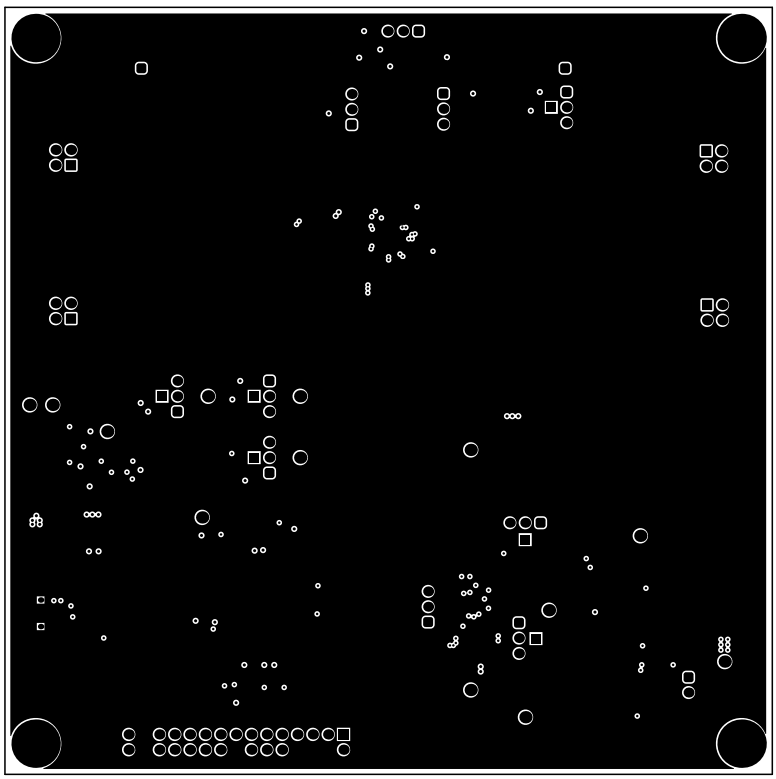


Figure 5-12. Signal Layer 4

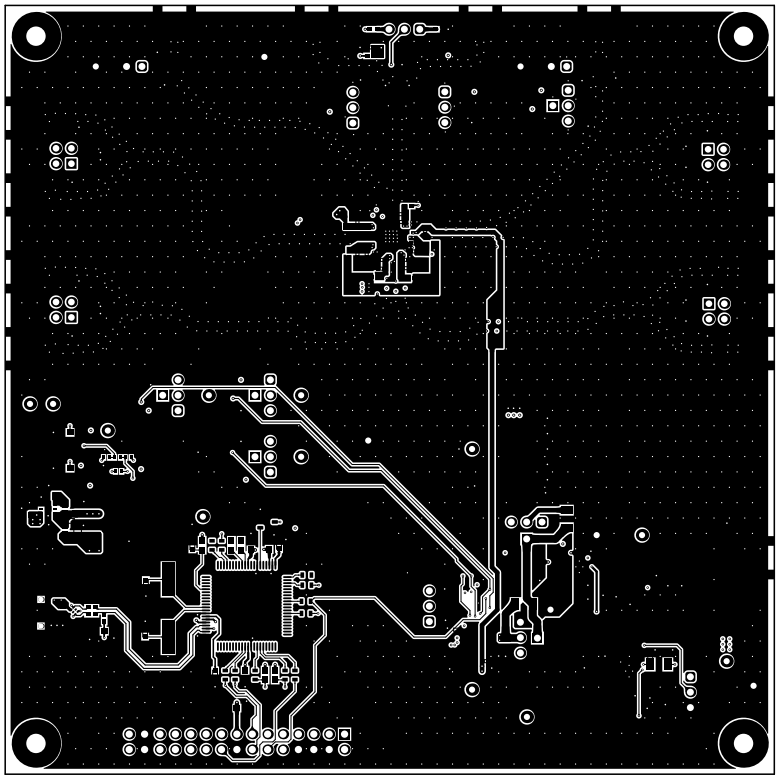


Figure 5-13. Bottom Layer

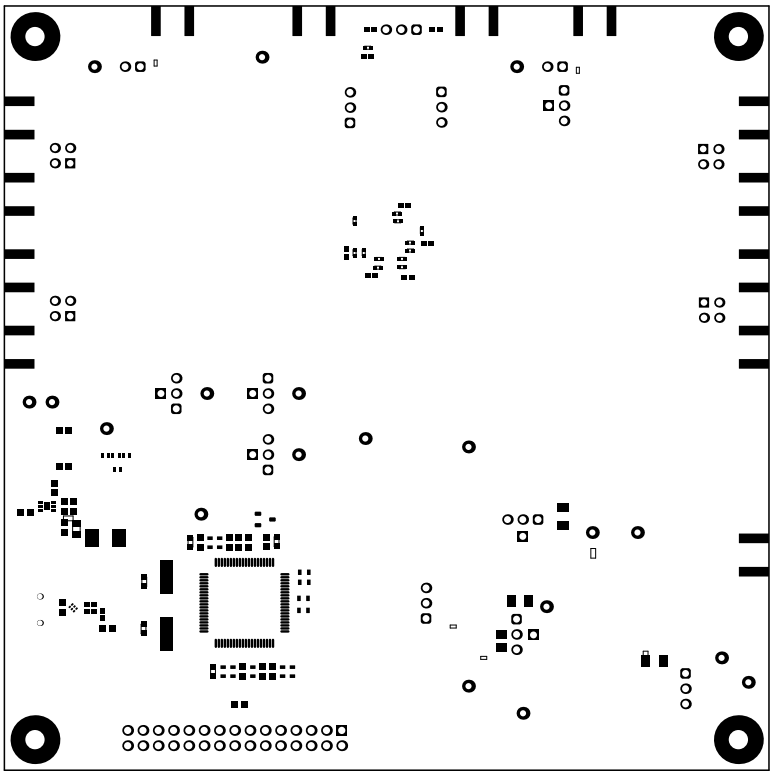


Figure 5-14. Bottom Solder Mask

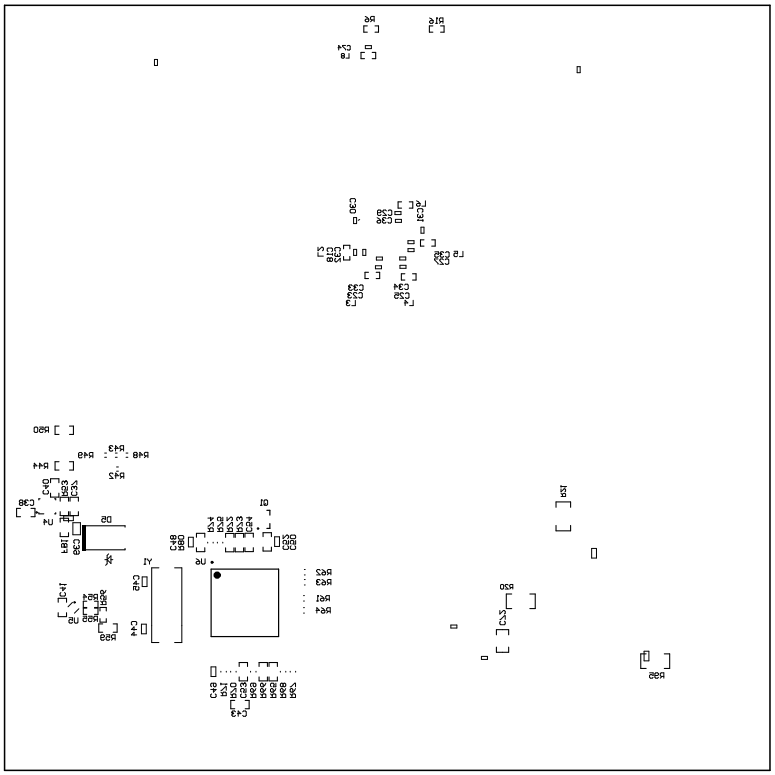
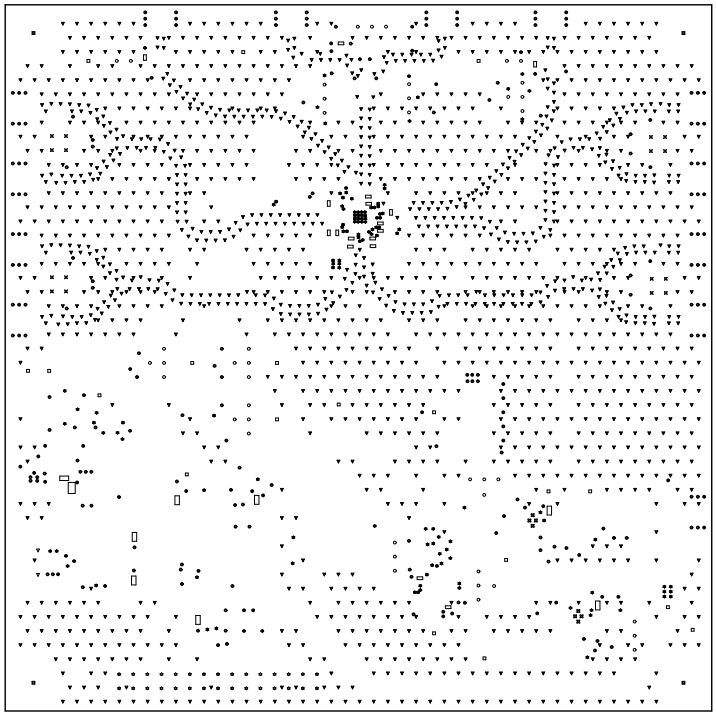


Figure 5-15. Bottom Overlay



DRILL TABLE

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
▽	2	35.43mil (0.900mm)	NPTH	Round	Top Layer - Bottom Layer	-0mil/+2mil
⧈	4	125.98mil (3.200mm)	NPTH	Round	Top Layer - Bottom Layer	-2mil/+2mil
⊠	8	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
✱	129	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
▼	1773	8.10mil (0.206mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
⊕	227	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
□	19	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
⌘	16	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	
○	49	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
✲	30	47.24mil (1.200mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
	2251 Total					

Figure 5-16. Drill Drawing

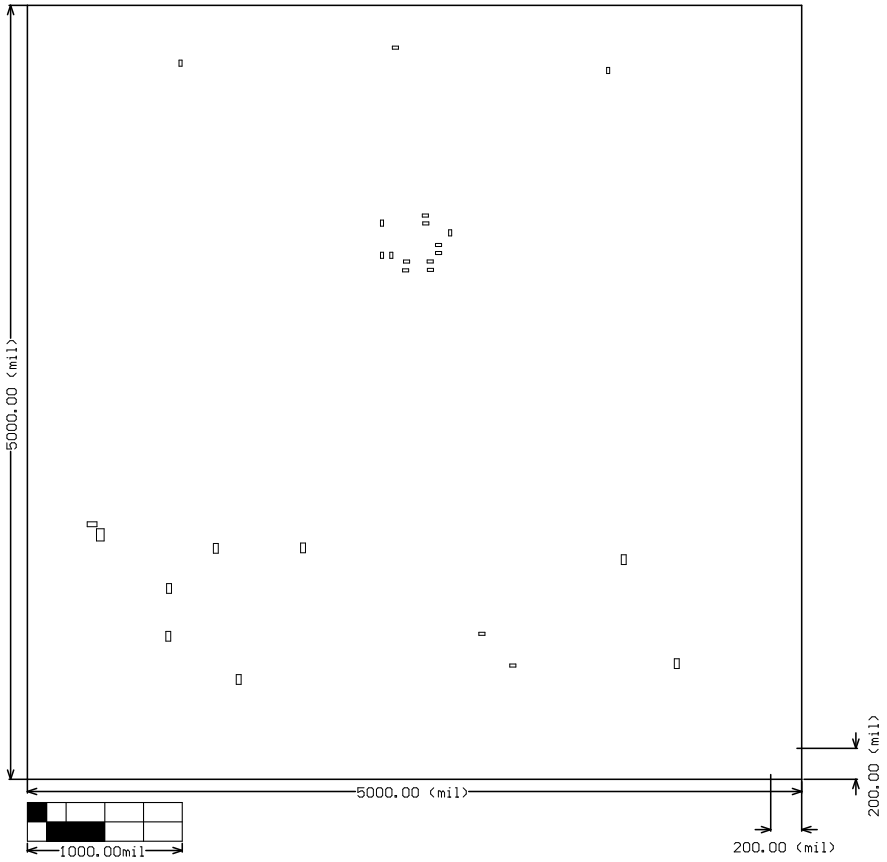


Figure 5-17. Board Dimensions

5.3 Bill of Materials (BOM)

Designator	Description	Manufacturer	Part Number	Quantity
!PCB	Printed Circuit Board	Any	DC321	1
C1, C4, C6, C16, C66, C67	CAP, CERM, 47µF, 10V, ±10%, X5R, AEC-Q200 Grade 1, 1206	MuRata	GRT31CR61A476KE13L	6
C2, C19	CAP, CERM, 22µF, 6.3V, ±10%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GRT31CR70J226KE13L	2
C3, C20, C40, C41, C52, C53, C54	CAP, CERM, 0.1µF, 16V, ±10%, X7R, 0603	Wurth Elektronik	885012206046	7
C5, C7, C8, C10, C17, C22, C24, C26, C28, C65, C68, C72	CAP, CERM, 10µF, 16V, ±10%, X7S, AEC-Q200 Grade 1, 0805	TDK	CGA4J1X7S1C106K125AC	12
C9, C15	CAP, CERM, 22µF, 6.3V,±20%, X7T, AEC-Q200 Grade 1, 0805	TDK	CGA4J1X7T0J226M	2
C11, C18, C23, C25, C27, C29, C73	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0402, X5R, 2.2µF, 6.3VDC	Wurth Elektronik	885012105007	7
C12, C14, C69, C71	CAP, CERM, 0.01µF, 50V,±10%, X7R, 0603	Wurth Elektronik	885012206089	4
C13, C70	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X5R, 1µF, 10VDC	Wurth Elektronik	885012106010	2
C30, C31, C32, C33, C34, C35, C36, C74	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0402, X7R, 100nF, 10VDC	Wurth Elektronik	885012205018	8
C37, C38, C43	CAP, CERM, 10µF, 10V, ±20%, X5R, 0603	TDK	C1608X5R1A106M080AC	3
C39	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0805, X5R, 22µF, 10VDC	Wurth Elektronik	885012107011	1
C42, C49	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, NP0, 220pF, 50VDC	Wurth Elektronik	885012006059	2
C44, C45	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, NP0, 100pF, 100VDC	Wurth Elektronik	885012006079	2
C46, C47	CAP, CERM, 0.1µF, 25V, ±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E2X7R1E104K080AA	2
C48	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 2.2nF, 50VDC	Wurth Elektronik	885012206085	1
C50	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 470nF, 10VDC	Wurth Elektronik	885012206024	1
C51	CAP, CERM, 1µF, 25V,±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1E105K080AC	1
C63, C64	WCAP-CSRF Multilayer Ceramic Chip Capacitor, High Frequency, size 0402, NP0 Class I, 3pF, 50VDC	Wurth Elektronik	885392005010	2
D1	Diode, Schottky, 20V, 2 A, SMA	Diodes Inc.	B220A-13-F	1
D3, D4	LED, Bright Green, SMD	Wurth Elektronik	150080VS75000	2
D5	Diode, Zener, 7.5V, 550mW, SMB	ON Semiconductor	1SMB5922BT3G	1
D6	LED, Green, SMD	Wurth Elektronik	150060VS75000	1
FB1	Ferrite Bead, 60Ω @ 100MHz, 3 A, 0603	Wurth Elektronik	742792602	1
H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4

Designator	Description	Manufacturer	Part Number	Quantity
H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
J1, J5, J6, J10, J11, J14, J15, J16, J17, J20, J21, J22, J23	CONN SMA JACK STR EDGE MNT	RF Solutions Ltd.	CON-SMA-EDGE-S	13
J7	Connector, Receptacle, USB Mini B 2.0, SMT	Wurth Elektronik	65100516121	1
J12, J13, J18, J19	THTVertical Pin Header WR-PHD, Pitch 2.54mm, Dual Row, 4 pins	Wurth Electronics	61300421121	4
J24, J25	Header, 2.54mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	2
J26	Header(shrouded), 2.54mm, 15x2, Gold, TH	On-Shore Technology	302-S301	1
JP1, JP2, JP8, JP9, JP10, JP11, JP12, JP13, JP15, JP16, JP20	Header, 2.54mm, 3x1, Gold, TH	Wurth Elektronik	61300311121	11
JP14	Header, 2.54mm, 3x1, Gold, SMT	Harwin	M20-8770342	1
JT1, JT2, JT3, JT4, JT5, JT6	Header, 2.54mm, 1x1, Gold, TH	Wurth Elektronik	61300111121	6
L1, L7	Ferrite Bead, 750Ω @ 100MHz, 0.4 A, 0603	Wurth Elektronik	742792656	2
L2, L3, L4, L5, L6, L8	Ferrite Bead, 600Ω @ 100MHz, 0.5 A, 0402	MuRata	BLM15AX601SN1D	6
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
Q1	MOSFET, N-CH, 50V, 0.22 A, SOT-23	Fairchild Semiconductor	BSS138	1
R1, R6, R7, R13, R16, R24, R137, R139, R140, R142, R143, R145, R146, R149	RES, 11.0 k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040211K0FKED	14
R2, R3, R83, R85	RES, 47 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060347K0JNEA	4
R4, R95	RES, 0, 5%, 0.25W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW12060000Z0EA	2
R5, R97	RES, 3.57 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06033K57FKEA	2
R8	1.15 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Anti-Sulfur Thick Film	Wurth Electronics	560112116118	1
R9, R10, R14, R15, R17, R25, R26, R28, R30, R31, R32, R34, R35, R37, R46, R47, R48, R49, R84, R86, R96, R98, R102, R104, R114, R116	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	26
R11, R12	RES, 470, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603470RJNEA	2
R19, R44, R50, R82	RES, 3.9 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06033K90JNEA	4
R22, R33	RES, 49.9, 1%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349R9FKEA	2
R36	RES, 33.2, 1%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040233R2FKED	1
R40, R41, R65, R66	RES, 1.5 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K50JNEA	4
R53, R57, R80	RES, 33 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333K0JNEA	3

Designator	Description	Manufacturer	Part Number	Quantity
R54, R55	RES, 33, 5%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040233R0JNED	2
R56	RES, 1.5 k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04021K50JNED	1
R58, R60	100 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Anti-Sulfur Thick Film	Wurth Electronics	560112116004	2
R59	RES, 1.2 M, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031M20JNEA	1
R61, R62, R63, R64, R67, R68, R69, R70, R71, R74, R75, R119, R120	0Ω Jumper Chip Resistor 0603 (1608 Metric) Anti-Sulfur Thick Film	Wurth Electronics	560112116001	13
R72, R73	RES, 1.0 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K00JNEA	2
R81	RES, 510, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603510RJNEA	1
R91, R92, R109, R110	100Ω ±0.1% 0.05W, 1/20W Chip Resistor 0402 (1005 Metric) RF, High Frequency Thin Film	Vishay Dale	FC0402E1000BST0	4
R101	RES, 2.87 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06032K87FKEA	1
R126	RES, 200 k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402200KFKED	1
R138, R141, R144, R147	RES, 1.00 k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04021K00FKED	4
S1, S2	Switch, SPST, Off-On, 2 Pos, SMD	Wurth Elektronik	416131160802	2
S3	Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	TE Connectivity	FSM4JSMA	1
SH1, SH3, SH9, SH12, SH13, SH16, SH17, SH18, SH19, SH20, SH21, SH22	Shunt, 2.54mm, Gold, Black	Wurth Elektronik	60900213421	12
TP2, TP3, TP4, TP5, TP6, TP7, TP17, TP18, TP24, TP25, TP26, TP27, TP28	Test Point, Miniature, Red, TH	Keystone	5000	13
TP10, TP11, TP12, TP13, TP15, TP16	Test Point, Miniature, Black, TH	Keystone	5001	6
U1, U8	Single Output LDO, 1.5 A, Adjustable 0.8 to 3.6V Output, 0.8 to 5.5V input, with Programmable Soft Start, 10-pin SON (DRC), -40°C to 105°C, Green (RoHS and no Sb/Br)	Texas Instruments	TPS74801TDRCRQ1	2
U2	4-Output PCIe Gen 1-6 Compliant Low jitter General Purpose BAW Clock Generator, QFN24	Texas Instruments	LMK3H2104QFN	1
U3	Dual Bidirectional Multi-Voltage Level Translator, DCU0008A (VSSOP-8)	Texas Instruments	LSF0102DCUR	1
U4	150mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	Texas Instruments	LP5900SD-3.3/NOPB	1
U5	4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	Texas Instruments	TPD4E004DRYR	1

Designator	Description	Manufacturer	Part Number	Quantity
U6	25MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40°C to 85°C, 80-pin QFP (PN), Green (RoHS and no Sb/Br)	Texas Instruments	MSP430F5529IPN	1
U7	Automotive 4-Bit BidirectionalVoltage-Level Translator with Auto Direction Sensing and ±15kV ESD, RUT0012A (UQFN-12)	Texas Instruments	TXB0104QRUTRQ1	1
Y1	Crystal, 24.000MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1
Y2	Low Jitter, High-Performance BAW Oscillator, 156.25MHz, 100MHz	Texas Instruments	LMK6HA10000ADLFR	1
C55, C56, C57, C58, C59, C60, C61, C62	CAP, CERM, 3 pF, 50V, ±5%, C0G/NP0, 0402	MuRata	GRM1555C1H3R0CA01D	0
FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
R18, R27, R29, R38, R39, R42, R43, R45, R51, R52, R88, R90, R93, R94, R103, R106, R108, R111, R112, R113, R115, R125, R127, R128, R129, R130, R131, R135	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	0
R20, R21	RES, 0, 5%, 0.25W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW12060000Z0EA	0
R23	RES, 100, 1%, 0.063W, AEC-Q200 Grade 0, 0402	Stackpole Electronics Inc	RMCF0402JT100R	0
R76, R77, R78, R79, R122, R124	RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	0
R87, R89, R99, R100, R105, R107, R117, R118	RES, 49.9, 1%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349R9FKEA	0
R121, R123	RES, 10 k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060310K0JNEA	0

6 Additional Information

6.1 Trademarks

All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

For details regarding implementation of all device behaviors, refer to the LMK3H2104 data sheet or the descriptions available by hovering over a field in TICS Pro 2.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (August 2025)	Page
• Added Bill of Materials (BOM)	25

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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