EVM User's Guide: LMX1205MSEVM

LMX1205 Multisite Evaluation Module

Description

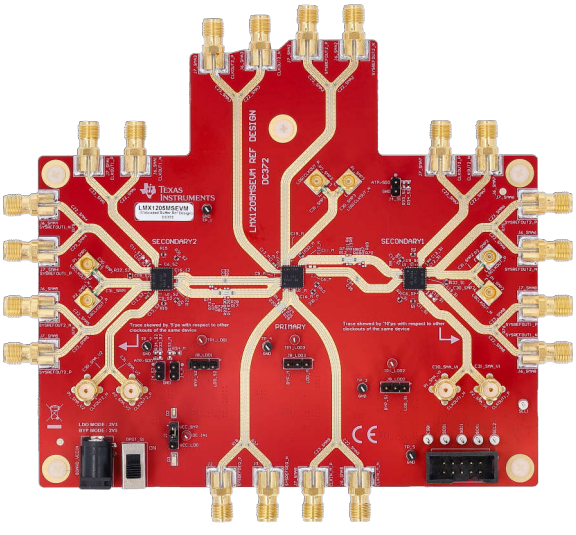
The LMX1205 multisite evaluation module (EVM) is designed to evaluate the cascaded performance of the LMX1205. The LMX1205 is a four-output, ultra-low, additive jitter radio-frequency (RF) buffer, divider and multiplier. The device buffers RF frequencies up to 12.8GHz, multiplies RF outputs from 6.4GHz up to 12.8GHz, and divides outputs by up to 12.8GHz. This board consists of three LMX1205 devices (one primary device that drives two secondary devices) and vertical header to connect IDC cable for USB2ANY interface. The multisite board also emphasizes features such as a multipart clock synchronization using *sync*, programmable delay, device-to-device SYSREF interface (single/differential ended, DC/AC coupled mode). Maximum device performance is extractable from the two secondary devices, the output of primary LMX1205 drives the clock and SYSREF inputs.

Features

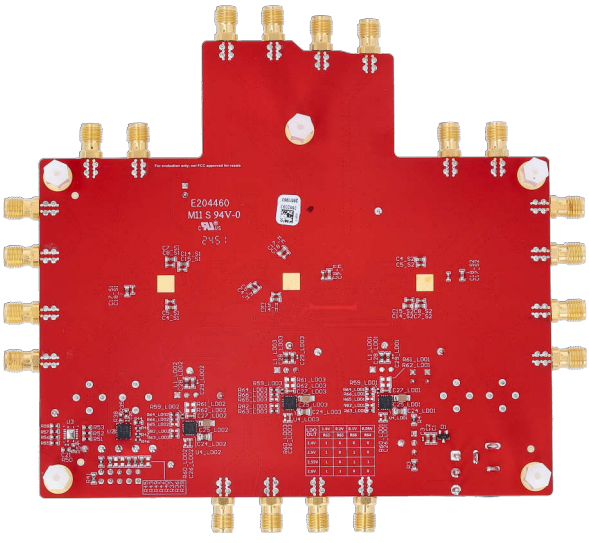
- 10MHz to 12.8GHz output frequency
- 4 high-frequency clocks with corresponding SYSREF outputs
  - Shared divide by 2, 3, 4, 5, 6, 7, and 8
  - Shared multiply by 2, 3, 4, 5, 6, 7, and 8
- Adjustable input delay up to 60ps with 1.1ps resolution
- Adjustable output delay up to 55ps with 0.9ps resolution
- 3.3V supply voltage (with onboard 2.5V LDOs for each device) or 2.5V supply voltage (with LDOs bypassed)
- –40°C to +85°C operating temperature

Applications

- Test and measurement:
  - Oscilloscope
  - Wireless equipment testers
  - Wideband digitizer
- Aerospace and defense:
  - Radar – electronic warfare
  - Seeker front end
  - Phased array antenna/beam forming
- General purpose:
  - Data converter clocking
  - Clock buffer distribution and division



LMX1205MSEVM PCB



LMX1205MSEVM (Bottom)

1 Evaluation Module Overview

1.1 Introduction

The LMX1205 is an ultra-low additive-jitter RF buffer, divider, and multiplier, with integrated SYSREF generation capability. Use a separate auxiliary clock divider with large divider values called logic clock for FPGAs or other logic ICs. Each RF output is paired with a differential SYSREF output with picosecond-precision delay-tuning capability and is operable as a generator (with synchronization capability across multiple devices) or as a repeater. The EVM operates with a 3.3V supply voltage when the onboard low dropout (LDO) regulators are used. When the supply voltage is 2.5V, LDO bypass is possible. The EVM contains three LMX1205, three LDO regulators, and a vertical header connector for the USB2ANY connection.

1.2 Kit Contents

Included within each evaluation kit is:

- One LMX1205 Multisite EVM board (DC372)
- USB2ANY controller
- One USB cable and IDC cable

1.3 Specifications

Parameter	Value	Conditions	
Supply voltage	3.0 to 3.4V	Onboard LDOs output are 2.5V	
	2.5V	Onboard LDOs are bypassed	
Supply current	3.9A maximum (1.9A maximum per device)	Various configurations	
CLKIN input frequency	10MHz to 12.8GHz	Buffer Mode	
	10MHz to 12.8GHz	Divider Mode	
	3.2GHz to 6.4GHz	Multiplier Mode	CLK_DIV = × 2
	2.133GHz to 4.266GHz		CLK_DIV = × 3
	1.6GHz to 3.2GHz		CLK_DIV = × 4
	1.28GHz to 2.56GHz		CLK_DIV = × 5
	1.067GHz to 2.133GHz		CLK_DIV = × 6
	0.914GHz to 1.828GHz		CLK_DIV = × 7
	800MHz to 1.6GHz		CLK_DIV = × 8

1.4 Device Information

The wide frequency range and ultra low additive jitter of the LMX1205 can be used as a 1:4 fan-out buffer to clock multiple high precision and high frequency data converters. Each of the four high-frequency clock outputs and additional LOGICLK output with larger divider range is paired with a SYSREF output clock signal. The SYSREF signal for JESD interfaces are either internally generated or buffered in as an input and re-clocked to the device clocks. For data converter clocking applications, verify that the jitter of the clock is less than the aperture jitter of the data converter. In applications where more than four data converters are clocked, use multiple devices to distribute all the high-frequency clocks and SYSREF signals required to develop a multitude of cascading architectures. With low jitter and noise floor, LMX1205MSEVM combined with an ultra-low noise reference clock source is designed for clocking data converters, especially when sampling above 3GHz.

2 Hardware

2.1 Additional Images

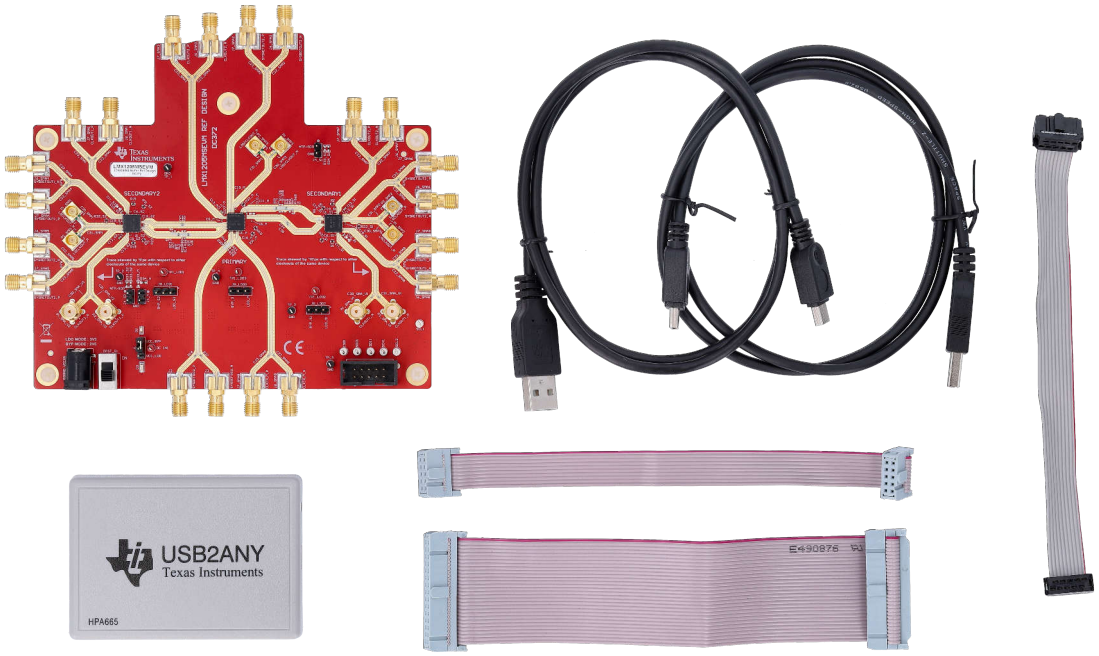


Figure 2-1. LMX1205MSEVM Box Contents

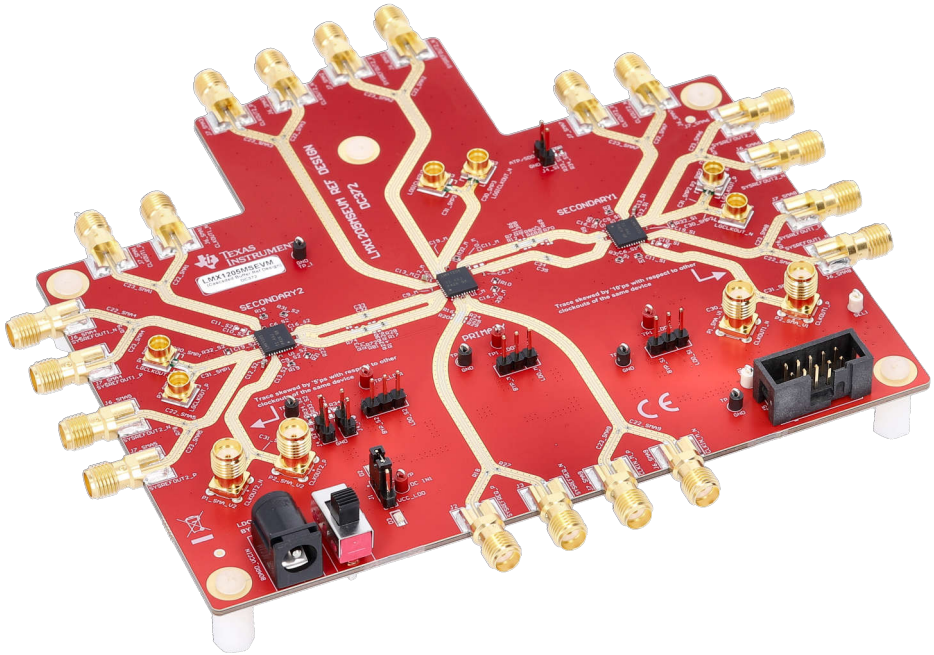


Figure 2-2. LMX1205MSEVM (Angled)

2.2 Jumper Information

Jumpers J8_LDO1, J8_LDO2, J8_LDO3, and J1 determine the supply voltage to the board. When using the onboard LDOs, set the jumpers to the *LDO* position. To bypass the LDOs, set these jumpers to the *BYP* position.

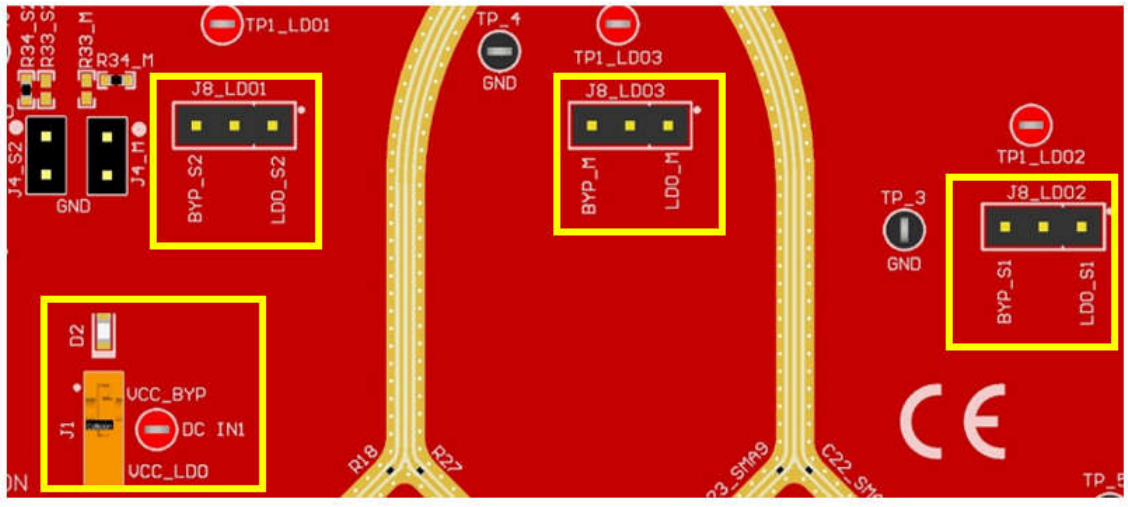


Figure 2-3. EVM Supply Jumper Configuration

2.3 Multiplier Lock Detect Jumper

Measure the clock multiplier lock status at the lock detect analog test point. To enable the lock detect test point jumpers, populate a 0Ω resistor at R33_M, R33_S1, and R33_S2.

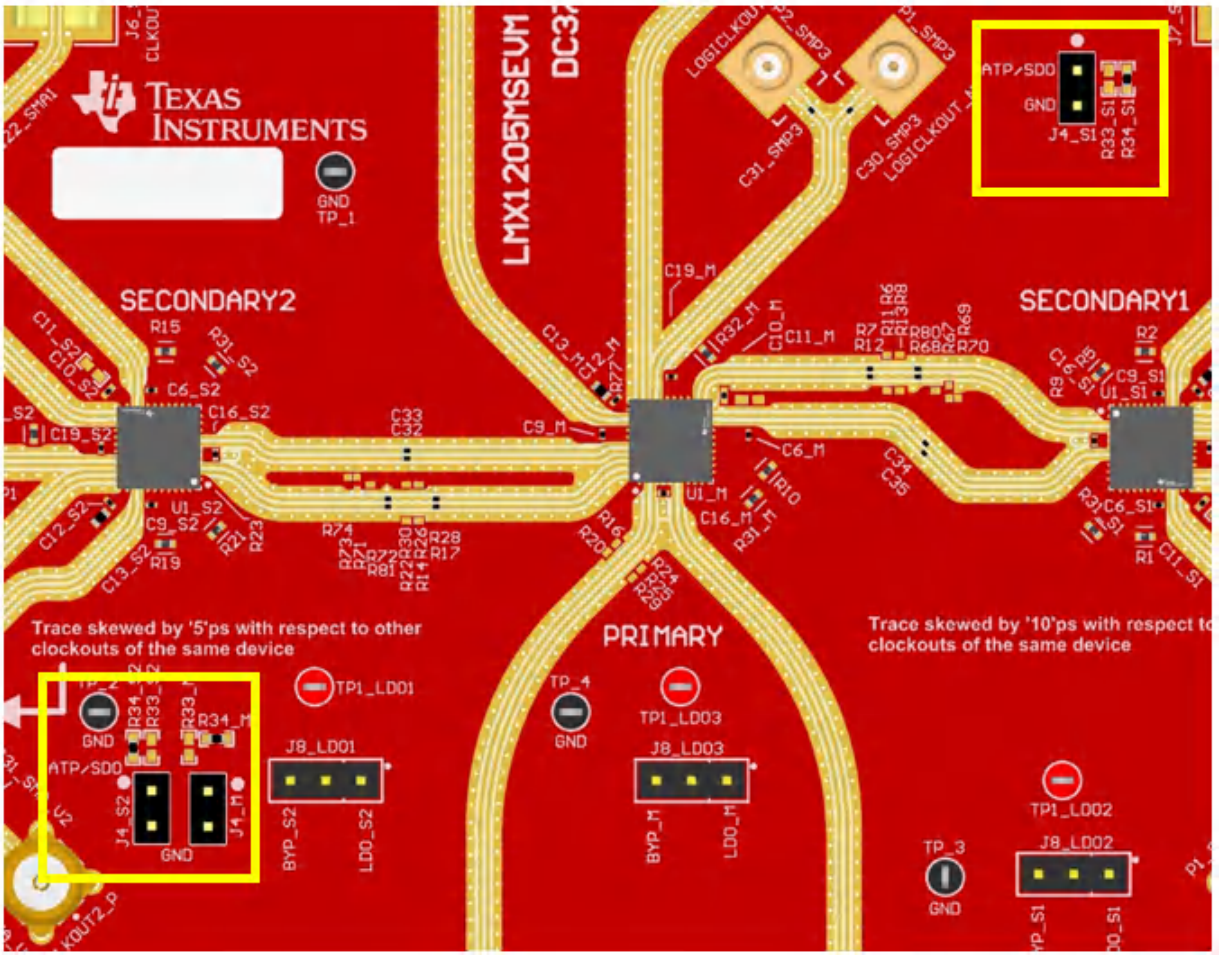


Figure 2-4. Multiplier Lock Detect Jumpers

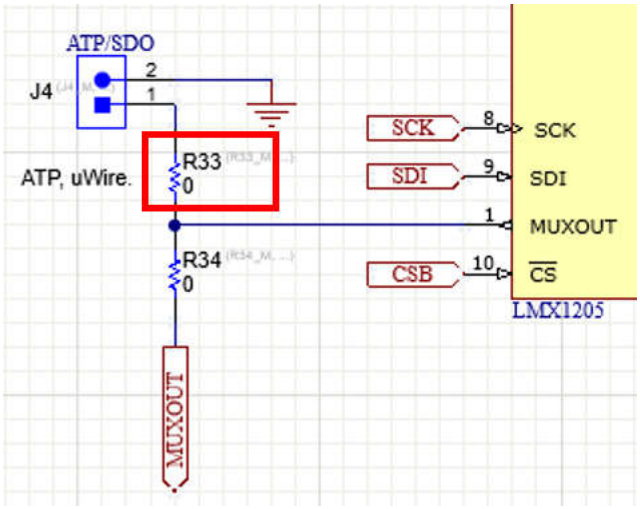


Figure 2-5. Jumper Resistor Network Configuration

2.4 Setup

2.4.1 Evaluation Setup Requirement

At a minimum, evaluation of the buffer mode for all three devices requires:

- A DC power supply capable of at least 3.3V, 5A (LDO mode) or 2.5V, 5A (bypass mode).
- A high-quality signal source, such as an SMA100B.
- A spectrum analyzer or phase noise analyzer.
- A PC running Windows 7 or a more recent version with *TICS Pro software* installed.

Full evaluation requires a high-speed four-channel oscilloscope with a minimum of 16GHz bandwidth capable of resolving 5ps step size for SYSREF delay tuning.

For driving the primary SYSREF input, use a 2-CH arbitrary function generator or other pulse source. The pulse source must be capable of outputting complementary LVDS pulses and 1.25V ± 0.2V differential into a 100Ω DC load DC levels. Alternatively, use the primary LMX1205 to trigger the SYSREF, SYNC the dividers, and determine SYSREF windowing values.

2.4.2 Connection Diagram

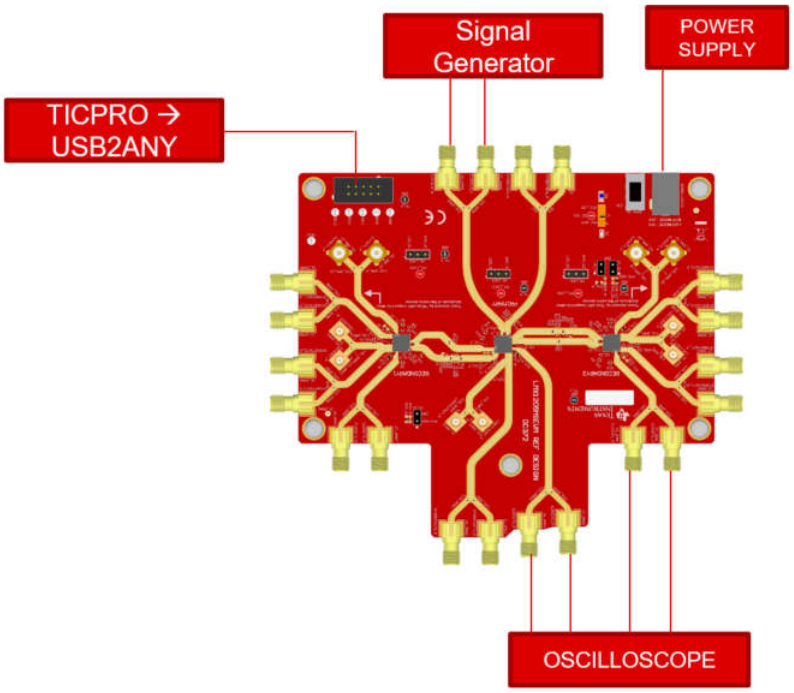


Figure 2-6. EVM Test Connections

2.5 Power Requirements

When using the onboard LDOs, apply 3.3V to the BOARD_VCCIN DC jack connector. The appropriate supply voltage range is 3.0V to 3.4V. Verify that the supply voltage is at least 500mV above 2.5V. The quiescent (I_Q) current of LDOs are approximately 5mA. If the LDO regulators are bypassed, apply 2.5V to the BOARD_VCCIN DC jack connector; account for IR drops.

The board draws a maximum 3.9A during operation. Enabling or disabling system functions and secondary devices can reduce the board current consumption, reducing the junction temperature of the device and reducing the board temperature.

2.6 Reference Clock

Connect the CLKINP SMA connector to a high-quality signal source, such as a SMA100B signal generator. Set the output power of the signal generator to 10dBm. Both CLKIN inputs terminate internally with 50Ω to AC-GND

which is formed by an internal capacitor, so no external termination is required. To drive input differentially, connect both CLKINP and CLKINN SMA connectors to a balun or differential clock source.

The default EVM profile configures the device in buffer mode. The input frequency is modifiable per the operating range of each functional element. This EVM setup guide and related plots assume 3200MHz input at CLKIN for buffer mode.

To evaluate SYSREF repeater and re-timer mode, connect the SYSREF input SMAs to a differential output source, such as an arbitrary function generator. The primary LMX1205 device drives the primary device or the secondary device SYSREF input. The primary LMX1205 device SYSREF is configured in SPI mode or Generation mode.

If the primary devices SYSREF input is driven using an arbitrary function generator, the EVM connections for the SYSREF input are DC-coupled and provide internal 100Ω termination. In DC-coupled mode, the common mode bias on the SYSREFREQ pins must be between 1V and 2V. A standard LVDS output buffer fulfills the input common mode requirements.

Configure the SYSREF output of the primary device and the SYSREF request input of the secondary device so that the interface termination is compatible. The SYSREF interface termination is differential ended, single ended, and AC/DC coupled. The common mode of the generated output SYSREF is set by the primary device.

Evaluate SYNC mode and SYSREF windowing in the secondary device. The primary device is configured either in SYNC or SYSREF Generation Mode and is fed to the secondary devices where the user can perform windowing and clock synchronization.

2.7 Output Connections

Only selected CLKOUT, SYSREFOUT, LOGICLKOUT channels are exposed from primary and secondary device.

Table 2-1. Clock and SYSREF Signals for Primary and Secondary Devices

SITE	OUTPUTS	COMMENTS
PRIMARY	CLKOUT0	TERMINATED
	CLKOUT1	*INPUT TO SECONDARY 1*
	CLKOUT2	**EDGE SMA**
	CLKOUT3	*INPUT TO SECONDARY 2*
	SYSREFOUT0	TERMINATED
	SYSREFOUT1	*INPUT TO SECONDARY 1*
	SYSREFOUT2	**EDGE SMA**
	SYSREFOUT3	*INPUT TO SECONDARY 2*
	LOGICLK	**VERTICAL SMP**
	LOGISYSREF	TERMINATED
SECONDARY 1	CLKOUT0	TERMINATED
	CLKOUT1	**VERTICAL SMA**
	CLKOUT2	**EDGE SMA**
	CLKOUT3	TERMINATED
	SYSREFOUT0	TERMINATED
	SYSREFOUT1	**EDGE SMA**
	SYSREFOUT2	**EDGE SMA**
	SYSREFOUT3	TERMINATED
	LOGICLK	**VERTICAL SMP**
	LOGISYSREF	TERMINATED

Table 2-1. Clock and SYSREF Signals for Primary and Secondary Devices (continued)

SITE	OUTPUTS	COMMENTS
SECONDARY 2	CLKOUT0	TERMINATED
	CLKOUT1	**EDGE SMA**
	CLKOUT2	**VERTICAL SMA**
	CLKOUT3	TERMINATED
	SYSREFOUT0	TERMINATED
	SYSREFOUT1	**EDGE SMA**
	SYSREFOUT2	**EDGE SMA**
	SYSREFOUT3	TERMINATED
	LOGICLK	**VERTICAL SMP**
	LOGISYSREF	TERMINATED

TERMINATED – terminated differentially on board with a 100ohm resistor, the clock path is not measurable.

All exposed output connections are AC-coupled with wideband caps and connect directly to RF instruments. An additional DC block is not required for the connection. Terminate the unused CLKOUT SMA connector with a 50Ω load. If a balun with the best frequency range is available, use a differential connection. Because LOGICCLK outputs are also AC-coupled, only LVDS output formats have been evaluated.

2.8 Test Points

Table 2-2. SPI Signal Test Points

TEST POINT NAME	SIGNAL
CSB1	CSB
SDO1	SDO
SDI1	SDI
SCK1	SCK
SEL1	SEL0
SEL2	SEL1

Table 2-3. Supply and Ground Test Points

TEST POINT NAME	SIGNAL
TP1, TP2, TP3, TP4	GND
DC IN1	Voltage from external power supply
TP1_LDO1	Voltage out of the onboard LDO1
	(DC IN1 = TP1_LDO1 in bypass mode)
TP1_LDO2	Voltage out of the onboard LDO2
	(DC IN1 = TP1_LDO2 in bypass mode)
TP1_LDO3	Voltage out of the onboard LDO3
	(DC IN1 = TP1_LDO3 in bypass mode)

3 Software

3.1 Software Description

Texas Instruments Clocks and Synthesizers (TICS) Pro software is used to program this evaluation module (EVM) through the on-board USB2ANY interface.

3.2 Software Installation

Download and install TICS Pro software from the TICSPRO-SW tool folder.

3.3 USB2ANY Interface

The on-board USB2ANY interface provides a bridge between TICS Pro software and the LMX1205 device. When the on-board USB2ANY controller is first connected to a PC, or if the firmware revision for the controller does not match with the version used by TICS Pro, a firmware update to the controller is required.

1. Connect the USB cable from the PC to the EVM. The USB interface provides the necessary power to enable the on-board USB2ANY controller.
2. Set up a USB device using Windows. Run TICS Pro on the PC.
3. Figure 3-1 shows the next screen.

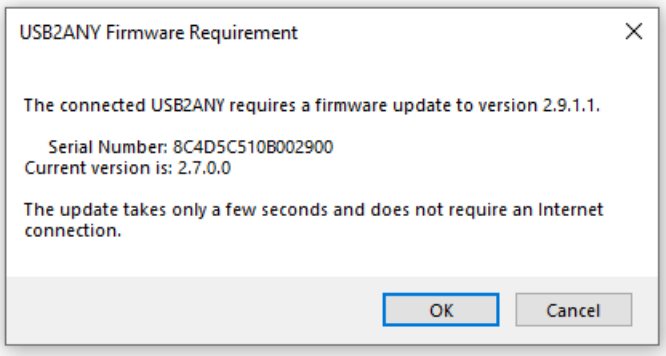


Figure 3-1. Firmware Update Request

4. Select *OK*, then the screen appears as the figure below. Select *Update Firmware*.

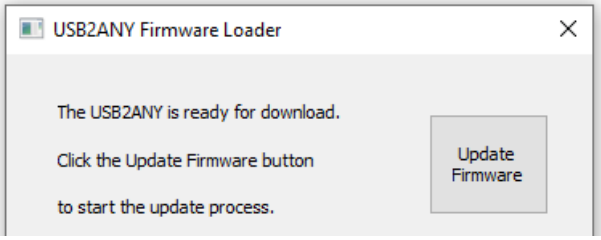


Figure 3-2. Firmware Loader

5. The following figure shows the next screen. Select the *Close* button to close the window.

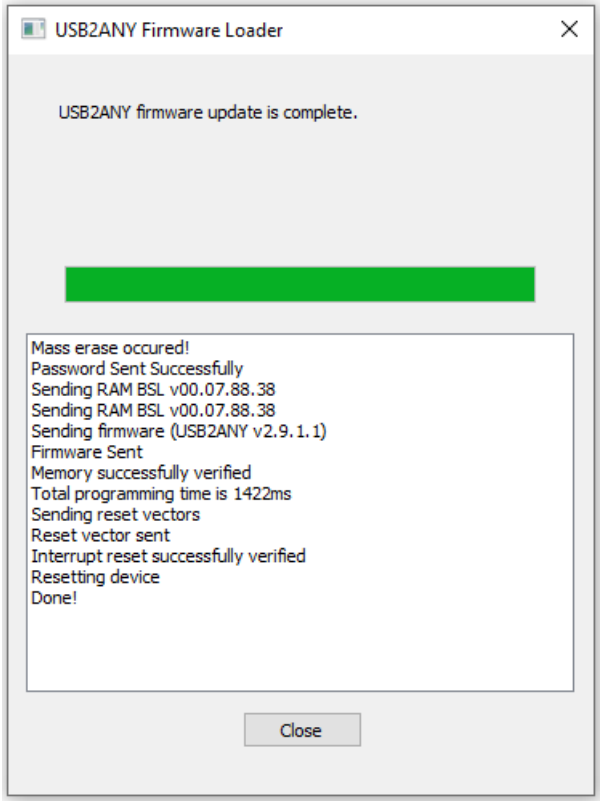


Figure 3-3. Firmware Update Complete

6. A TICS Pro default device appears. Verify a green light on Connection Mode at the bottom of the GUI.

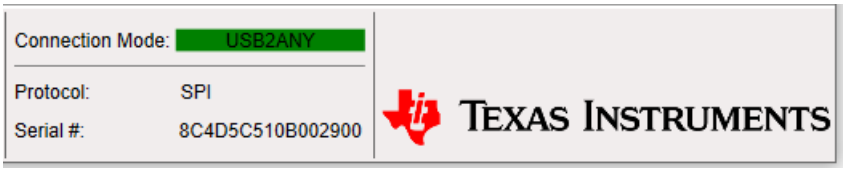


Figure 3-4. Connection Mode

7. Navigate to the menu bar, select *USB Communications*, then select *Interface*.

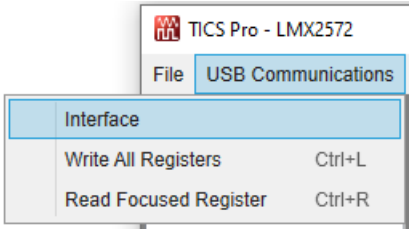


Figure 3-5. USB Communications

8. Select the *Identify* button, the LED in the USB2ANY interface flashes.

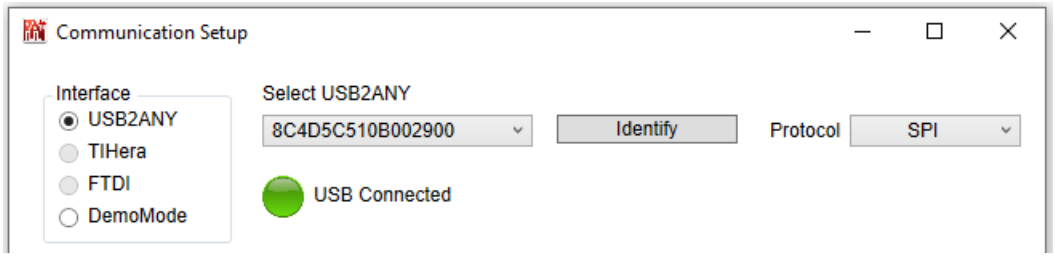


Figure 3-6. Identify USB2ANY Controller

9. Now, the USB2ANY is ready to use. Select the *Close* button to close the window.

4 Implementation Results

4.1 Buffer Mode

After a POR or soft reset, LMX1205 powers up is buffer mode, and all outputs are enabled with maximum output power. LOGICLK is also enabled in this mode, with a fixed divider value of 64. All SYSREF clocks are disabled. To evaluate the device in a different configuration, use TICS Pro.

To specify the device, select the *MultisiteBoard* page, then select the device from the *Select Device* drop down menu.

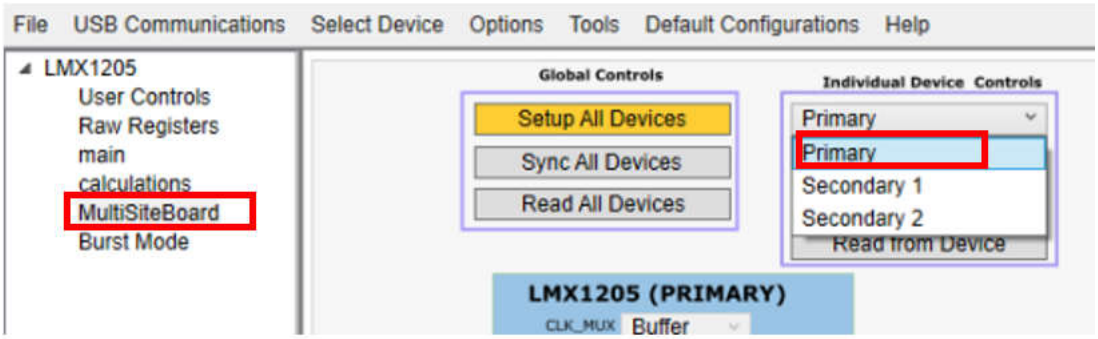


Figure 4-1. Software Configuration for Device Selection

From the top-menu, select *Default Configuration* and then select *Buffer Mode*. The *Buffer Mode* selection automatically loads the buffer mode profile.

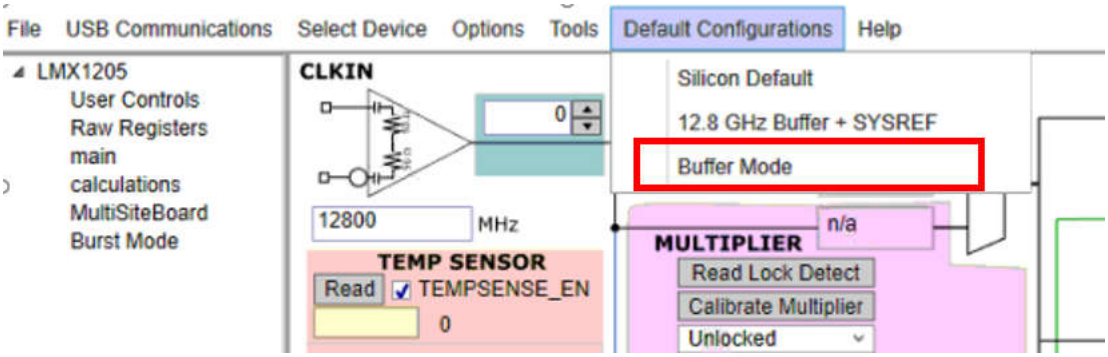


Figure 4-2. Software Configuration to set the Buffer Mode

If termination is not applied on all output pins, manually disable the unused outputs. Use the CHx_EN fields to completely power down unused channels or the CLKOUTx_EN fields to only power down output buffers. Powering down unused channels reduces current consumption.

Load the profile and make and required changes. Select *USB Communications* then select *Write All Registers* to program the device.

In the figures below, the yellow trace is the 1GHz source clock from Crystek RedBox Source CRBSCS-01-1000.000. The green and orange traces are the clockouts from primary, secondary1 and secondary2.

The figures below show that the magnitude of additive far-off noise from the LMX1205 is very low, approximately −163dBc/Hz.

Figure 4-3 shows:

- Source noise
- Source and primary DUT noise
- Source, primary DUT, and secondary2 DUT noise (edge SMA)
- Source, primary DUT, and secondary1 DUT noise (vertical SMA)

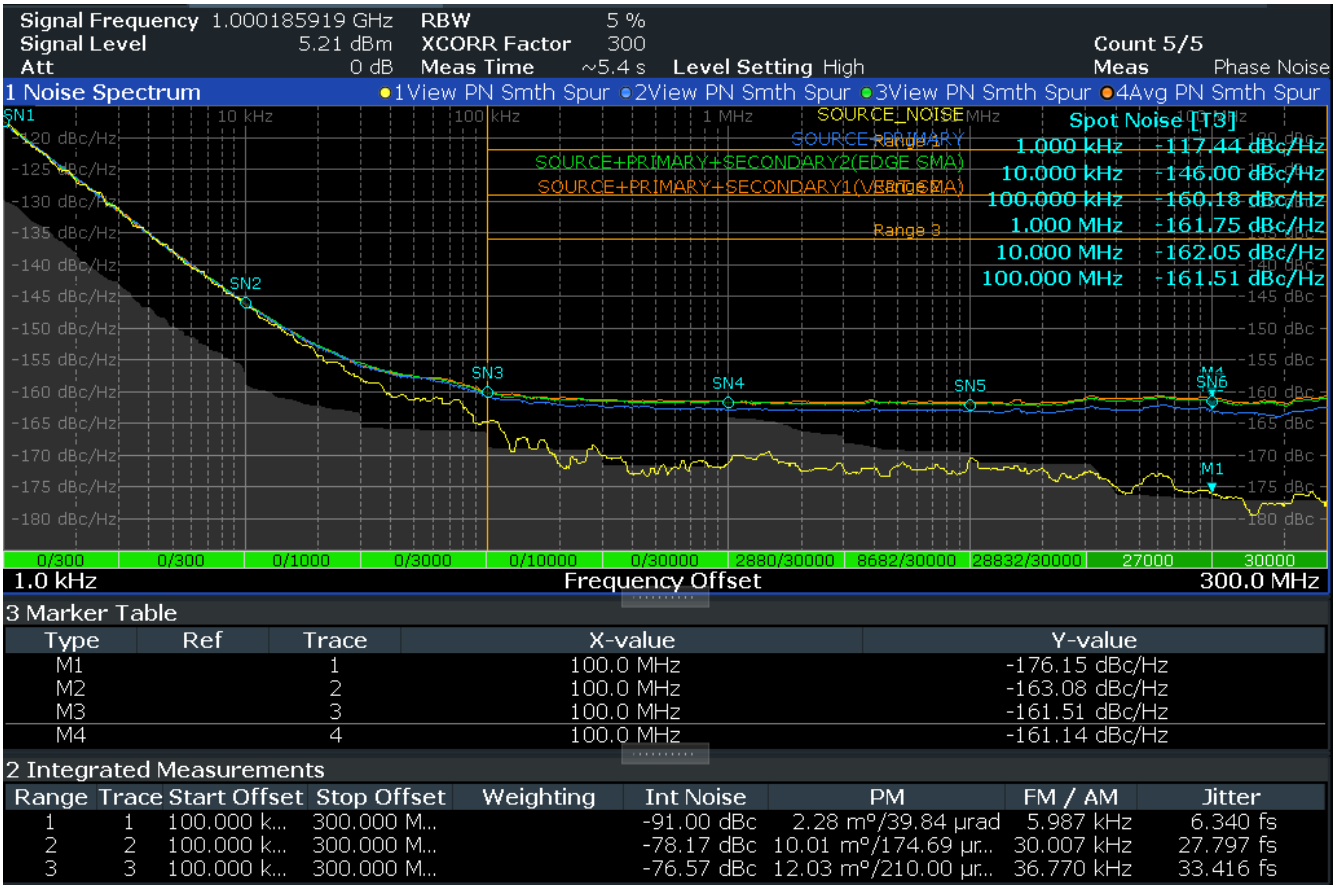


Figure 4-3. Phase Noise in Buffer Mode

4.2 Multiplier and Divider Modes

The LMX1205 contains a cascaded topology and facilitates the ability to adjust different multiply and divider values for custom frequencies within required operating frequency ranges.

Use the following steps to set the LMX1205 to divider mode:

1. Select CLK_MUX = Divide.
2. Select CLK_DIV to the appropriate divider value for respective CLKIN frequency.

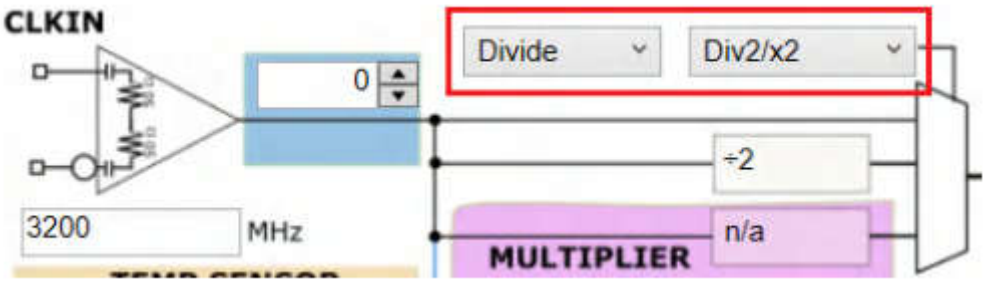


Figure 4-4. Software Configuration for Divider Mode

Use the following steps to set the LMX1205 to multiplier mode:

1. Select CLK_MUX = Multiply.
2. Select CLK_DIV to the appropriate multiplier value for respective CLKIN frequency.
3. Select the Calibrate Multiplier button.

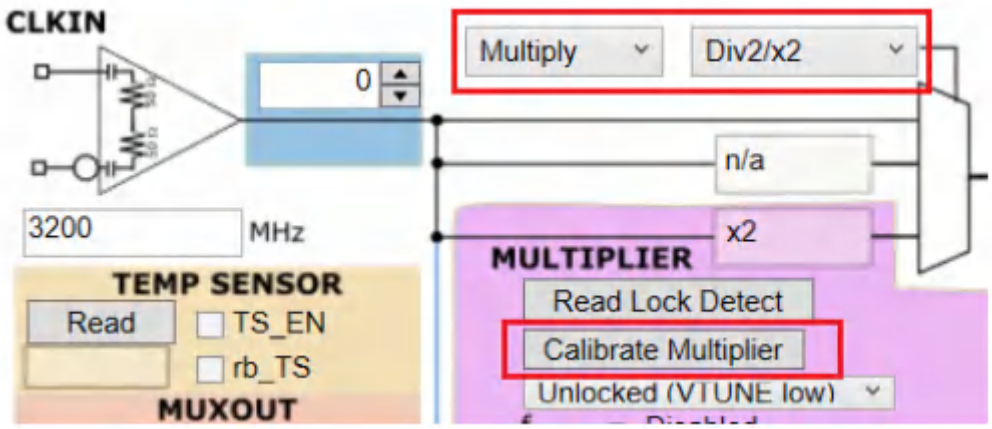


Figure 4-5. Software Configuration for Multiplier Mode

In Figure 4-6, the primary device is set in multiplier mode (× 8), the secondary device is set in divider mode (÷ 4), and the reference clock to primary is 1GHz.

Figure 4-6. Phase Noise Plots for Multiplier Mode (× 8), 1GHz Reference, and (÷ 4) Divider Mode

In Figure 4-7, the primary device is set in divider mode (÷ 3), the secondary device is set in multiplier mode (× 7), and the reference clock to primary is 3GHz.

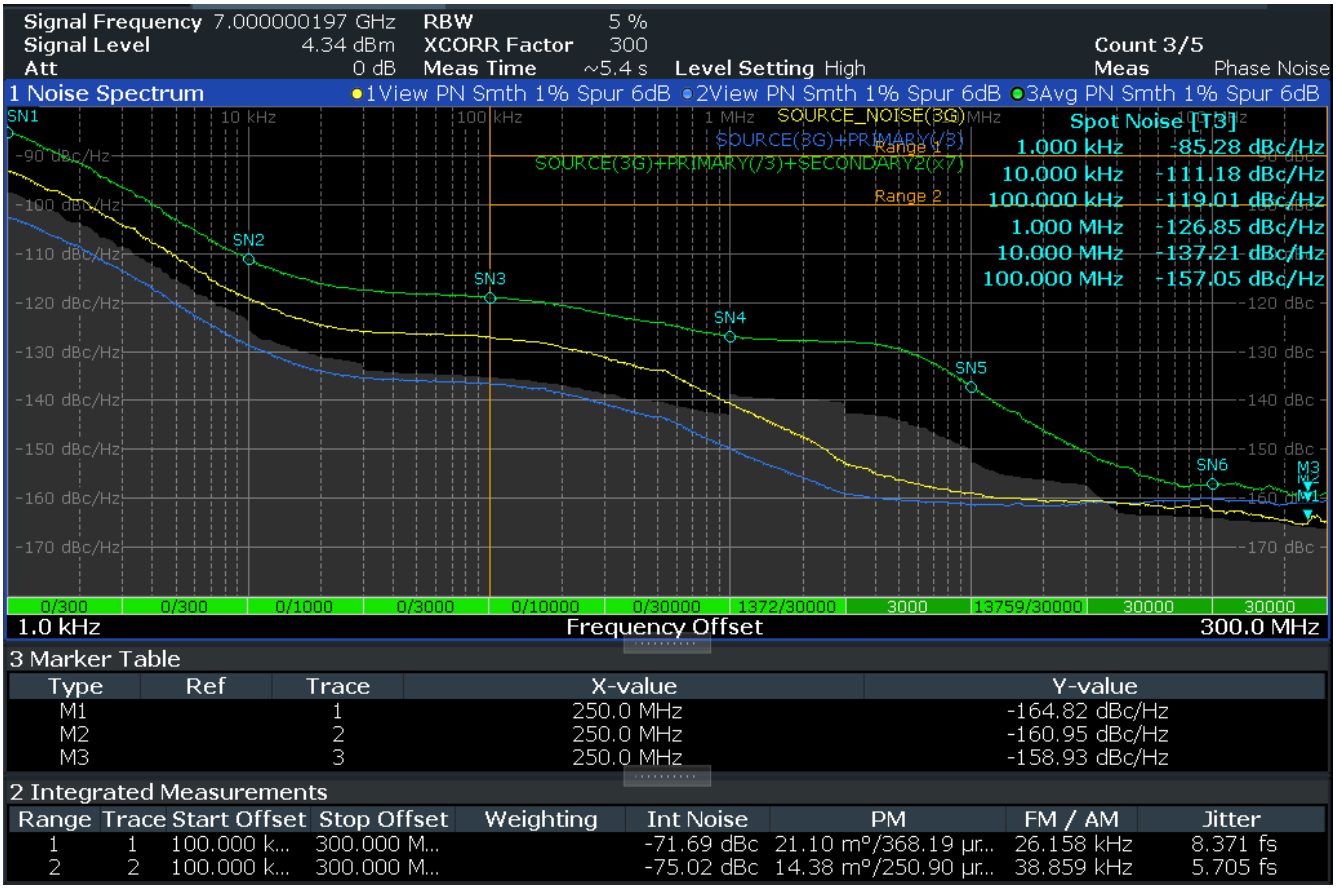


Figure 4-7. Phase Noise Plots for Reference at 3GHz, (÷ 3) Divider mode, and Multiplier Mode (× 7)

Figure 4-6 and Figure 4-7 demonstrate that the LMX1205 synthesizes any frequency in a cascaded clock tree using multiplier and divider modes. The LMX1205 complies with the operating range of frequencies for the device.

4.3 Logic Clock

Figure 4-8 shows that the logic clock is enabled by default in the LVDS output format.

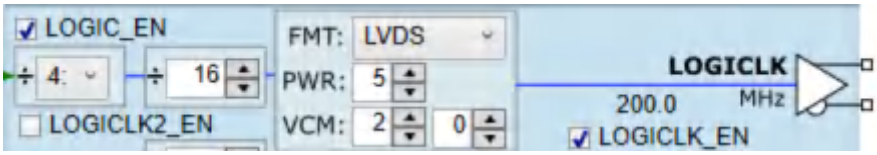


Figure 4-8. Software Configuration to select Logic Clock

Figure 4-9 shows an input clock frequency of 2GHz. The dividers operate in default settings to generate 31.25MHz at the logic clock output.

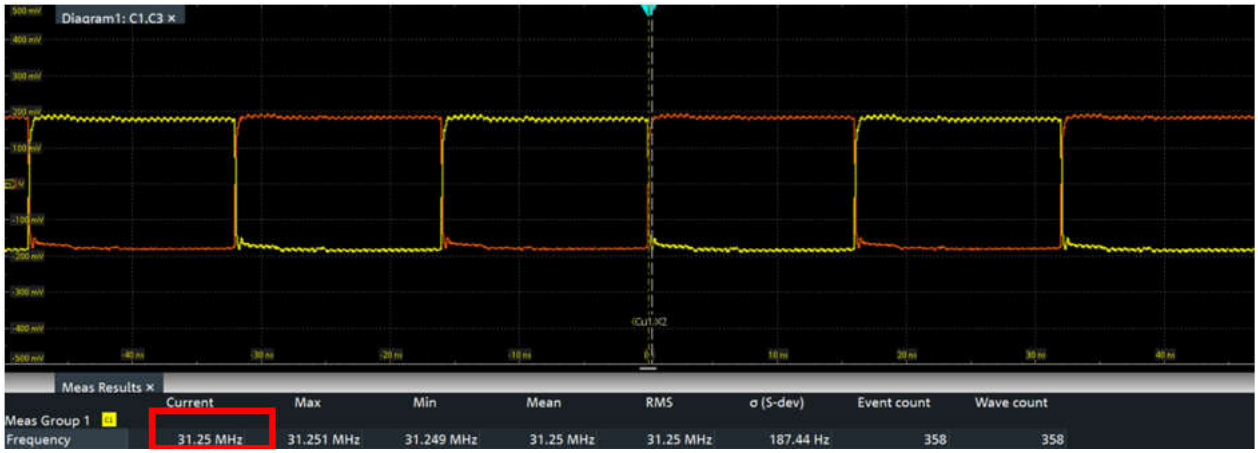


Figure 4-9. Output Waveform of Logic Clock

4.4 Programmable Delay

The input and output path clock have individually programmable delays. The clock signal delay is up to 60ps, with 1.1ps resolution per code from the input path and 55ps with 0.9ps resolution per code at the output path. To highlight the feature, skew an output clock (CLKOUT1) channel trace by approximately 10ps in secondary1 device with respect to CLKOUT2 of the same device. CLKOUT2 of secondary 2 device is skewed by approximately 5ps with respect to CLKOUT1 of the same device. The secondary 2 device skew allows the user to validate the programmable delay feature offered by the device.

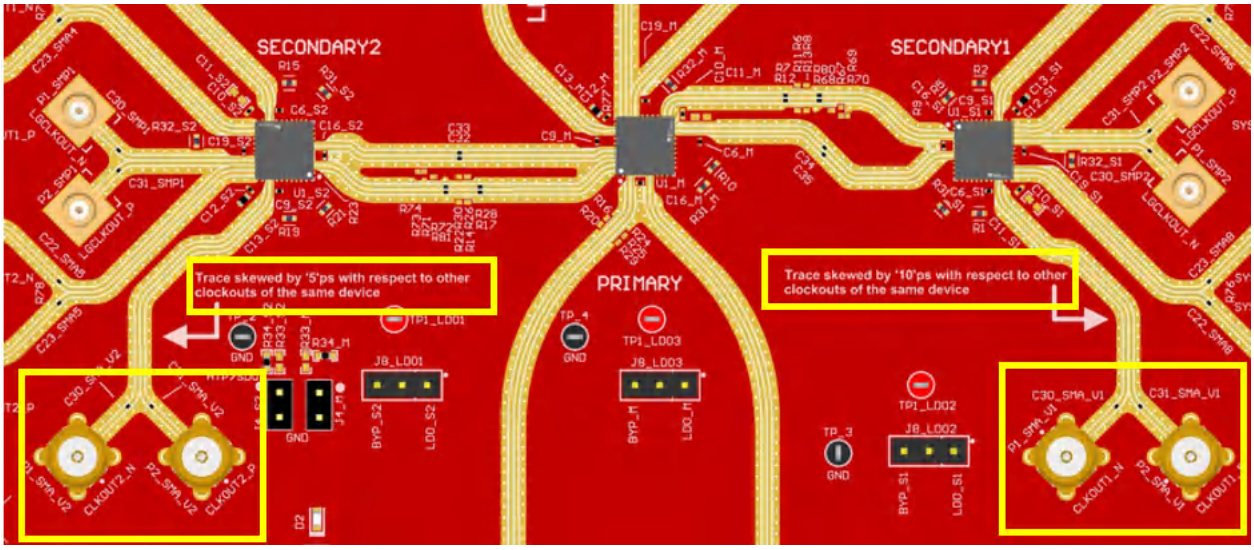


Figure 4-10. Clock Out Path with Trace Length Skewed

Figure 4-11 shows the waveform plot of the secondary1 device. Figure 4-11 shows a 10.8ps skew from other channels.

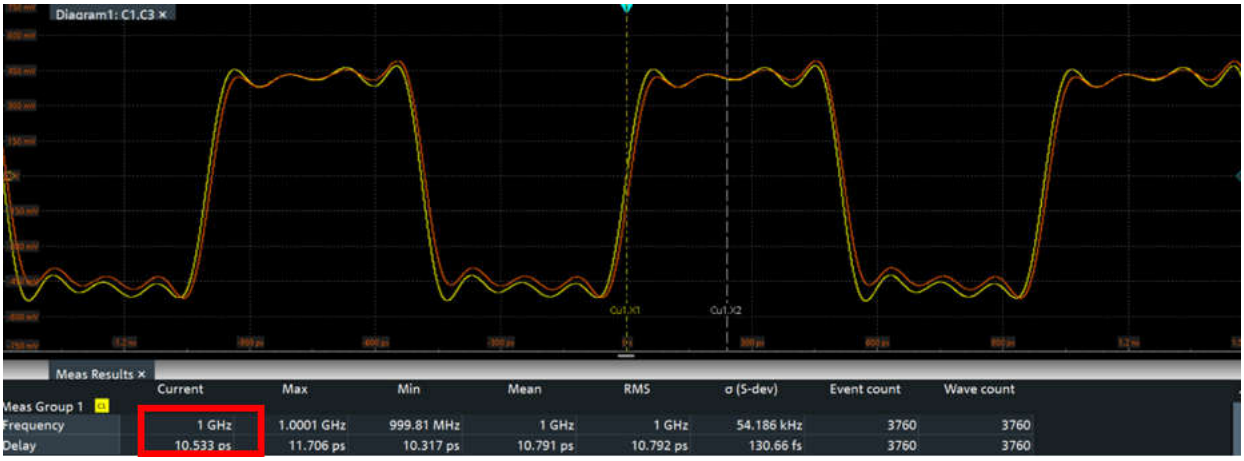


Figure 4-11. Channel to Channel Skew of Clock Path with Trace length mismatch

To skew the waveform:

1. Select the device.
2. Select the *MultisiteBoard* page.
3. Select the *Select Device* drop-down menu.
4. Select the device.

Figure 4-12. Software Configuration for Device Selection

5. Navigate to *device selected*.
6. Identify the trace that is skewed on the board, adjust the delay of the skewed trace channel.

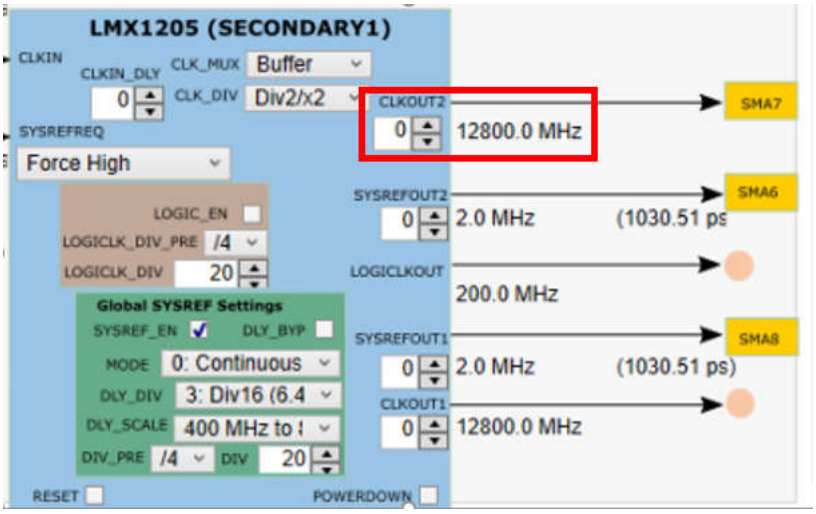


Figure 4-13. Software Configuration for changing Clock Path Output Delay

Figure 4-14 shows the waveform after adjusting the output delay so that the channel-to-channel skew is < 1ps.

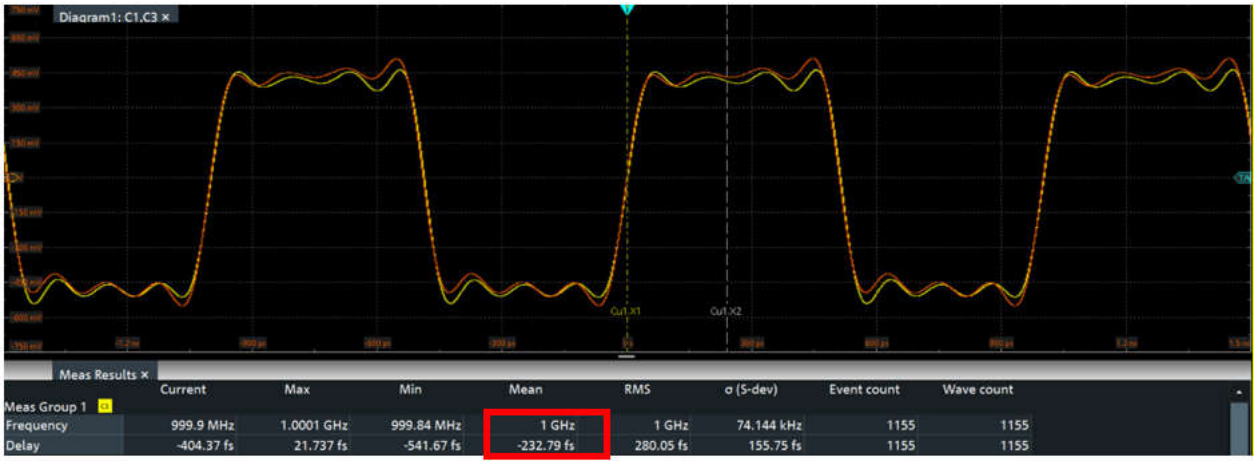


Figure 4-14. Channel to Channel Skew After Adjusting the Output Delay of the Clock Path

The programmable delay feature of the device has wide range of applications. One application of the delay features is to calibrate and adjust the output delays of clock path to align all clock output edges in a large phased array cascaded clock tree. Another application is to offset a mismatch in:

- Trace lengths
- PCB interconnects
- Cables
- Channel to Channel skew

The delay features also uses windowing to align the SYSREF edges to the clock falling edge.

5 Hardware Design Files

5.1 Schematics

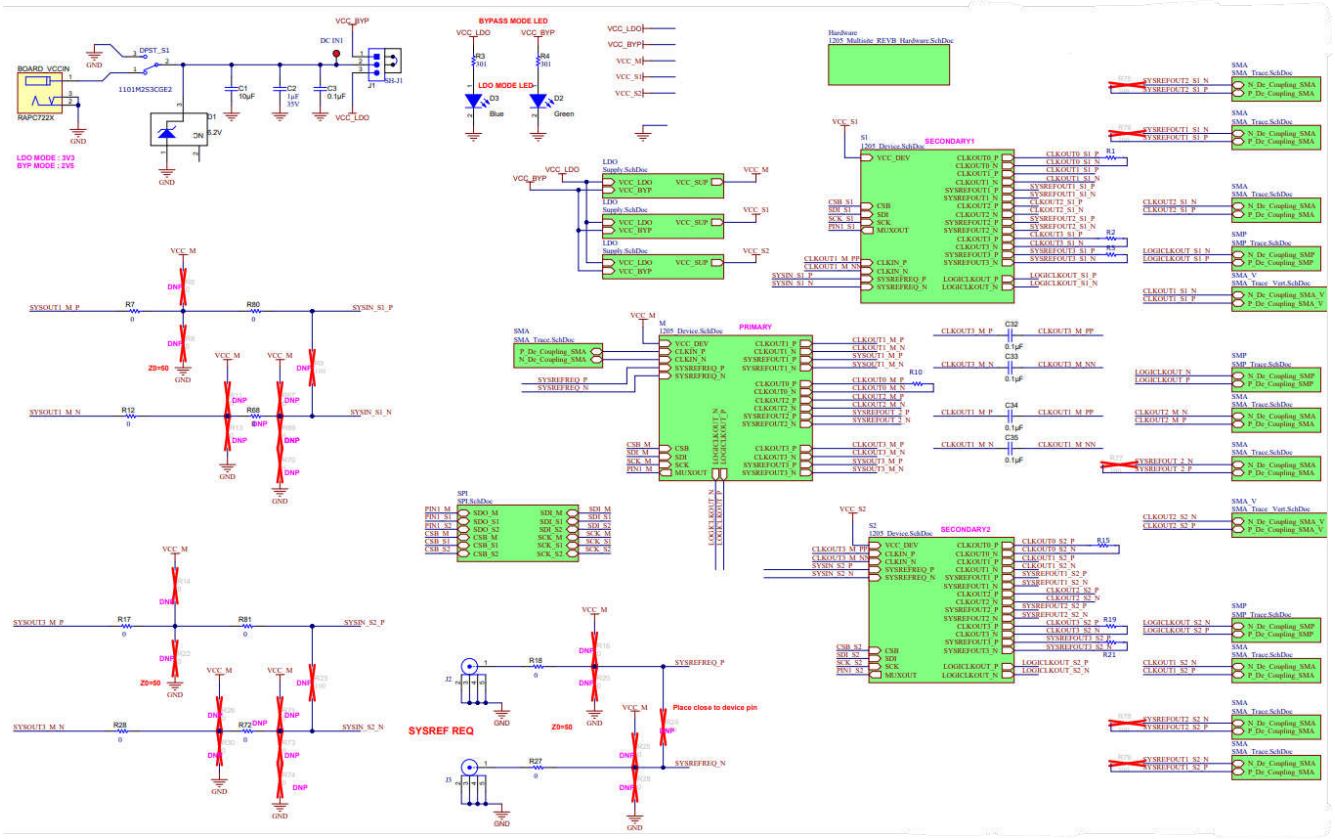


Figure 5-1. LMX1205 Multisite EVM Schematic

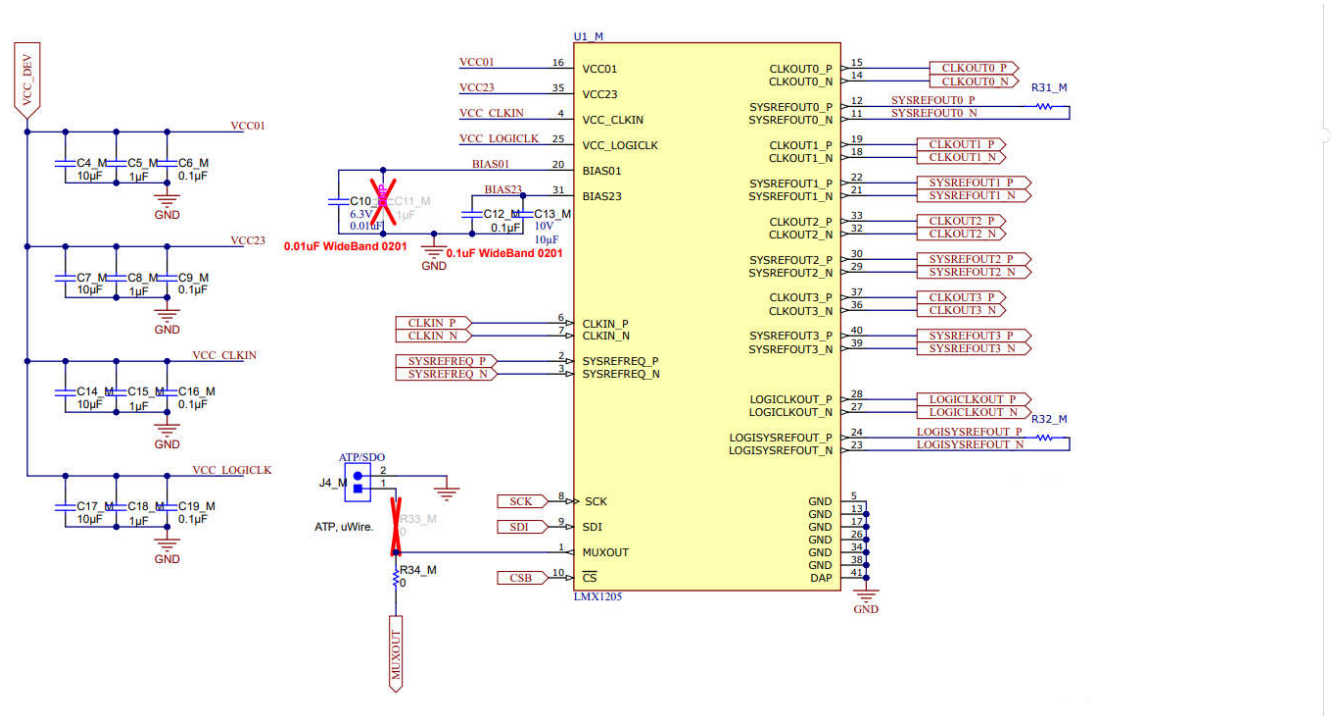


Figure 5-2. Main Device Schematic for Primary and Secondary

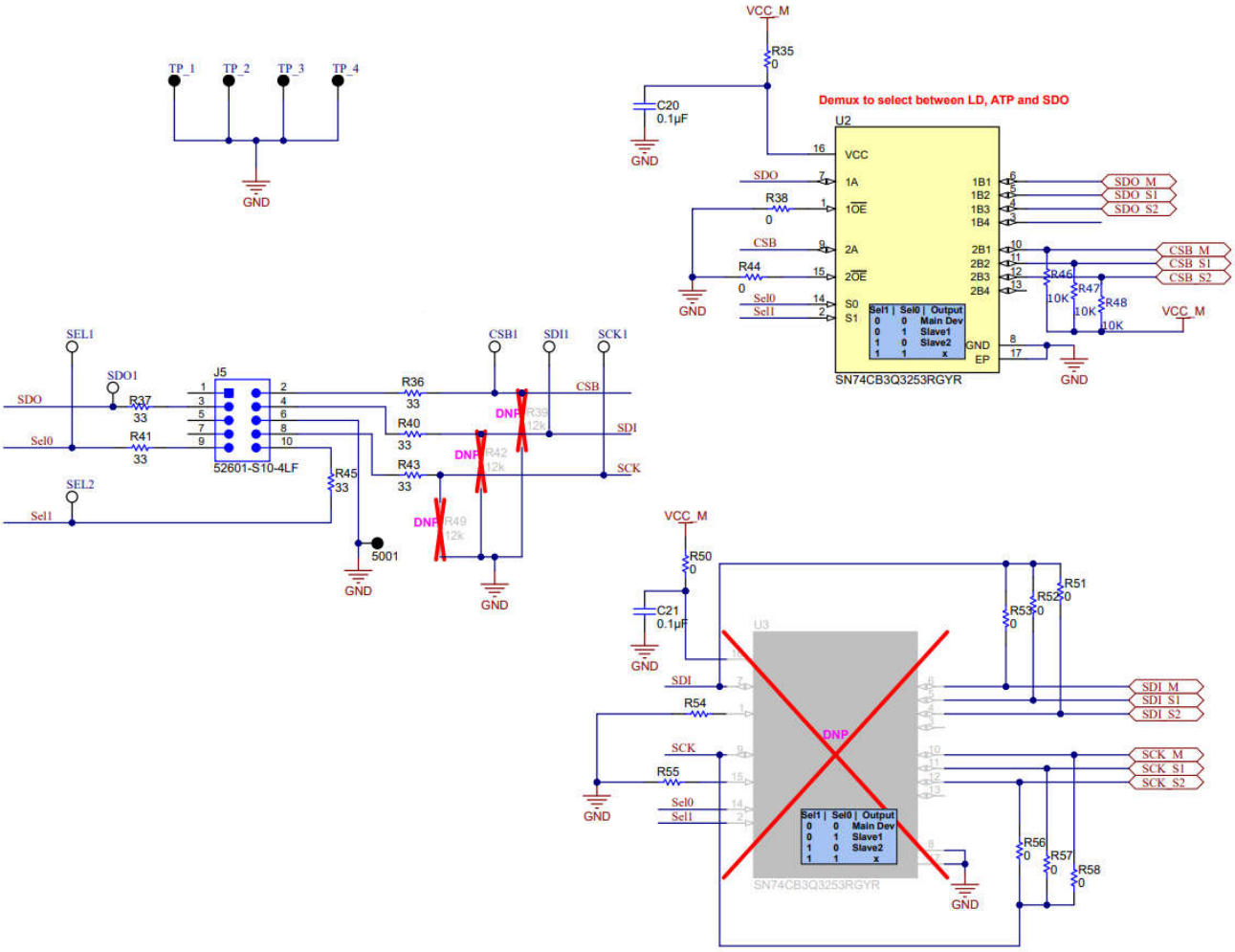
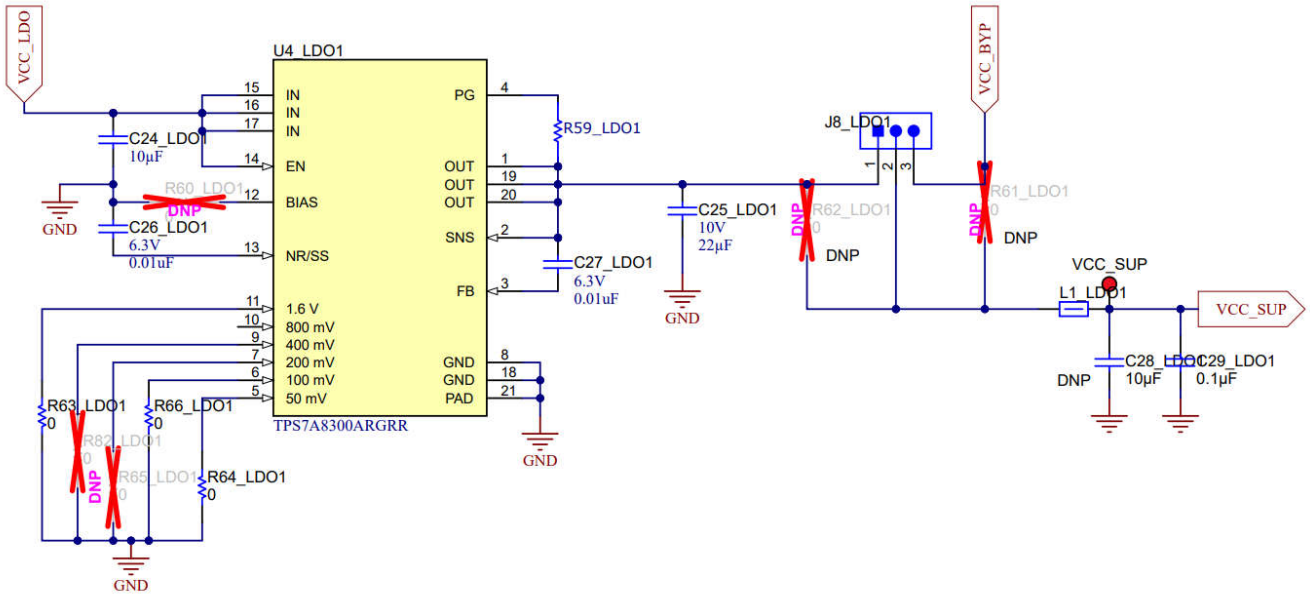


Figure 5-3. SPI Lines



LDO OUT	1.6V	0.4V	0.2V	0.1V	0.05V
	R63	R82	R65	R66	R64
2.4V	1	X	X	X	X
2.5V	1	X	X	1	X
2.55V	1	X	X	1	1
2.6V	1	X	1	X	X
2.7V	1	X	1	1	X
2.8V	1	1	X	X	X

Figure 5-4. Device Supply LDO

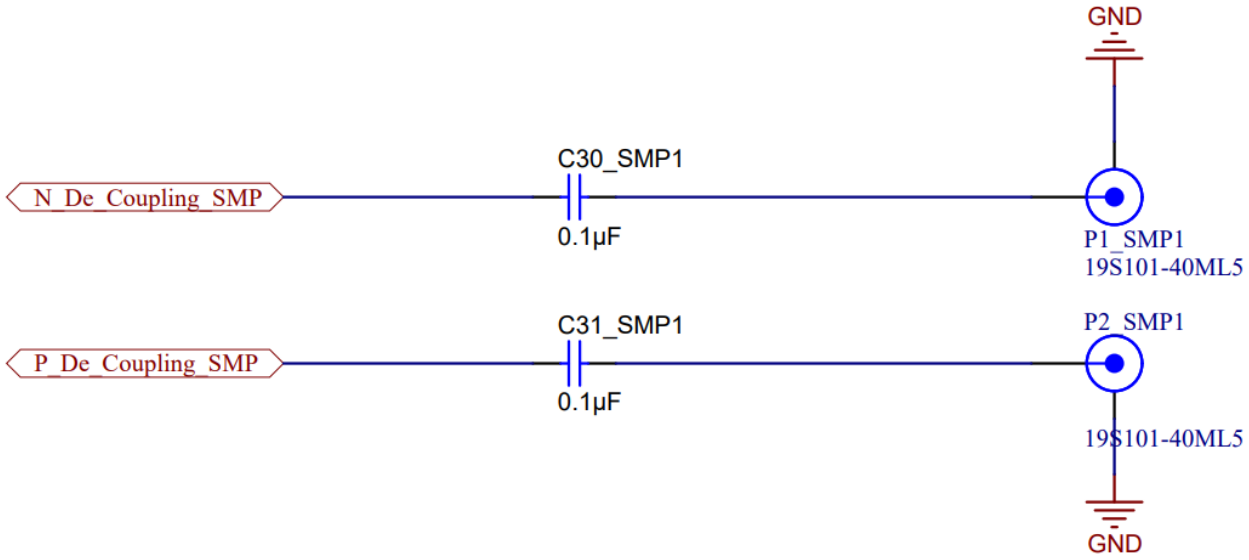


Figure 5-5. Logic Clock SMP Output

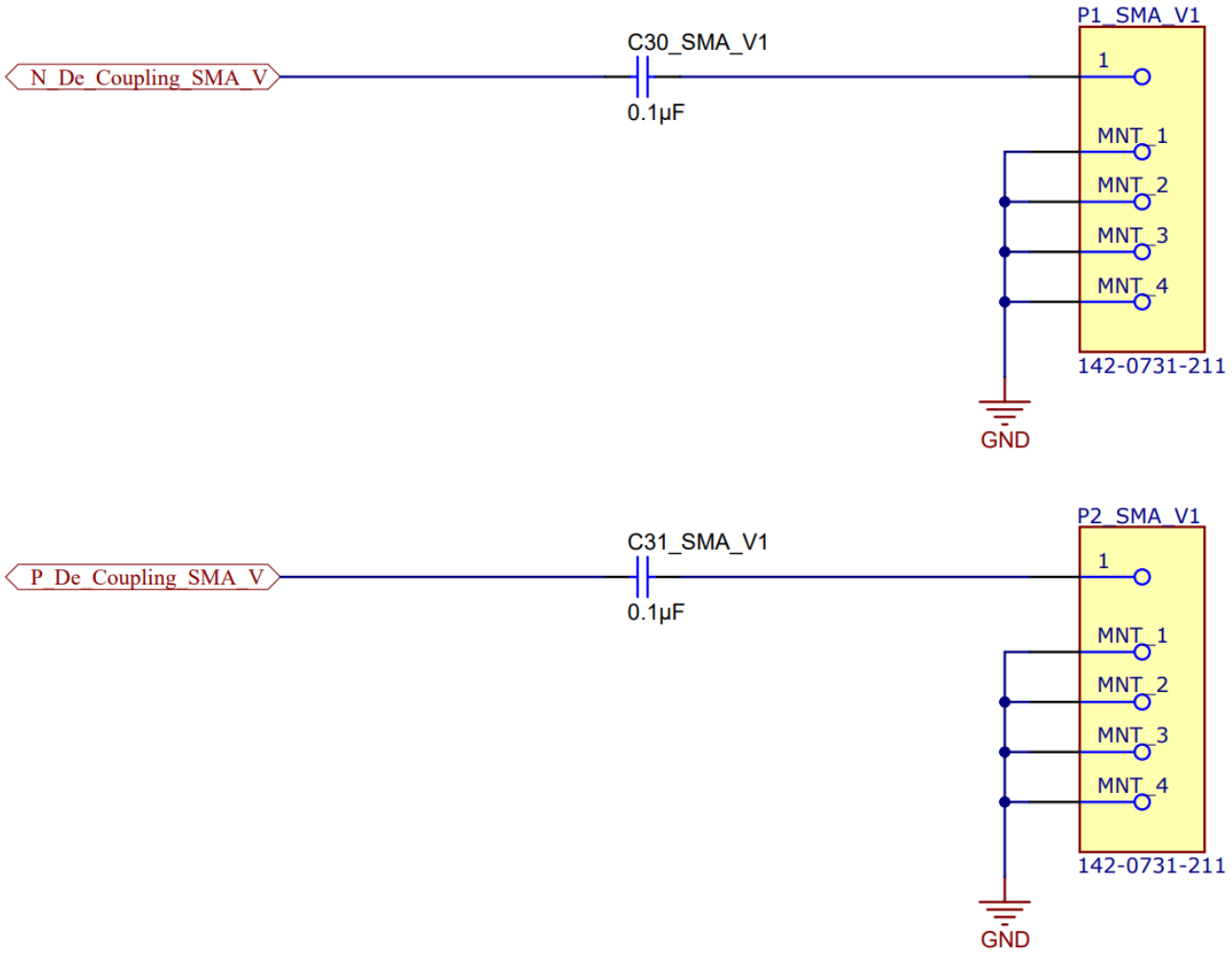


Figure 5-6. Vertical SMA for Secondary Device

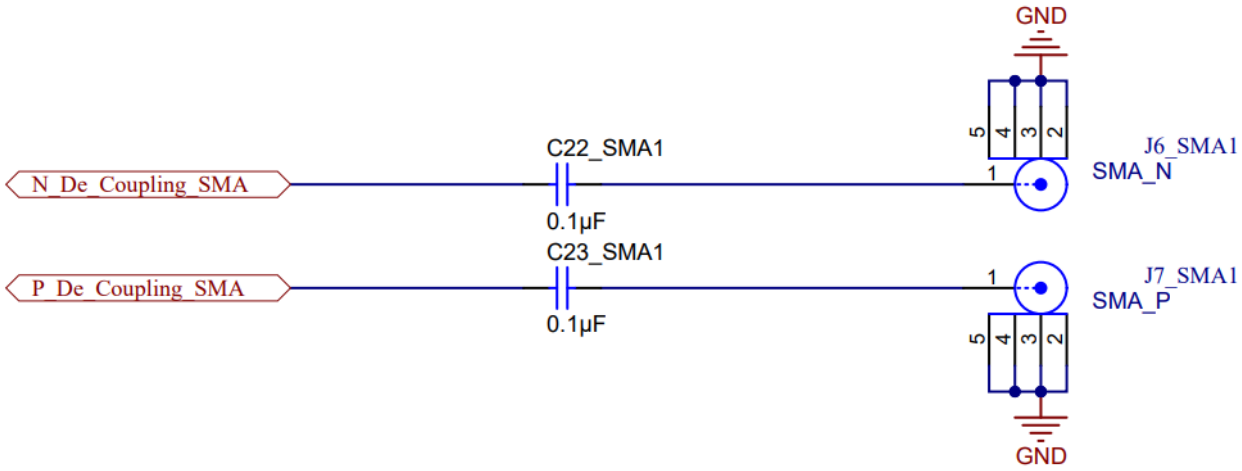


Figure 5-7. Edge SMA for all Devices

5.2 PCB Layouts

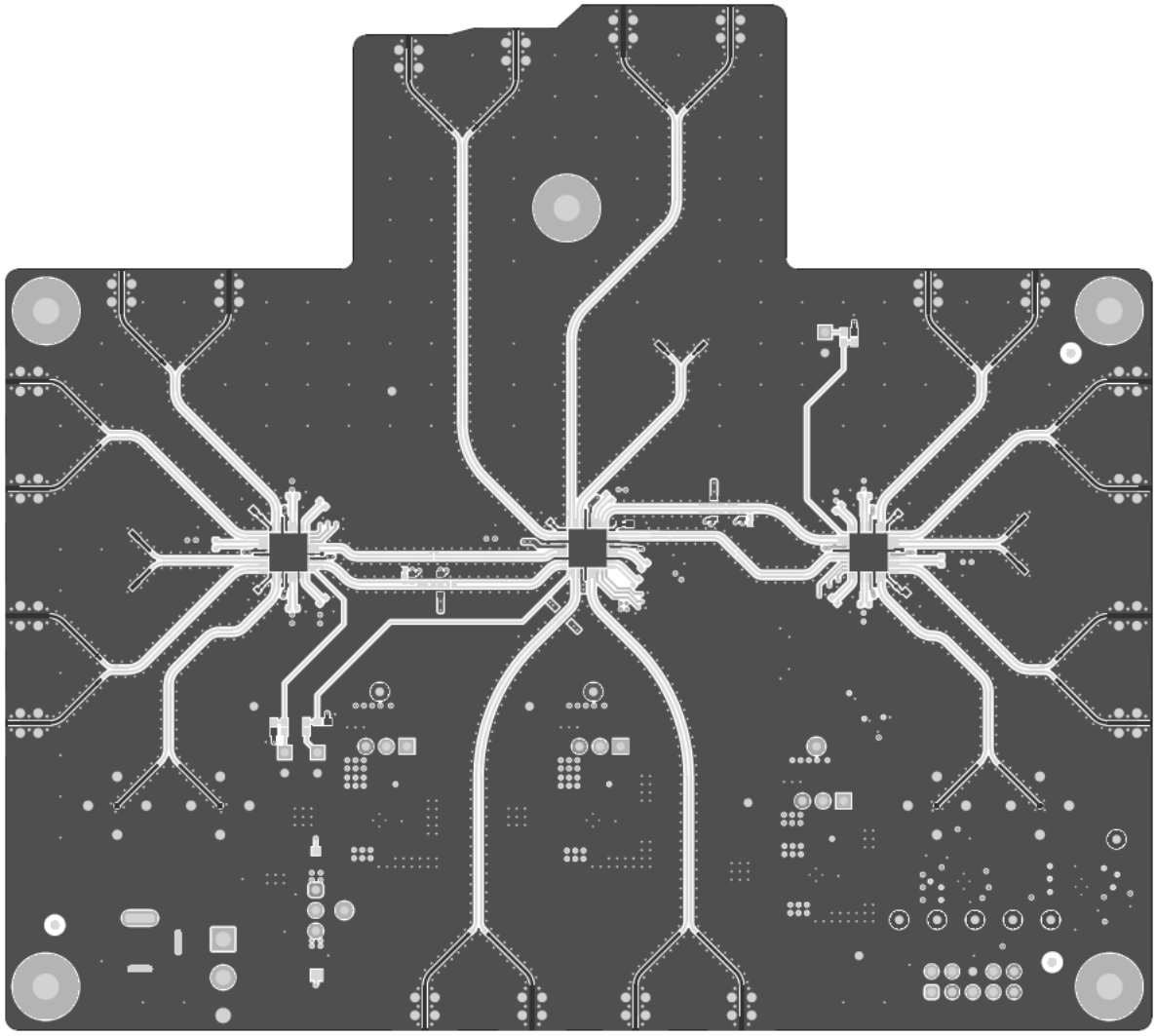


Figure 5-8. Top Layer

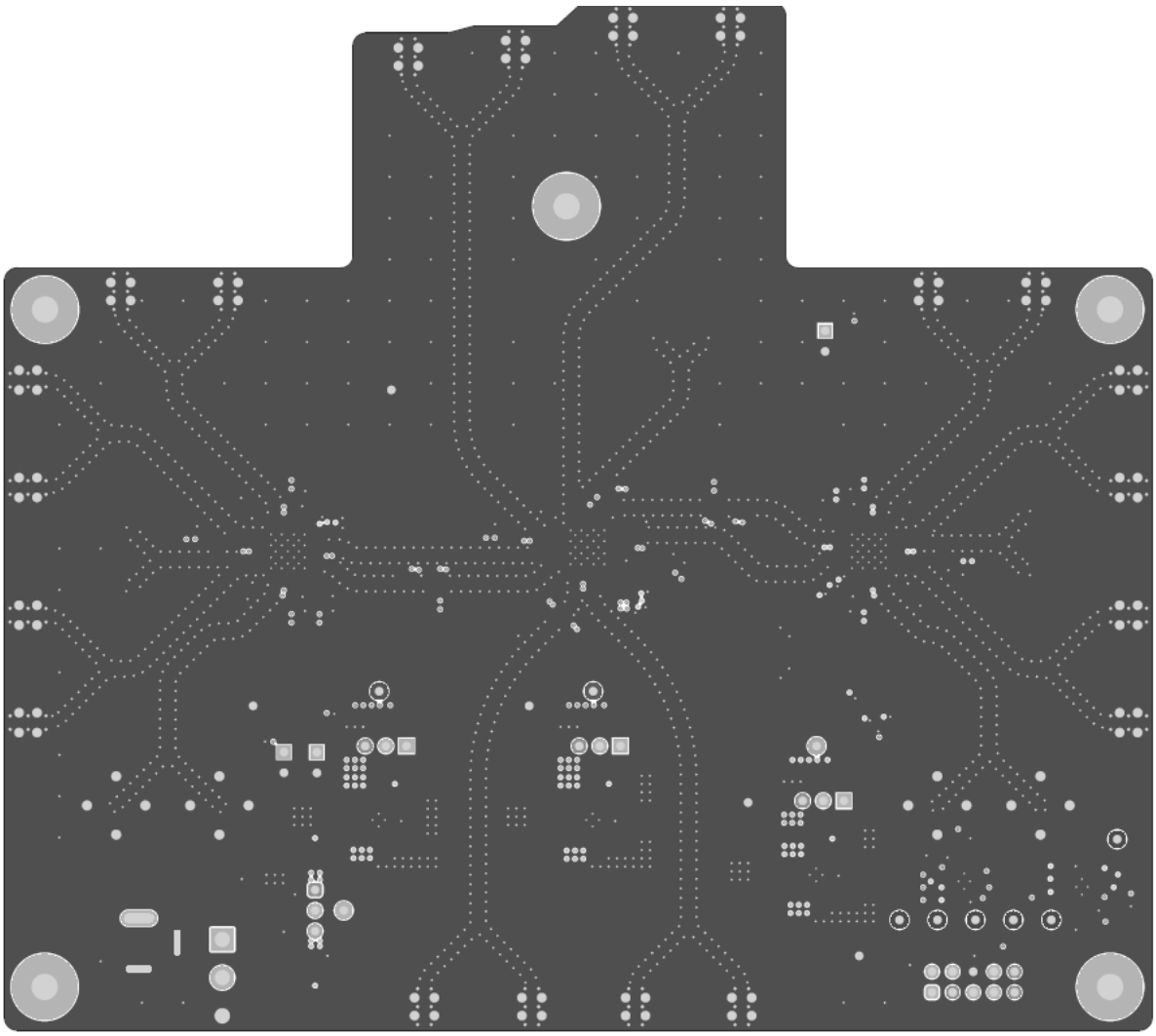


Figure 5-9. Layer2 GND

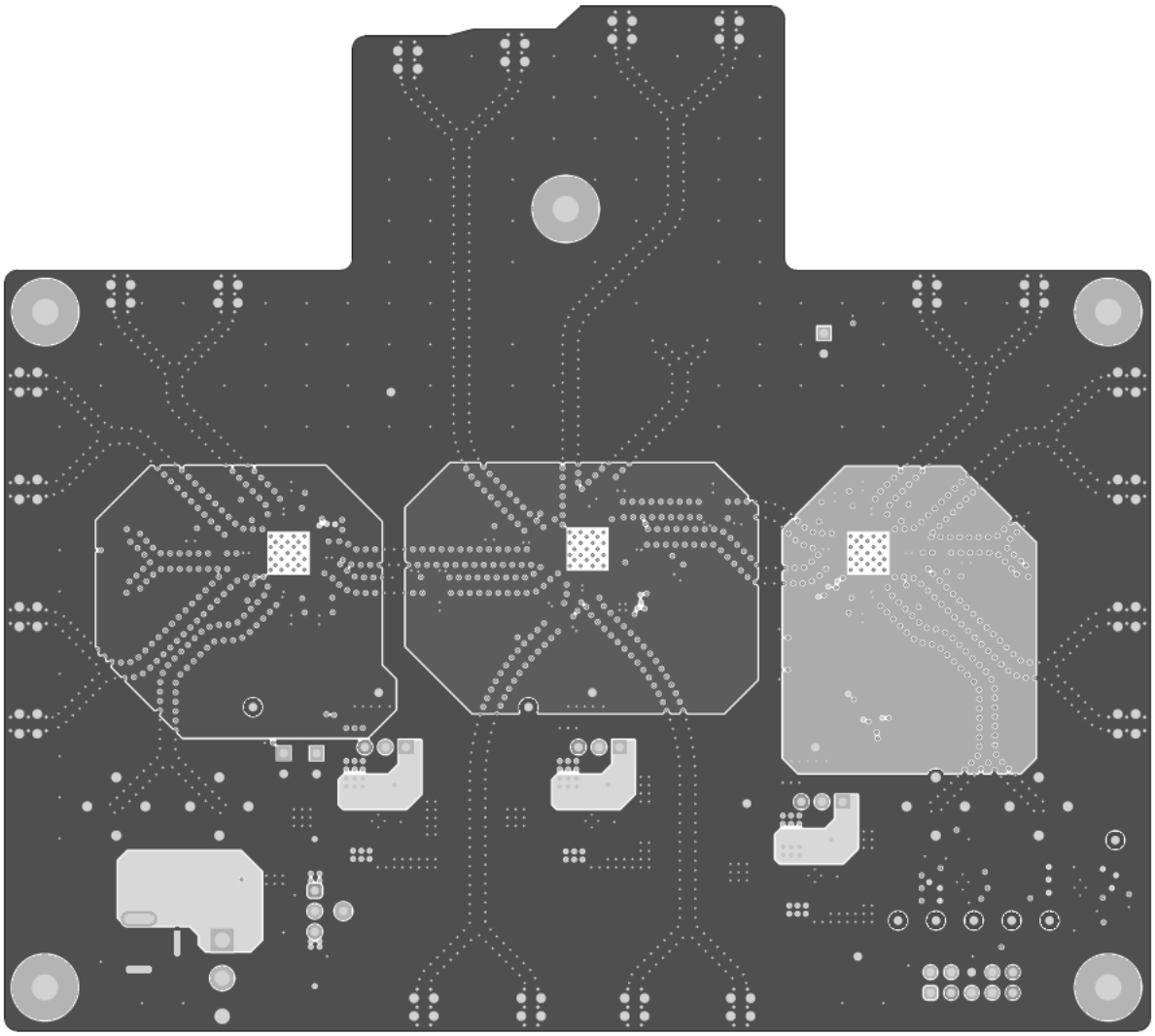


Figure 5-10. Layer3 Power

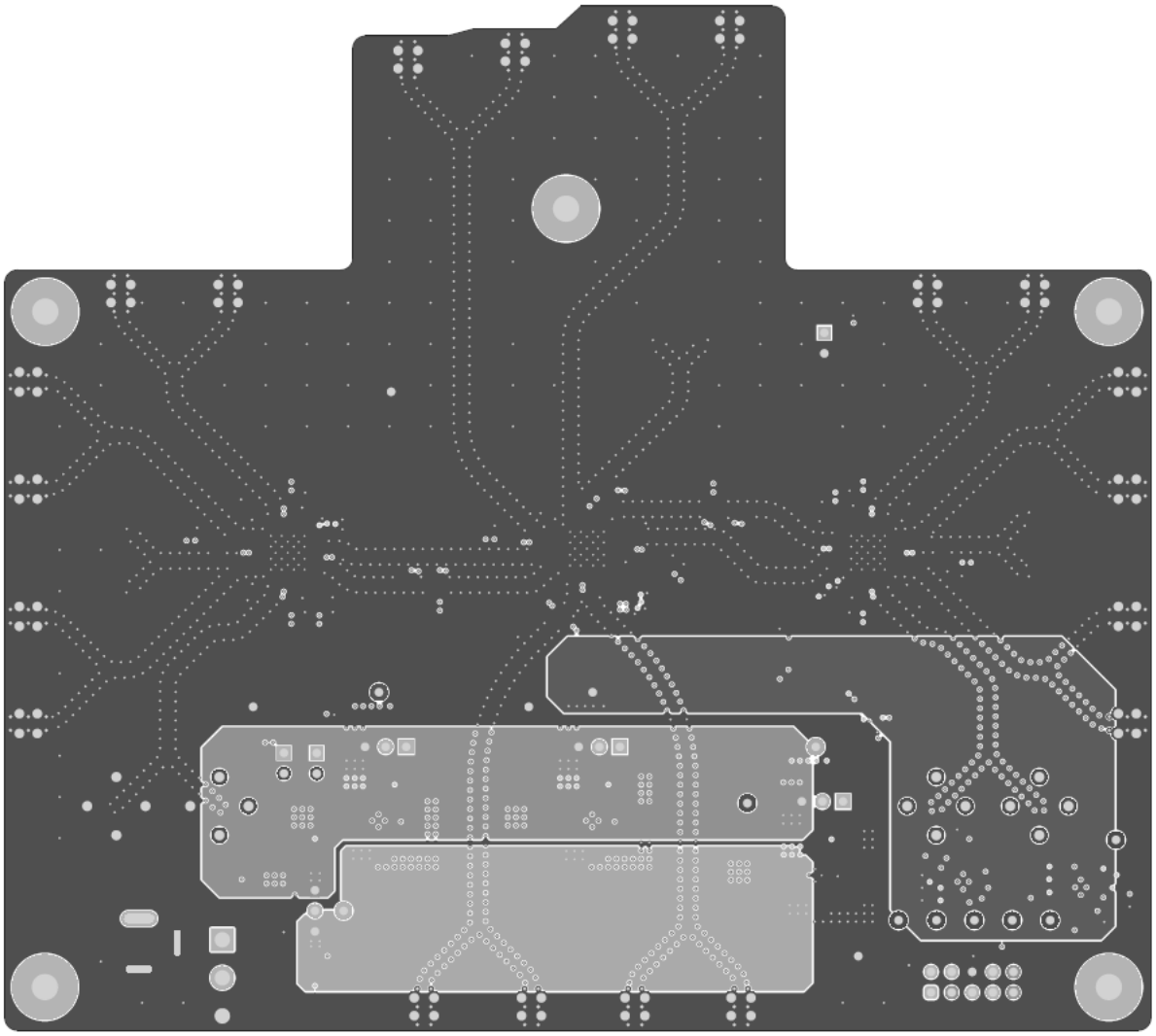


Figure 5-11. Layer4 Power

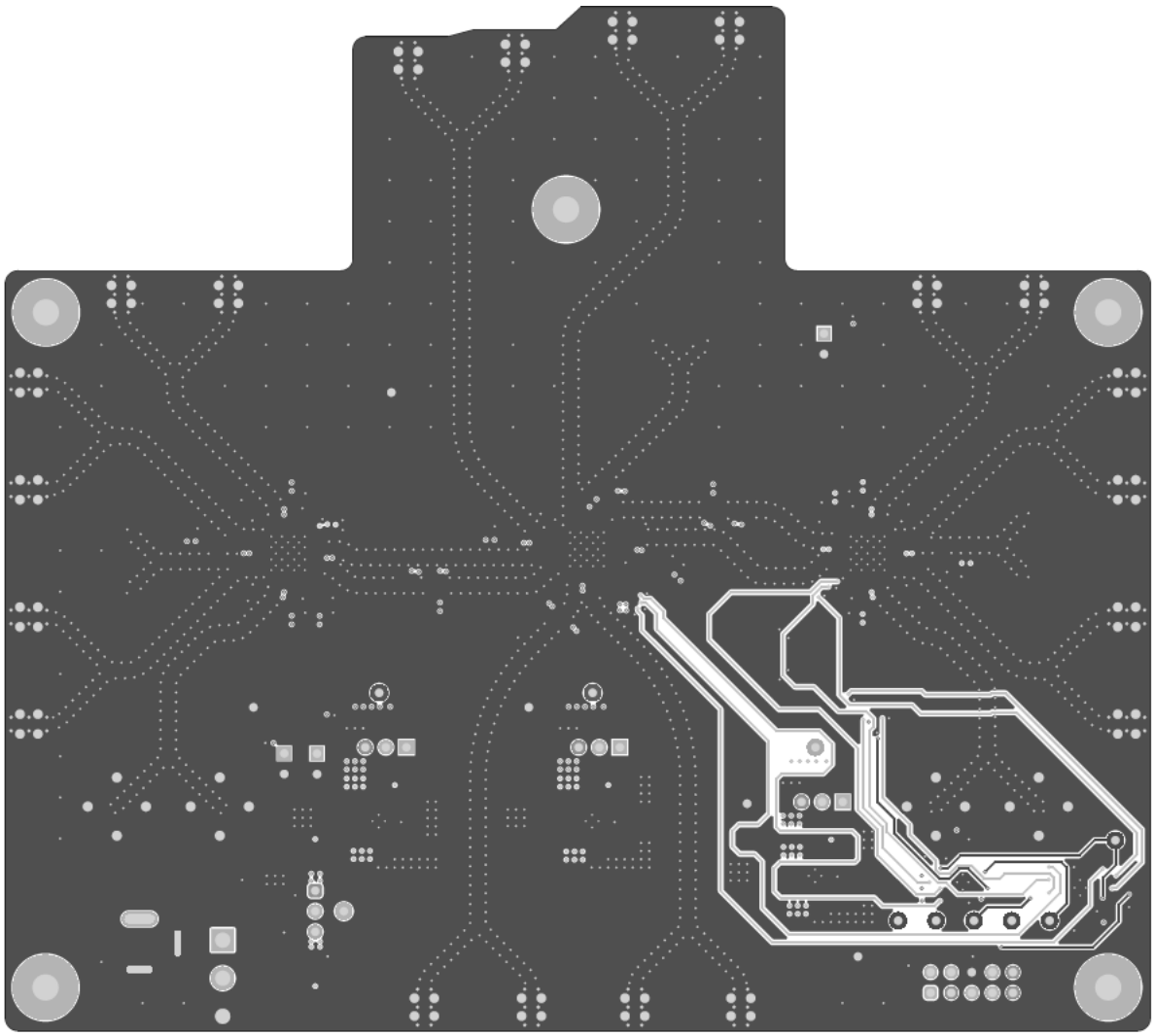


Figure 5-12. Layer5 GND

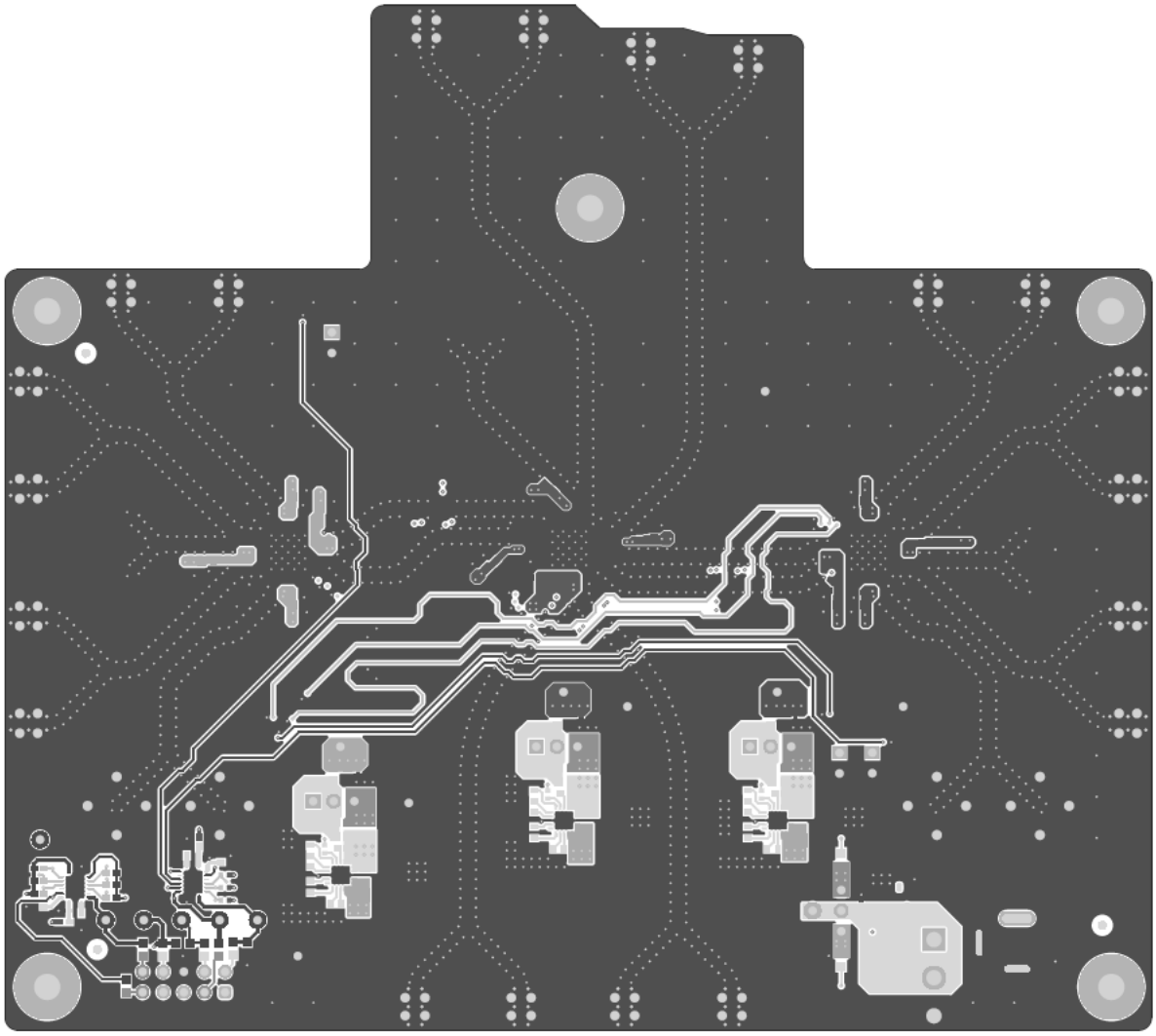


Figure 5-13. Bottom Layer

5.3 Bill of Materials (BOM)

Designator	Description	Package	Part Number	Manufacturer
BOARD_VCCIN	Power Jack, mini, 2.1mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC722X	Switchcraft
C1, C4_M, C4_S1, C4_S2, C7_M, C7_S1, C7_S2, C14_M, C14_S1, C14_S2, C17_M, C17_S1, C17_S2, C28_LDO1, C28_LDO2, C28_LDO3	CAP, CERM, 10 µF, 10 V,+/- 10%, X5R, 0603	0603	GRM188R61A106KAALD	MuRata
C2	CAP, CERM, 1 µF, 35 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1V105K080AE	TDK
C3, C20, C21, C29_LDO1, C29_LDO2, C29_LDO3	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X5R, 0201	0201	GRM033R61C104KE84D	MuRata
C5_M, C5_S1, C5_S2, C8_M, C8_S1, C8_S2, C15_M, C15_S1, C15_S2, C18_M, C18_S1, C18_S2	CAP, CERM, 1 uF, 6.3 V,+/- 10%, X7R, 0402	0402	GRM155R70J105KA12D	MuRata

Designator	Description	Package	Part Number	Manufacturer
C6_M, C6_S1, C6_S2, C9_M, C9_S1, C9_S2, C12_M, C12_S1, C12_S2, C16_M, C16_S1, C16_S2, C19_M, C19_S1, C19_S2, C22_SMA1, C22_SMA2, C22_SMA3, C22_SMA4, C22_SMA5, C22_SMA6, C22_SMA7, C22_SMA8, C22_SMA9, C23_SMA1, C23_SMA2, C23_SMA3, C23_SMA4, C23_SMA5, C23_SMA6, C23_SMA7, C23_SMA8, C23_SMA9, C30_SMA_V1, C30_SMA_V2, C30_SMP1, C30_SMP2, C30_SMP3, C31_SMA_V1, C31_SMA_V2, C31_SMP1, C31_SMP2, C31_SMP3, C32, C33, C34, C35	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X5R, 0201	0201	530Z104KT10T	American Technical Ceramics
C10_M, C10_S1, C10_S2	CAP, CERM, 0.01 uF, 6.3 V, +100/-0%, C0G/NP0, 0201	0201	550Z103PTT	AT Ceramics
C13_M, C13_S1, C13_S2	CAP, CERM, 10 µF, 10 V,+/- 20%, X5R, 0402	0402	CC0402MRX5R6BB106	Yageo
C24_LDO1, C24_LDO2, C24_LDO3	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata
C25_LDO1, C25_LDO2, C25_LDO3	CAP, CERM, 22 µF, 10 V,+/- 10%, X7R, 1206	1206	GRJ31CR71A226KE12L	MuRata
C26_LDO1, C26_LDO2, C26_LDO3, C27_LDO1, C27_LDO2, C27_LDO3	CAP, CERM, 0.01 uF, 6.3 V, +/- 10%, X5R, 0402	0402	GRM155R60J103KA01D	MuRata
CSB1, SCK1, SDI1, SDO1, SEL1, SEL2	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics
D1	Diode, Zener, 6.2 V, 225 mW, SOT-23	SOT-23	MMBZ5234BLT1G	ON Semiconductor
D2	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
D3	LED, Blue, SMD	LED_0805	LTST-C170TBKT	Lite-On
DC IN1, TP1_LDO1, TP1_LDO2, TP1_LDO3	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone Electronics, Keystone
DPST_S1	SWITCH SLIDE SPDT 6A 120V	SIP3	1101M2S3CGE2	C&K Components
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4, H14	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8, H16	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J8_LDO1, J8_LDO2, J8_LDO3	Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec

Designator	Description	Package	Part Number	Manufacturer
J2, J3, J6_SMA1, J6_SMA2, J6_SMA3, J6_SMA4, J6_SMA5, J6_SMA6, J6_SMA7, J6_SMA8, J6_SMA9, J7_SMA1, J7_SMA2, J7_SMA3, J7_SMA4, J7_SMA5, J7_SMA6, J7_SMA7, J7_SMA8, J7_SMA9	Connector, End launch SMA 50 ohm, TH	Connector, TH, End launch SMA	142-0761-881	Cinch Connectivity
J4_M, J4_S1, J4_S2	Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
J5	Header(shrouded), 2.54mm, 5x2, Gold with Tin tail, TH	Header(shrouded), 2.54mm, 5x2, TH	52601-S10-4LF	FCI
L1_LDO1, L1_LDO2, L1_LDO3	Ferrite Bead, 120 ohm at 100 MHz, 2 A, 0603	0603	742792625	Wurth Elektronik
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
P1_SMA_V1, P1_SMA_V2, P2_SMA_V1, P2_SMA_V2	SMA Connector Jack, Female Socket 50 Ohms Through Hole Solder	CONN_SMA_JACK	142-0731-211	Cinch Connectivity Solutions
P1_SMP1, P1_SMP2, P1_SMP3, P2_SMP1, P2_SMP2, P2_SMP3	SMP Straight Plug, Limited Detent, Small, Up to 26.5 GHz, -65 to 155 degC	19S101-40ML5	19S101-40ML5	Rosenberger
R1, R2, R5, R10, R15, R19, R21, R31_M, R31_S1, R31_S2, R32_M, R32_S1, R32_S2	100Ω ±1% 0.063W 0402 Thick Film Chip Resistor AEC-Q200 compliant	0402	RMCF0402FT100R	Stackpole Electronics
R3, R4	RES, 301, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603301RFKEA	Vishay-Dale
R7, R12, R17, R18, R27, R28, R68, R72, R80, R81	RES, 0, 5%, .05 W, AEC-Q200 Grade 0, 0201	0201	ERJ-1GN0R00C	Panasonic
R34_M, R34_S1, R34_S2, R35, R38, R44, R50, R51, R52, R53, R54, R55, R56, R57, R58, R63_LDO1, R63_LDO2, R63_LDO3, R64_LDO1, R64_LDO2, R64_LDO3, R66_LDO1, R66_LDO2, R66_LDO3	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R36, R37, R40, R41, R43, R45	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333R0JNEA	Vishay-Dale
R46, R47, R48	10k ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Moisture Resistant Thick Film	0402	RC0402JR-1310KL	Yageo
R59_LDO1, R59_LDO2, R59_LDO3	100 kOhms ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Moisture Resistant Thick Film	0402	RC0402JR-07100KL	YAGEO
SH-J1	Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP_1, TP_2, TP_3, TP_4, TP_5	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone Electronics
U1_M, U1_S1, U1_S2	Low-Noise, High-Frequency JESD Buffer/ Multiplier/Divider	VQFN40	LMX1205	Texas Instruments

Designator	Description	Package	Part Number	Manufacturer
U2	Dual 1-of-4 FET Multiplexer/Demultiplexer 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch, RGY0016A (VQFN-16)	RGY0016A	SN74CB3Q3253RGYR	Texas Instruments
U4_LDO1, U4_LDO2, U4_LDO3	2A High-Accuracy (0.75%) Low-Noise (4.4uVRMS) LDO Regulator, RGR0020A (VQFN-20)	RGR0020A	TPS7A8300ARGRR	Texas Instruments

6 Additional Information

6.1 Trademarks

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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