Application Note 881 ABT Design Considerations for Fault Tolerant Backplanes

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ABT Design Considerations for Fault Tolerant Backplanes

National Semiconductor
Application Note 881
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INTRODUCTION

National Semiconductor's high speed Advanced BiCMOS Technology, ABT is a 1.0 µm process product introduced to provide a high speed fault tolerant solution for interface needs. Some of the targeted interface environments include computer servers, mainframes and central office switches.

Each of these interface environments suffer from glitching or level degradation on their backplane or bus, generated from either live insertion of a board or a power up and down cycle used when performing maintenance on a system. Board designers need to address live insertion and power cycling requirements when designing a fault tolerant system. Definitions and applications of live insertion and power cycling change based on the product that interfaces with a backplane environment.

Discussion of a fault tolerant benefits from a review of definitions and solutions for fault tolerant interfacing and a review of device specs and how they contribute to a fault tolerant environment.

DEFINITION OF TERMS

— Live Insertion

Boards like those seen in a telephone company's central office switch are often removed and inserted while the backplane remains active. Insertion and removal generates glitches and voltage level changes on the backplane. The level of isolation that a board mounted interface device provides the backplane can be broken down into three major groups.

— **1st Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board to which it is mounted without having to power the system down. Requirements include a method of suspending the bus activity to prevent glitch or level corruption of bus data.

— **2nd Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board without the need to power the system down or suspend bus activity. Requirements include a method by which the bus can check for, and correct, faults introduced on the backplane during board insertion or a method for providing proper biasing of the board interface devices with a staggered pin arrangement on the board-backplane connector. Precondition biasing circuitry for the interface device may also provide the required isolation.

— **3rd Level of Isolation** is defined as the ability of the interface devices to allow board insertion without any limitations, restrictions or requirements of other circuits on the preservation of bus data.

The level of isolation that an interface device mounted on a board provides for the backplane has a direct impact on system uptime. Increasing levels of isolation allow for increased serviceability without system interruption. Board isolation provided by an interface device gives more freedom to the designer for focusing on purpose built board functions, reducing board design complexity and ultimately, board cost. ABT products reward the board designer and the board user these benefits with a 2nd Level isolation solution.

— Fault Tolerance

Fault tolerance in a backplane environment is the ability of the bus to detect and/or correct errant signals from any source including glitches, level changes, etc., generated from the insertion or extraction of a board into a backplane. A system populated with ABT products minimizes the need for errant signal processing associated with the live insertion and extraction process when biased correctly.

— Power Up/Down TRI-STATE®

When the devices that interface with the backplane power up or down, their connection to the bus will ideally maintain a high impedance state. With respect to the ABT product family, the output enable circuitry has control of the output state of the interface device during power up and down so as to prevent intermittent low impedance loading or glitch generation commonly associated with conventional CMOS and Bipolar devices.

— Partial System Power Down

Partial system power down implies that a system comprised of a combination of hardware and firmware provides power switching control of a backplane slot to allow for insertion, or removal of a board. Partial system power down facilitates system serviceability. Board-mounted ABT interface products enhance serviceability for permitting backplane slot power cycling while maintaining high impedance, glitch free isolation with the board and its backplane.

SOLUTIONS FOR FAULT TOLERANT INTERFACING

The achievement of a fault tolerant system solution with live insertion capabilities begins with a review of some of the bus protection solutions available. Options available to the ABT product family include:

— Staggered Pin Arrangement

For a PC edge connector arrangement, the solution in *Figure 1* can be adopted to provide proper biasing of the output enable pin ($\overline{OE}$) to ensure high impedance on the backplane. It will satisfy both insert and removal requirements. While this configuration provides an ideal connector, constraints often limit the number of different pin lengths to two. By offsetting the $\overline{OE}$ pin, we want to ensure that it will either reach a high level of ≥2.0V, before V_{CC} is applied, or that $\overline{OE}$ will maintain a ≥50% V_{CC} level during the V_{CC} ramp.

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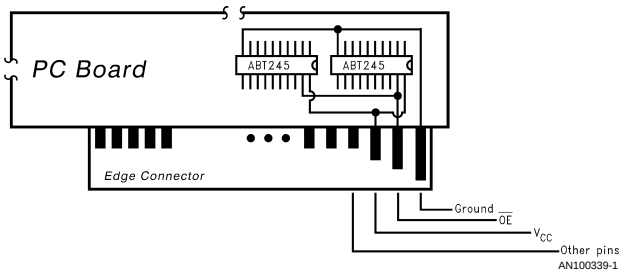


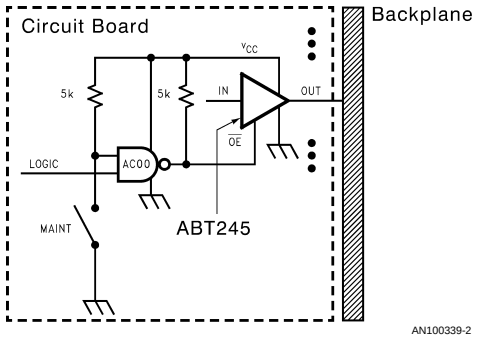
FIGURE 1.

— Isolation Circuitry

Isolation circuitry provides another option for board and backplane isolation. Again, this solution will provide the necessary $\overline{OE}$ pin biasing to assure a level of 2.0V or to assure $\overline{OE}$ maintains ≥50% of V_{CC} as V_{CC} powers up or down for guaranteed high impedance interface to the backplane.

The design of Circuit-1 below provides >50% of V_{CC} for the $\overline{OE}$ pin throughout the V_{CC} ramp then switches to a voltage level of a logic high once the AC00 reaches its turn-on V_{CC}. After board insertion, the MAINT switch is opened and the LOGIC pin becomes the $\overline{OE}$ control. Live insertion or removal for this solution requires a technician to manually operate the maintenance switch (MAINT) to ensure proper biasing of $\overline{OE}$ and board-backplane isolation.

Circuit-1



SPECIFICATIONS AND THEIR CONTRIBUTION TO FAULT TOLERANT SYSTEMS

DC specifications and their characteristic input/output curves help map out the loading effects of an interface device on bus or backplane. The loading characteristics of typical ABT input and output pins are shown in *Figure 2–Figure 4*. National Semiconductor's ABT245 characteristic curves are used for this demonstration.

— Powered Down Backplane Isolation

The power down leakage characteristics of a bus interface device assist the interface board designer in understanding the effects of loading on his backplane. During live insertion, the board is not powered up and the instantaneous loading upon contact would look like the curves of VID and IZZ in *Figure 2* and *Figure 3*. Typically, loading leakages in the +200 µA range begin to affect the V_{OH}/V_{OL} levels in a backplane application. The VID and IZZ curves illustrate the loading effects on the backplane over a range of backplane voltages from 0.0V to 5.5V.

— VID

VID is a voltage that is measured on an input pin at a current loading of 1.9 µA in a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VID vs IID in *Figure 2* shows the current leakage of a typical ABT input pin. The ABT inputs limit loading leakage to <1.9 µA over an input voltage range from 0V to 5.5V.

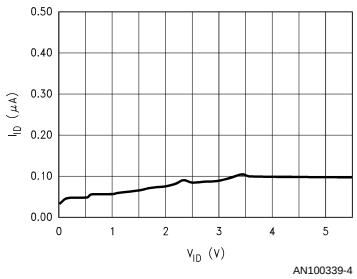


FIGURE 2.

— IZZ

IZZ is a current that is measured on an output pin at a voltage of 5.5V during a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VZZ vs IZZ in *Figure 3* shows the current leakage of a typical ABT input/output (I/O) pin and how

it loads a bus or backplane over a range of bus voltages from 0.0V to 5.5V. I/O pin configurations exhibit combined current characteristics from components of the input circuitry and output circuitry. ABT I/O pins specify loading leakage at 100 µA max. with a typical loading leakage at 3 µA at room temperature.

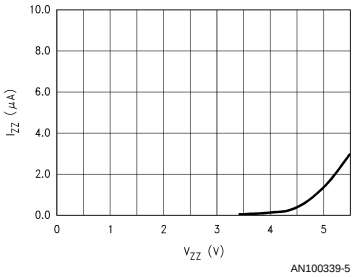


FIGURE 3.

— Powered Up Backplane Isolation

During power up operation, the output enable pin, $\overline{OE}$, controls backplane isolation. The IOZH/IOZL parameters provide the interface board designer with the leakage characteristics of the interface device during a tri-stated condition.

— IOZL/IOZH

IOZL is a parameter that quantifies the output leakage current while the part is powered up and the output is conditioned low before it was tri-stated (disabled). IOZH is the same as IOZL except that the output was conditioned high before being tri-stated.

The IOZL/H curve in *Figure 4* shows an I/O pin leakage characteristic during TRI-STATE operation over a range of bus voltages from 0.0V to 5.5V. ABT devices specify IOZH/L at a maximum of 50 µA while typical leakage is in the vicinity of 12 µA at room temperature.

— Powering Cycling and Backplane Isolation

During the transition of a power up or power down cycle, an interface device output might act erratically by glitching or seeking a voltage level that is disruptive to the backplane. These transition characteristics degrade fault tolerant systems and would increase system down time.

The curves in *Figure 5* and *Figure 6* demonstrate the capability of the ABT245 to maintain isolation from an active bus and provide a glitch free output while being powered up and down. With the $\overline{OE}$ pin conditioned high, V_{CC} was cycled between 0.0V and 5.5V to monitor the output voltage levels as they would appear on a bus. Bus loads of 1 kΩ pull-up and pull-down were used. The bus voltage level disruption is in the micro-volts range attesting to the minimal impact ABT interface products would have on the backplane.

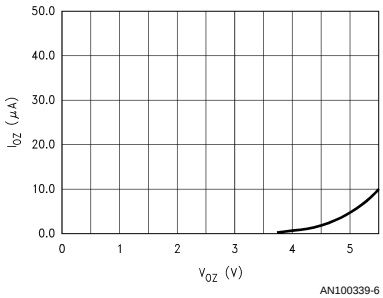


FIGURE 4.

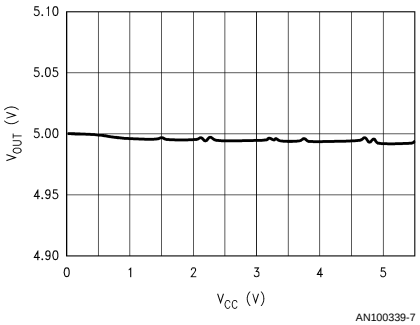


FIGURE 5. Bus High Effects

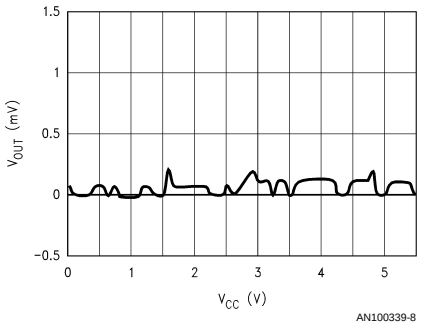


FIGURE 6. Bus Low Effects

SUMMARY

ABT interface devices offer glitch free power cycling provided that the $\overline{OE}$ pin is held at the device specified V_{IH} (2.0V) level. In practice, $\overline{OE}$ will provide an output high impedance condition if $\overline{OE}$ maintains a level of ≥50% of V_{CC} through the 0V to 5.5V range. In fact, the $\overline{OE}$ pin circuitry gains control once V_{CC} is ≥1.0V. Interface device output characteristics for V_{CC} levels before 1.0V are controlled through the isolation circuitry discussed earlier.

ABT designs and specifications recognize the need for more fault tolerant interface devices. Live insertion guarantees such as VID/IZZ, IOZL/H and glitch free power cycling all promote better system uptime, especially for telecom switching environments. Together with extended AC specifications that reduce the need for complex performance evaluations, ABT live insertion guarantees allow designers to spend more time on total system performance features and not worry about the logic.

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