Application Note 1059 High Speed Transmission with LVDS Link Devices

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High Speed Transmission with LVDS Link Devices

National Semiconductor
Application Note 1059
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High speed data transmission requires a designer to be aware of factors which may impact the correct sampling of data. In particular, items such as excessive skew and jitter can lead to data sampling errors, limiting the maximum bandwidth performance of the LVDS Link. The following is a discussion of LVDS Link receiver data sampling, skew and jitter margin, and an explanation of skew and jitter components.

LVDS LINK DATA SAMPLING

The advantage of using the LVDS Link devices (FPD Link and Channel Link) is the ability to convert many parallel data lines into a narrower serialized interface. This serialized LVDS interface is capable of running at seven times the data rate of the parallel TTL interface. This means that the width of a data bit on the LVDS interface is one seventh of the width of the data on the TTL interface. For example, data transmitted at 65 MHz on the TTL interface has a width of 15.38 ns; the corresponding bit width on the LVDS interface is 2.19 ns. This requires an accurate strobe to correctly sample the LVDS data at the receiver. *Figure 2* describes how internal receiver strobes are generated to sample the LVDS data bits. The LVDS clock and data arrive at the receiver input. The clock moves through a delay element. The delay lines generate sampling strobes: the first strobe is based on the rising edge of the receiver input clock (LVDS clock), and all subsequent strobes are based on the previous strobe. Each strobe samples one data bit of the *next* data cycle. Strobes are resynchronized with the rising clock edge for each new clock cycle. Any jitter on the incoming clock source (transmitter input clock) may be directly passed on to the strobes. Sources of this jitter are discussed later.

The ideal strobe should be targeted at the center of the data bit to allow for skew and jitter while maintaining a sufficient margin for sampling data. *Figure 1* shows this ideal relationship of the strobe to a single data bit.

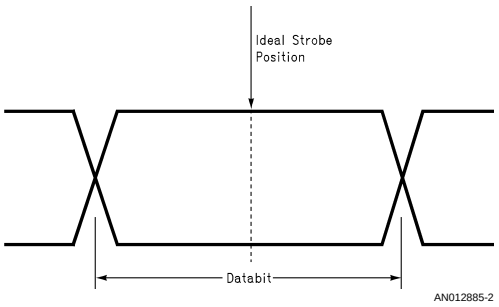

FIGURE 1. Receiver Strobe Position

MARGIN

In an ideal situation, the strobe could occur anywhere in the data window and sample data correctly. However, there are several factors which reduce the available sampling window; this sampling window is “margin”. Margin is required to assure that valid data is sampled correctly by the receiver input strobe.

The receiver itself has a limitation on sampling of valid data. There is an inherent internal setup and hold time for the data with respect to the clock (Rspos). Data must be available for a period of time before it may be sampled (setup time) and held for a period of time after sampling (hold time). These parameters reduce the effective available sampling window. In addition, if the strobe is not centered within the data bit the margin is reduced. This receiver input margin is limited by the smallest data sampling window before or after the strobe. The transmitter output introduces clock to data skew which further impacts the available margin **(d)**. The position of the data bit relative to the clock may not be constant, thus moving the strobe further from the ideal center of the data bit. This variation of pulse position is defined as Tppos. TCCS is the nominal distribution of pulse position skew; this is within the Tppos distribution. The total margin available after accounting for strobe and pulse position variation is known as the receiver input skew margin (RSKM).

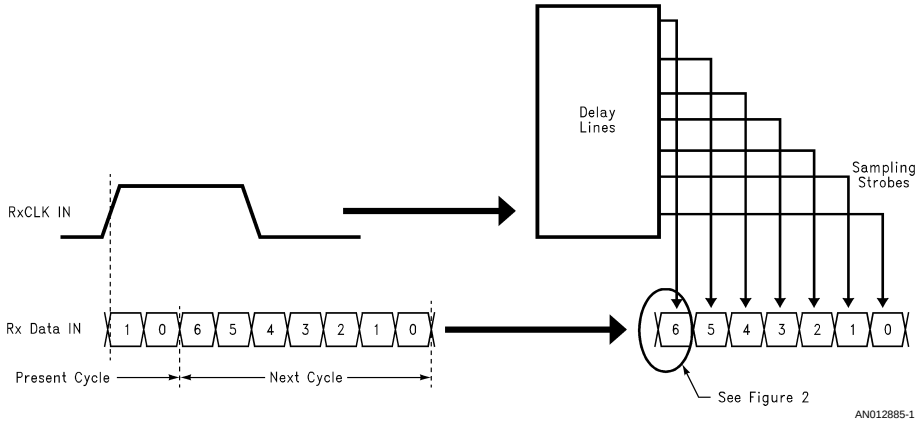

FIGURE 2. RxCLK IN during Present Cycle Generates Strobes to Sample Data of Next Cycle

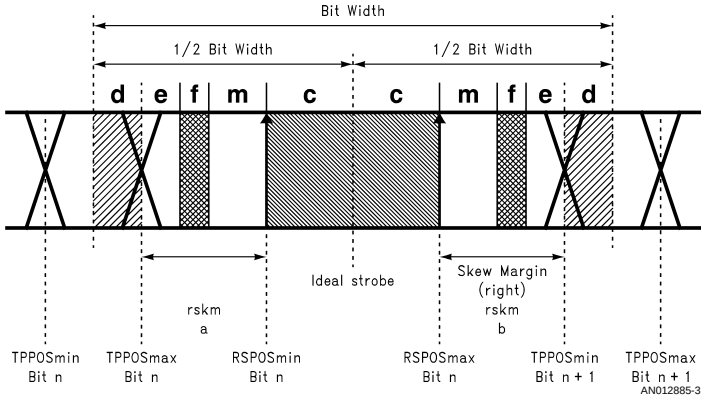

FIGURE 3. Receiver Skew Margin

After accounting for the characteristics of the LVDS devices, (rskm) external cable skew and input clock jitter must be considered. *Figure 3* illustrates the components of the dat-abit sampling window.

Where:

"a", "b": rskm is the margin for data sampling at the receiver inputs. This number is based on the pulse position (Tppos) and strobe position (Rspos) characteristics of the device.

"c": represents the setup and hold times for the receiver strobe relative to the ideal strobe position (Rspos min and Rspos max).

"d": is the variation of transmitter pulse position from ideal (Tppos max-ideal and ideal-Tppos min).

"e": is the cable skew

"f": is the clock jitter

"m": is the remaining margin for data sampling

and...

$$m = rskm - (e + f)$$

SYSTEM DESIGN: SKEW AND JITTER

The two primary components of a skew/jitter budget are cable skew **(e)** and input clock jitter **(f).** The system designer needs to evaluate these components and make trade-offs as necessary to remain within the budget and maintain the desired margin.

The Interconnect

A wide variety of cable options are available for the LVDS interface. The main factors contributing to skew are cable length, cable type and quality of cable. Skew for a given cable is typically specified by the manufacturer as skew (in picoseconds) per unit length. The longer the cable, the higher the skew. A flat cable in which all signal lines are parallel will typically have less skew per unit length than a twisted pair cable of comparable quality. The twist in the cable and the fact that some differential pairs are on the outside of the cable and others inside can result in differences in signal line lengths. Some twisted pair cables are designed with special construction to greatly reduce skew between

signal lines. The quality of cable — and the price — can also make a difference in the skew. Higher quality cables must meet more stringent requirements to guarantee a lower skew per unit length. This value is typically 10 ps/ft to 40 ps/ft depending on the cable quality.

The total skew path also includes the connector skew and PCB trace skew. The skew at the connector interface is typically much less than the contribution of the cable. "Zero skew" connectors are available on the market today. Such connectors are configured with a single row of pins/leads. The PCB traces between the connectors and LVDS device pins may be routed to ensure equal trace lengths and add little or no skew (*Figure 4*).

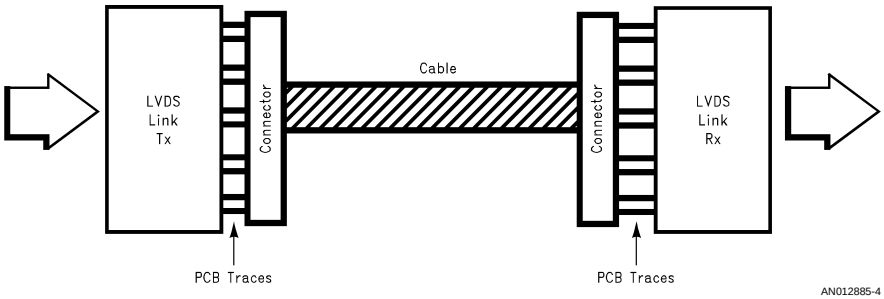

FIGURE 4. Interconnect Skew = PCB + Connector + Cable + Connector + PCB

Clock Jitter

Jitter on the input clock to the transmitter is also a concern. Any jitter that is introduced at this point may be passed on to the LVDS clock and data. Since the rising edge of the LVDS clock is used to initiate the receiver strobes, the receiver strobes in turn will jitter as the data jitters. Ideally, this would appear to maintain the desired relationship between data and the receiver sampling strobe. However, since sampling strobes are generated by the clock of the previous cycle, the receiver sampling strobes will be off-center in proportion to the cycle-to-cycle input clock jitter. This increases the probability of sampling data incorrectly.

Figure 5 and *Figure 6* show the impact of clock jitter on strobe position relative to the databit. In both figures a cable skew has been assumed (e). *Figure 5* shows the strobe position relative to the databit with a stable clock edge. Additional margin remains for data sampling. *Figure 6* shows the databit and strobe position with jitter on the input clock edge. The databit has moved relative to the strobe position (set by the previous clock cycle). No margin for data sampling remains.

It is important to distinguish between short term and long term clock jitter. Short term jitter, as applies to the LVDS Link devices, is the variation of a transmitter input clock edge (rising or falling) between adjacent clock cycles and is typically on the order of 10's or 100's of picoseconds. This jitter may impact the margin. Clock drift describes the long term shift of a clock edge. This number can be on the order of nanoseconds and may be intentionally introduced as a means of lowering EMI. This long term clock drift does not impact jitter margin since receiver resynchronizes with every clock cycle.

The FPD Link transmitters have been redesigned to enhance the rejection of cycle-to-cycle jitter. The cycle-to-cycle jitter at the TxCLK input is not passed directly to the TxCLK output. TxCLK output cycle-to-cycle jitter is maintained below 250 ps with a TxCLK input cycle-to-cycle jitter of up to 6 ns. This eliminates the variability of clock jitter from the margin equation (**"f"** = 250 ps). This feature is implemented in the 65/66 MHz devices and will be incorporated in future products.

Sample Calculation

Please note that all values are provided for example purposes. These are NOT necessarily typical values.

An example of margin calculation at 40 MHz is shown below.

m = rskm − (e + f) = margin

where:

rskm = 1 ns @ 40 MHz shfclk

e = 30 ps (1m cable)

f = 250 ps

m = 1000 − (30 + 250)

m = 720 ps

Total margin remaining is 720 ps.

At 65 MHz the receiver input skew margin (RSKM) will decrease due to the decrease in databit width.

m = rskm − (e + f) = margin

where:

rskm = 500 ps @ 65 MHz shfclk

e = 30 ps (1m cable)

f = 250 ps

m = 500 − (30 + 250)

m = 220 ps

Total margin remaining is 220 ps.

Note: The datasheets for FPD Link and Channel Link products account for transmitter output skew ("d") in the Tppos specification.

CONCLUSION

Designing for high speed data transmission requires attention to factors which will impact the margin for correct data sampling. Input clock jitter and cable skew are key components to be evaluated when designing to maintain high bandwidth performance. Minimizing this input clock jitter will improve the ability to correctly transmit data at high speeds. This has been controlled by redesigning the transmitter to maintain a cycle-to-cycle jitter below 250 ps. The second component — cable skew — may be addressed by selecting a cable based on media, quality and distance requirements. The designer must decide how to best minimize each component — cable skew and TTL input clock jitter — while also minimizing system costs.

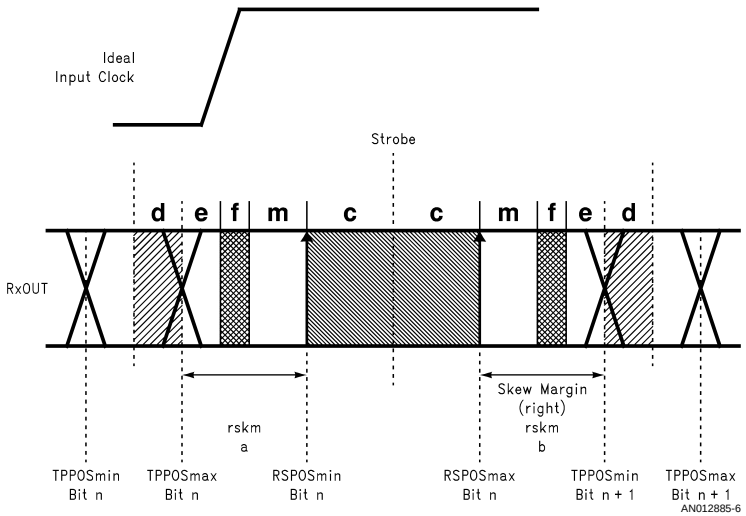

FIGURE 5. Databit and Strobe Position with Ideal Input Clock

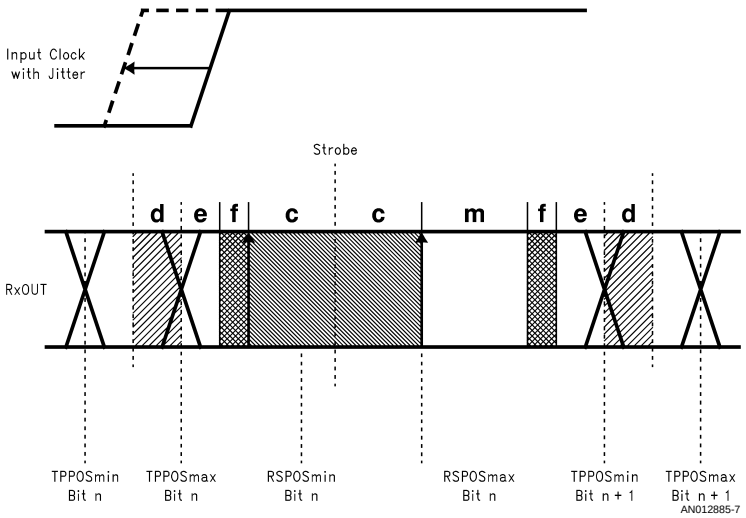

FIGURE 6. Databit and Strobe Position with Jitter on Input Clock. No Margin Available for Sampling Data.

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