Application Report
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AN-1971 Triple Rate SDI IP FPGA Resource Utilization on the SDXILEVK/AES-EXP-SDI-G Reference Design

Nate Unger

ABSTRACT

Texas Instruments triple rate (SD/HD/3G) SDI demonstration board showcases the LMH0340 serializer, LMH0341 deserializer, LMH0344 equalizer, LMH1981 sync separator, LMH1982 clock generator with genlock and the DS25CP104 cross-point switch. There are many advantages to using the Texas Instruments chipset that include superior performance, reduced cost using inexpensive FPGAs such as the Xilinx Spartan 3A series of parts, and the flexibility to add or modify features such as SMPTE 299 3G audio.

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1 Introduction

The intention of this application report is to outline some of the features of the National Semiconductor triple rate SDI FPGA IP and show the resources that are used for the outlined features. The full FPGA IP for the SDXILEVK is compliant with SMPTE 259-C, SMPTE 292, SMPTE 424, and the SD and HD portion of SMPTE 299. Below is a list of SDXILEVK FPGA IP features.

- Standalone video generator with internal test patterns and standalone video termination
- Video pass-thru from input and reclocked to the output
- Video generator using internal test patterns or video input synchronized to:
  - SDI video input
  - Genlocked to analog sync
  - Genlocked to SDI video input
- SD/HD SMPTE 299 audio embed/de-embed:
  - 2 channel I2S I/O
  - 2 channel internal audio synthesizer
  - Audio group detection and audio group embed selection

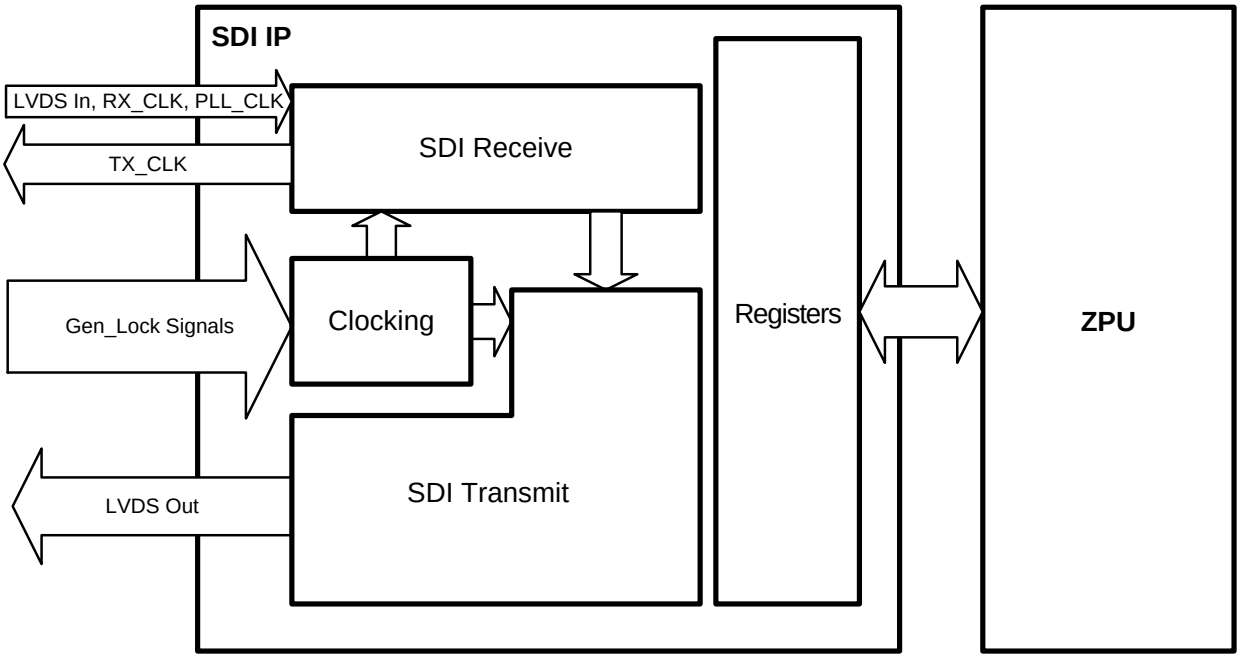

Figure 1. FPGA IP Block Diagram

Table 1. Evaluation Kit Part Numbers

National Semiconductor Part Number	SDXILEVK
Avnet Part Number	AES-EXP-SDI-G

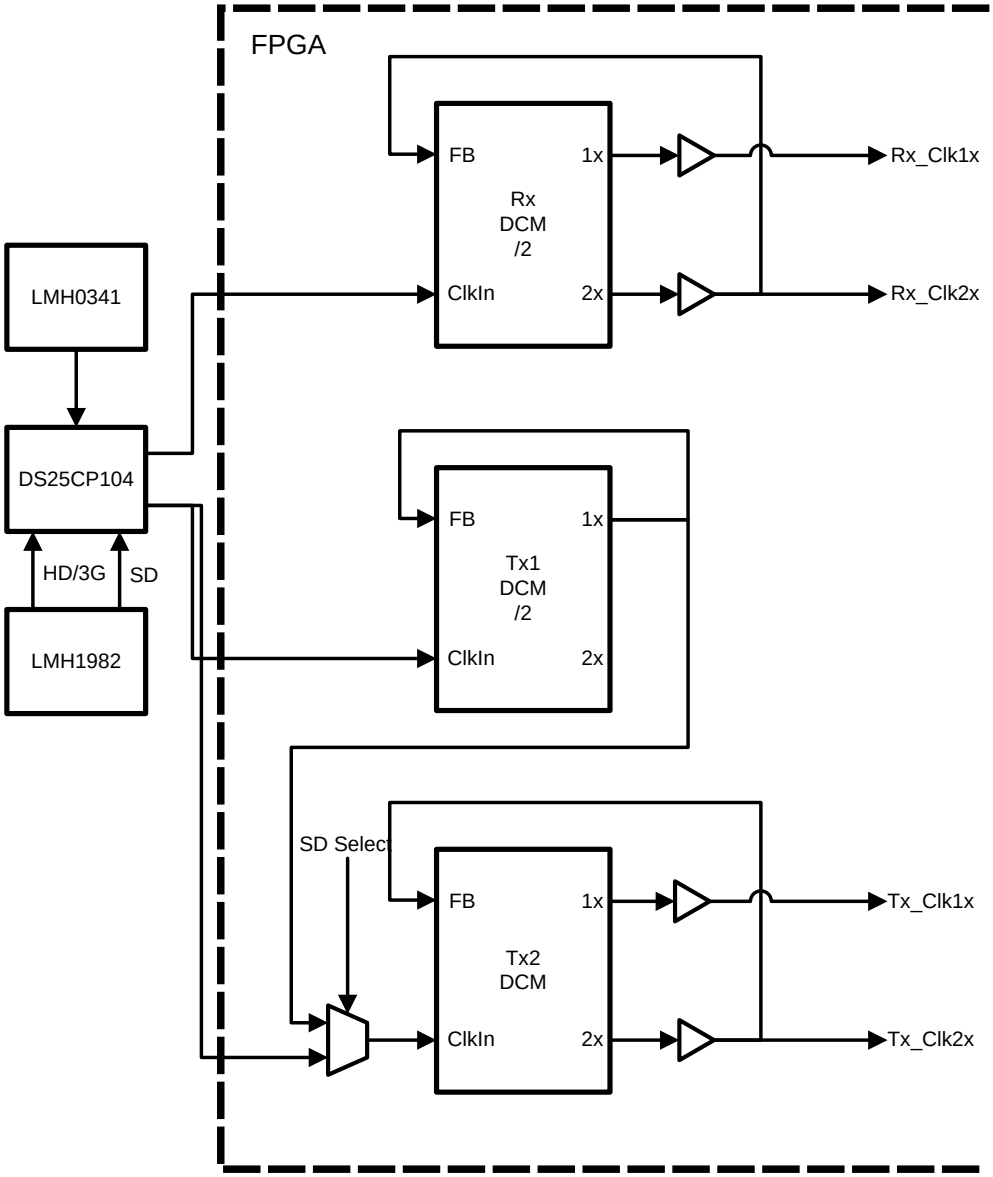

Figure 2. Full SDI Clocking: ZPU, Genlock, RX, TX and Audio In/Out

2 SDXILEVK FPGA IP Features

The SDXILEVK evaluation platform provides a complete SDI evaluation platform. The FPGA IP is shown in Figure 1. The datapath is broken into a receive and transmit path and the clocking IP multiplexes the required clocks for each of the different supported modes of operation. The integrated ZPU (freeware CPU) runs the control interface for the terminal user interface or push-button modes.

3 SDI Clocking Resources

One of the most important resources to understand is clocking resources since these can be one of the earliest limiting factors. Clocking resources are usually similar across an FPGA family but can vary slightly. This section describes the clocking resources needed for the full SDI FPGA IP and isolates the resources based on lower level functions.

4 Full RX and TX Data Path with Gen-Lock

Figure 2 shows the clocking structure for the full FPGA IP SDI stack. The datapath is a 20 bit interface running at 1/4 the data rate of the of serializer/deserializer (SerDes) 5-bit DDR interface. The FPGA IP has a 1x and 2x clock domain. There is a 20:5 and 5:20 SerDes implemented in the FPGA to transition from the 5-bit DDR SerDes clock domain to the FPGA 20-bit datapath clock domain. Three DCMs and six BUFGMUXs are needed for the complete FPGA IP with genlock, independent TX and RX paths, and pass through mode where the TX clock domain is the same as the RX clock domain. Five of the six BUFGMUXs are used as global clock buffers (global clocks). Not shown in Figure 2 is an always on clock used for state machine logic and the ZPU, which is the name of the embedded CPU.

In this implementation, the DS25CP104 crosspoint switch is used to select the clock to be used for the TX path. It can be the SD (27 MHz) or the HD/3G (74.25, 148.5 MHz) clock from the LMH1982. These clocks can be either genlocked or in free-run mode. The clock from the LMH0341 can also be selected when pass through mode is desired.

When the LMH1982 is genlocked or in free run mode TX1 DCM and the “SD Select“ BUFGMUX are needed. In the past, the SD datapath would be 10 bits running at 27 MHz. The Texas Instruments FPGA IP maintains a 20-bit datapath across SD, HD, and 3G to maintain a seamless triple rate datapath. In SD mode, the 27 MHz clock from the LMH1982 needs to be divided to provide a 13.5 MHz clock.

5 Reduced Functionality

Figure 3 shows the clocking structure for a system that can either have independent RX and TX datapaths or the TX datapath can be clocked using the clock from the LMH0341. Figure 3 does not show the always on clock used for state machine logic and the ZPU. The always on clock requires one global clock buffer. Subsections will only discuss datapath clocking and will not include the always on clock.

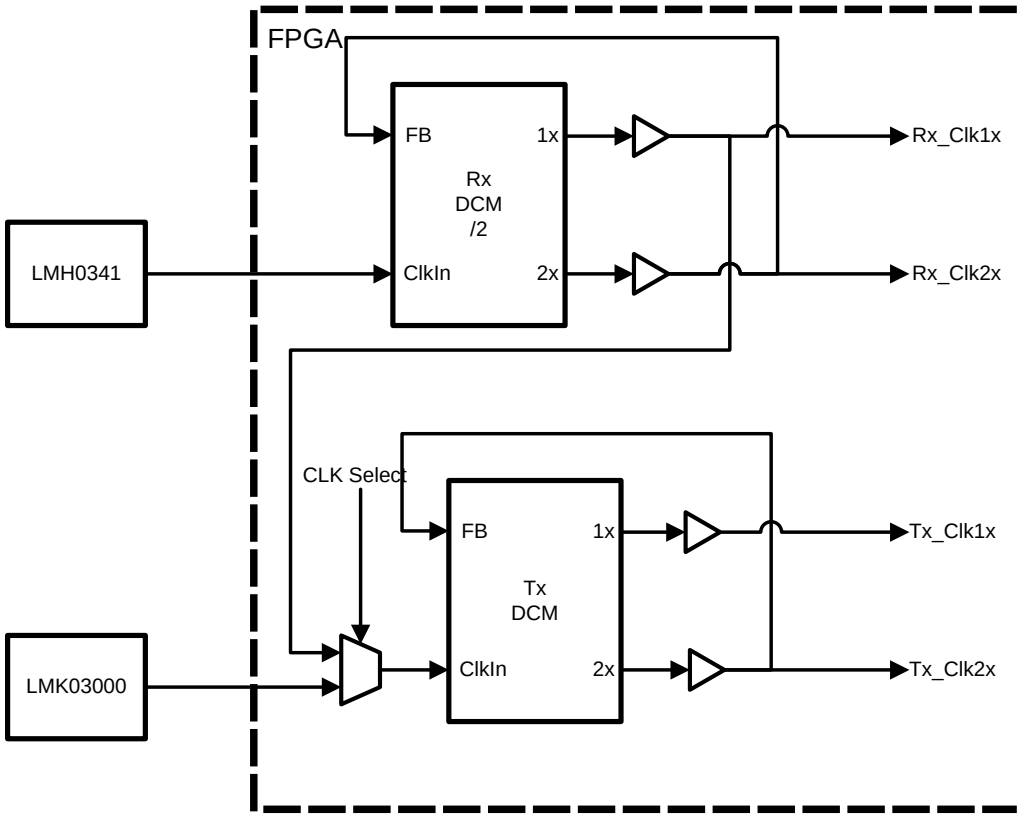

Figure 3. Clocking for Pass Thru and Independent RX and TX Data Paths

6 Independent RX and TX Paths

An independent RX datapath requires one DCM and two global clock buffers. For example, in HD pass though mode the LMH0341 sends a 148.5 MHz clock to the FPGA, which is divided by 2 in the RX DCM to generate a 1x (20 bit) 74.25 MHz clock and a 2x (5-bit DDR) 148.5 MHz clock synchronized to the input data. An independent TX datapath has the same clocking resource requirements as a independent RX datapath.

7 Combining RX and TX Paths

When combining RX and TX capability, the resources will increase depending on the functionality required.

In pass-through mode only, one DCM and two global clock buffers are required. The TX datapath uses the clocks from the RX datapath. The “CLK Select” BUFGMUX, TX DCM, and its two global clock buffers are not needed.

Independent RX and TX paths require two DCMs and four global clock buffers since the assumption is that RX and TX paths are on different clock domains. To combine pass-through mode and independent RX and TX datapaths, the “CLK Select” BUFGMUX is added to select the desired clock for the TX datapath.

8 Break Out of All SDI Resources

Subsequent sections will break out the resources used for various portions of the SDI FPGA IP. The data was obtained by removing sections of the full IP and running a build. A “Global Clocks” row was added to the summary tables to show how many BUFGMUXs are being used as global clock buffers. The following FPGA IP will be isolated:

- Full SDI FPGA IP
- Full SDI FPGA IP without the ZPU
- Transmit Only FPGA IP
- Receive Only FPGA IP
- Audio Only FPGA IP
- ASIC interface 5:20 and 20:5 and clocking

The FPGA resource utilization for various hardware implementations of the SDI stack, ZPU(CPU) control hardware, LMH0340, LMH0044, LMH0341, LMH01981, LMH1982, and DS25CP104 hardware interface are summarized below. The results were taken from Xilinx ISE 10.1.3 using the SDXILEVK daughter card and the Xilinx XtremeDSP Spartan-3A DSP 1800A baseboard. The results are not exact but should give a good idea of the resources needed for the specific implementations.

Table 2. Full SDI FPGA IP

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	3,947	33,280	11%
	4 Input LUTs	6,613	33,280	19%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	4,827	16,640	29%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	6	24	25%
	Global Clocks	5	8	63%
	DCMs	3	8	37%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	29	84	34%

Table 3. Full SDI FPGA IP without ZPU

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	3,517	33,280	11%
	4 Input LUTs	5,676	33,280	17%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	4,139	16,640	25%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	6	24	25%
	Global Clocks	5	8	63%
	DCMs	3	8	37%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	21	84	25%

Table 4. TX SDI FPGA IP without ZPU or Audio (TX Path Only)

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	913	33,280	3%
	4 Input LUTs	1,376	33,280	4%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	1,155	16,640	7%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	4	24	17%
	Global Clocks	3	8	38%
	DCMs	2	8	25%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	5	84	6%

Table 5. RX SDI FPGA IP without ZPU or Audio (RX Path Only)

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	940	33,280	3%
	4 Input LUTs	1,348	33,280	4%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	1,044	16,640	6%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	3	24	13%
	Global Clocks	3	8	38%
	DCMs	1	8	13%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	0	84	0%

Table 6. SDI FPGA IP Audio Only

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	1,664	33,280	5%
	4 Input LUTs	2,952	33,280	9%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	1,947	16,640	12%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	0	24	0%
	Global Clocks	1	8	13%
	DCMs	0	8	0%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	16	84	19%

Table 7. ASIC Interface, 5:20, 20:5 and Clocking

Logic Utilization		**Used**	**Available**	**Utilization**
	Slice Flip Flops	233	33,280	1%
	4 Input LUTs	171	33,280	1%
Logic Distribution		**Used**	**Available**	**Utilization**
	Occupied Slices	211	16,640	1%
Clock Utilization		**Used**	**Available**	**Utilization**
	BUFGMUXs	1	24	4%
	Global Clocks	5	8	63%
	DCMs	2	8	25%
Memory Utilization		**Used**	**Available**	**Utilization**
	RAMB16BWERs	0	84	0%

9 Summary

The triple-rate SDI FPGA IP utilization for the Spartan 3A 1800 series has been broken down into common IP usage; full SDI (without ZPU) and individual transmit and receive functions. The application report also details the clocking requirements of the IP and the LMH0340 saves using an extra DCM by delaying the clock and data paths. After the complete triple rate SDI IP has been implemented, over 80% of logic gates, 75% FPGA memory resources and 30% of clocking resources remain. The triple rate SDI FPGA IP provides broadcast video system designers a comprehensive platform for rapid evaluation and prototyping of new designs to reduce time to market.

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