Making of IEEE 802.3 Compliant Equipment

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White Paper

Making of IEEE 802.3 Compliant Equipment

--- A Discussion on Interoperability of Ethernet Over Copper

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1 Introduction

The objective of this paper is to create awareness of the interoperability issues among the products designed and manufactured by different vendors. The interoperability issues have impacted the business growth, rapid adopting technology and, profitability. The focus of the discussion is on Ethernet implementation over copper. The issues highlighted are related to 1000BASE-T and 100BASE-TX.

This paper also highlights the work carried out by the Interoperability Lab at University of New Hampshire (IOL at UNH) to ensure the IEEE standard compliance. The discussion also carries to the approaches National Semiconductor has taken to avoid interoperability issues and what original equipment manufacturer/original design manufacturer (OEM/ODM) vendors can to do to prevent producing noncompliant products. After all, the issues centered on interoperability are mainly attributed to each vendor's philosophy and test procedures.

2 Case Studies

It takes IEEE committee years and numerous meetings to draft and pass standards. The endeavor is to create a conformance among the products designed and manufactured by different vendors. The compliance to the standard allows products from different vendors to interoperate seamlessly without any adapting alteration. Regardless of the efforts made in creating the standards, this paper reviews what has encountered in the Ethernet real world due to lack of conformance to the standards. The following are the cases found at the National Semiconductor PC and Networking Group (PCNG) laboratory during the system level test and interoperability test. These cases showed that the devices from different vendors were not able to operate with each other.

2.1 Gigabit Ethernet

2.1.1 Incorrect Polynomial Sequence

In one case, the polynomial sequence algorithm implemented in the silicon caused the devices not to operate with each other. During PCNG silicon interoperability test, it was found that a vendor's product could only link and communicate with its own gigabit products but not with other vendor's Ethernet products. After days of laboratory testing and analysis, the PCNG design team found that the transmission implementation in the physical coding sublayer (PCS) of that vendor's silicon was incorrect.

According to the IEEE 802.3ab section 40.3.1.3.1, the PCS transmit function employs side-stream scrambling. The slave transmitter side-stream scrambler generator polynomial is as follows

$$G_S(x) = 1 + x^{20} + x^{33}$$

The master transmitter scrambler is

$$G_M(x) = 1 + x^{13} + x^{33}$$

That vendor implemented different polynomial sequences in their transmitter causing other vendor's parts not being able to establish link. Finding the root cause of the incompatibility, National Semiconductor was able to solve the problem by implementing a special "non-compliant" mode to work with that vendor's non-compliant devices in additional to the IEEE 802.3ab compliant mode making the National device more tolerant and user friendly.

2.1.2 Excessive Timing Jitter

In other cases, the non-compliance is not caused by the silicon design but rather caused by using out of tolerance peripheral parts.

For example, in order to meet jitter specification per IEEE 802.3 standard, the gigabit reference clock jitter has to be within certain tolerance. The external reference clock provides a clock source for the internal phase lock loop (PLL) clock generator that generates the clock for internal use and data transmission. The PLL has a feedback loop that acts as a low pass filter (LPF). The LPF function is to filter out high frequency clock jitter. The bandwidth of the LPF limits the jitter filtering frequency. If the external clock source has jitter in the low frequency bandwidth (i.e., in the passing bandwidth), this low frequency jitter will pass through the whole silicon and eventually show up on the data transmission outputs.

In the Gigabit operation, one device is the master that sources the clock through data transmission and, the other link partner device will be the slave that recovers the clock from the master's transmission. In the case that the master is transmitting with excessive low frequency jitter, the slave device may not be able to recover the clock from the master. The failure is commonly referred as "out of frequency lock range".

To prevent such incompatibility between master and slave devices, the IEEE 802.3ab section 40.6.1.2.5 specifies the transmitting timing jitter. The master mode transmit jitter is measured by adding the transmit test clock jitter and the transmit data out jitter. The specification limits this jitter to be under 300 ps.

During the interoperability lab test, it was found that some vendor's transmit jitter to be 1,260 ps, grossly exceeded the 300 ps limit (Figure 1). The excessive jitter can cause link partner's clock recovery circuitry to fail and it will be shown as inability to establish stable link. The transmit jitter of a compliant device is shown in Figure 2.

Further analysis also revealed that the system vendor used a clock distribution circuit to distribute clock to multiple physical layer devices. The clock distributor had excessive jitter.

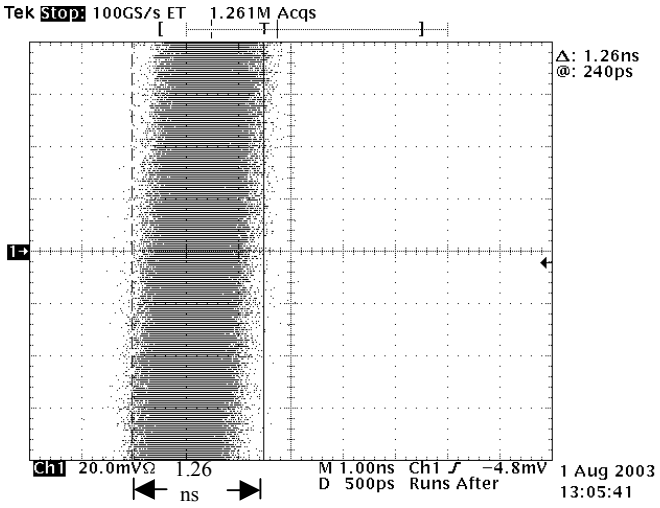

Figure 1. Excessive jitter measured at the Jtxout in IEEE 802.3 gigabit Test Mode 2 on a non-compliant GPHY device. The captured is the rising edge of the Test Mode 2 waveform.

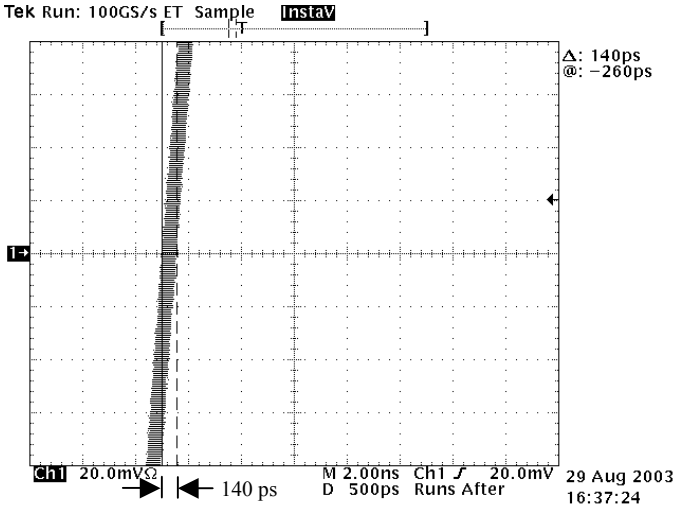

Figure 2. Typical jitter measured at the Jtxout in IEEE 802.3 gigabit Test Mode 2 on a compliant GPHY device.

2.2 100BASE-TX

2.2.1 VOD Amplitude Out of Tolerance

According to IEEE 802.3 section 25.2 and ANSI 3.263 section 9.1.2.2, the 100BASE-TX waveform peak amplitude should be

$$950 \text{ mV} < Vout_{p-p} < 1050 \text{ mV},$$

that is ±5% of the 1V nominal output voltage. During the interoperability tests, it was found that some vendor's part has as much as 20% deviations. (Figure 3)

A typical behavior with exceedingly high 100BASE-TX VOD is that the link partners are not able to achieve link at short cable length, but are able to obtain link at longer cable length. At shorter cable length, there is minimum signal attenuation and the transmitted signal would exceed link partner amplifier input range or the ADC input range. The exceedingly high amplitude signal causes clipping so that the signal cannot be recovered. At longer cable length, the high amplitude transmitted signal is attenuated to be within the link partner's input tolerance so that the part links normally.

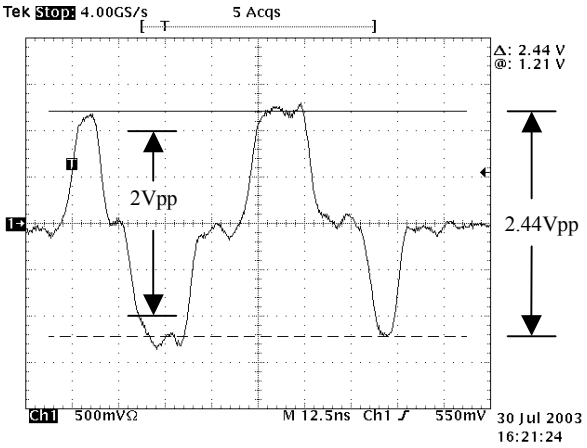

Figure 3. 100BASE-TX MLT-3 waveform captured at Jtxout. The peak of the waveform is above the IEEE limit.

At other occasions, the link partner has found the output amplitude tolerance could be as much as 25% below nominal voltage. (Figure 4)

With low amplitude, the data link would work fine at shorter cable length but not at longer cable reach. At longer cable reach, the signal amplitude becomes very tiny after cable attenuation and making it difficult for the link partner to recover.

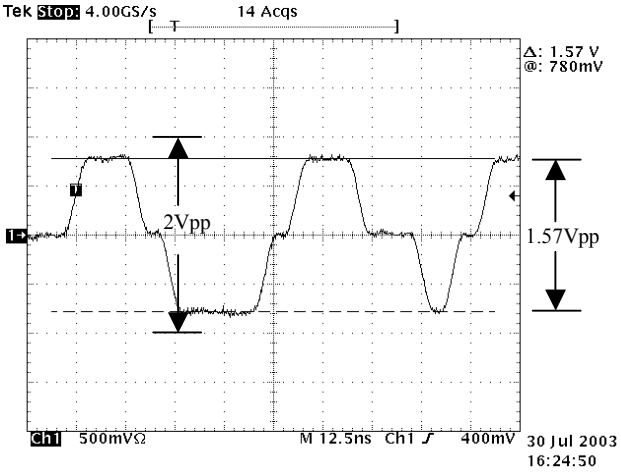

Figure 4. 100BASE-TX output waveform captured at Jtxout. The peak amplitude is below the IEEE limit.

2.3 Other Non-compliance

System vendors are constantly pressured by market competition and by their customers in lowering the cost. The component selection process is an easy place to cut the system cost. However, this process should not be dictated merely on pricing. Much of the emphasis should be on the quality of the peripheral components.

The two most important peripheral components for the gigabit PHY are:

1) The clock generator

2) The isolation transformer.

For this reason, these components' requirements are listed in the "Component Selection" of the National Semiconductor datasheet or design notes. The system vendor should verify whether the clock oscillator or clock crystal, and the transformer candidates are meeting the requirements of the physical layer device. For the convenience of the board designer, a few tested clock and transformer component vendor part numbers are also listed in the component selection of the design notes.

As mentioned in section 2.1.2, the clock oscillator would affect the frequency lock of the slave link partner device. The important specifications to watch for are (1) frequency stability within the operating temperature, (2) cycle-to-cycle jitter, (3) accumulative jitter, (4) rise and fall time, (5) symmetry.

Just as the clock oscillator, the isolation transformer also has great impact on the transmitted signal being IEEE compliant. The transformer specification has a large impact on the Gigabit transmit template and the cable length performance. The key specifications are (1) turn ratio, (2) insertion loss, (3) return loss differential to common rejection ratio, (4) crosstalk, (5) rise time, (6) isolation.

3 Prevent Making of Non-compliant Products

There are three steps recommended for the Ethernet system vendor to prevent making the non-compliant or none interoperable products. These three steps cover (1) the component qualification, (2) in-house board level testing, and (3) outside agency testing.

3.1 Silicon Vendor Selection

Driven by time-to-market, some silicon manufacturers may sacrifice the quality for delivery. At National Semiconductor, time-to-market and quality are equally important. At National, there are processes to ensure the thoroughness of the silicon device testing before releasing to the customer. There are established procedures to ensure the coverage of the production ATE tests.

In the silicon qualification process, most system vendors have the capability to test the silicon device for IEEE 802.3 compliance. This is highly encouraged by National Semiconductor. The more the test coverage of the standard, the higher the confidence that the silicon will interoperate with other vendor's Ethernet devices and also guarantee the performance of the silicon. A recommended device checklist is attached in the appendix.

In the case that the Ethernet system vendor does not have the capability or resources to fully test the silicon device, a request for test report may be made to the silicon vendor to ensure that the silicon is being properly tested and passed the tests before releasing to the system manufacturers.

3.2 In-house Board Level Tests

National provides demo vehicle to show the GPHY performance. The demo board is used by the system vendor to evaluate the GPHY compliance and performance.

Most system vendors have the capability to extensively test and evaluate the GPHY using the demo system. A typical set of tests are listed as follows:

- Interoperability with other vendor's PHY
- Auto negotiation and parallel detection
- Cable reach performance
- IEEE template testing

These tests assure that the silicon delivered will adhere to the IEEE specifications and will interoperate with other vendor's GPHY.

3.3 UNH- IOL

Although it is not the scope of this paper to review the organization of the Interoperability Lab at University of New Hampshire (UNH-IOL), the UNH-IOL is mentioned here because of what it can offer to prevent interoperability problem. It needs to be emphasized that IOL testing is performed from a quality assurance point of view not from product marketing or promotions point of view. Therefore, consortium agreements limit the disclosure of specific product test results to respective members only.

The UNH-IOL is a fee-based testing service. Companies pay an annual consortium membership fee and donate at least one of the products that they wish to test to the IOL. The requirement to leave a platform at the IOL allows the users of the lab to perform interoperability testing with current equipment throughout the year and without having to make special legal arrangements with other players in the technology. This becomes one of the major benefits of consortium membership: the ability to test against other vendors' products in a neutral setting without having to incur the capital expense of setting up and operating individual vendor test facilities. Consortiums within the IOL use the same facilities and tools, and thus are able to build on each other's work. By using this simple cooperative approach, the IOL has quietly built an extensive interoperability test environment, kept costs to a minimum, and provided for incremental growth through new consortiums.

The objectives of the UNH-IOL are to provide a long-term independent facility where products including Ethernet products can be tested in a heterogeneous environment operating outside of normal Ethernet design limits. The interoperability tests and testing procedures provide a high level of confidence in product interoperability. In the case that problems do surface during the test, UNH-IOL could also assist to diagnose and resolve the issues.

To the Ethernet vendors, UNH-IOL also provides a forum for the exchange of technical information between consortium members concerning issues related to Ethernet networks and products. Because of its involvement of the standards development, the issues and concerns are brought to the standards committee for reviewing or revision. Especially in interpreting and resolving conflicts or inconsistencies within the specifications, UNH-IOL could contribute significantly to prevent any future misinterpretation of the standards leading to interoperability issues.

To find out more detailed information about the UNH-IOL, what the organization can do to benefit the products, please refer to the website in the reference section and appendix section.

3.4 Conclusion

The impact of making non-compliant equipment could be very negative. There are untold stories of delayed shipment causing loss of profit margin due to price erosion, return of merchandize for costly replacement that leads to loss of profitability. All these events would also have a negative impact on company's reputation.

Non-compliance also can unfairly impact the link partner device vendor. The link partner vendor may have to increase specification tolerance in order to interoperate with the non-compliant device. This could sometimes be a controversy and a challenge. Many questions arise, such as how much should R&D over-design to cope with out of spec parts? Looking at the IEEE 1500-page 802.3 standard, which specification should a vendor over design for? The great irony is that if each and every vendor's products do not comply with the standards, then the IEEE standard becomes a lost cause.

There are three ways to prevent the making of the non-compliant equipment. They are “test, test, and test”. Only by exhaustive test of the device before shipping can a vendor guarantee the quality of the product – be paranoid of product quality.

When it comes to re-spin the silicon, no matter if it is a major spin to add more features or a minor spin to improve one small aspect of the device, the whole test suite must be repeated to ensure nothing else is affected by the device change. At National Semiconductor, a comprehensive test suite from design validation and verification, IEEE compliance tests, tolerance and performance test, interoperability test, ATE and bench correlation to ATE characterization are established to ensure the released silicon meets standards and the manufactured silicon is being screened thoroughly.

Present industry trend is toward multi-port GPHY device with higher levels of integration. The number of tests multiplies as the port count increases. Not only must each port be tested and screened for compliance, but also the interactions between the ports are examined. To address the increased number of tests for each port on a multi-port device, National Semiconductor has implemented automated test using computer control to cycle through the suites of the tests for each port without human intervention. This has greatly improved the test efficiency and the test coverage. All these verification and test procedures are a reflection of the National’s Quality Policy, i.e., **“To continuously improve our processes, products, and services to deliver solutions of the highest value, thereby providing a competitive advantage to our customers”**.

4 Appendix

UNH-IOL 1000 BASE-T Test Suites

- 1000BASE-X MAC Test Suite
- 802.3x Flow Control Test Suite
- Clause 28 Auto-Negotiation State Machine Test Suite
- Clause 28 Auto-Negotiation Next Page Test Suite
- Clause 28 Auto-Negotiation Management Register Test Suite
- Clause 28 Auto-Negotiation Management System Test Suite
- 1000BASE-T PMA Test Suite
- Interoperability Test Suite

http://www.iol.unh.edu/testsuites/ge/

http://www.iol.unh.edu/consortiums/ge/grouptest/oct03gtp/GTP_test_plan.pdf

UNH-IOL 100 BASE-TX Fast Ethernet Test Suites

- Clause 4 Media Access Control (MAC) Test Suite
- 100BASE-X PCS Test Suite
- Clause 25 Physical Medium Dependent Test Suite
- Clause 28 Auto-Negotiation State Machine Base Page Exchange Test Suite
- Clause 28 Auto-Negotiation Next Page Exchange Test Suite
- Clause 22, 28, and 40 Management Registers Test Suite
- Clause 28 and 40 Auto-Negotiation Management System Test Suite
- Clause 28 and 40 Auto-Negotiation Management System Test Suite
- Interoperability Test Suite

http://www.iol.unh.edu/testsuites/fe/

UNH-IOL 10 BASE-T Test Suites:

- Clause 4 Media Access Control (MAC) Test Suite

- 10BASE-T Repeater Test Suite
- IOL 10BASE-T test suite for an embedded MAU
- IEEE 10BASE-T abstract test suite for an external MAU

http://www.iol.unh.edu/testsuites/10baset/

5 References

IEEE Standard 802.3, "**Part3: Carrier sense multiple access with collision detection (CAMA/CD) access method and physical layer specifications**", 2000 Edition.

UNH-IOL website : http://www.iol.unh.edu/

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