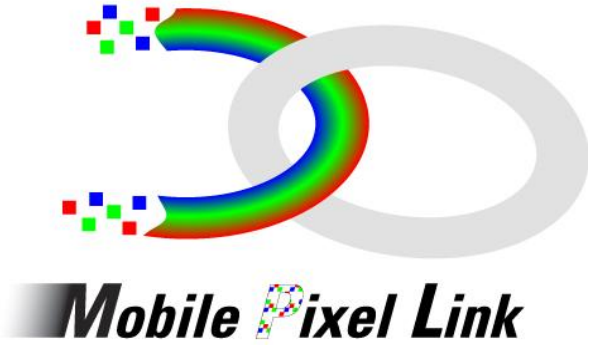
Mobile Pixel Link Level-0



Definition:
Mobile Pixel Link Level Zero (MPL Level-0) defines the electrical specifications, clocking and bit order for three video interfaces; these include image sensors, RGB displays and CPU-style displays. MPL Level 0 is intended for use within a mobile handheld device environment.

Purpose:
To provide a solution to the problems associated with wide parallel video data interconnects. MPL Level 0 reduces wires, power, and radiated EMI without sacrificing speed.

Version 0.9

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1 Overview

System and module makers have a huge problem with wide parallel interconnects now. MPL-Level 0 provides a cost-effective solution to that problem. It uses a protocol that directly serializes the legacy CPU, display, and image sensor parallel interfaces. In doing so, it necessarily carries a large overhead that would not be needed if the interface were one that included a more optimal packetized interface that MPL-Level 1 intends to use. So while MPL-Level 0 does provide a narrow, low-power, low-EMI interconnect to displays and cameras, it does not optimize its use of bandwidth or provide a standard programming model.

MPL-Level 1 is intended to take full advantage of the architectural breakpoint in moving from parallel to serial interfaces. It implements a modern packetized video interface that integrates command and data paths and optimizes the use of link bandwidth. National believes that a collaborative effort between handset OEMs, module, and semiconductor makers is necessary to complete MPL-Level 1.

MPL uses a Master-Slave, point-to-point bi-directional physical interface for the CPU Modes support and unidirectional interface for Camera and RGB Display support. Since MPL is physically a point-to-point interface, a Master-Slave method of media access removes the need for any arbitration. The Slave only responds to commands from the Master, thus the directional state of the bus is easily determined at all times. Provision is made for a Slave that has been powered down by the Master to awaken that Master at will.

1.1 Licensing

MPL Level 0 is released into the public domain by National Semiconductor and does not require a royalty payment or license fee for any implementation that conforms to this specification.

1.1 Interface Model

MPL standardizes three common parallel interfaces:

- CPU Modes (i80 and m68 types)
- RGB Displays
- Image Sensors

MPL does not correspond to the ISO Open Systems Interconnect model, but for reference includes elements from the PHY and LINK layers.

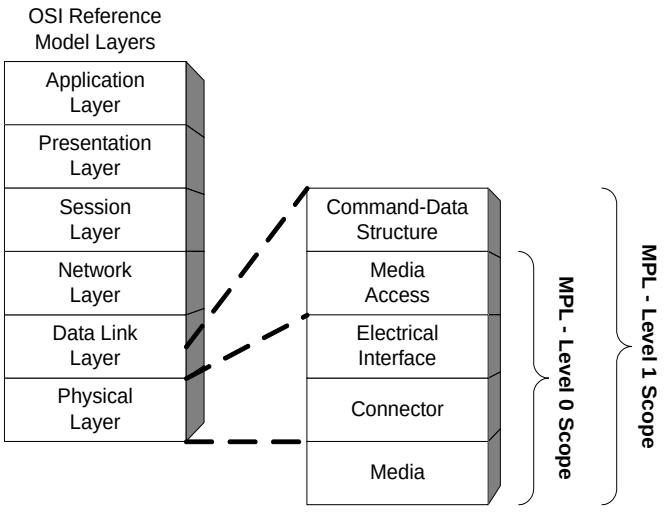

Figure 1 - Standard Scope

1.2 Standard Objectives

It would be very easy for this interface to grow into a much more general purpose communication standard which, while attractive from a functional standpoint, would likely diverge and damage the original purpose behind its creation. MPL is only meant to replace existing display, camera, and other video physical bus standards. Its fundamental purpose is to fill a need not currently addressed by existing standards, while making the minimal hardware and software changes to existing interfaces and command sets.

Choices on each function and feature should be guided by certain principles. MPL must achieve lower power consumption than the alternatives and it must do so with lower radiated EMI. It must also be low cost to both ends of the system, while easily implemented in existing semiconductor processes. It must also be open from the onset and as free as possible from patent licensing restrictions. MPL Level-0 achieves these goals and adheres to the following principles.

- Few Wires – Clock and Data (1 or 2 lines)
- VERY Low Power and EMI
- Initial Speed to Accommodate VGA format cameras and displays, yet be scalable to gigabit per second link speeds. Initial speeds will range from 160Mb/s to 320Mb/s using one or two data lines.
- Short Distance Internal-only Interconnect (~0.2m typ.)
- Simple Protocol – Low Gate Count
- Low voltage, supply independent
- Initially Video or Graphic Data Only
- Point to Point, Bi-directional Link
- Open Standard

To maximize the interoperability of multi-vendor systems, options should be eliminated or minimized. To the extent options or vendor-unique implementations are allowed, interoperability suffers.

1.2.1 Application Drivers

Although MPL could accommodate many interconnected devices within a handheld mobile environment, its quintessential use is between a Baseband Processor (BBP) or Application Processor and color TFT LCD displays and Camera modules. These applications drive the standard because only when the color depth and pixel count of these displays are utilized, and a camera function is added to handheld devices do the power consumption and interface width (and therefore connector and cable cost) undergo a step function increase.

It is these two device types, represented by three popular legacy interface types, that constitute the focus of MPL Level-0**Reference Documents**

- LM2501 Data Sheet – National Semiconductor, www.national.com/appinfo/mpl
- LM2502 Data Sheet – National Semiconductor, www.national.com/appinfo/mpl

1.4 Standard Scope

MPL Level-0, as defined by the interface model, defines a complete data link for the three legacy interfaces described. It does not include definition of the legacy parallel interface itself. The highlighted section of each of the following diagrams shows the scope of what is standardized in MPL Level-0.

1.4.1 CPU Modes (i80 and m68 types)

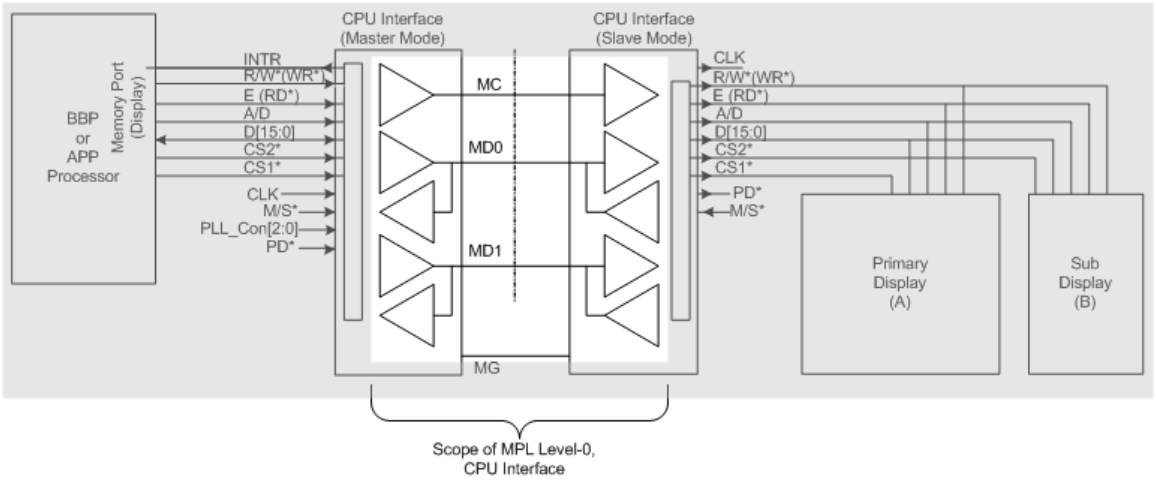

Figure 2 - CPU System

1.4.2 RGB Displays

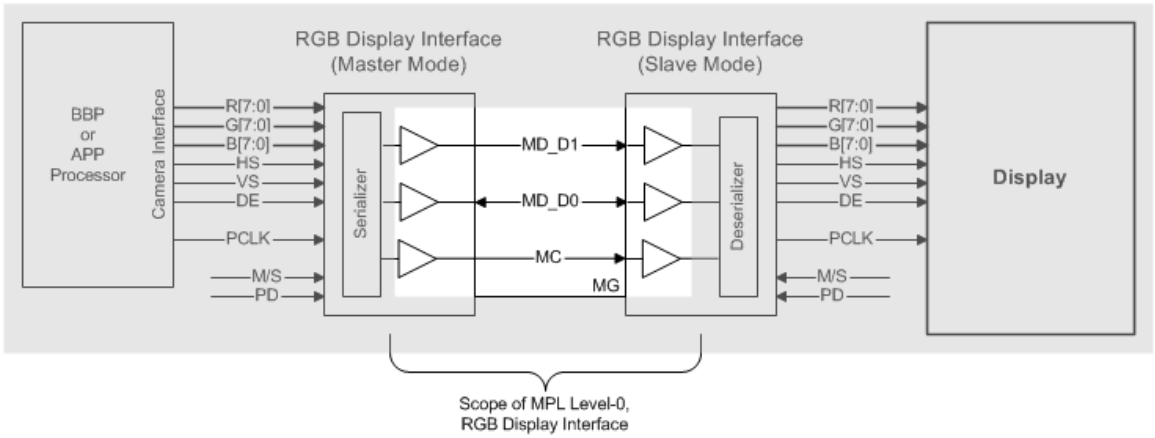

Figure 3 - RGB Display System

1.4.3 Image Sensors

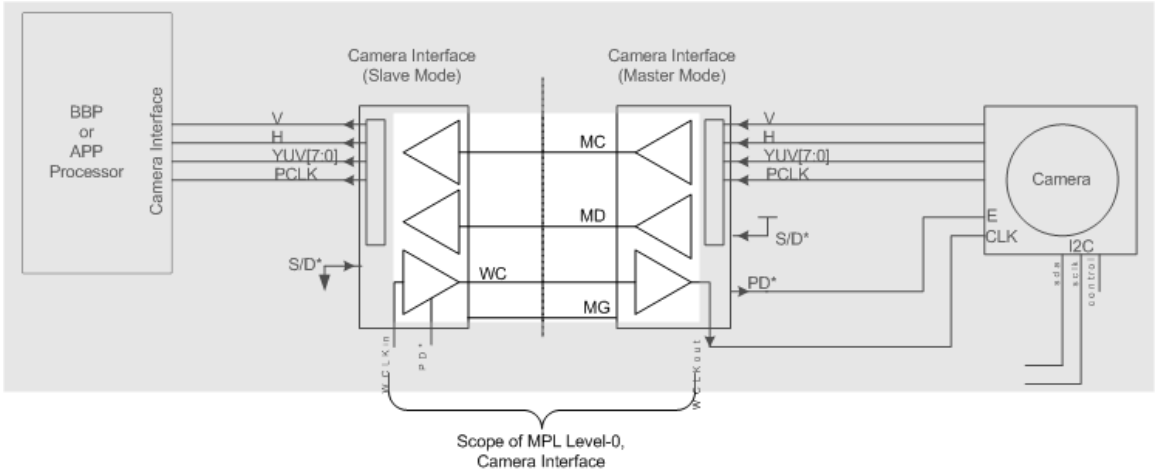

Figure 4 - Camera System

2 Serial Bus Operation – Common Features

2.1 Bus Overview

The MPL Level-0 bus is simple 3-line interface that is intended to replace wide low voltage CMOS video busses inside handheld portable devices. MPL is a point-to-point bus that provides a bi-directional half duplex link. Bus control and a single-direction Clock are provided by the Master. Data may be driven by the Master or the Slave. Various data rates are supported with initial applications targeted at 160 Mbps. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver.

The MPL interface is designed to be used with common 50 Ohm lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 0.2 meters, although the interface is capable of longer distances.

2.2 Serial Data Signaling Rates

The basic data rate for the MPL Level-0 transceiver is up to 160 Mbps in the Master to Slave direction. In this mode the maximum transmission rate is 160 Mbps (6.25 ns unit interval), and the clock is 80 MHz since both edges of the clock are used. Using both edges allows for a low frequency clock signal (vs 160 MHz single edge), which aids in reducing EMI. For the back channel, (Data flow from Slave to Master) only the rising edge of the clock is used by the slave to gate the data, allowing more time for data sampling in the Slave-to-Master direction based on the Master supplied clock. By maintaining the 80 MHz clock, an 80 Mbps back channel transmission rate is supported.

It is foreseen in the future that the physical layer is capable of operating into the gigabit per second range. These higher data rates are under study now.

2.3 Serial Bus Timing

The following figures provide information about the bus timing for the two directions of the bus.

For the Master to Slave direction (Master sends both Clock and Data) data valid is relative to both edges as shown in Figure 5. Data valid is specified as:

- Setup and Hold around Rising Edge of Clock
- Setup and Hold around Falling Edge of Clock

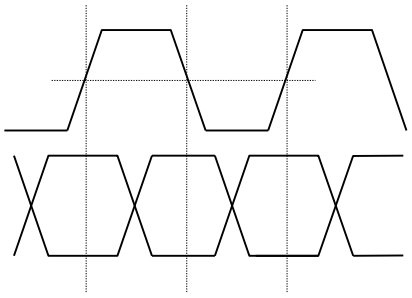

Figure 5 – Master-to-Slave Timing (MC, MDm)

For the Slave to Master direction (Master provides Clock, Slave provides Data) data is gated by the rising edge only as shown in Figure 6.

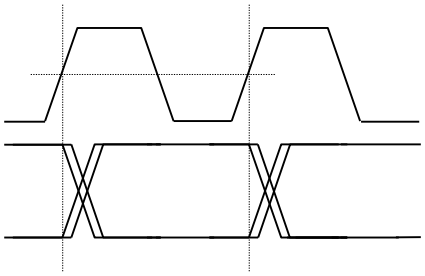

Figure 6 - Slave-to-Master Timing (MC, MDs)

2.4 Serial Bus Phases

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. Two of the bus phases have options. The MPL bus phases are shown in Table 1.

Name		MC state	MD state	Phase Description
OFF (O)		0	0	Link is Off
IDLE (I)		A	L	Data is static (Low)
ACTIVE (A)	Command (C)	A	X	Command information
	Turn Around (TA', TA")	A	L/0/L	Turn Around – MD line is OFF to turn around the direction
	Data In (DI)	A	X	Data In (Read) – includes command, TA, Data In, TA sub phases
	Data Out (DO)	A	X	Data Out (Write) – includes command, Data Out phases
LINK-UP (LU)	Master (M)	H	-	Master initiated Link-Up
	Slave (S)	-	H	Slave requested Link-Up
	Dual (D)	H	H	Dual requested Link-Up

Notes on MC / MD Line State:

0 = no current (off)
L = Logic Low – The higher level of current on the MC and MD lines
H = Logic High – The lower level of current on the MC and MD lines
X = Low or High
A = active clock

Table 1 - Link Phases

2.5 Bus Power Up or Start Up Timing

Start up timing varies depending on the legacy interface and is covered in the specific sections for each interface.

2.6 Power-Off

In the power-off state, both MD(0) (and MD1 if used) and MC are turned off with zero current flowing. This is considered the Power-Off bus phase and the transition off may occur after the last data bit time or at any time afterwards from an Idle phase as shown in Figure 7.

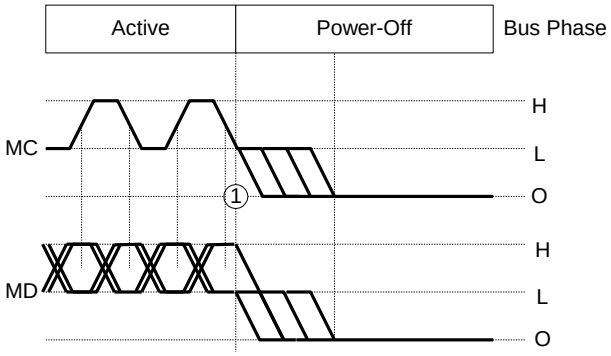

Figure 7 - Bus Power Down Timing

The link may be powered down by asserting the Master's PD* input pin (Low). This causes the Master to immediately put the link to the OFF Phase and internally enter a low power state. When the Slave detects a lack of current flow on the MC it will immediately also enter a low power state and assert its PD* output pin (Low). In CPU mode, to avoid loss of data the Master's PD* input should only be asserted after the MPL bus has been in the IDLE state for at least 5 MC clock cycles. This gives the Slave enough time to complete any write operations received from the MPL bus.

3 CPU Modes Protocol

Some timing diagrams necessarily show signals and signal timing for the legacy parallel interfaces. This is done for clarity and is not to be considered part of the MPL Level-0 Standard or requirements for interoperability with that standard.

3.1 Bus Power Up

In the Serial Bus OFF phase, Master transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the Master and the Slave are internally held in a low power state. When the Master's PD* input pin is de-asserted (driven High) and if used, the Master enables its PLL and waits for enough time to pass for its PLL to lock. After the Master's PLL is locked (t0 = 4,096 CLK Cycles), the Master will perform an MPL start up sequence. The PLL is not part of the MPL Level-0 standard, but time is included in the protocol to allow for implementations that contain PLL clock multipliers.

The MPL start up sequence gives the Slave an opportunity to optimize the current sources in its transceiver and to emerge from its low power state. The Master begins the sequence by driving the MC line logically Low for 11 CLK cycles (t1). During this part of the sequence the Slave's transceiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the Master drives the MC line logically HIGH for 11 CLK cycles (t2). On the Low-to-High transition of the MC – point B – the Slave latches the current source configuration. This optimized configuration is held as long as the MPL remains up. Next, the Master drives both the MC and the MD lines to a logical Low for another 11 CLK cycles (t3), after which it begins to toggle the MC line at a rate determined by its PLL Configuration pins. The Master will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point the MPL bus may remain in IDLE phase, enter the ACTIVE phase or return to the OFF phase. Active data will occur at the Slave output latency delays (Master + line _+ Slave) after the data is applied to the Master input. Possible start points are shown by the "C" arrow in Figure 8.

After seven subsequent MC cycles the Slave will start toggling its CLK pin at a rate configured by its CLK Divisor. The Slave then waits an additional 17 CLK cycles before de-asserting its PD* Output pin (t4). Implementation of the PD* pin is not mandatory.

In the Figure 8 example, an IDLE bus phase is shown until point C, after which the bus is active and the High start bit on MD initiates the transfer of information.

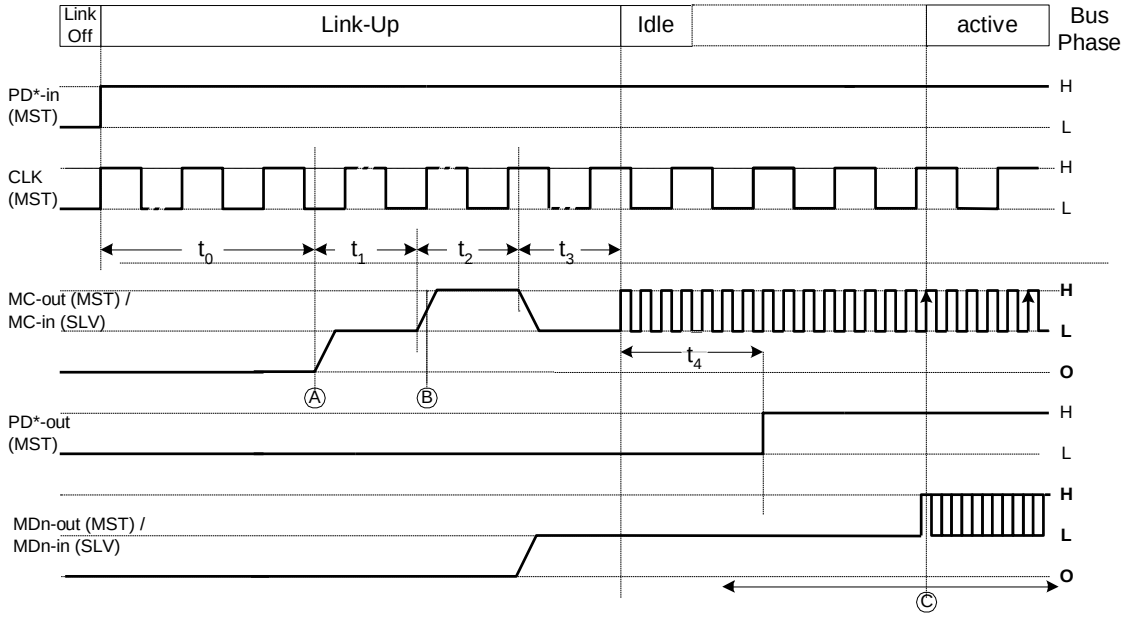

Figure 8 - Bus Power Up Timing

3.2 CPU Interface Compatibility

The CPU Interface mode provides compatibility between a CPU Interface and a small form factor (SFF) Display or other fixed I/O port application. Two options are allowed:

Mode	Description
0	m68 Interface (E, R/W*), 16-bit support
1	i80 Interface (WR*, RD*), 16-bit support

Table 2 - Modes

It is not required that both the Master and the Slave to be configured in the same mode. For example the Master may be configured as an i80 interface while the Slave is configured for an m68 interface. CPU interface mode translation may be accomplished in this manner.

Control information is carried over both MD lines. MD0 carries the D0-7 data bits while MD1 the D8-15 data bits. See Figure 9.

3.3 WRITE Transaction

The WRITE transaction consists of two MC edges of control information followed by 8 MC edges of write data. Since WRITE transactions transfer information on both edges of MC it take 5 MC cycles to complete a write transaction. The MD0 line carries the Start bit (High), the A/D (Address/Data) bit and then the data payload of 8 bits (D0-7). The MD1 line carries the R/W* bit (Read/Write*), the CS1/2 bit and then the data payload of 8 bits (D8-15). The data payload is

sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* LOW is not allowed.

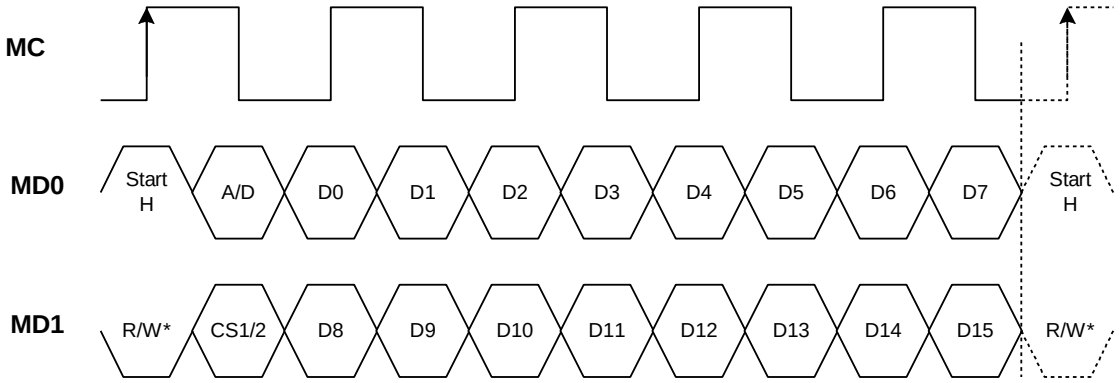

Figure 9 - Write Transaction

3.4 READ Transaction

The READ transaction is variable in length. It consists of four sections.

In the first section the Master sends a READ Command to the slave. This command is sent in a single MC cycle (2 edges) and uses a similar format to the 1st cycle of the WRITE transaction. The MD0 line carries the Start bit (High) and the A/D (Address/Data) bit. The MD1 line carries the R/W* bit (High for reads) and the CS1/2 bit.

In the second section (TA') the MD lines are turned around, such that the Master becomes the receiver and Slave becomes the transmitter. The Slave must drive the MD lines low by the 14th clock edge. It may then idle the line at the Logic Low state or drive the line High to indicate that read data transmission is starting. This ensures that the MD lines are a stable LOW state and that the Low-to-High transition of the "Start" bit is seen by the Master.

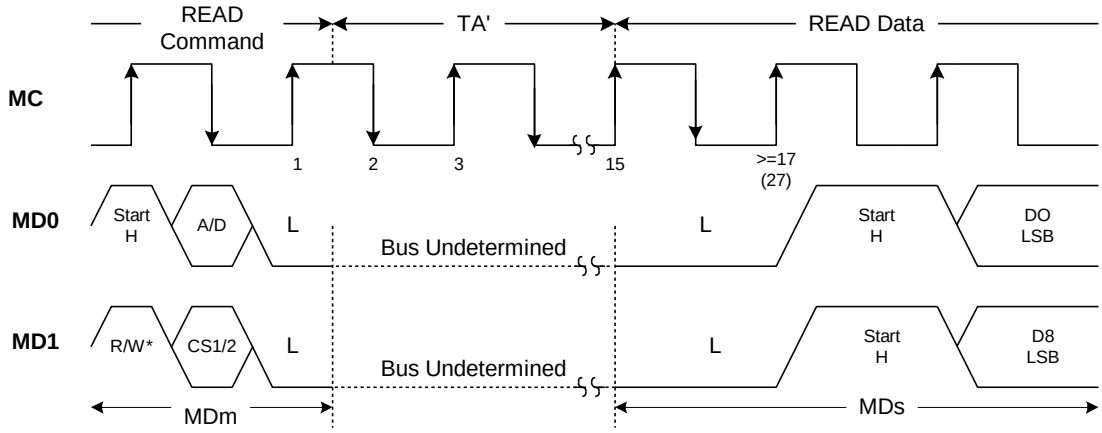

Figure 10 - READ Command and TA'

The third section is consists of the transfer of the read data from the Slave to the Master. Note that the READ_Data operates on single-edge clocking (Rising Edge ONLY). Therefore the back channel data signaling rate is ½ of the forward channel (Master-to-Slave direction). When the Slave is ready to transmit data back to the Master it drives the MD lines High to indicate start of read data, followed by 8 MC cycles of the actual read data payload. As in the WRITE command MD0 carries D0-7 and MD1 carries D8-15.

The fourth and final section (TA") occurs after the read data has been transferred from the Slave to the Master. In the fourth section the MD lines are again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the MD lines Low for 1 bit with and then turns off. The MD lines are off momentarily to avoid driver contention. The Master then drives the MD line Low for 1 bit time and then idles the bus until the next transaction is sent.

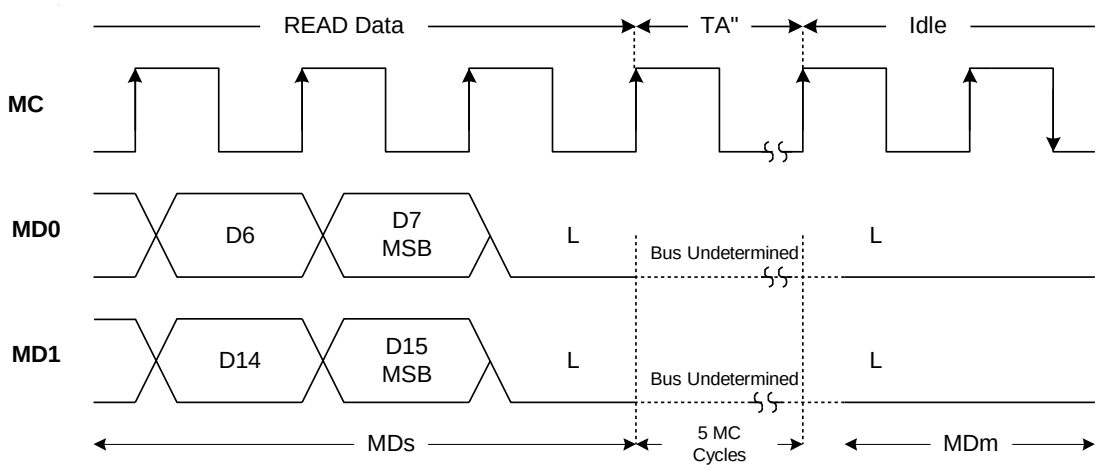

Figure 11 - READ Data and TA"

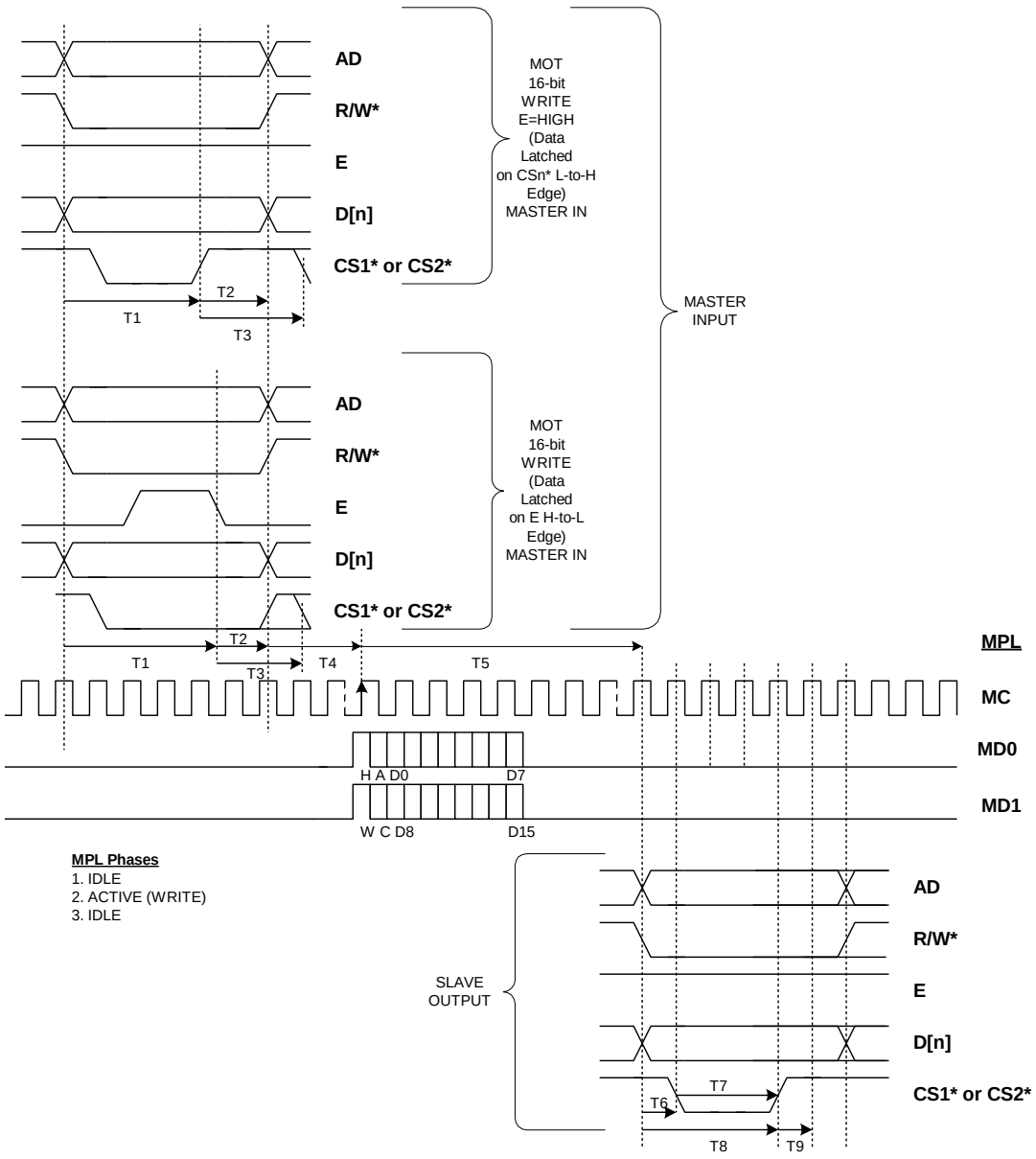

Figure 12 - WRITE – m68 Interface

No.		Parameter	MIN	TYP	MAX	Units
T1	MasterIN	Data Setup Time before ChipSelect* Low-High (or E High-Low)	TBD	3.6		ns
T2	MasterIN	Data Hold after ChipSelect* Low-High (or E High-Low)	0	TBD		ns
T3	MasterIN	ChipSelect* Recovery Time		TBD		MC cycles
T4	Master	Master Latency		4		MC cycles
T5	Slave	Slave Latency		8		MC cycles
T6	SlaveOUT	Data Valid before Chip Select* High-Low		1		MC cycles
T7	SlaveOUT	CS* Low Pulse Width		3		MC cycles
T8	SlaveOUT	Data Valid before ChipSelect* Low-High		4		MC cycles
T9	SlaveOUT	Data Valid after ChipSelect* Low-High		1		MC cycles

Table 3- WRITE – m68 Interface Parameters

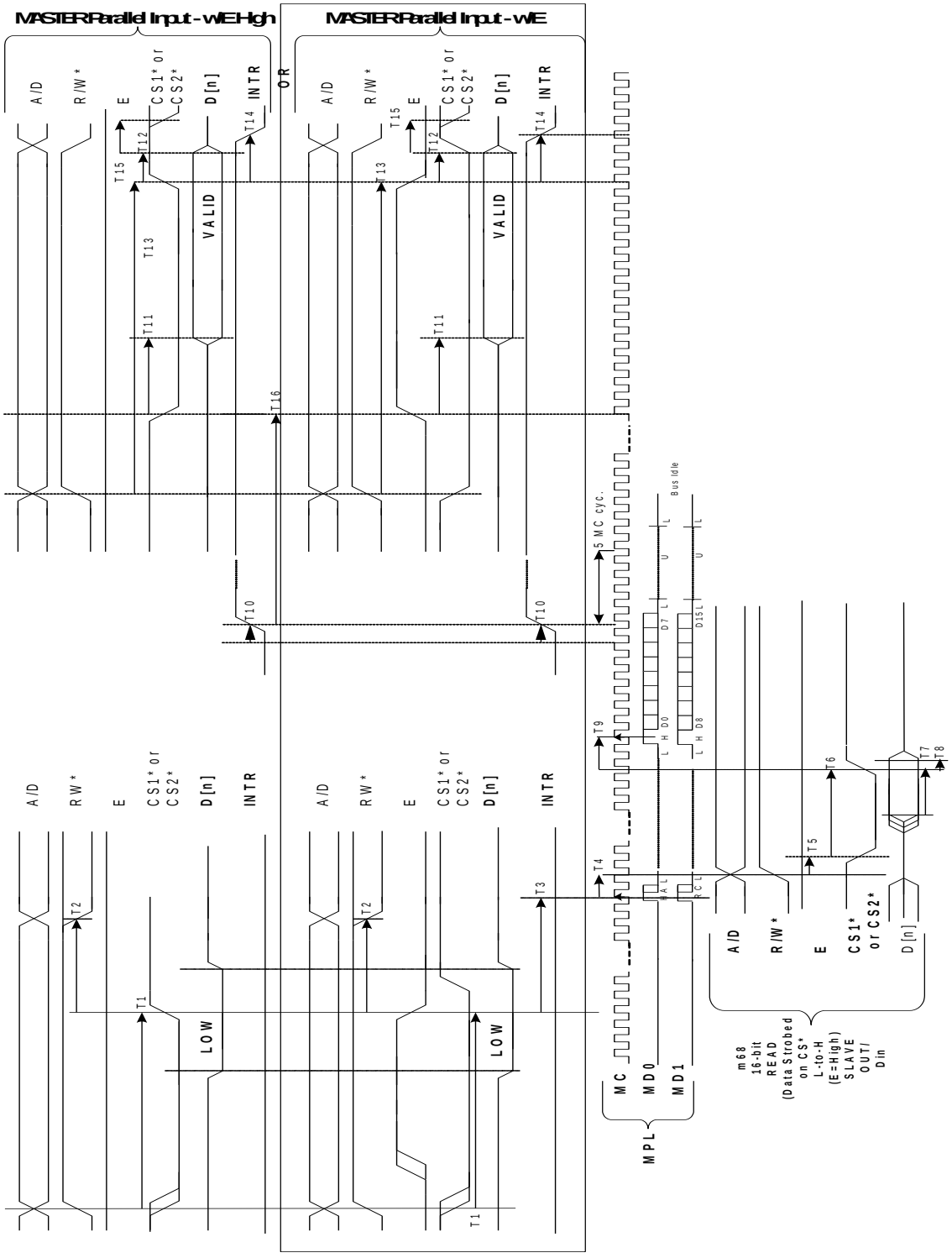

Figure 13 - READ – m68 Interface

No.		Parameter	MIN	TYP	MAX	Units
T1	MasterIN	Set Up Time		3.6		ns
T2	MasterIN	Hold Time		0		ns
T3	Master	Master Latency		4		MC cycles
T4	Slave	Slave Latency		5		MC cycles
T5	Slave	ChipSelect* Delay		1		MC cycles
T6	Slave	ChipSelect Low Pulse Width		6		MC cycles
T7	Slave	Data Set Up Time		3.6		ns
T8	Slave	Data Hold Time		0		ns
T9	Slave	Slave Read Latency		6		MC cycles
T10	Master	INTR Delay		1		MC cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after strobe		TBD		ns
T13	MasterOUT	CS* or E active pulse width	3.6			ns
T14	MasterOUT	INTR De-assert		4		MC cycles
T15	MasterOUT	Recovery Time		TBD		MC cycles
T16	MasterOUT	INTR Response	0			MC cycles

Table 4 - READ – m68 Interface

For the m68 mode, the Master accepts data on the CS* Low-to-High transition or the E High-to-Low transition, which ever come first. The Slave output only uses the CS* pin for data strobe/latch, as the E signal is held constantly High.

3.5 i80 Mode (mode = 1)

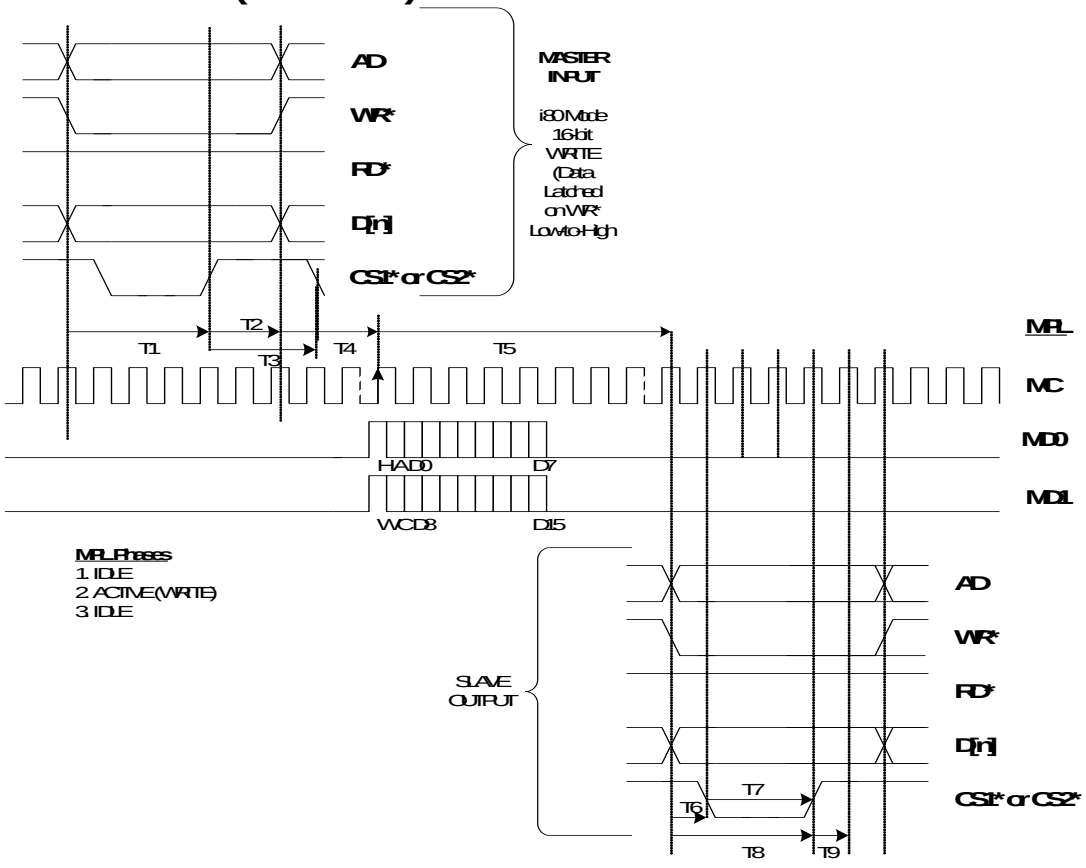

Figure 14 - WRITE – i80 Interface

No.		Parameter	MIN	TYP	MAX	Units
T1	MasterIN	Data Setup before ChipSelect* High		3.6		ns
T2	MasterIN	Data Hold after ChipSelect* High	0	TBD		ns
T3	MasterIN	ChipSelect* Recovery Time		TBD		ns
T4	Master	Master Latency		4		MC cycles
T5	Slave	Slave Latency		8		MC cycles
T6	SlaveOUT	Data Valid before Chip Select* High-to-Low		1		MC cycles
T7	SlaveOUT	CS* Pulse Width Low		3		MC cycles
T8	SlaveOUT	Data Valid before ChipSelect* Low-to-High		4		MC cycles
T9	SlaveOUT	Data Valid after Chipselect* Low-to-High		1		MC cycles

Table 5 - WRITE – i80 Interface Parameters

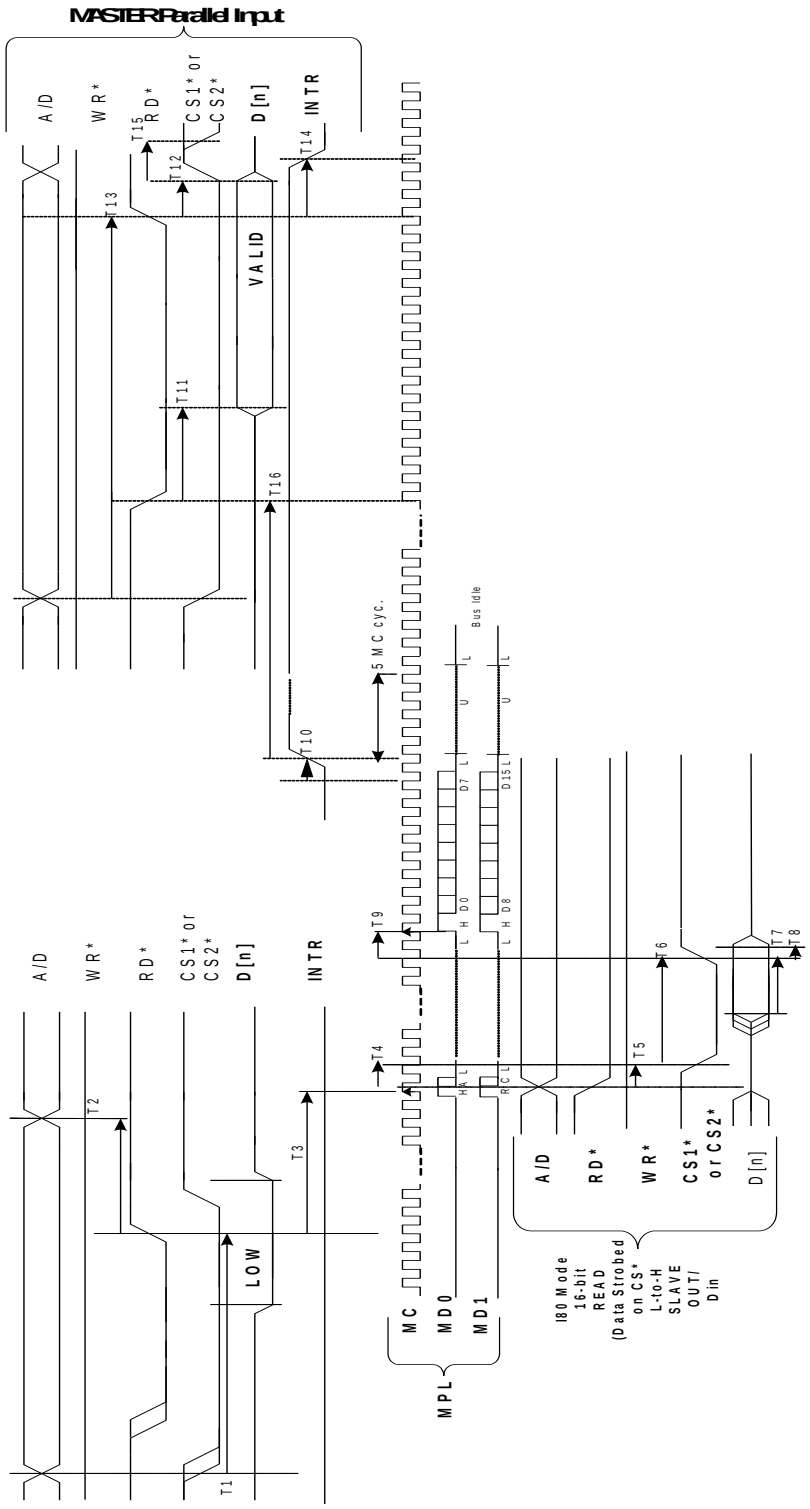

Figure 15 - READ – i80 Interface

No.		Parameter	MIN	TYP	MAX	Units
T1	MasterIN	Set Up Time		3.6		ns
T2	MasterIN	Hold Time		0		ns
T3	Master	Master Latency		4		MC cycles
T4	Slave	Slave Latency		5		MC cycles
T5	Slave	ChipSelect* Delay		1		MC cycles
T6	Slave	ChipSelect Low Pulse Width		6		MC cycles
T7	Slave	Data Set Up Time		3.6		ns
T8	Slave	Data Hold Time		0		ns
T9	Slave	Slave Read Latency		6		MC cycles
T10	Master	INTR Delay		1		MC cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after strobe		TBD		ns
T13	MasterOUT	RD* active pulse width		TBD		MC cycles
T14	MasterOUT	INTR De-assert		4		MC cycles
T15	MasterOUT	Recovery Time		TBD		MC cycles
T16	MasterOUT	INTR Response	0			MC cycles

Table 6 - READ – i80 Interface

To account for the latency through the MPL link, a dual READ operation is required by the host. The first read returns invalid data (all Low), which the host ignores. Once data has returned to the Master, the INTR signal is asserted to inform the host to initiate a second read operation. During this second read operation the MD line is held in the idle bus phase. After the CS* Low-to-High transition the INTR is de-asserted.

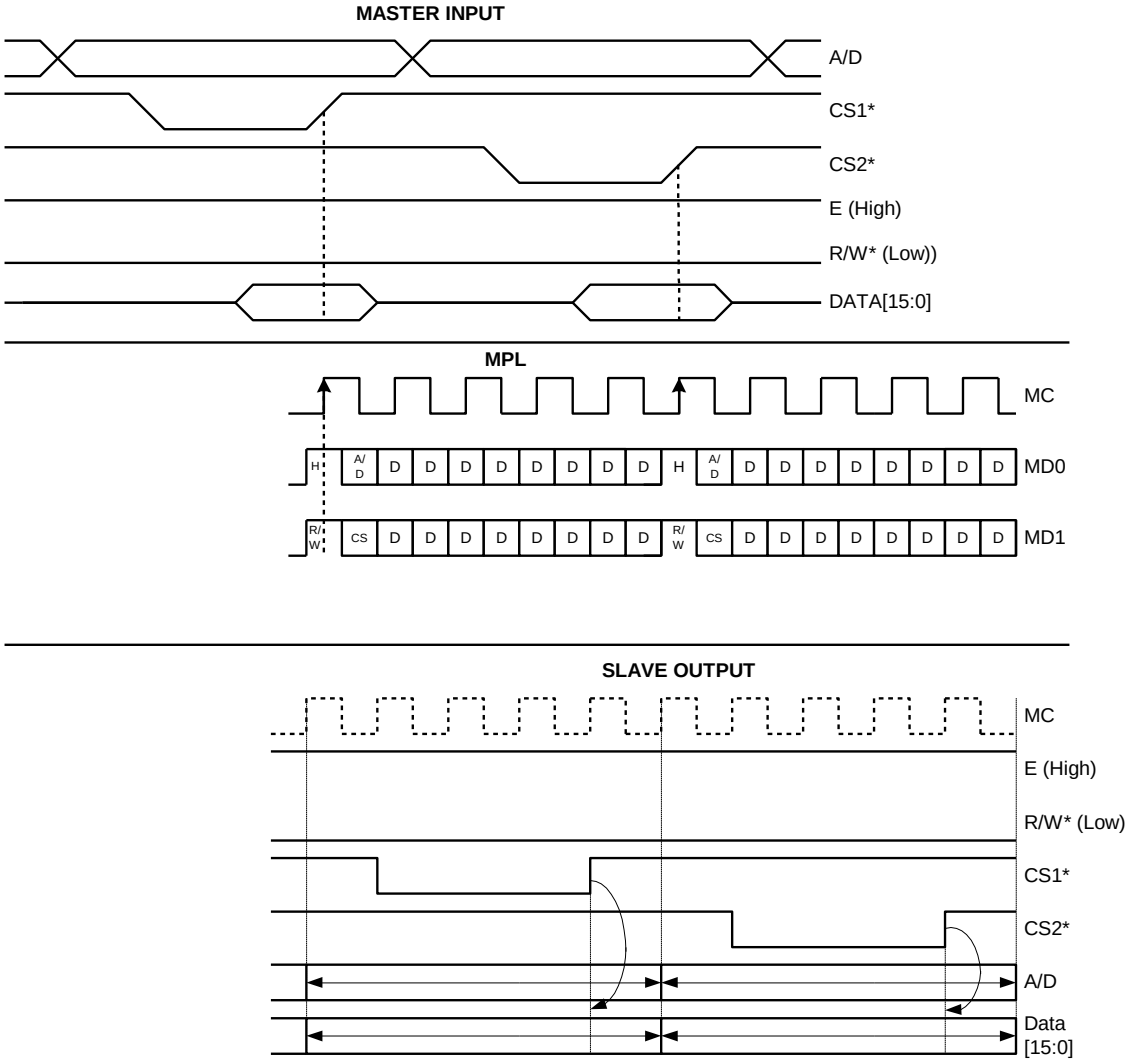

Figure 16 - Back-to-Back WRITE operations – m68 mode

4 RGB Display Protocol

Some timing diagrams necessarily show signals and signal timing for the legacy parallel interfaces. This is done for clarity and is not to be considered part of the MPL Level-0 Standard or requirements for interoperability with that standard.

Protocols for both 18-bit color depth and 24-bit color depth are defined. When transporting color depth below 18-bit, the 18-bit protocol can be used by offsetting the color data. The LSBs of the RGB are not used and data is offset toward the upper (MSB) end of the bit fields.

4.1 Color Depth of 18-bits

The control bits VSYNC (VS), HSYNC (HS), DE are sent first, followed by the 18-bit RGB (RD0-5, GD0-5, BD0-5) color information the and General Purpose (GP) bits. Data is sent LSB first.

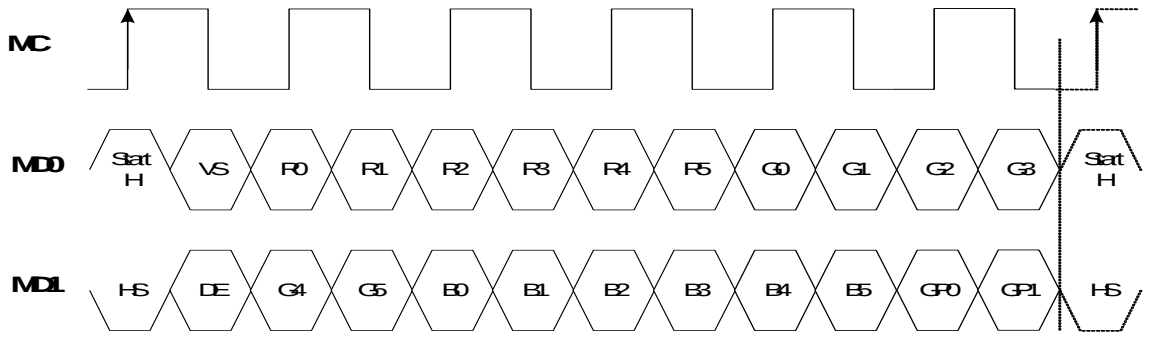

Figure 17 – RGB Display Mode Transaction, 18-bit

4.2 Color Depth of 24-bits

24-bit color data formats follow the 18-bit protocol by simple extension.

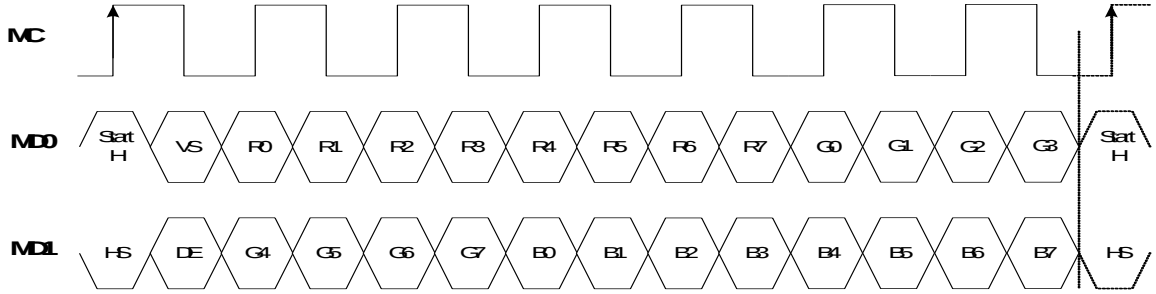

Figure 18 - RGB Display Mode Transaction, 24-bit

5 Image Sensor Protocol

Some timing diagrams necessarily show signals and signal timing for the legacy parallel interfaces. This is done for clarity and is not to be considered part of the MPL Level-0 Standard or requirements for interoperability with that standard.

5.1 Bus Power Up

In the sleep state, WC, MC and MD are turned off with zero current flowing. The Deserializer may inform the Serializer to power up by driving the WC line L-H-L as shown in Figure 19. The DES waits 7 WC cycles before its WCLKout is active. It then waits another 7 WC cycles and then de-asserts its PD* output. Note, there is no phase or frequency relationship between WC and MC.

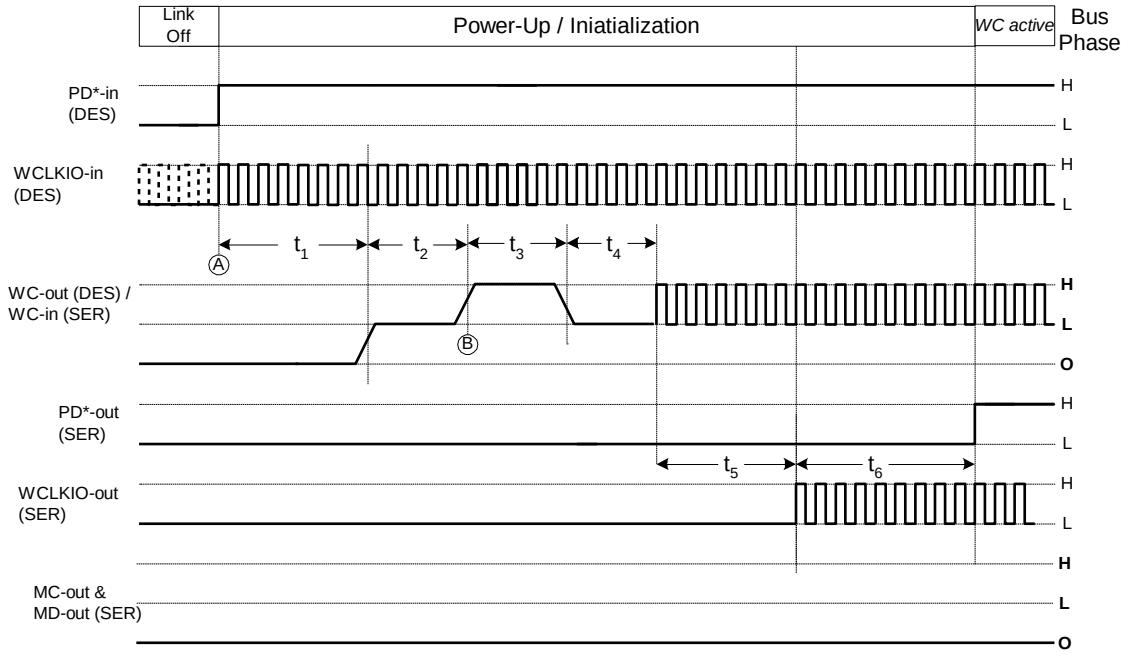

Figure 19 - Bus Power Up Timing - WC

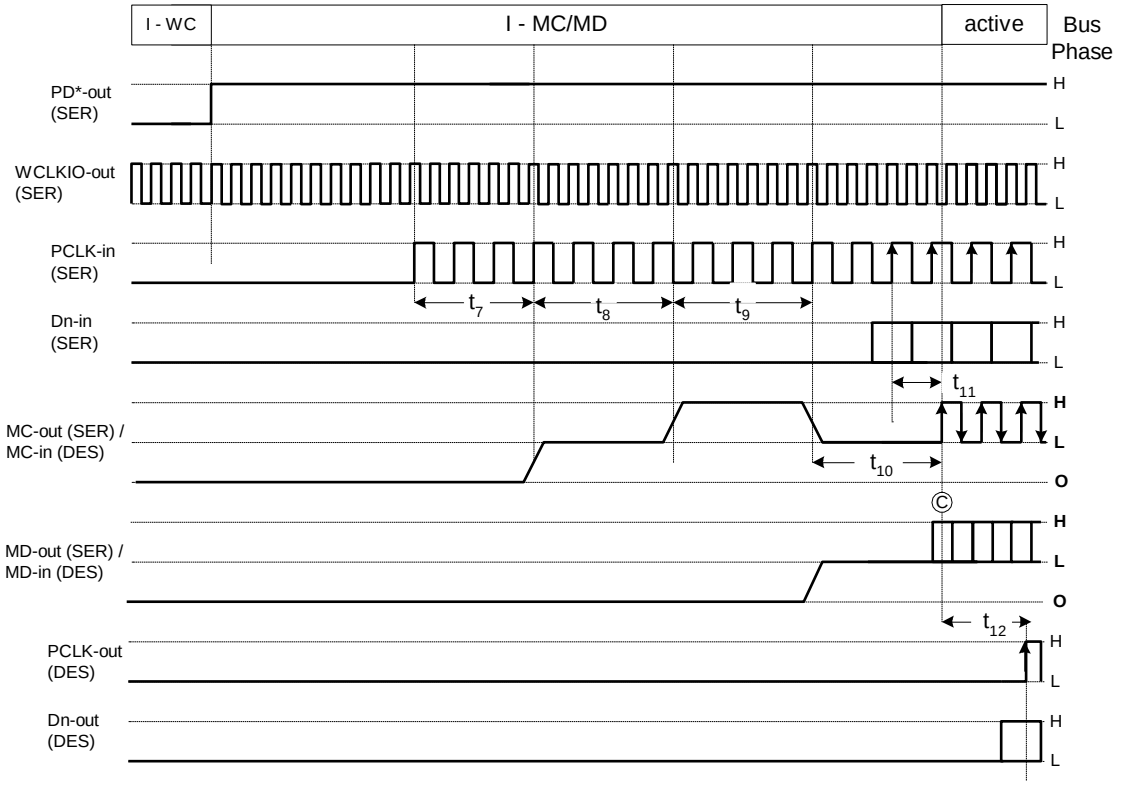

Figure 20 - Bus Power Up Timing – MC/MD

In Figure 20, the Serializer timing is shown. For the part to establish lock, PD* (out) must be High, and a valid PCLK applied. After lock is obtained, the MC and MD lines are initialized and then active transmission occurs. Table 7 lists the timing parameters of Figure 19 and 20.

SYM	Definition		MIN	TYP	MAX	Units
A	MPL Bus Phase OFF	Figure 19	-		-	-
t_1	WC Start Up delay (100 WC CLK cycles)				5	µs
t_2	WC Low Initialization Low State		11	12	13	WCcyc
B	WC Initialization Point		-		-	-
t_3	WC Pulse Width High		11	12	13	WCcyc
t_4	WC Low State		11	12	13	WCcyc
t_5	WCin to WCout latency (SER)		6	7	8	WCcyc
t_6	PD*out Delay		6	7	8	WCcyc
t_7	SER PLL Lock Time (4,096 PCLK cycles)	Figure 20	1024		256	µs
t_8	MC Low Initialization Low State		11	12	13	MCcyc
t_9	MC Pulse Width High		11	12	13	MCcyc
t_{10}	MC Low State		11	12	13	MCcyc
t_{11}	SER Latency			TBD		MCcyc
t_{12}	DES Latency			TBD		MCcyc
C	MPL Bus Phase ACTIVE		-	-	-	-

Table 7 - Power Up – Initialization Parameters

5.2 Protocol

The Camera Interface provides serialization of color and control bits. The interface provides data transport in a single direction. Byte alignment is provided by the intrinsic first rising edge of the MC line. PCLK is required and must be free-running. Data may be any format, including raw Bayer (8-bit only) or BT656 color information. Data is strobed on the rising-edge on the input to the Serializer. Data is sent LSB first (D0).

MPL provides the data transport path from the image sensor. It does not provide control of the image sensor by the typical I^2C bus. These are out of band signals.

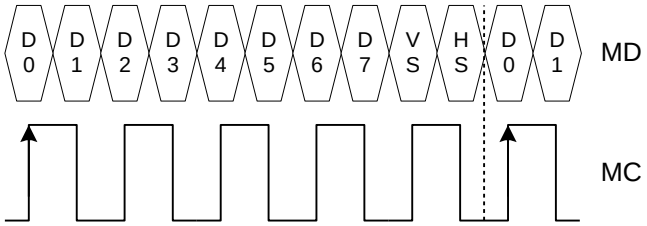

Figure 21 - Camera Mode Serial Transaction

5.3 Image Sensor Clock Transport

An additional clock signal is sent from the Deserializer to the Serializer. This can be used to pass a clock reference (4 to 28 MHz) up to the Camera device from the host. This link is independent of the Serial data path (opposite direction). This clock is denoted with the symbol "WC" in the following diagrams.

Error! Objects cannot be created from editing field codes.

Figure 22 - Sleep to Active

When the Deserializer's PD* signal is de-asserted, the WC output will power up and initialize the serializer and start transmitting the clock reference. Once the Serializer received the clock, it waits TBD cycles, and then outputs the clock signal. TBD cycles later, the Serializer's PLL (if used) will begin to lock if PCLK is present.

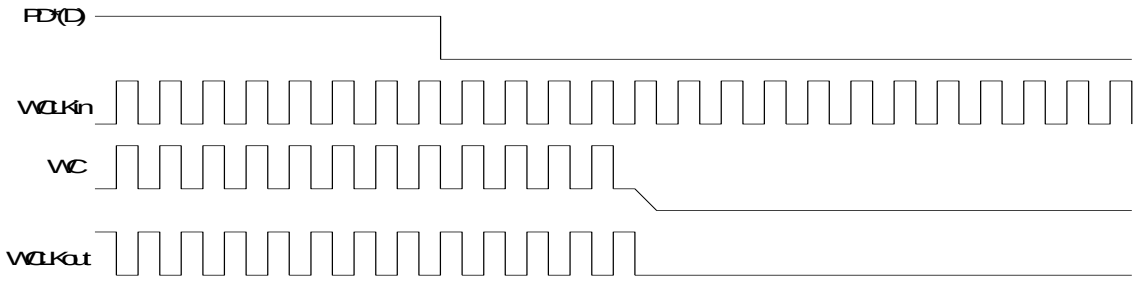

Figure 23 - Active to Sleep

When the Deserializer's PD* signal is asserted, the WC signal is turned off. The Serializer detects this change and drives Low the extra clock (WCLKIO) output.

6 Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OH}	Logic High Current		$2.8I_B$	$3.0I_B$	$3.3I_B$	µA
I_{OMS}	Mid Scale Current			$2.0I_B$		µA
I_{OL}	Logic Low Current		$0.8I_B$	$1.0I_B$	$1.2I_B$	µA
I_B	Current Bias			150		µA

7 Revision History

Version	Description
0.9	Initial public version

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