Application Note

How to Tune TI PCIe Gen5 Redrivers

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ABSTRACT

PCI-Express (or PCIe) 5.0 links provide an overall loss budget of 36dB at 16GHz. Unsurprisingly, many systems have PCIe links that exceed the loss budget, imperfect implementations that reduce the available loss budget, or both. TI PCIe Gen5 redrivers with integrated signal conditioning can reduce deterministic jitter caused by channel losses, increase the loss budget, and ultimately increase the reach of PCIe 5.0 links by up to 45%. This application note provides guidance on using the DS320PR810 and DS320PR1601 for better signal integrity and reach extension. PCIe is also applicable for related devices such as the SN75LVPE5421 and SN75LVPE5412 with integrated multiplexers and de-multiplexers, respectively.

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1 Introduction

Tuning the PCIe Gen5 linear redriver is one of the main tasks when designing a line card based on a linear redriver. The *linear* nature is important. PCIe negotiation requires link training to achieve suitable signaling conditions across pre-redriver and post-redriver (pre- or post-channel loss) profiles. To accomplish this goal, different levels of the pre-shoot and post-shoot (or de-emphasis) are exchanged between the Root Complex (RC) and the End Point (EP) to compensate for the overall channel loss profile. A linear redriver must act like a seamless entity and operate in its linear region to enhance high frequency content without compressing the signals. An incorrect tuning can compress or over-equalize these signals, resulting in degraded performance and/or difficulties with link training. Linear operation of the device allows Continuous Time Linear Equalization (CTLE) and Decision Feedback Equalization (DFE) on both sides of the redriver to train up normally.

This application note discusses key features of the redriver relevant to the PCIe negotiation and provides pre- and post- channel loss analysis to help fine-tune and facilitate redriver CTLE settings. This document includes validation and system level results, suggests recommendations for redriver placement, outlines possible PCIe link extensions, and provides redriver step-by-step tuning instructions using real system examples. With a complete understanding of redriver capabilities, limitations, and tuning steps, system designers are better equipped to extend the reach of PCIe 5.0 links using linear redrivers.

2 Device Overview

The DS320PR810, DS320PR1601, and other PCIe Gen5 redrivers amplify high frequency content of incoming signals affected by ISI (Inter-Symbol-Interference). This amplification is done while adding minimal RMS jitter. PCIe Gen5 redrivers are designed for Gen4 and lower rates as well. Furthermore, these devices are protocol agnostic and can be used for SAS and other applications.

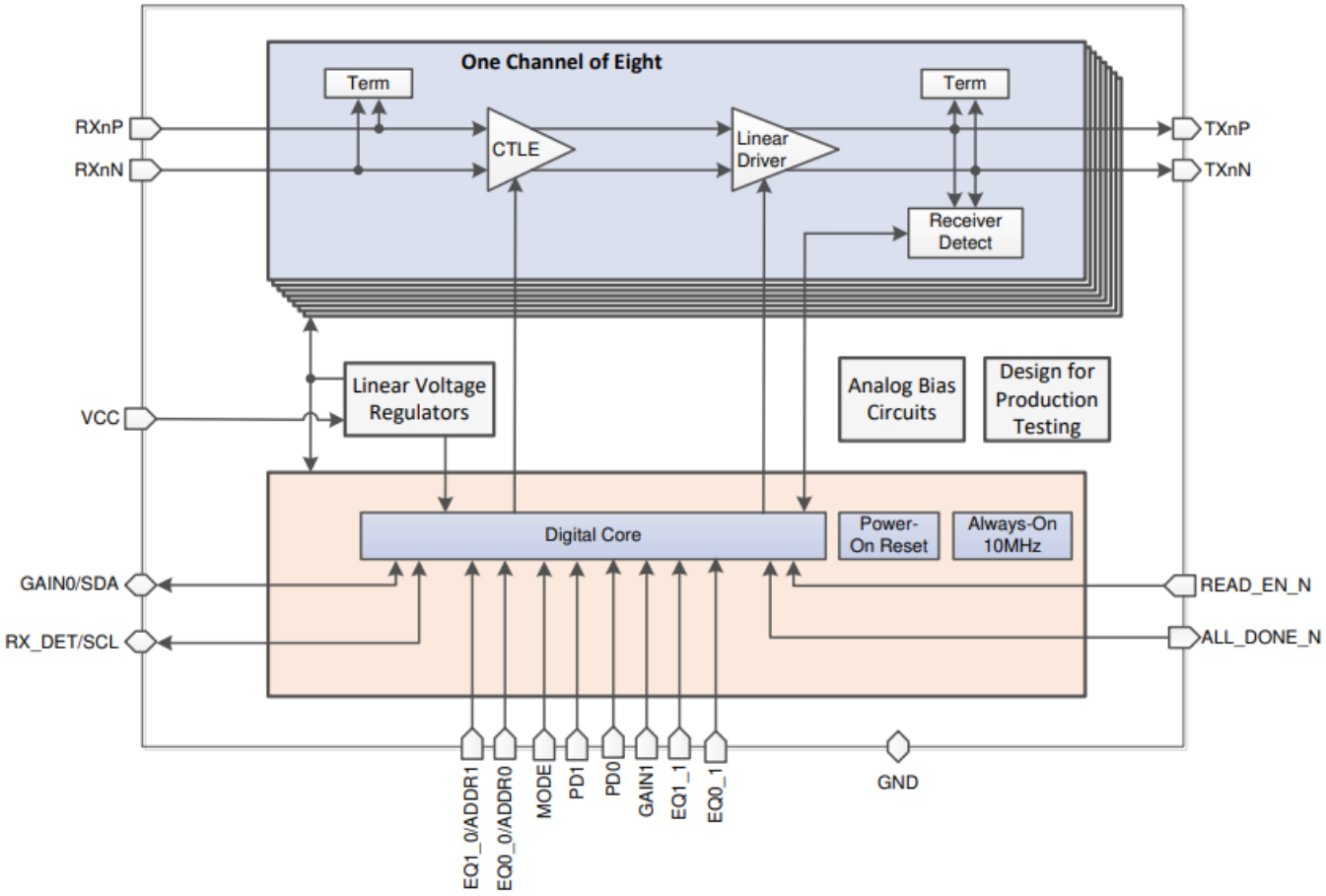

Figure 2-1. DS320PR810 Block Diagram

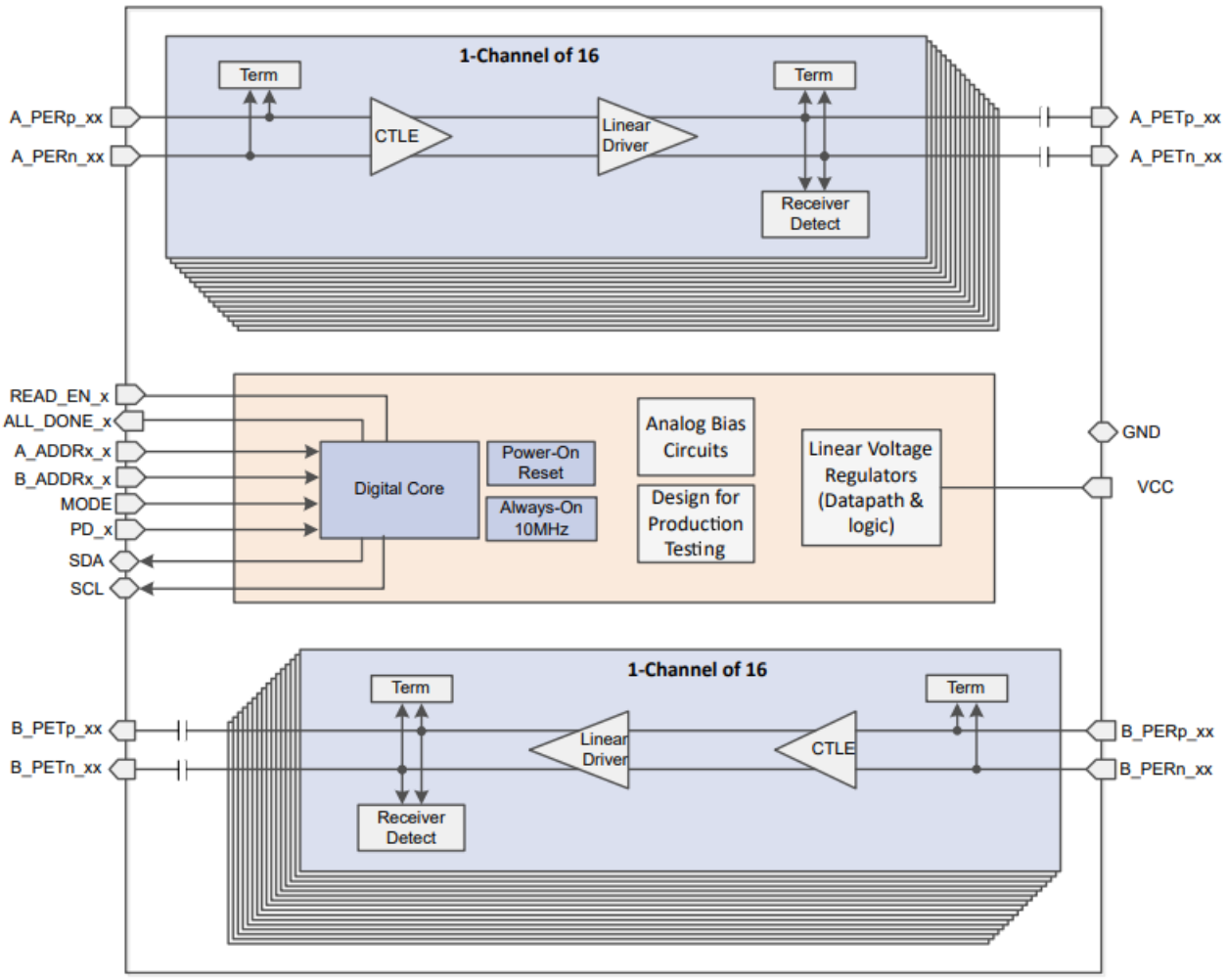

Figure 2-2. DS320PR1601 Block Diagram

2.1 Receiver Equalization

PCIe Gen5 redrivers feature a continuous-time linear equalizer (CTLE) that applies a high-frequency boost and a low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The device has 20 available equalization (EQ) boost and 5 gain settings. The gain settings are *Flat-Gain*, increasing signal strength equally across the bandwidth. The overall data path Flat-Gain (DC and AC) can be programmed through SMBus/I2C registers. The default recommendation for most systems is 0 dB. The Flat-Gain and equalization of the redriver must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively. Refer to the programming guide for more details.

Table 2-1 provides an idea of the EQ boosts offered by TI's PCIe Gen5 redriver architecture. The actual boosts in dB for each EQ Index setting are similar, but not identical between different PCIe Gen5 redriver devices. For full details, please refer to the tables in the *Feature Description* sections of the data sheets of the individual parts.

Table 2-1 is for illustrative purposes only — refer to part data sheets when designing.

Table 2-1. Generic EQ Index Boosts for TI PCIe Gen5 Redrivers

Equalization Selection	Typical EQ Boost	
EQ Index	Gain at 8 GHz (dB)	Gain at 16 GHz (dB)
0	2.0	3.0
1	3.5	5.0
2	5.0	7.0
3	7.0	9.0
4	8.0	12.0
5	9.0	16.0
6	9.8	17.0
7	10.2	18.0
8	10.8	18.5
9	11.2	19.0
10	11.8	19.5
11	12.2	20.0
12	12.8	20.5
13	13.2	21.0
14	13.8	21.5
15	14.2	22.0
16	14.8	22.5
17	15.2	23.0
18	15.6	23.5
19	16.0	24.0

2.2 Redriver Linearity

The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective. It allows unobstructed PCIe 5.0 link training for automatic optimization of the PCIe TX and RX equalization functions on both the root complex and the endpoint sides of the link. Table 2-2 shows typical PCIe TX preset values (pre-shoot and de-emphasis levels) before the presets are passed through the redrivers and after the PCIe TX presets are re-driven. This data was measured with adherence to the PCI-Express 5.0 Base specification. Note that the pre- and post- are well within the required limits.

Table 2-2. PCIe TX Preset Values Before and After Redrivers

Preset	PCIe Preset Limits		Typical Measured after Redriver	
	Recommended Pre-Shoot	Recommended Post-Shoot	Pre-Shoot (dB)	Post-Shoot (dB)
P0	0	-6 ± 1.5	0	-5.69
P1	0	-3.5 ± 1.0	0	-3.34
P2	0	-4.4 ± 1.5	0	-3.9
P3	0	-2.5 ± 1.0	0	-2.41
P4	0	0	0	0
P5	1.9 ± 1.0	0	1.97	0
P6	2.5 ± 1.5	0	2.42	0
P7	3.5 ± 1.0	-6.0 ± 1.5	3.43	-5.36
P8	3.5 ± 1.0	-3.5 ± 1.0	3.37	-3.36
P9	3.5 ± 1.0	0	3.36	0

2.3 PCIe Links with Linear Redrivers

PCI-Express (PCIe) links are typically implemented with 4-lane (x4), 8-lane (x8), and 16-lane (x16) widths. Bidirectional communication between a PCIe root complex (RC) and a PCIe endpoint (EP) is carried over downstream (from RC to EP) and upstream (from EP to RC) channels.

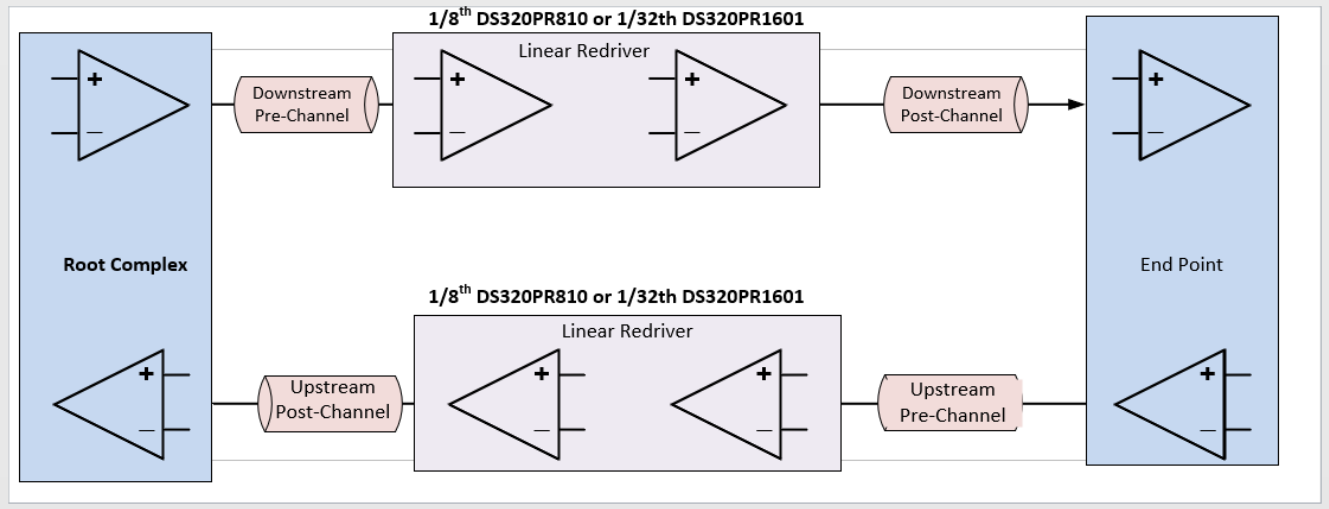

Figure 2-3. Diagram of a PCIe Link

Transmission media between a PCIe transmitter (TX) and a redriver is a *pre-channel*, while a channel between a redriver and a PCIe receiver (RX) is a *post-channel*, indicating the channels' positions relative to the redriver. It is important to note that the pre-channel loss compensation is handled by both PCIe TX equalization and the redriver CTLE.

For systems approaching or surpassing the total system loss budget of 36dB, it is recommended to use higher-grade, low-loss materials such as Megtron-6 and also recommended to place the redriver such that the

loss between CPU and redriver is approximately 27-36dB, allowing the redriver to compensate for the additional system loss.

To check RX EQ compliance, the Phoenix utility is used to do post processing to check that the eye margin conforms to PCIe Gen5 requirements. This post processing involves PCIe Gen5 RX package compensation, behavioral CTLE/DFE, and CDR implementation. This calls for 15 mv vertical eye opening with at least 0.3 UI or 9.375 ps horizontal eye opening. A series of tests—using a BERT with the P9 preset and 800 mVpp amplitude—are done to show redriver ISI or DJ compensation capabilities. In these tests, different pre- and post-channel losses are used.

As shown in Figure 2-3, for pre- and post-channel losses of 20 dB, a Gen5 redriver with a CTLE setting of 0 can meet PCI-SIG requirements.

Note

1. Pre-channel loss consists of root complex or end point package loss plus PCB trace loss before the device.
2. In the second case, we are using the same pre-channel loss, but a higher CTLE (EQ index 6) is used to compensate for the 25 dB post channel loss. The post-channel loss is typically handled by the PCIe receiver through adaptive CTLE, DFE, and negotiated TX equalization. In this case, additional gain provides over-equalization to compensate for the higher 25 dB post channel loss.

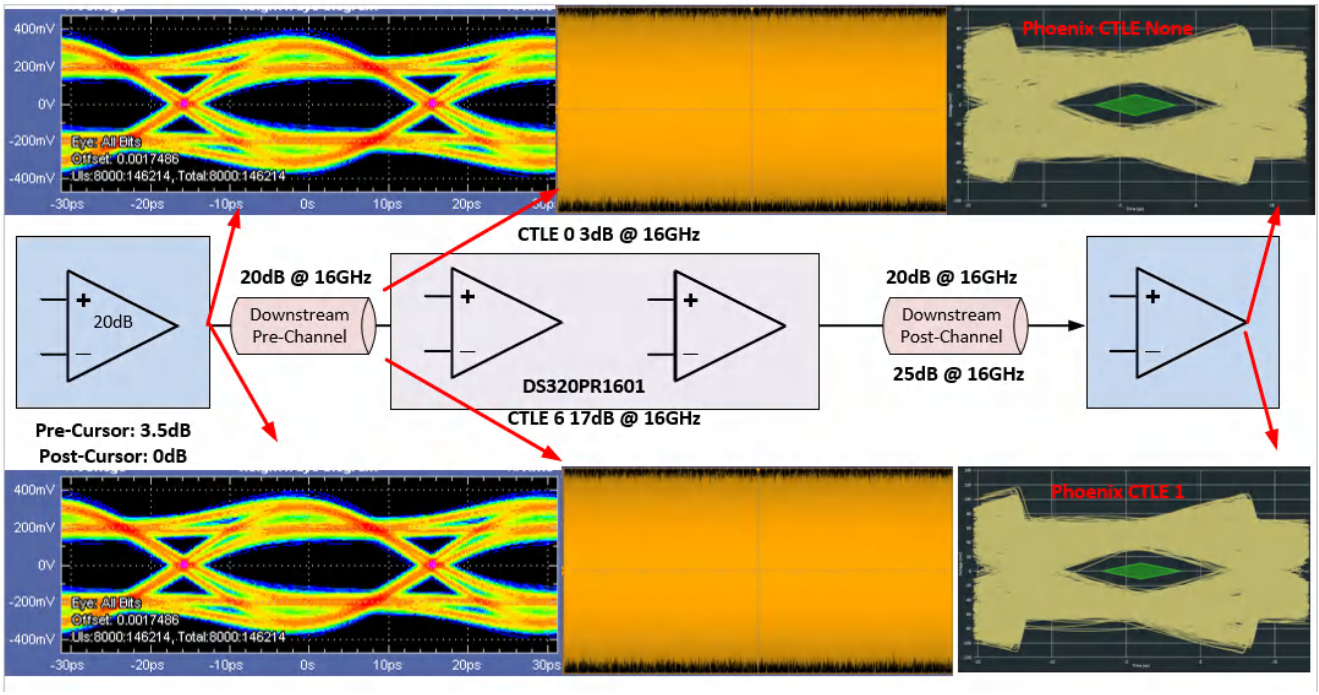

Figure 2-4. PCIe Link Analysis Example with 20 dB Pre-channel, 20-25 dB Post-channel

In Figure 2-5 and Figure 2-6, we are using a higher pre-channel loss (30 dB) with the same earlier variations of post-channel loss. The redriver mainly compensates for the pre-channel loss and can perform marginal over-compensation to address the increase in pre-channel loss.

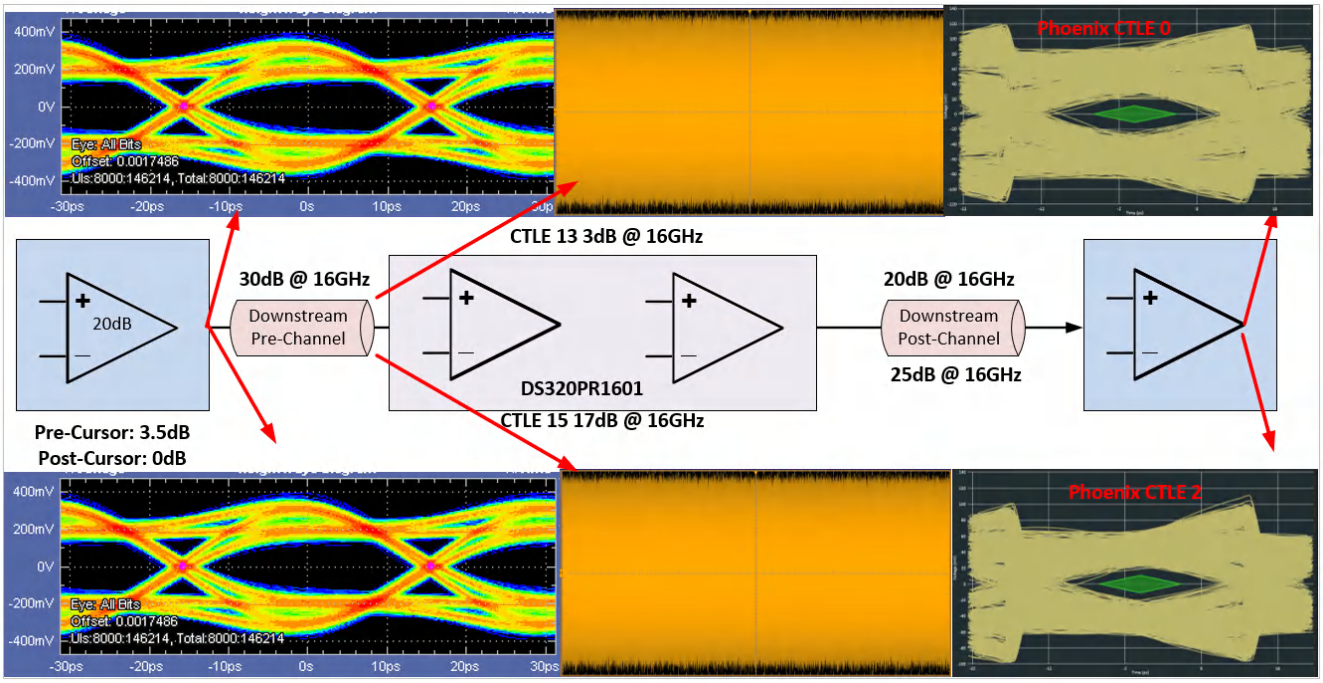

Figure 2-5. PCIe Link Analysis Example with 30 dB Pre-channel, 20-25 dB Post-channel

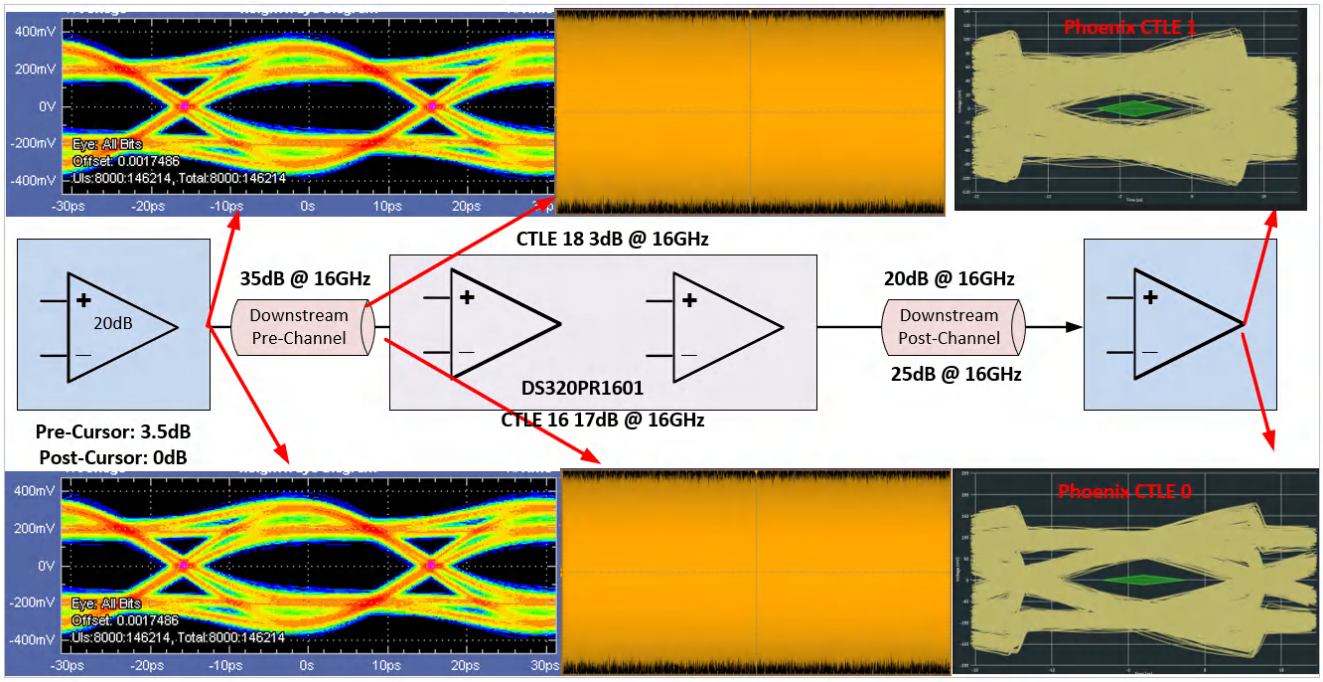

Figure 2-6. PCIe Link Analysis Example with 35 dB Pre-channel, 20-25 dB Post-channel

As shown, the redriver compensates for the ISI (Inter-Symbol-Interference) on the input due to the transmission media low-pass filtering effects. Either the RC or the EP can compensate for the stressed eye diagram due to other factors: random jitter (RJ), sinusoidal jitter (SJ), reflections caused by impedance discontinuities, skew from mismatched trace lengths, and differential and common mode interferences.

2.4 Redriver EQ Tuning

In most cases, PCIe Gen5 redrivers require tuning the CTLE setting to provide satisfactory eye openings. The recommendation is to leave DC gain at the default setting of 0 dB. Refer to *PCI Express Compliance Testing with the DS320PR810* for direct effects of DC gain and equalization settings.

Receiver link equalization compliance is done on system or Add-In-Cards to verify interoperability at 1E-12 under stressed conditions. First, different parameters calibration is done to provide the same environment for different systems or AIC applications. The following setups are used for the RX EQ compliance adherence. Images are courtesy of PCI-SIG.

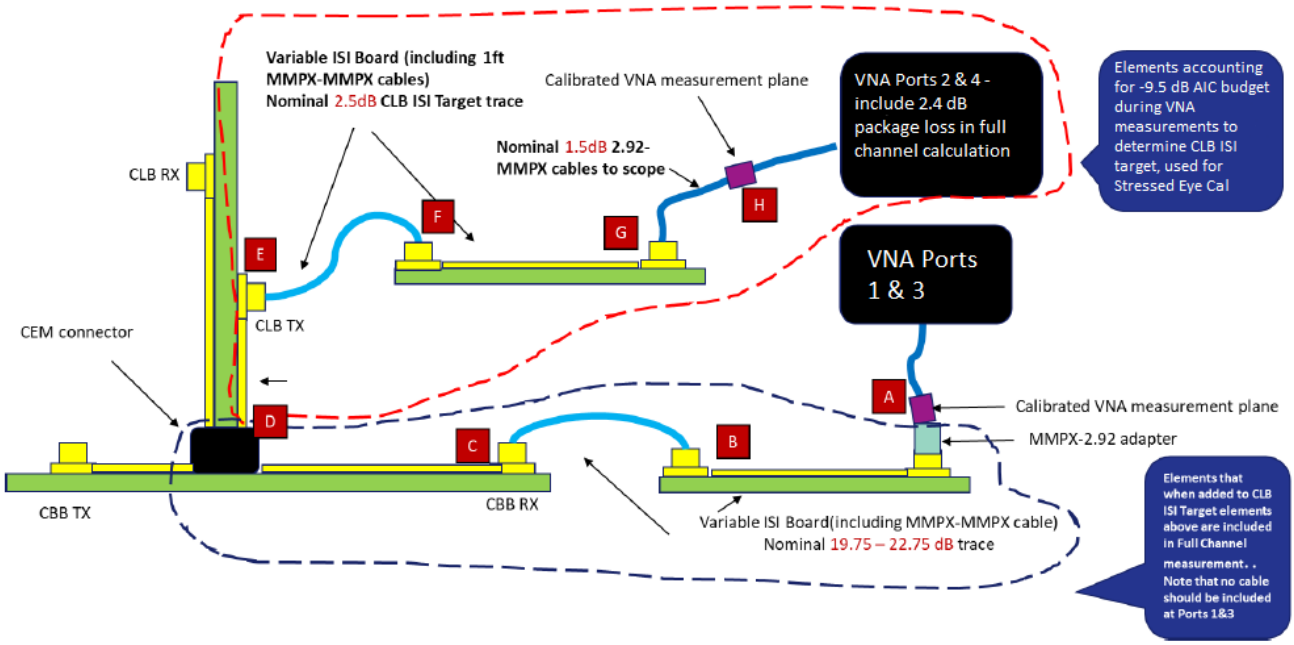

Figure 2-7. PCI-SIG AIC RX Calibration Specifications

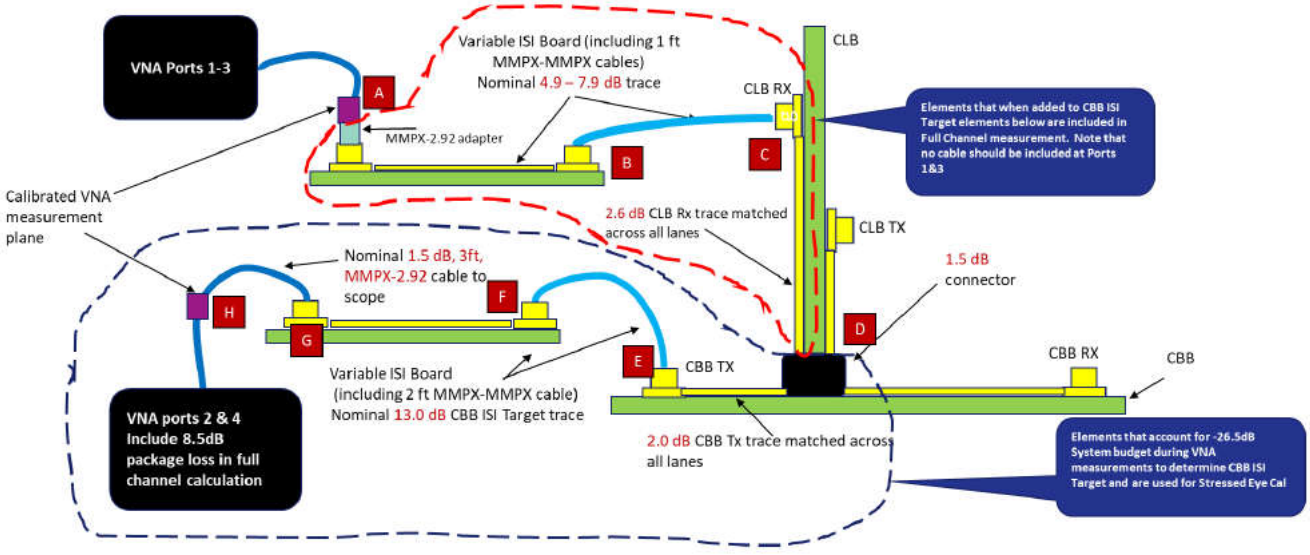

Figure 2-8. PCI-SIG System RX Calibration Specifications

Note

Whether in a system or AIC scenario, VNA port 1 and 3, and the block are used by the PCIe aware BERT to put the link partner one lane into loopback mode through protocol. Using calibrated stressed eye, 1E-12 BER one error or less needs to be achieved.

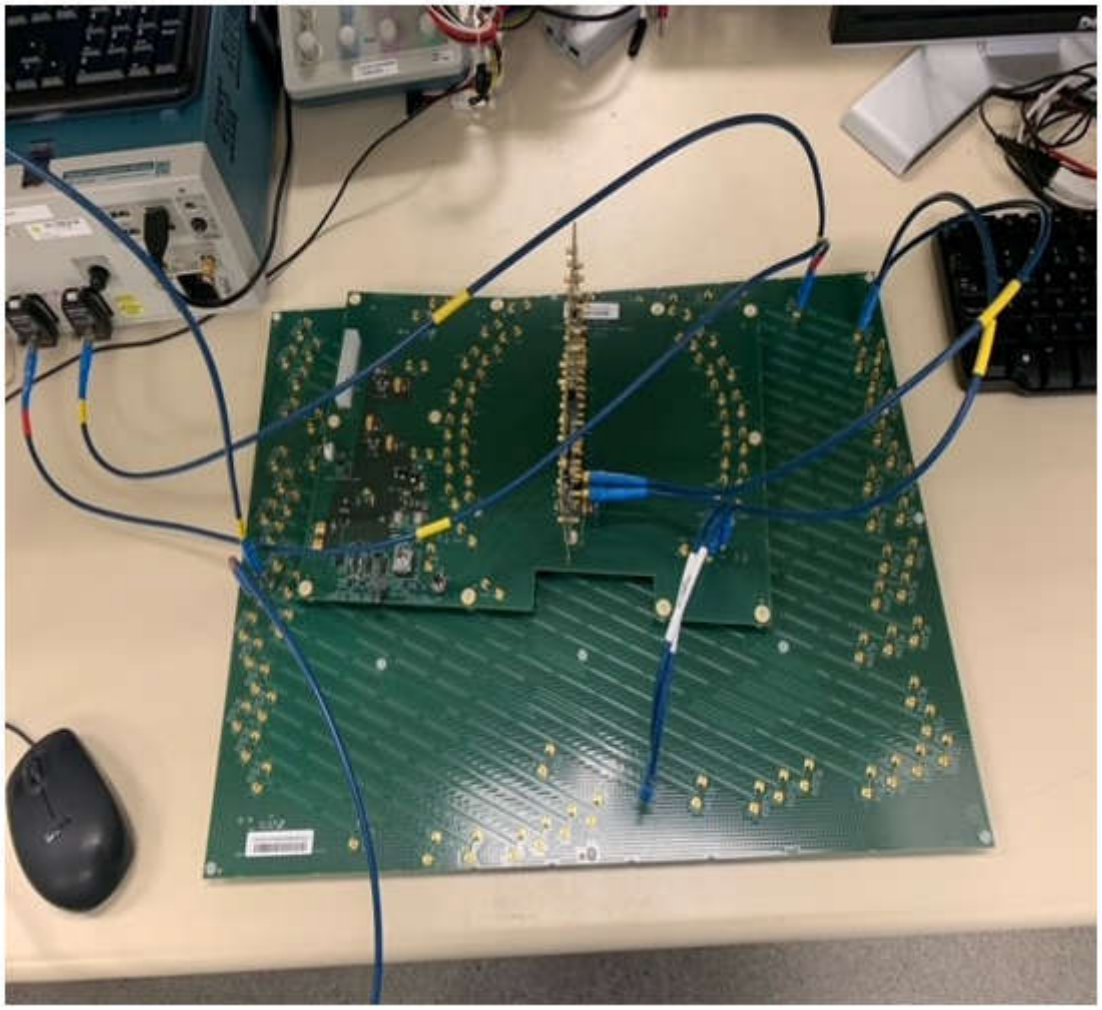

Figure 2-9. PCIe Gen5 SI, CBB, and CLB Boards

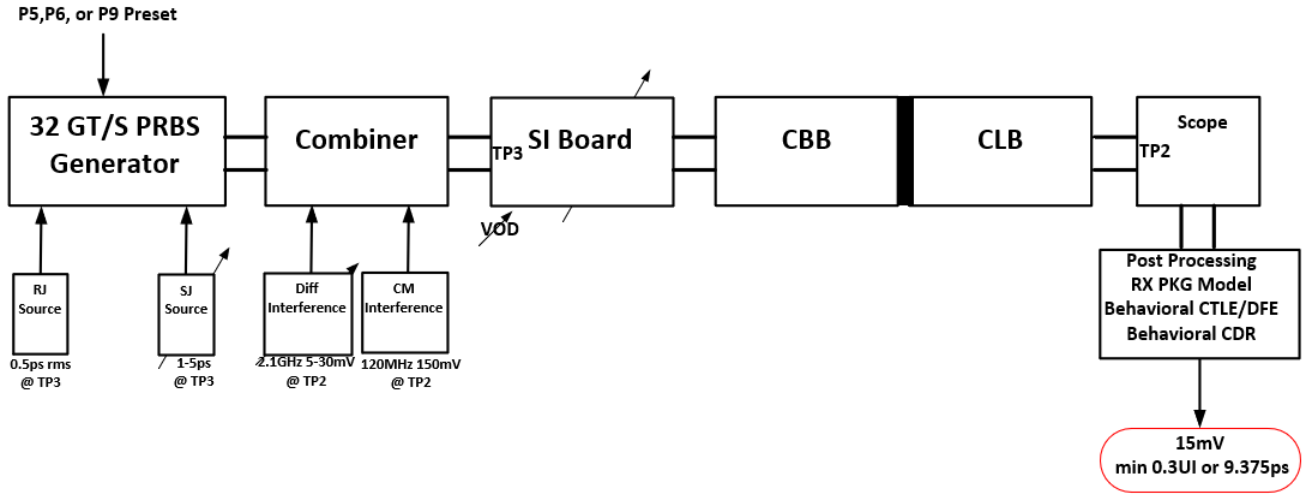

Figure 2-10. RX Compliance Block Diagram

2.4.1 Detailed Description of Parameters Calibration

1. Amplitude or VOD Calibration: Amplitude calibration is done at TP3 using a mixed clock and low frequency pattern at 32Gbps. Under this condition, compliance must be confirmed with PCIe Gen5 using P1 through P9 presets.
2. RJ Calibration is performed at TP3. PCIE calibration pattern is used at P4 along with the SigTest Phoenix 5.1.04 RJ_SJ_CAL template to analyze RJ. Target RJ is 0.5ps rms at TP3.
3. SJ Calibration is similar to RJ and the target value is 1-5ps.
4. Insertion Loss Calibration is performed at TP2. Figure 2-7 and Figure 2-8 show loss targets for different elements within the signal path and CBB/CLB with ISI loss board setup.
5. AIC DMI (Differential Mode Interference) is performed at TP2 with 31.8 dB total channel loss at TP2. Phoenix uses 4.2 dB for AIC package loss. P4 preset and DMI/CMI patterns modulated with 2.1 GHz signal are used to achieve targeted 5-30 mV DMI at TP2.
6. CMI is the same as DMI and performed at TP2 is as well. A 120 MHz CMI is used to achieve a target value of 150 mV.
7. TX EQ Calibration: BERT is calibrated to the noise values. Using presets P5/6/8/9, the best CTLE and preset are selected based on which produce the best eye area at TP2.
8. Insertion loss decremented—from 36 dB—in 0.5 d B/step, DMI in 3 mV increments, SJ in 10 mUI increments, SJ in 10 mV increments, and device CTLE gain swept from 7 through 12 to achieve best Eye Height (EH) and Eye Width (EW).

The DS320PR1601 performance matrix in Table 2-3 shows the device performance with various pre-channel and post-channel combinations using the RX Equalization methodology just discussed.

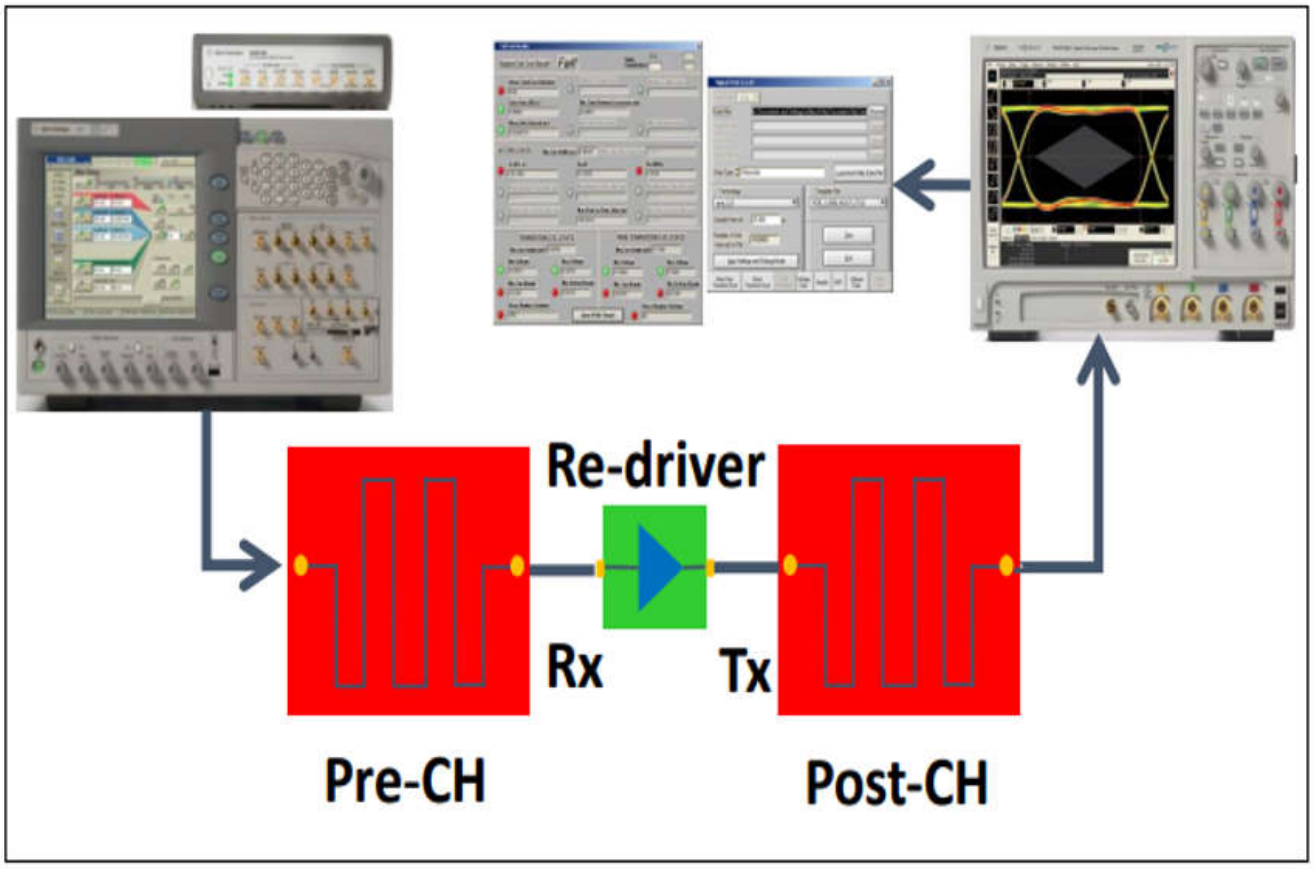

Figure 2-11. AIC Testing Overview

After calibration and operating in AIC mode, Table 2-3 shows the device performance with various pre-channel and post-channel combinations using PCIe Gen5 RX Equalization methodology

Table 2-3. Device Performance Across Pre-Channel and Post-Channel Losses

Pre-Channel Loss (dB)	Post-Channel Loss (dB)	EQ Index/DC Gain/Preset	Eye Width (UI)	Eye Height (mV)
10	32	2/L2/P6	0.39	35.74
14	26	2/L2/P6	0.41	46
14	32	7/L2/P6	0.35	36.83
18	22	2/L4/P6	0.4	72.5
18	26	3/L2/P6	0.4	48.21
22	18	1/L2/P6	0.44	67.7
22	22	3/L2/P6	0.39	40.91
22	26	7/L2/P6	0.43	48
26	18	3/L2/P5	0.37	33.1
26	22	4/L2/P6	0.4	39.7
26	26	4/L2/P6	0.36	28.4
29	18	4/L2/P6	0.35	39.7
29	22	4/L2/P6	0.34	29.59

3 General Guidelines for Optimal CTLE and Gain Selection

The following steps provide general guidance for selecting the redriver CTLE settings:

1. It is highly desirable to perform signal integrity analysis using actual media, connectors, vias, root complex, end point, and redriver S-parameter models. The aim is to provide margin to meet high requirements of bit error rate and eye dimensions.
2. Understand the overall channel media loss profile. Temperature, humidity, signal-to-noise ratio, and crosstalk all require additional margin for a stable operation.
3. Each end point or root complex requires a certain IO margin. It is desirable to add margin to ensure error-free operation over PVT.
4. The redriver mainly provides boost at its input to compensate for the signal loss. On the other hand, it is limited on its output signal conditioning. When there is high loss on its output (post-channel loss), there are two options for marginal signal conditioning:
   a. Over-equalize the input signal by 1-2 steps, such that the input signal is not compressed.
   b. Provide flat gain to increase eye height.
5. After understanding pre- and post- channel loss, use Table 2-3 to choose starting CTLE settings. Different root complexes, end points, or BIOS revisions can differ in performance. Thus, fine tuning can be required on top of the recommended values shown in Table 2-3.
6. Table 2-3 was measured using a PCIe recommended SI board. Actual applications can have a different loss profile. As such, CTLE indexes mentioned in this table can be a good starting point for an actual application.
7. Verify the CTLE settings for the downstream redrivers. Sweep the CTLE settings of the downstream redrivers up and down from the initially selected CTLE setting (while keeping the initially selected CTLE setting of the upstream redrivers) to determine the range of CTLE settings that allow a successful system link up, if testing an actual system, or meet the minimum predefined eye mask if performing system simulations or measuring eye diagrams.
8. Verify the CTLE settings for the upstream redrivers. Sweep the CTLE settings of the upstream redrivers up and down from the initially selected CTLE setting (while keeping the previously chosen CTLE setting of the downstream redrivers) to determine the range of CTLE setting that allow a successful system link up or meet the minimum predefined eye mask.
9. Another general, systematic method of tuning is as follows:
   a. Determine if the redriver use case is a system or AIC format. This can determine what end of the PCIe link (root complex or endpoint) that the redriver is most associated with, which is referred to as the *main link partner* for now.
   b. Perform TX compliance testing in the downstream direction from the main link partner. The objective is for the downstream redrivers to compensate for the pre-channel loss: their direct output needs to reproduce the signal originally transmitted by the main link partner as closely as possible. Once this is achieved, the CTLE settings for the downstream redrivers can be frozen.
   c. Next, perform IOMT or lane margining testing in the upstream direction. The objective is to tune the upstream redrivers such that the signal received by the main link partner is of acceptable quality. Different tools and criteria can be used for this process. Successful upstream tuning needs to result in a received signal that not only passes all requirements but has enough margin to compensate for some levels of noise, stress, and other unforeseen effects.
   d. This overall method is not always possible due to physical or software limitations, but is the most comprehensive approach to redriver tuning and is recommended if possible.

4 PCIe Warm Resets

In applications where the redriver is operated in an I2C mode and can be configured by an external controller, it is common to perform redriver tuning in a live environment where the redriver and other system elements maintain power and new EQ settings can be written directly to the device. This is convenient, not needing a power cycle compared to when changes are applied to EEPROM or a board hardware reconfiguration if the device is operated in pin mode.

However, if the redriver testing procedure involves a live PCIe link, then it is important to perform a warm reset of the link before evaluating the signal quality through lane margining and similar tests. Both the PCIe transmitter sending signals to the redriver, and the PCIe receiver that the redriver outputs signals to, have their own settings relating to signal conditioning that are automatically negotiated and calibrated during the link training process. For example, the transmitter is expected to automatically evaluate various PCIe presets applied to transmitted data and select one for use. When the redriver settings are changed while the link is in a normal operational state (L0), the electromagnetic characteristics of the channel are now different, but the transmitter does not dynamically re-evaluate and renegotiate its chosen PCIe preset in response. It is possible that the PCIe preset setting held from the initial negotiations can be sub-optimal for the new channel conditions. To address this, performing a warm reset causes the link to be renegotiated, and since the system power is maintained, the redriver keeps its adjusted EQ settings. Depending on the type of system being tested, a warm reset can be performed by running a relevant PCIe protocol command in CPU configuration software, or alternatively by performing a warm reboot of the operating system or BIOS.

Although warm resets are performed at a protocol level and a protocol-agnostic redriver has relatively little involvement, it is helpful to make sure that the board design that the RX detection subsystem of the redriver is cleared and reactivated in sync with the other PCIe devices during a warm reset and similar conditions by manipulating the PD pin. The operation of the redriver RX detection in relation to the PD pin is shown in Figure 4-1.

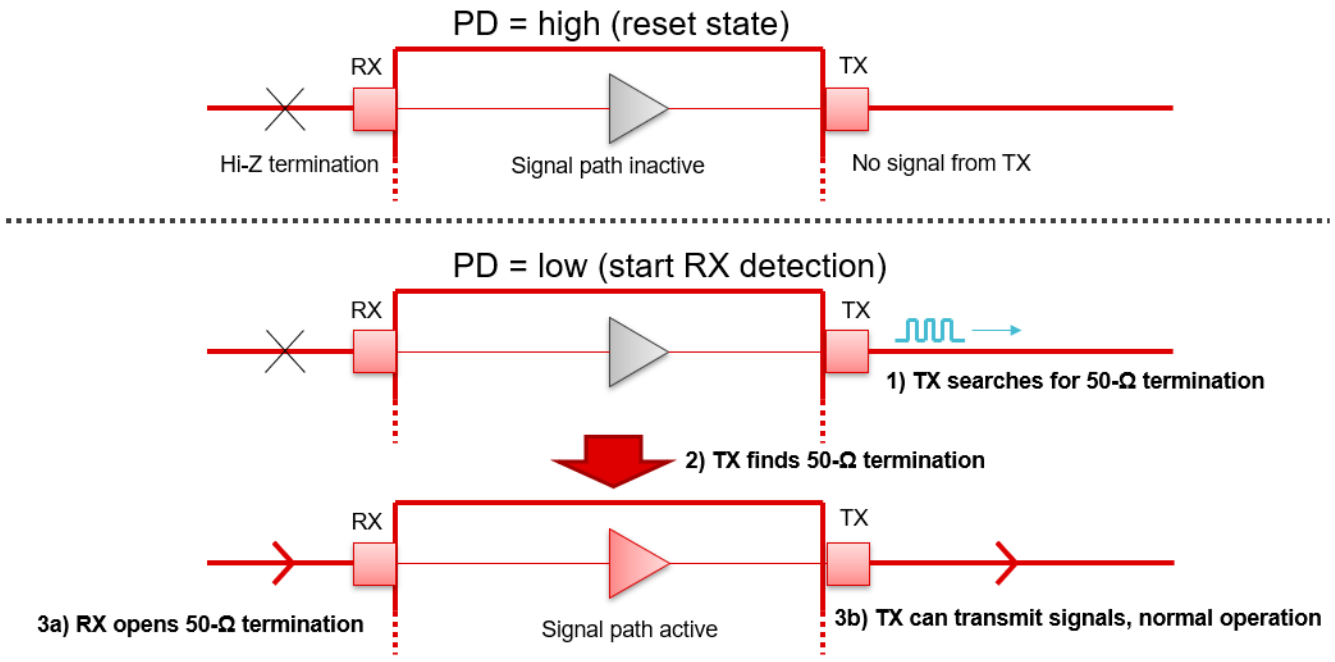

Figure 4-1. Redriver RX Detection Functionality

The redriver is positioned in the middle of the link and is expected to act like a middleman for RX detection sequencing, showing 50Ω terminations on the redriver RX pins only when the redriver TX pins on the other side have successfully detected 50Ω terminations from the device they are facing. That device whose RX is connected to the redriver TX is expected to only enable the 50Ω terminations when the internal startup is fully complete and it is ready to begin PCIe negotiations. If the redriver does not clear the RX terminations after a

warm reset and wait until the appropriate conditions to turn them on, the root complex may see the redriver's terminations immediately (the moment it starts to look) and then begin PCIe negotiations when the endpoint may not be completely ready. This can increase the risk of linkup problems.

Synchronizing the redriver RX detection process to the control of the PCIe protocol is done by connecting the PD pin to an inverted version of the PCIe PERST# signal. PERST# is held low when the link is in reset (either a warm reset or power-on reset) and during this time the inverted connection to PD holds the redriver in reset with RX terminations cleared. The transition from low to high indicates to all PCIe devices that the linkup process needs to be initiated, and the redriver's role is to start searching for terminations at TX pins.

In typical applications, PERST# is routed from the root complex to the endpoint. Branching it to an inverter and routing the inverted signal to a redriver pin or multiple redriver pins is usually not an inconvenience to the board layout. The inverter implementation is left to the designer's discretion, but a basic MOSFET inverter or an inverter IC can both be suitable. Ensure that the input and output voltages of the inverter implementation are compatible with the PERST# signal and the PD pin. Figure 4-2 shows an example of how PERST# can be inverted and distributed to redriver PD pins.

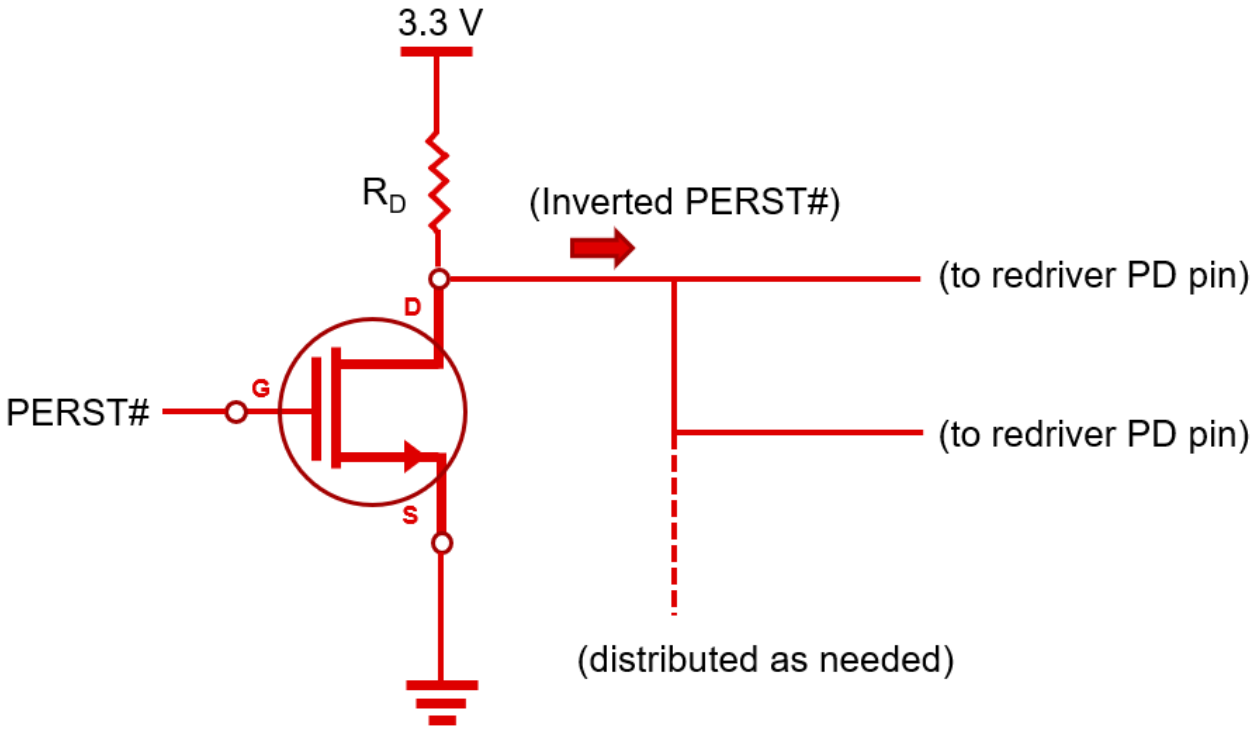

Figure 4-2. Inverted PERST# Distribution Example to Redriver PD Pins

An additional benefit of this PD configuration scheme happens during the initial system power-up: because PERST# initially stays low, the redriver can be held in reset until the PERST# transition triggers it to begin RX detection synchronously with the other system elements. If PD is simply pulled low with a hardwired connection to ground, the redriver begins RX detection as soon as its comparatively fast power-on sequence completes. At this early point in time prior to the PERST# transition, certain PCIe endpoints may present erroneous or unsynchronized terminations before their own power-up sequences are fully completed, which the redriver can then detect and act on. Leading to a similar situation as the warm reset case, the root complex can see erroneous early terminations from the redriver and the chance of linkup problems is higher.

In cases where the PD pins are intended to be controlled with other signals in addition to the inverted PERST#, such as a connection to PRSNT# for hot-plug functionality, it is safer to arbitrate the multiple control signals with a logic OR gate, as shown in the example of Figure 4-3. Without detailed knowledge of the mechanisms generating each control signal, it is difficult to predict if connecting them to the same node at the PD pins can operate normally, or if there can be conflicts resulting in incorrect voltages and other problems.

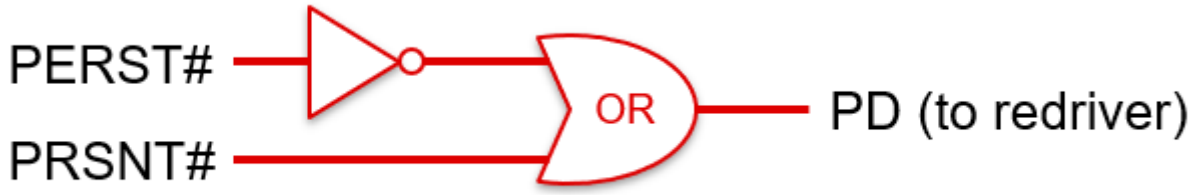

Figure 4-3. PD Control Logic Example with Two Input Signals

5 Summary

PCIe Gen 5 redrivers require tuning to be successfully integrated into a new system. Care must be taken in creating a test setup and a method of evaluating the receiver performance, but there are established guidelines, hardware, and utilities for these processes. Once testing is underway, most applications can be successfully tuned by adjusting only the EQ Index until the results are satisfactory and PCIe-compliant. The data provided in this document can assist in choosing both the placement of the redriver within the overall loss profile and starting CTLE settings to begin testing from, shortening the time and effort needed. Once tuning is complete, PCIe Gen 5 redrivers can fulfill their intended role as a simple method of extending the reach and maintaining the quality of PCIe links.

6 References

- Texas Instruments, *DS320PR810 Eight-Channel Linear Redriver for PCIe 5.0, CXL 1.1*, data sheet.
- Texas Instruments, *DS320PR1601 32 Gbps 16 Lane PCIe® 5.0, CXL 2.0 Linear Redriver*, data sheet.
- Texas Instruments, *SN75LVPE5412 PCIe® 5.0 32 Gbps 4-Channel Linear Redriver with 1:2 Demux*, data sheet.
- Texas Instruments, *SN75LVPE5421 PCIe® 5.0 32 Gbps 4-Channel Linear Redriver with 2:1 Mux*, data sheet.
- Texas Instruments, *PCI Express Compliance Testing with the DS320PR810*, application note.

7 Revision History

Changes from Revision A (August 2023) to Revision B (January 2026)	Page
• Added redriver location recommendation for large system loss	5

Changes from Revision * (August 2023) to Revision A (December 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *PCIe Warm Resets* section..... 14

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