DS280BR810EVM, DS280BR820EVM

The DS280BR810 and DS280BR820 are 8-Channel Linear Repeaters with the ability to extend the reach and robustness of high-speed serial links for up to 28 Gbps interfaces. The DS280BR810EVM and DS280BR820EVM evaluation boards (hereafter referred to as DS280BR8x0EVM) provide users the ability to evaluate the performance and features of the DS280BR810 and DS280BR820 devices, respectively.

NOTE: The DS280BR820 offers improved high-frequency boost and bandwidth compared to the DS280BR810. The DS280BR810 has series AC coupling capacitors on both the RX and TX pins, whereas the DS280BR820 has series AC coupling capacitors on the RX inputs only. The DS280BR820 and DS280BR810 are otherwise pin-to-pin compatible and share the same register programming interface. The DS280BR810EVM and DS280BR820EVM evaluation boards share the same graphical user interface (GUI) software.

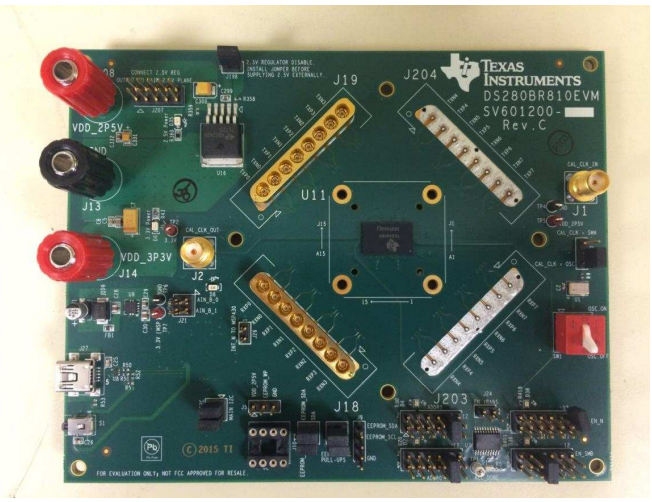

Figure 1. DS280BR810EVM

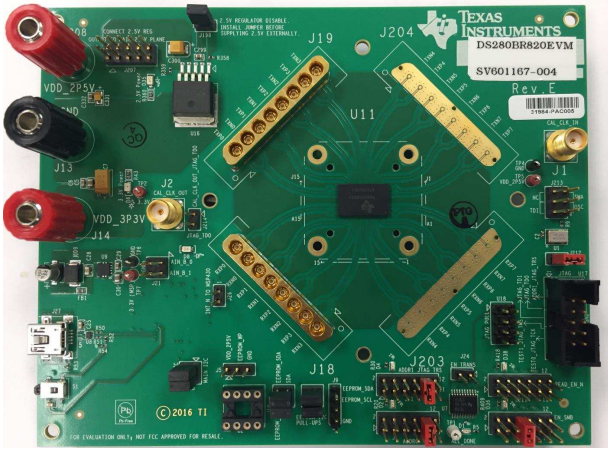

Figure 2. DS280BR820EVM

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Trademarks

1 Features

- 8-Channel uni-directional Repeater operating at rates up to 28 Gbps; 4 channels available for EVM testing
- Linear Equalization that allows for support of link training protocols
- Programmed by on-board USB-to-I2C circuit (USB2ANY)
- Single supply operation: 2.5V ± 5% supplied directly to IC, or 3.3 V ± 5% supplied to 3.3V-to-2.5V on-board LDO

2 Applications

- Backplane/Mid-plane Reach Extension (100G-KR4)
- Front-Port Eye Opener for Optical (28G-VSR and CAUI-4) and Copper Cables (100G-CR4)
- SFP28, QSFP28, CFP2/CFP4, CDFP

3 Ordering Information

Table 1. DS280BR810 Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
DS280BR810EVM	DS280BR810	nfBGA (135)
DS280BR820EVM	DS280BR820	nfBGA (135)

NOTE: Huber+Suhner MXP cable assembles are not provided with this EVM. Users are expected to provide cabling to connect to other boards and test equipment. For MXP cabling recommendations, refer to Section 8.

4 Setup

This section describes the jumpers and connectors on the EVM as well as how to connect, set up, and use the DS280BR8x0EVM.

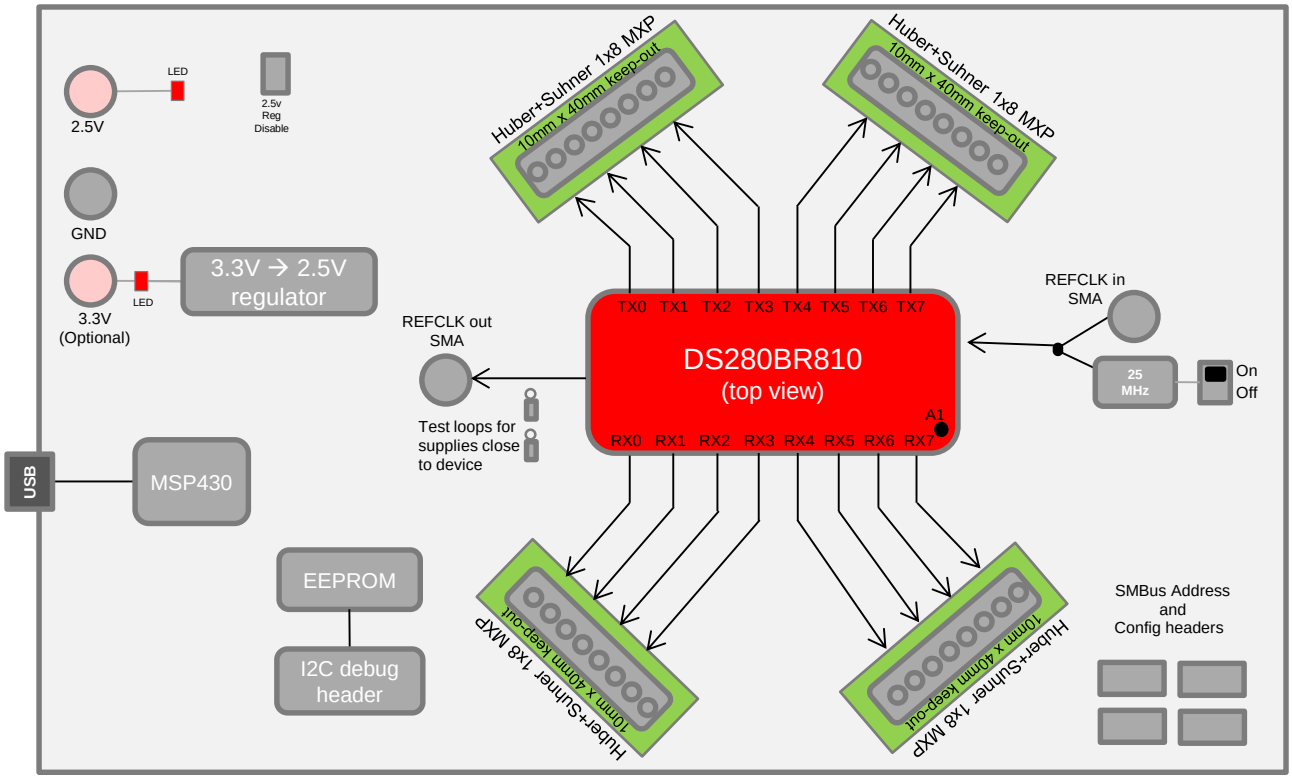

Figure 3. DS280BR8x0EVM Block Diagram

4.1 Modes of Programmable Communication

The DS280BR8x0EVM can be programmed in one of two modes:

1. **SMBus Mode** – Provides full access to the DS280BR8x0 status and control settings via the on-board USB2ANY. ADDR0 (J6) and ADDR1 (J11) headers are used to set the SMBus slave address.
2. **External EEPROM** – Provides access to the DS280BR8x0's EEPROM-programmable control settings via an 8-pin EEPROM. A subset of SMBus register bits are writeable via the EPROM. The EEPROM can program up to 16 DS280BR8x0 devices.

For convenient use, a USB-to-Mini cable provides a direct connection via J27.

4.2 Configuration Overview

The following tables provide a description of the connectors on the DS280BR8x0EVM.

Table 2. Description of SMBus and EEPROM Connections

COMPONENT	NAME	DESCRIPTION
J18.1, J18.2, J18.3, J18.4, J18.5, J18.6, J18.7, J18.8	RXN3, RXP3, RXN2, RXP2, RXN1, RXP1, RXN0, RXP0	High-speed differential input pairs
J19.1, J19.2, J19.3, J19.4, J19.5, J19.6, J19.7, J19.8	TXP0, TXN0, TXP1, TXN1, TXP2, TXN2, TXP3, TXN3	High-speed differential output pairs
J14.1, J14.3	SDA, SCL	SMBus Access (Optional; use this if not using the on-board USB2ANY)
J6	ADDR0	4-level strap pins used to set the SMBus address
J11	ADDR1	
J209	EN_SMB	4-level input to select between SMBus master (float) or slave mode (high)
J211	READ_EN_N	Assert low to initiate EEPROM read in SMBus master mode (weak pull-up)
U2	EEPROM	8-pin DIP Socket for EEPROM
J1	CAL_CLK_IN	External 25MHz Calibration Clock Input (for pin-compatible Retimer only)
J2	CAL_CLK_OUT	25MHz Calibration Clock Output (for pin-compatible Retimer only)
J208	PWR	2.5 V for DC Power
J14	PWR	3.3 V for DC Power
J19	GND	Ground
J27	USB2ANY	USB connection for EVM software control

Table 3. Test Point Connections (Output Voltage)

COMPONENT	NAME	DESCRIPTION
TP4	GND	Common Ground
TP5	VDD	+2.5 V Input
TP6	GND	Common Ground
TP2	VDD	+3.3 V Input

4.3 Software Setup with SigCon Architect

The general procedure for setting up and testing with the DS280BR8x0EVM is as follows. For hardware setup and connections in the steps below, reference the illustrations in Figure 3 and Figure 6 to implement the appropriate setup.

1. **(One-time step)** Choose one of the TI SigCon Architect installers to download from the SigCon Architect Tools Folder on TI.com. Follow the prompts to install software.
   - **SNLC055:** With LabVIEW RTE embedded. Download this folder to install SigCon Architect on a computer without Internet access.
   - **SNLC054:** Without LabVIEW RTE embedded. Download this folder to install SigCon Architect on a computer with Internet access.
2. **(One-time step)**Download the relevant zip folder containing the device profile for the DS280BR810. Note that both the DS280BR810 and DS280BR820 device use the same DS280BR810 device profile.

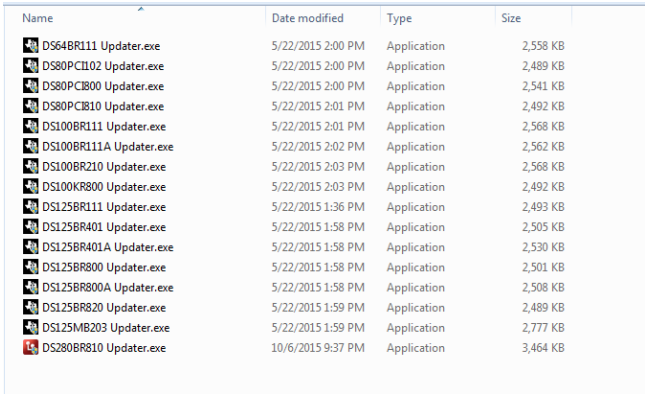

Figure 4. Repeater Profile Updater Installers

Choose the Updater.exe profile for the relevant device. In this case, install “DS280BR810 Updater.exe.” Follow the prompts to install. Once SigCon Architect and the correct updater profiles are installed, close any existing instance of SigCon Architect.

3. Connect 2.5 V power via banana plugs to VDD_2P5V on J208 and GND to GND on J13. Alternatively, connect 3.3 V power via banana plugs to VDD_3P3V on J14 and GND to GND on J13.
   - For VDD = 2.5 V operation: Tie J198 jumper pins 1-2.
   - For VDD = 3.3 V operation (uses on-board 3.3V-to-2.5V regulator): Remove jumper shunt between pins 1 and 2 on J198. Tie J207 jumper pins 10-9, 8-7, 6-5, 4-3, and 2-1.
4. Install the appropriate jumper shunts to operate in SMBus Slave Mode or EEPROM Master Mode. The default configuration for the DS280BR8x0EVM is SMBus Slave Mode, as shown in Figure 2 and Figure 2.

HEADER	SIGNAL NAME / SILKSCREEN	DEFAULT (RECOMMENDED) JUMPER SETTING	COMMENT
J209	EN_SMB	5-6	**(SMBus slave mode)** J209: Tie jumper pins 5-6 to set ENSMB = 1 (1 kΩ to VDD). **(SMBus Master EEPROM mode)** J209: Float the jumper shunt to set ENSMB=F.
J6	ADDR0	9-10	Tie jumper pins 9-10 in order to set the DS280BR8x0's 8-bit slave address = 0x30. ADDR0 and ADDR1 are four-level inputs and can be configured for 0 (1 kΩ to GND), R (10 kΩ to GND), F (floating), or 1 (1 kΩ to VDD) by setting the appropriate jumper position on J6 and J11, respectively. For example, populating no jumpers on J6 and J11 results in ADDR0=ADDR1=F, which corresponds to 8-bit slave address 0x44. For all other SMBus slave addresses, reference the DS280BR8x0 data sheet.
J11	ADDR1	9-10	
J25	MAIN I2C	1-3, 2-4	
J10	EEPROM_SDA, EEPROM_SCL	1-3, 2-4	
J8	EEPROM I2C PULL-UPS	1-3, 2-4	
J212		1-2	
J198	2.5V REGULATOR DISABLE	1-2	Configures the EVM for 2.5 V power supply mode.

5. Connect a PC to DS280BR810EVM with a USB-to-Mini cable via J27.

6. Open SigCon Architect, and navigate to the “Configuration” page of DS280BR810 via the “Selection” column. Choose “Slave Address” “0x30” from the drop down menu. Verify the “USB2ANY Details” specify “USB2ANY 0," and click “Apply." Successful connection is indicated by the green “CONNECTED” indicator on the bottom of the application, as seen below in Figure 5. Once connection is successfully established, users can read and write various settings to the device in real-time, as described in the following steps.

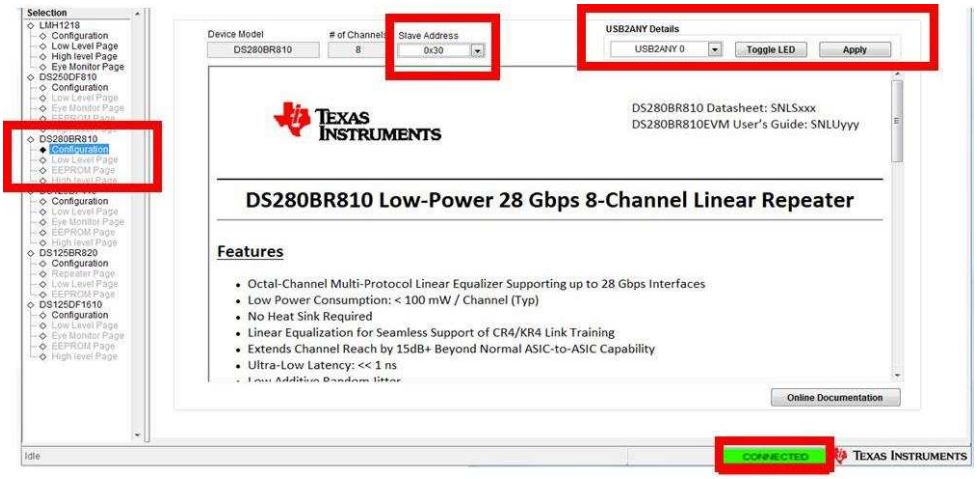

Figure 5. SigCon Architect Configuration Page

7. To view a high-level summary of the device status and control settings, navigate to the “High Level Page," and click on the “Device Status tab” as shown in Figure 6. Click “Refresh From Device” to ensure the settings shown are from the device. The settings on this page are information and read-only.
   - **Signal Detect Status:** For each channel the device status is displayed as “Signal Not Detected” if there is not a signal present at the RX side of this channel or “Signal Detected” if there is a signal present at the RX side of this channel.
   - **Driver Power:** The Driver Power can be turned ON or OFF and the current status is displayed on the Device Status page. The Driver Power is detected at the TX side of each channel.
   - **Control Settings:** The remaining control settings are programmable through SigCon Architect on the High Level page Block Diagram view . The displayed values are the current settings programmed in the device.

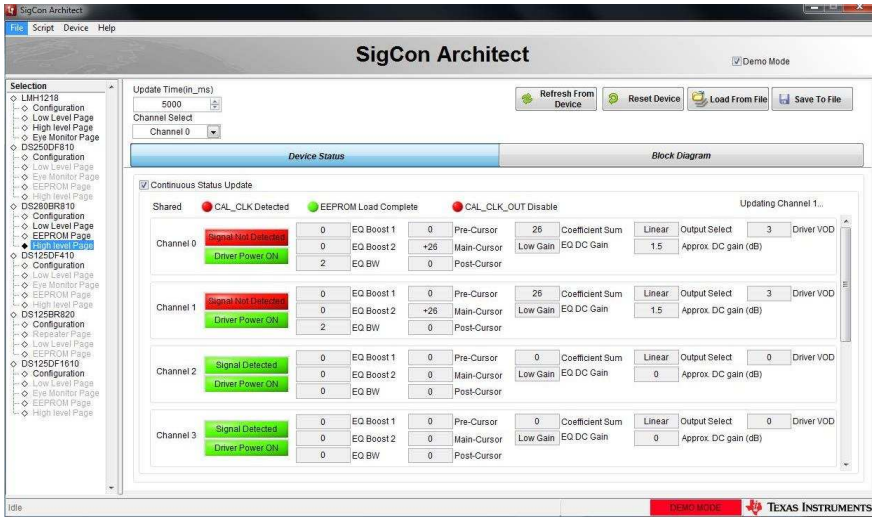

Figure 6. SigCon Architect High Level Page: Device Status

8. To program high-level settings, navigate to the “Block Diagram” tab on the “High Level Page” as shown below in Figure 7. The EQ Settings, FIR Controls, and Output Configurations are programmable from this page. In order to navigate to specific channels use the “Channel Select” drop down menu. Click “Refresh from Device” to apply the device’s current settings to the control setting boxes. Click “Apply to Channel” to program the device from the “Block Diagram” page. After programming the device, the changed settings can be verified on the “Device Status” page, Figure 6. The CAL_CLK Detected indicator provides a visual representation of whether a calibration clock is active. Note that the DS280BR8x0's ability to receive, buffer, and re-drive a calibration clock is only for the purpose of supporting a pin-compatible Retimer device.
   - **EQ Settings:**
     - The Equalizer works as a high-pass filter compensating for input channel loss.
     - The EQ Boost 1, EQ Boost 2, and EQ Boost BW values respectively apply boost to their respective segments as shown below on the block diagram.
     - The EQ DC Gain setting can be either Low or High Gain. This affects the input-to-output wide-band amplitude gain/attenuation.
   - **Output Configurations:**
     - The Output Select can be Limiting or Linear. In the limiting mode, a limiting amplifier is added to achieve the FIR functionality. The FIR is only available in limiting mode. Linear mode does not utilize the limiting amplifier. Linear mode is necessary for applications where Link Training is required.
     - For limiting mode, the Approx. Output Differential Voltage is calculated and displayed in the GUI based on the absolute sum of the FIR coefficients.
     - For linear mode, the Approx. DC Gain will be automatically updated based on the Driver VOD and EQ DC Gain settings.
     - **FIR Controls (Limiting Mode Only):**
       - The FIR filter allows for Main-Cursor, Pre-Cursor, and Post-Cursor adjustments.
       - The Pre-Cursor and Post-Cursor values can only be negative. This allows each tap to apply only boost and no attenuation.
       - The Main-Cursor values can only be positive. This FIR filter implementation is not capable of inverting the signal.
       - The Coefficient Sum will automatically update based on the Pre-Cursor, Main-Cursor, and Post-Cursor. The maximum value for the Coeff. Sum is 31.

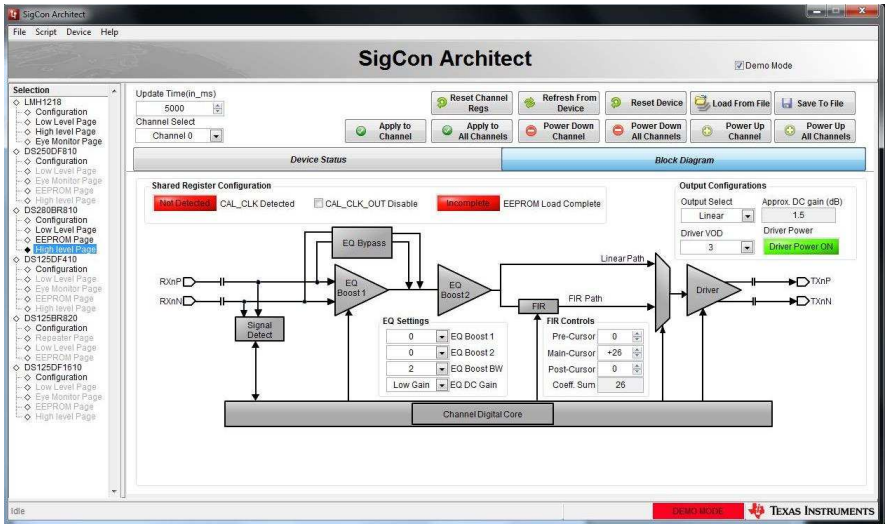

Figure 7. SigCon Architect High Level Page: Block Diagram

9. To read and write to all registers on the DS280BR8x0, navigate to the “Low Level Page," as shown below in Figure 8. Only in SMBus Slave Mode can the user read and write to all programmable registers. Click “Read All” in order to load the data in each register from the device to the “Register Map."
   - **Read Register:** Type the readable address in the “Current Address” text box. Click “Read Register." The data in this register will appear in the “Data” text box.
   - **Write Register:** Type the writable address in the “Current Address” text box, and type the data to write to this address in the “Data” text box. Click “Write Register.”

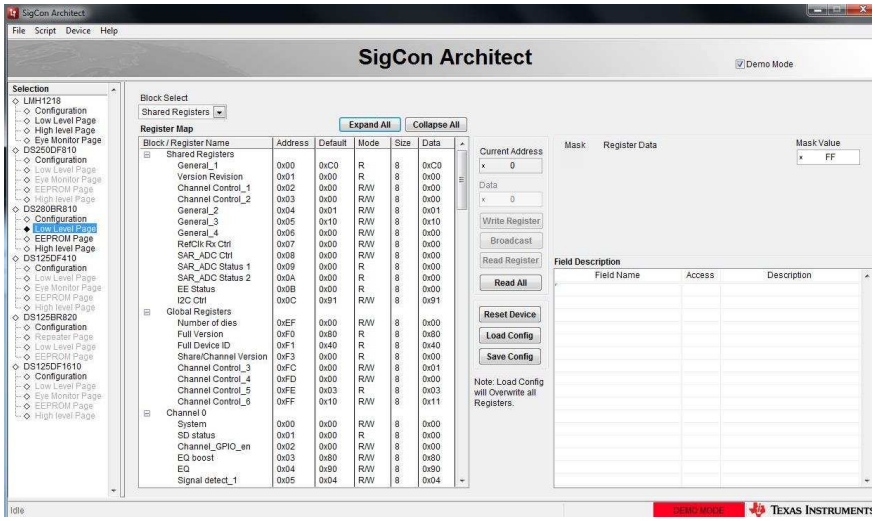

Figure 8. SigCon Architect Low Level Page

10. To create an EEPROM hex file consisting of device settings, navigate to the “EEPROM Page," as shown in Figure 9. To update the settings from the device click “Update Slot from Device." To create the programmable hex file, click “Write to EEPROM Hex." The evaluation module does not include an EEPROM, but an external EEPROM can be inserted in the available socket (U2). SigCon Architect cannot directly program the EEPROM. The EEPROM Hex File can be burned on the EEPROM via I2C communication (i.e. AARDVARK or equivalent interface adapter). The EEPROM control settings are described in greater detail below. Refer to SNLA244 for more information on EEPROM hex files for 25G/28G Repeater/Retimer products.
    - **Output Configurations:** If this box is checked, all channels receive the same configuration. Different devices can receive different configurations, but within one device, all channels will receive the same configuration. If this box is unchecked, then the EEPROM will store the configurations as unique channel configurations. Each of the four channels can receive a unique configuration.
    - **EEPROM > 256:**
      - This setting must be enabled if there are more than 4 EEPROM slots.
      - When this box is checked, the “EEPROM Size” drop down menu is automatically populated by 512 Bytes if previously populated by 256 Bytes.
      - When this box is unchecked, the “EEPROM Size” drop down menu is automatically populated by 256 Bytes. Up to 4 EEPROM slots can be programmed.
    - **Enable CRC:** If enabled, each device will have a CRC value specific to the base header, address map header, and data. If disabled, the CRC is not computed.
    - **Slot Update Details:** The number of slots refers to the total number of unique SMBus register settings to load from the EEPROM. The user can choose to update all slots, or which slot number to update the SigCon Architect EEPROM page from.
    - **EEPROM Size:** The EEPROM size must be set to 256, 512, or 1024 bytes. A single external EEPROM can be used by up to 16 x DS280BR810 devices.
      - The first 3 bytes of EEPROM data is the base header. The base header contains the CRC Enable Bit, Aaddress Map Header Enable Bit, EEPROM > 256 Bytes Enable Bit, device count,

and maximum EEPROM burst size settings.

– If multiple devices are programmed, an address map header is needed for each device. The address map header specifies the CRC value and the Device EEPROM Start Address.
– If EEPROM Size > 256 Bytes Enable Bit is NOT set:
  • EEPROM Size = 3 Bytes (Base Header) + Number of devices x 8 Bytes/device (Address Header) + Number of slots x 66 Bytes/slot (Data)
– If EEPROM Size > 256 Bytes Enable Bit is set:
  • EEPROM Size = 3 Bytes (Base Header) + Number of devices x 12 Bytes/device (Address Header) + Number of slots x 66 Bytes/slot (Data)

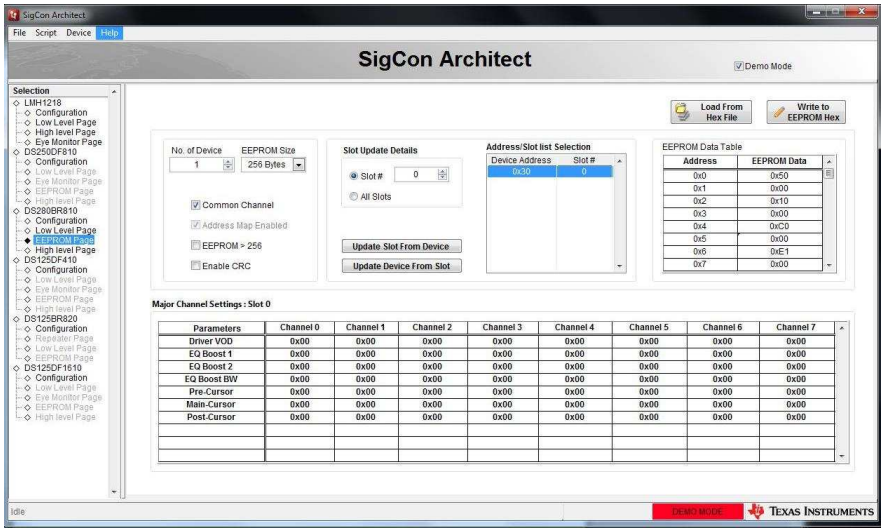

Figure 9. SigCon Architect EEPROM Page

NOTE: Profile versions 1.0.1.0 and earlier do not support CRC with EEPROM size set to larger 256 bytes.

5 Example Hardware Test Setup

5.1 Equalizing Moderate Pre-Channel Loss

The following is an example test setup configuration which demonstrates the DS280BR8x0 equalizing for moderate pre-channel insertion loss introduced by an FR4 channel at 25.78125 Gbps and 10.3125 Gbps.

Figure 10. 5in Input Channel And minimal Output Channel Test Setup

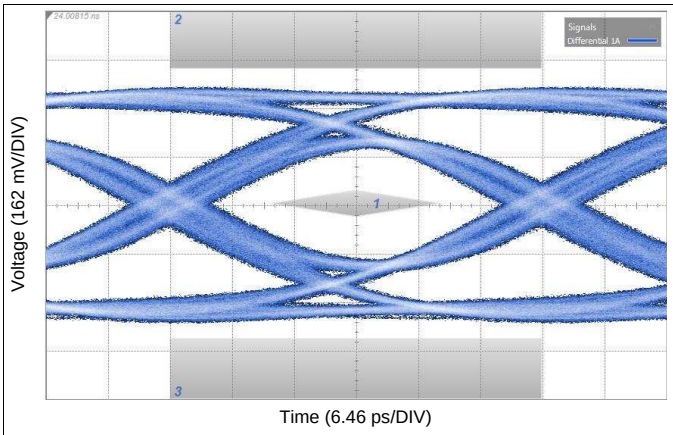

Figure 11. 25.78125 Gbps CAUI-4 Eye Mask With 5in Input Channel And Minimal Output Channel

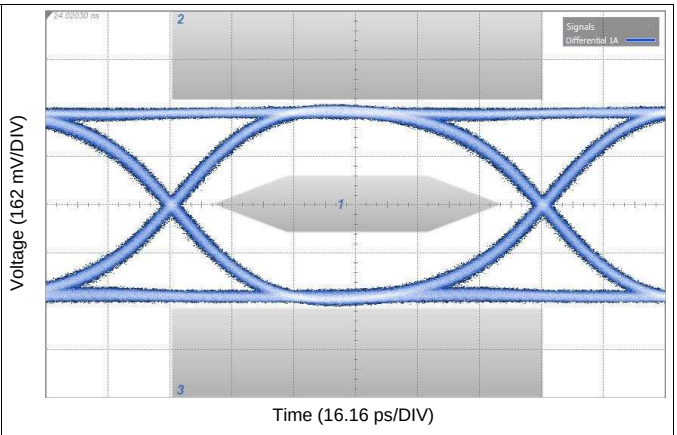

Figure 12. 10.3125 Gbps nPPI Eye Mask with 5in Input Channel and Minimal Output Channel

Table 4. Settings and Measurements for CAUI-4 and nPPI with 5in Input Channel and Minimal Output Channel

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line 1	5 in 5 mil FR4 + 8in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR820 Rx Channel Loss	14 dB @ 12.9 GHz (includes 4 dB from the EVM and Huber+Suhner cable assembly)	6 dB @ 5.2 GHz (includes 2 dB from the EVM and Huber+Suhner cable assembly)
DS280BR820 Tx Channel Loss	4.5 dB @ 12.9 GHz (includes 4 dB from the EVM and Huber+Suhner cable assembly)	2 dB @ 5.2 GHz (attributed to the EVM and Huber+Suhner cable assembly)
EQ BST1	3	3
EQ BST2	0	0
EQ BW	3	3
VOD	3	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	11.9 ps_{P-P}	13.0 ps_{P-P}
Differential Eye Height @ 1E-15	338 mV_{P-P}	544 mV_{P-P}
Mask violations	0	0

5.2 Equalizing High Pre-Channel Loss

The following is an example test setup configuration which demonstrates the DS280BR8x0 equalizing for high pre-channel insertion loss introduced by an FR4 channel at 25.78125 Gbps and 10.3125 Gbps

Figure 13. 10in Input Channel and Minimal Output Channel Test Setup

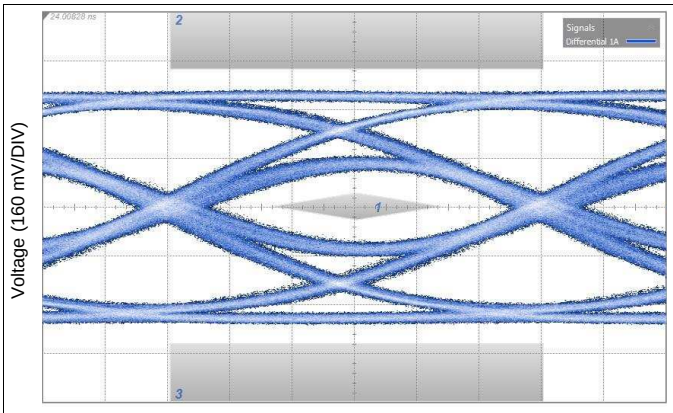

Figure 14. 25.78125 Gbps CAUI-4 Eye Mask with 10in Input Channel and Minimal Output Channel

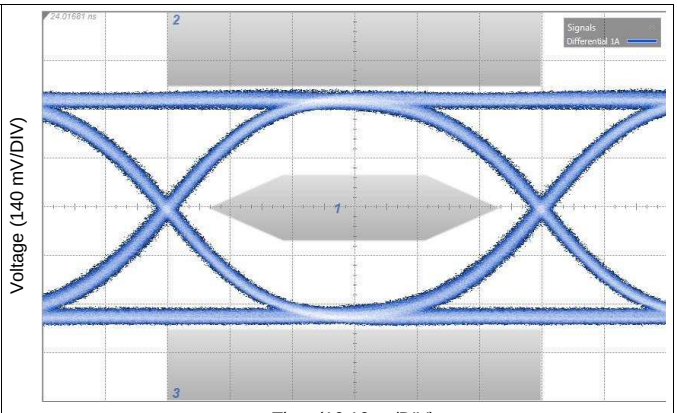

Figure 15. 10.3125 Gbps nPPI Eye Mask with 10in Input Channel and Minimal Output Channel

Table 5. Settings and Measurements for CAUI-4 and nPPI with 10in Input Channel and Minimal Output Channel

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line 1	10 in 5 mil FR4 + 8in SMA cable	10 in 5 mil FR4 + 8 in SMA cable
DS280BR820 Rx Channel Loss	22 dB @ 12.9 GHz (includes 4 dB from the EVM and Huber+Suhner cable assembly)	10 dB @ 5.2 GHz (includes 2 dB from the EVM and Huber+Suhner cable assembly)
DS280BR820 Tx Channel Loss	4.5 dB @ 12.9 GHz (includes 4 dB from the EVM and Huber+Suhner cable assembly)	2 dB @ 5.2 GHz (attributed to the EVM and Huber+Suhner cable assembly)
EQ BST1	6	6
EQ BST2	1	1
EQ BW	3	3
VOD	3	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	11.3 ps_{P-P}	13.5 ps_{P-P}
Differential Eye Height @ 1E-15	210 mV_{P-P}	532 mV_{P-P}
Mask violations	0	0

6 Common Problems and Suggested Solutions

PROBLEM	ADDITIONAL INFORMATION	POSSIBLE SOLUTIONS
Cannot power on the EVM	2.5 Volt Power mode D35 LED is off	• J198: jumper pins 1-2 tied. • J207: jumper pins should be set to float. • Verify configuration with Figure 6 .
	3.3 Volt Power mode D35 LED is off	• J198: remove jumper shunt; This shunt needs to be removed in order toenable 2.5 V regulator. • J207: jumper pins 9-10, 7-8, 5-6, 3-4, and 1-2 tied to connect the regulator output to the DS280BR8x0 VDD supply.
Cannot connect to the device in SMBus Slave Mode	SigCon Architect is operating in Demo Mode	• Verify the jumper settings are correct (Figure 6).
		• Verify the slave address is set to 0x30 for SMBus Slave Mode.
		• Verify the device is powered on.
		• Update Firmware on EVM using “USB2ANY Explorer."
	Never used SigCon Architect, and cannot establish connection with device	• Reinstall SigCon Architect. It is essential SigCon Architect is closed during any portion of the installation process.
Oscilloscope’s Eye Diagram is not as expected	Pattern does not lock on oscilloscope	• Transmit a signal from the pattern generator (i.e. BERT) with a different PRBS pattern. Once initial pattern lock is established, re-attempt desired pattern.
		• Transmit a signal from the pattern generator (i.e. BERT) with a lower frequency. Once initial pattern lock is established, re-attempt desired frequency.
	Eye diagram does not pass mask	• Vary EQ Boost Settings as seen in Figure 7.
Cannot vary FIR parameters	Attempting to change pre-cursor and post-cursor to positive values	• The pre-cursor and post-cursor can only be negative values. • The FIR is only available in limiting mode.
	Can vary FIR parameters on SigCon Architect, but do not see change on Oscilloscope	• Verify the “Channel Select” drop down menu reads the desired channel. • The FIR parameters will not be applied to the device until the “Apply to Channel” or “Apply to All Channels” button is clicked. • The FIR is only available in limiting mode. • Verify the evaluation module is powered on.
Cannot burn EEPROM Hex File to EEPROM with SigCon Architect		• SigCon Architect can only be used to generate the Hex File. Another interface adapter must be used to burn the Hex File to the EPPROM. (i.e. AARDVARK or equivalent).

7 Bill of Materials

The following table represents the bill of materials (BOM) for the DS280BR810EVM.

#	QUANTITY	REFERENCE	VALUE	PART NUMBER	DESCRIPTION
1	1	C327	1 uF	C0603X5R0J105M030BC	CAP CER 1UF 6.3V 20% X5R 0201
2	1	C2	0.1uF	C1005X7R1H104K050BB	CAP CER 0.1UF 50V 10% X7R 0402
3	12	C68,C69,C70,C71,C329,C330,C333,C334,C335,C336,C337,C338	0.1uF	C0603X5R1E104K030BB	CAP CER 0.1UF 25V 10% X5R 0201
4	1	C5	10 uF	GRM21BR61E106KA73L	CAP CER 10UF 25V 10% X5R 0805
5	1	C6	1 uF	GRM188R61E105KA12D	CAP CER 1UF 25V 10% X5R 0603
5	1	C7	22 uF	T491C226M016ZT	CAP TANT 22UF 16V 20% 2413
6	1	C18	2.2 nF	C0603C222M3RACTU	CAP CER 2200PF 25V 20% X7R 0603
7	3	C19,C22,C24	0.1 uF	GRM155R71C104KA88D	CAP CER 0.1UF 16V 10% X7R 0402
8	2	C20,C21	30 pF	GRM1885C1H300JA01D	CAP CER 30PF 50V 5% NP0 0603
9	1	C23	0.47 uF	EMK107B7474KA-T	CAP CER 0.47UF 16V 10% X7R 0603
10	1	C25	0.1 uF	C0603C104K4RACTU	CAP CER 0.1UF 16V 10% X7R 0603
11	2	C26,C31	220 pF	C0603C221K5RACTU	CAP CER 220PF 50V 10% X7R 0603
12	1	C27	22 uF	EEE-1AA220WR	CAP ALUM 22UF 10V 20% SMD
13	1	C28	1 uF	C2012X7R1C105K125AA	CAP CER 1UF 16V 10% X7R 0805
14	1	C29	0.01 uF	CGJ3E2X7R1C103K080AA	CAP CER 10000PF 16V 10% X7R 0603
15	1	C30	2.2 uF	LMK212B7225KG-T	CAP CER 2.2UF 10V 10% X7R 0805
16	2	C299,C332	1 uF	CC0603ZRY5V6BB105	CAP CER 1UF 10V Y5V 0603
17	1	C300	47 uF	TAJB476K010RNJ	CAP TANT 47UF 10V 10% 1210
18	1	C328	10 uF	AMK105CBJ106MV-F	CAP CER 10UF 4V 20% X5R 0402
19	1	C331	10 uF	TAJP106M010RNJ	CAP TANT 10UF 10V 20% 0805
20	5	D1,D2,D4,D36,D38	LED	LTST-C191KGKT	LED GREEN CLEAR THIN 0603 SMD.
21	3	D6,D8,D35	RED-LED	LS M67K-J2L1-1-Z	LED MINI TOPLED RED 630NM SMD
22	1	D9	1SMB5922BTS	1SMB5922BT3G	DIODE ZENER 7.5V 3W SMB
23	1	FB1	BK1608HS600-T	BK1608HS600-T	FERRITE BEAD 60 OHM 0603
24	2	J1,J2	SMA	142-0701-201	CONN SMA JACK STR 50 OHM PCB
25	2	J5,J210	HEADER_3	87224-3	CONN HEADER VERT .100 3POS 15AU
26	4	J6,J11,J209,J211	HEADER 6X2	87227-6	CONN HEADER VERT .100 12POS 15AU
27	4	J8,J10,J21,J25	HEADER 2X2	87227-2	CONN HEADER VERT .100 4POS 15AU
28	1	J9	4 HEADER	901200764	CONN HEADER 4POS .100" STR GOLD
29	1	J13	Binding Post, Keystone 7007, Black	7007	POST BINDING ECON NYLON-INS BLK

#	QUANTITY	REFERENCE	VALUE	PART NUMBER	DESCRIPTION
30	2	J14,J208	Binding Post, Keystone 7006, Red	7006	POST BINDING ECON NYLON-INS RED
31	4	J18,J19,J203,J204	1x8A_81_MXP-S50-0-2	1x8A_81_MXP-S50-0-2/111_NE	
32	2	J24,J26	HEADER 2	87224-2	CONN HEADER VERT .100 2POS 15AU
33	1	J27	USB_Conn_1734035-2	1734035-2	CONN MINI USB RCPT RA TYPE B SMD
34	1	J198	HEADER, 2-PIN	87224-2	CONN HEADER VERT .100 2POS 15AU
35	1	J207	HEADER 5x2/SM_1	87227-5	CONN HEADER VERT .100 10POS 15AU
36	1	Q1	BSS138	BSS138	MOSFET N-CH 50V 220MA SOT-23
37	3	R1,R3,R48	4.7K	ERJ-2GEJ472X	RES 4.7K OHM 1/10W 5% 0402 SMD
38	2	R2,R4	100	CRCW0402100RFKEDHP	RES 100 OHM .125W 1% 0402 SMD
39	6	R5,R20,R30,R47,R409,R418	249	RC1005F2490CS	RES 249 OHM 1/16W 1% 0402
40	3	R6,R7,R8	2.7K	ERJ-2GEJ272X	RES 2.7K OHM 1/10W 5% 0402 SMD
41	2	R9,R10	0	ERJ-2GE0R00X	RES 0.0 OHM 1/10W JUMP 0402 SMD
42	5	R13,R14,R15,R17,R18	2.7K	ERJ-2GEJ272X	RES 2.7K OHM 1/10W 5% 0402 SMD
43	2	R16,R19	4.7K	ERJ-2GEJ472X	RES 4.7K OHM 1/10W 5% 0402 SMD
44	8	R21,R27,R33,R37,R406,R408,R415,R417	1K	ERJ-2GEJ102X	RES 1.0K OHM 1/10W 5% 0402 SMD
45	4	R26,R36,R407,R416	10K	ERJ-2GEJ103X	RES SMD 10K OHM 5% 1/10W 0402
46	1	R43	750	ERJ-3GEYJ751V	RES 750 OHM 1/10W 5% 0603 SMD
47	1	R45	33k	RC0402JR-0733KL	RES 33K OHM 1/16W 5% 0402 SMD
48	1	R46	200	ERJ-3GEYJ201V	RES 200 OHM 1/10W 5% 0603 SMD
49	1	R49	10.0K	ERJ3EKF1002V	RES 10K OHM 1/10W 1% 0603 SMD
50	2	R50,R51	33	CRCW040233R2FKEDHP	RES 33.2 OHM .125W 1% 0402 SMD
51	1	R52	1.5K	CRCW04021K50FKEDHP	RES 1.50K OHM .125W 1% 0402 SMD
52	1	R53	33K	ERJ-2GEJ333X	RES 33K OHM 1/10W 5% 0402 SMD
53	1	R54	1.2M	ERJ-2GEJ125X	RES 1.2M OHM 1/10W 5% 0402 SMD
54	2	R358,R359	10K	CRCW040210K0FKEDHP	RES 10.0K OHM .125W 1% 0402 SMD
55	1	R360	360	ERJ-3GEYJ361V	RES 360 OHM 1/10W 5% 0603 SMD
56	1	SW1	SW_DIP_SWITCH	76STD01T	SWITCH DIP TOGGLE 1POS
57	1	S1	EVQPSD02K	EVQ-PSD02K	SWITCH TACTILE SPST-NO 0.05A 12V
58	1	TP1	TEST POINT	5002	TEST POINT PC MINI .040"D WHITE
59	3	TP2,TP5,TP7	TEST POINT	5000	TEST POINT PC MINI .040"D RED
60	2	TP4,TP6	TEST POINT	5001	TEST POINT PC MINI .040"D BLACK
61	1	U1	Oscillator, 25 MHz, 2.5V	7C-25.000MCB-T	OSC XO 25.000MHZ CMOS SMD
62	1	U2	PDIP	111-43-308-41-001000	IC SOCKET 8PIN .300 SOLDER TAIL

#	QUANTITY	REFERENCE	VALUE	PART NUMBER	DESCRIPTION
63	1	U6	MSP430	MSP430F5529IPN or MSP430F5529IPNR	IC MCU 16BIT 128KB FLASH 80LQFP
64	1	U7	TXB0108	TXB0108PWR	IC 8-BIT TRNSTR 15KV ESD 20TSSOP
65	1	U8	TPD4E004DRY	TPD4E004DRYR	TVS DIODE 6SON
66	1	U9	TPS73533DRB	TPS73533DRBT	IC REG LDO 3.3V 0.5A 8SON
67	1	U11	DS280BR8xx_DS280DF8xx		
68	1	U16	TPS75725	TPS75725KTTRG3	IC REG LDO 2.5V 3A DDPAK
69	1	Y1	24.0 MHz	ECS-240-20-5PX-TR	CRYSTAL 24.000MHZ 20PF SMD
70	1	SV601200 REVC BOARD PCB			

8 EVM Cable Assemblies

The DS280BR810EVM uses Huber+Suhner 1x8 MXP cable assemblies. For Huber+Suhner quotes or additional information requests, please contact:
Info.us@hubersuhner.com
HUBER+SUHNER Inc.
8530 Steele Creek Place Drive, Suite H
Charlotte-NC- 28273
+1 704-790-7300

Below are suggested part numbers that can be used with this EVM. Other part numbers and cable lengths have not been tested, but can be considered for use.

1. 85014420, MF53/1x8A_21MXP/21SMA/152: “MXP-18 cable assembly”. This is a lower cost cable assembly compared to the MXP-40, but the SI performance is very good and more than adequate for 25Gbps operation.
2. 84099607, MF53/1x8A_21MXP/11SK/305: “MXP-40 cable assembly”. This cable assembly is designed specifically for 40+ GHz. It features a male cable end and longer cable length options.
3. 84098900, MF53/1x8A_21MXP/21SK_ergo/305: “MXP-40 cable assembly”. This cable assembly is designed specifically for 40+ GHz. It features a female cable end and longer cable length options.
4. 84099634, MF53/1x8A_21MXP/21/MXP/305: "MXP-50 cable assembly". This cable assembly is designed specifically for 50+ GHz. It features a MXP connections on both ends of the cable for board bridging and longer cable length options.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2015) to B Revision	Page
• Initial Public Release	1

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