ABT,Ratings,,Specifications,and

ABT Ratings, Specifications and Waveforms

Literature Number: SNOA004

National Semiconductor

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ABT Ratings, Specifications and Waveforms

Definition of Terms

DC Characteristics

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

I_{BVI} Input HIGH Current (Breakdown Test). The current flowing into an input when a specified Absolute MAX HIGH voltage is applied to that input.

I_{BVIT} I/O Pin HIGH Current (Breakdown Test). The current flowing into a disabled (output is high impedance) I/O pin when a specified Absolute MAX HIGH voltage is applied to that I/O pin.

I_{CEX} Output HIGH Leakage Current. The current flowing into a HIGH output due to the application of a specified HIGH voltage to that output.

I_{CCH} The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL} The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

I_{CCT} Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ} The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_{IL} Input LOW Current. The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{IH} Input HIGH Current. The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{OH} Output HIGH Current. The current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW Current. The current flowing into an output which is in the LOW state.

I_{OS} Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

I_{OZL} Output OFF current (LOW). The current flowing out of a disabled TRI-STATE® output when a specified LOW voltage is applied to that output.

I_{OZH} Output OFF current (HIGH). The current flowing into a disabled TRI-STATE output when a specified HIGH voltage is applied to that output.

I_{ZZ} Bus Drainage. The current flowing into an output or I/O pin when a specified HIGH level is applied to the output or I/O pin of a power-down device.

V_{CC} Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

V_{CD} Input Clamp Diode Voltage. The voltage on an input (−) when a specified current is pulled from that input.

V_{ID} Input Breakdown Voltage. The voltage on an input of a powered-down device when a specified current is forced into that input.

V_{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

V_{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

V_{IL} Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

V_{ILD} Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

V_{OHV} Minimum (valley) voltage induced on a static HIGH high output during switching of other outputs.

V_{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

V_{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_t Maximum Transistor Operating Frequency — The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Toggle Frequency/Operating Frequency — The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time — The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time — The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w Pulse Width — The time between 1.5V amplitude points of the leading and trailing edges of a pulse.

t_h Hold Time — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recogni-

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AC Characteristics (Continued)

tion. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup Time — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level — The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level — The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level — The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level — The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW levels.

t_{rec} Recovery Time — The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

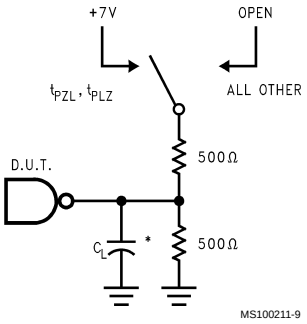
AC Loading and Waveforms

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all ABT devices, unless otherwise specified in the data sheet of a specific device. The value of the capacitive load (C_L) is variable and is defined in the AC Electrical Characteristics.

The 500Ω resistor to ground in *Figure 1* is intended to slightly load the output and limit the quiescent HIGH-state voltage to about +3.5V. Also shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establishes a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

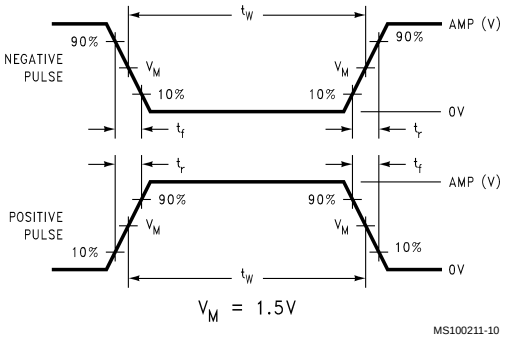
Figure 2 describes the input pulse requirements necessary when testing ABT circuits. *Figure 3* and *Figure 5* show waveforms for all propagation delay and pulse width measurements while *Figure 4* shows waveforms for TRI-STATE enable and disable times. The waveforms shown in *Figure 6* describe setup, hold and recovery times. These diagrams define all input and output measure points used in testing ABT devices.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2. Test Input Signal Levels and Requirements

AC Waveforms

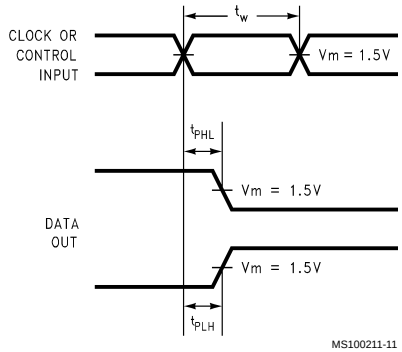


FIGURE 3. Propagation Delay, Pulse Width Waveforms

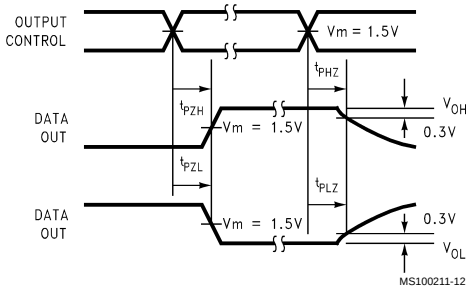


FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

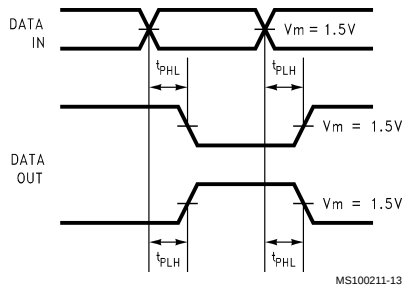


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

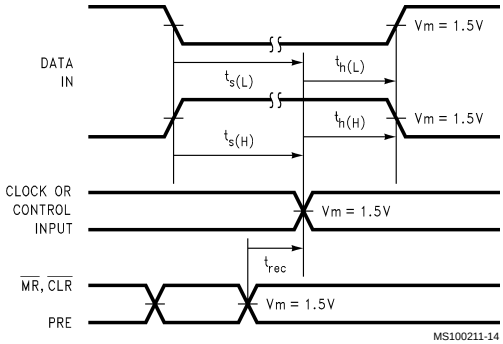


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into the ABT family of devices.

This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 8*.

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

Skew Definitions and Examples (Continued)

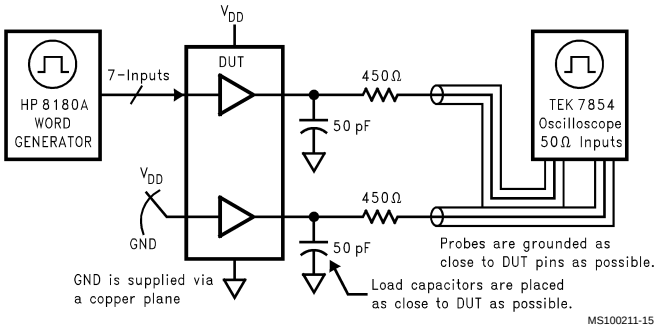


FIGURE 7. Simultaneous Switching Test Circuit

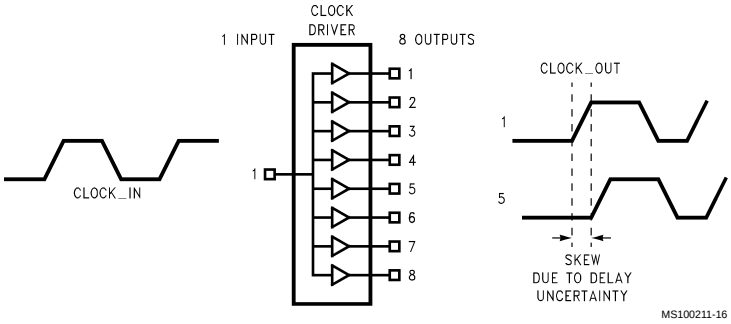


FIGURE 8. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

FIGURE 9. Sources of Clock Skew

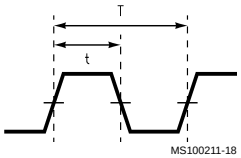
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles		
Total system skew budget = 10% of clock cycle = 2 ns*	→	2 ns
If extrinsic skew = 1 ns	→	− 1 ns
Device skew (intrinsic skew) must be less than 1 ns!	←	1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



Duty Cycle = t/T * 100%

FIGURE 10. Duty Cycle Calculation

Skew Definitions and Examples

(Continued)

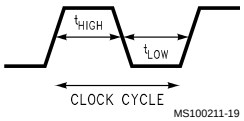


FIGURE 11. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

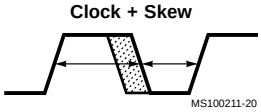


FIGURE 12. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE 1.

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle	
50 MHz	0 ns	10 ns	10 ns	50/50%	← Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%	
50 MHz	1 ns	11 ns	9 ns	55/45%	
33 MHz	2 ns	17 ns	15 ns	55/45%	← Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHLMAX} - t_{PHLMIN}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLHMAX} - t_{PLHMIN}|$

Propagation delays are measured across the outputs of any given device.

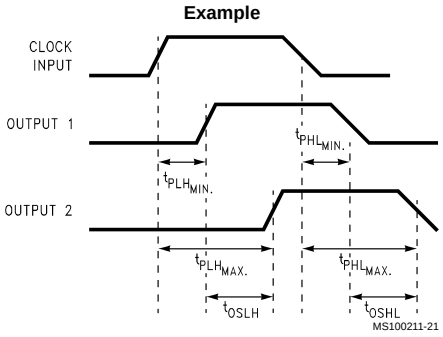


FIGURE 13. t_{OSLH}, t_{OSHL}

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

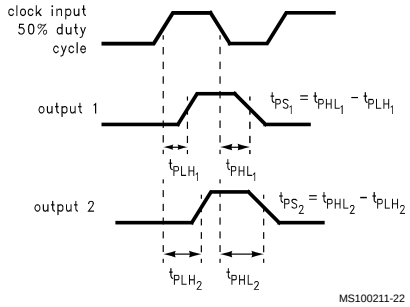


FIGURE 14. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE 2. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**

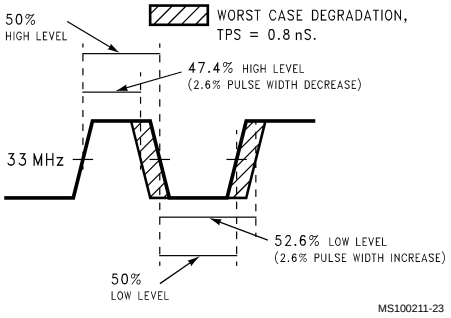


FIGURE 15. Pulse Width Degradation

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

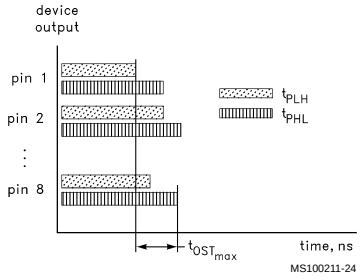


FIGURE 16. t_{OST}

Definition

t_{OST} (Opposite Edge Skew):

$t_{OST} = |t_{P\phi m} - t_{P\phi n}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example

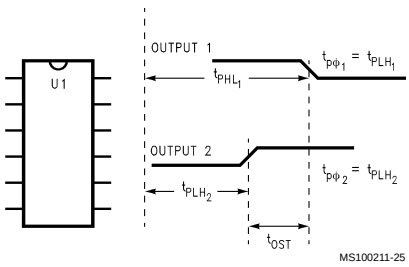


FIGURE 17. t_{OST}

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

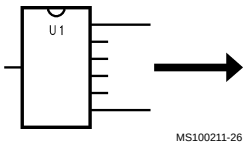
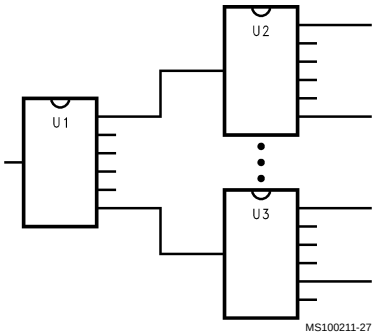


FIGURE 18. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1

= t_{OSLH} or t_{OSHL} of U1



Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\phi u,v} - t_{P\phi x,y}|$

where ϕ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.

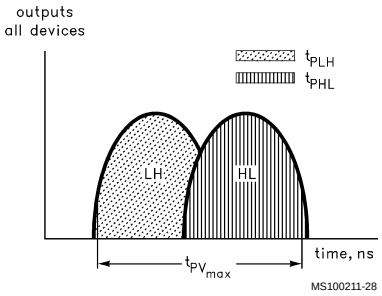


FIGURE 19. t_{PV}

Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Example

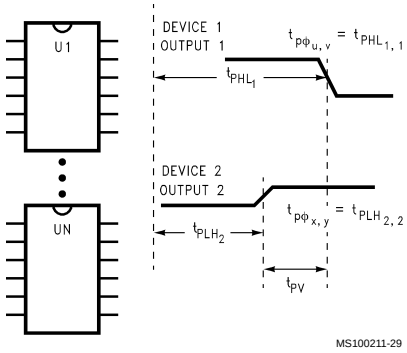


FIGURE 20. t_{PV}

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
Plastic	−55˚C to +150˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Commercial	−40˚C to +85˚C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

(except as noted on device datasheet)

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage					V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −12 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test					V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V (I/O Pins)
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V (I/O Pins)
I_{OS}	Output Short-Circuit Current				−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	V_{OUT} = HIGH Z

DC Electrical Characteristics (Continued)

(except as noted on device datasheet)

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
I_{CCT}	Additional	Outputs Enabled			2.5	mA		$V_I = V_{CC} - 2.1V$
	I_{CC}/Input	Outputs TRI-STATE			2.5	mA	Max	Enable Input $V_I = V_{CC} - 2.1V$
		Outputs TRI-STATE			50	µA		Data Input $V_I = V_{CC} - 2.1V$
								All Others at V_{CC} or GND
								$\overline{OE} = V_{CC}$; V_{OUT} = HIGH Z

Characterization and Extended Test Specifications

Philosophy

During the National new product introduction process for logic IC's, a new ABT IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, V_{tn}, V_{tp} L_{eff}, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, V_{CC} , temperature, and condition. This allows product to be shipped on demand without problems or delays.

The following are brief summaries of characterization tests performed.

Test Summaries

AC Electrical Characteristics

Single Output Switching propagation delays

Testing includes measured propagation delays at 50 pF and 250 pF output load capacitances.

t_{PLH}	Active Propagation Delays
t_{PHL}	
t_{PZH}	Enable Propagation Delays
t_{PZL}	
t_{PLZ}	Disable Propagation Delays
t_{PHZ}	

Also included are input timing parameters

t_S	Setup Time
t_H	Hold Time

Multiple (Simultaneous) Output Switching Propagation Delays

These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF and 250 pF output loads.

Multiple Output Switching Skew

Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

FMAX (synchronous logic)

FMAX determines the minimum frequency at which the device is guaranteed to operate for a clocked IC. This test is package and test environment sensitive.

Pulse Width (synchronous logic)

Pulse Width testing is used to define the minimum pulse duration that a flip-flop or latch input will accept and still function properly. This test is package and test environment sensitive.

F-Toggle (asynchronous logic)

F-Toggle is the minimum frequency at which the IC is guaranteed to function under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

AC Dynamic (Noise) Characteristics

V_{OLP}, V_{OLV} — Ground Bounce (Quiet Output Switching)

Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

V_{ILD}, V_{IHD} — Dynamic Threshold

Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

Input Edge Rate

This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

DC Electrical Characteristics

Automated Test Equipment (ATE) DC Tests

DC test data gathered show the performance of an IC to statically applied voltages and currents.

Functional Shmoo

The function shmoo shows the function operational window of an IC at a wide range of V_{CC}'s and temperatures.

Power Up & Power Down Output Shmoo

Similar to the function shmoo, the power up and power down output shmoo shows the DC operation of an output during power up and power down conditions.

Transfer Characteristic (V_{IN}/V_{OUT})

Input Traces (V_{IN}/I_{IN})

Output Traces (V_{OL}/I_{OL}, V_{OH}/I_{OH})

Power

Power-Up I_{CC} Traces

Shows how the supply current reacts to various input conditions during power up.

I_{CC} vs V_{IN} Traces

Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

I_{CCD} (Dynamic I_{CC})

Determines the amount of current an IC will consume at frequency.

Capacitance

Input/Output Capacitance (C_{IN}/C_{OUT})

Reliability Tests

Latch-up

Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

HBM Electrostatic Discharge, Human Body Model

Per MIL-STD-883C method 3015.6.

Extended Specifications

With the introduction of the ABT product family, National has taken new steps in aiding the system designer with a better method to predict device performance in his application. National now offers system oriented performance specifications so a designer can feel confident in the way a device will preform over a wider variety of switching conditions. Performance specifications in the form of Extended Specifications are provided with each product datasheet

In the past, most extended databook specifications depended on a representative product family function to provide the guaranteed performance data for the rest of the family. The drawback from this method of test and specmanship leaves rather large process, tester and function guardbands in the final maximum or minimum specifications. The test data for National's ABT product family, taken during product development on each function, provides the ABT family with device specific and guaranteed extended specifications that can be passed directly to the system designers. National offers the extended specifications with the belief that customers can reduce their incoming test requirements and in essence reduce the cost and time for product design-in.

Additional guaranteed specifications provided by National include: Single Output Switching (SOS) for 250 pF loads; Multiple Output Switching (MOS) for 50 pF and 250 pF loads; Skew; Quiet Output Switching (QOS) V_{OLP}, V_{OLV}, V_{OHP}, V_{OHV} and Dynamic Threshold (DVTH), V_{ILH}, and V_{IHD}.

Each of the guaranteed extended specifications involve multiple output switching events, with exception to the SOS specifications. During a multiple output switching event, stray inductance and capacitance inhibit product performance. National has developed standardized hardware that aligns with the industry for ABT product evaluations. Some of the features of the test fixturing include ground planes and low inductive connections, critical in evaluating the product and not the fixture. See Section 2.7 for more information on test fixture hardware.

The extended specfication tests have very similiar if not identical test setups. The results of the measurements from each test depend on the application focus. The quantitative analysis from the tests provides insight into product performance. The parameters and typical results from each test type can be easily explained in the sections that follow. Sample plots are generated from National's ABT244 and represent room temperature data at 5.0V V_{CC}.

TABLE 3. Test Conditions for MOS, Skew, QOS, DVTH

Parameter	Value
Input Edge Rate	2.5 ns
Input Skew	< 300 pS
Input Amplitude	0V to 3.0V
Input Frequency	1 MHz
Output Load	50 pF, 500Ω;
	250 pF, 500Ω

MULTIPLE OUTPUT SWITCHING

Multiple output switching simulates a worst case switching environment. With input edges deskewed to < 300 pS, the device has to provide simultaneous switching current for the output. The cumulative effect of environmental inductance and capacitance impacts the output edge rate and ultimately impacts propagation delay and noise immunity performance.

The plots of *Figure 21* thru *Figure 26* demonstrate the ability of the ABT product family to minimize enviromental inductance and capacitance effects as well as propagation delay degradation from increased number of outputs switching.

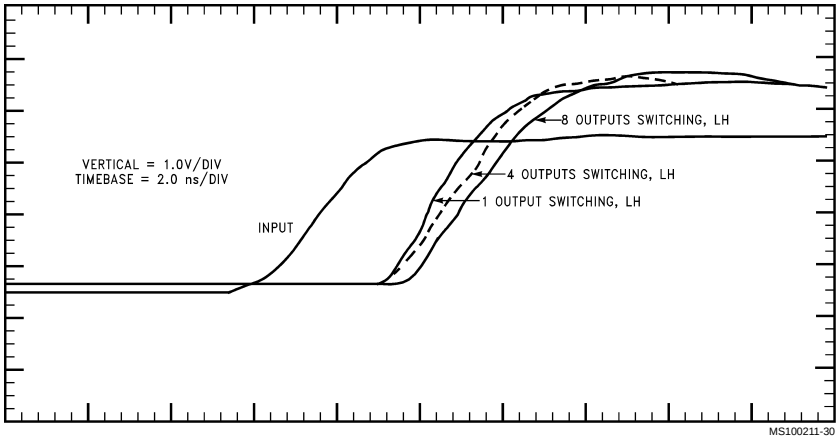


FIGURE 21. Multiple Outputs Switching, LH, 1, 4, 8 Outputs
74ABT244, V_{CC} = 5.0V, T_A = 25˚C

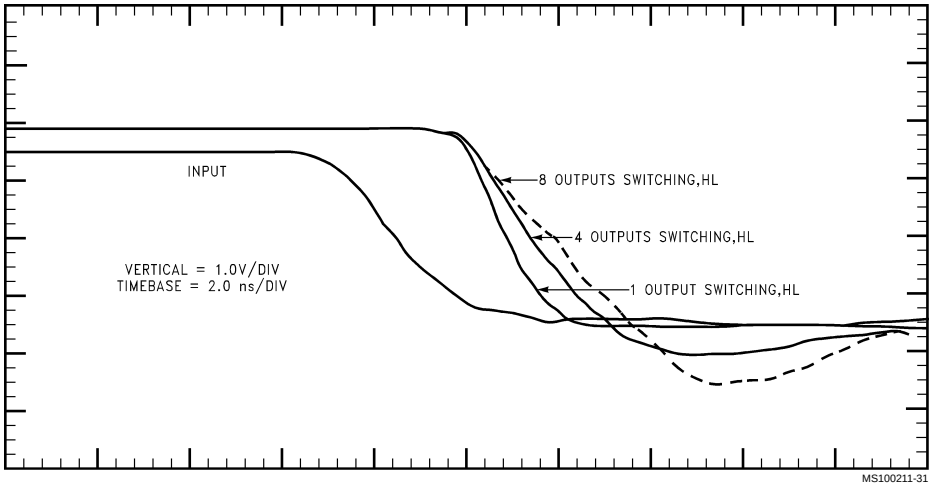


FIGURE 22. Multiple Output Switching, HL, 1, 4, 8 Outputs
74ABT244, V_{CC} = 5.0V, T_A = 25˚C

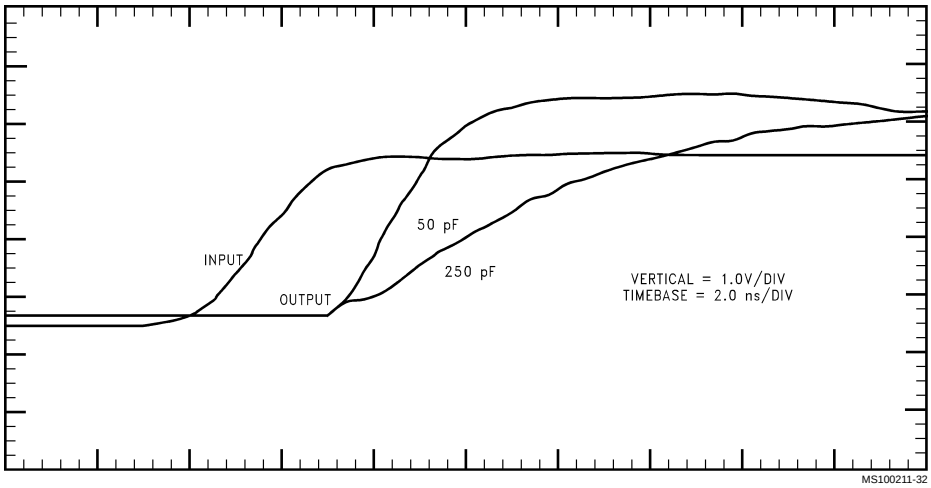


FIGURE 23. Single Output Switching, LH, 50 pF, 250 pF Capacitive Loading
74ABT244, V_{CC} = 5.0V, T_A = 25°C

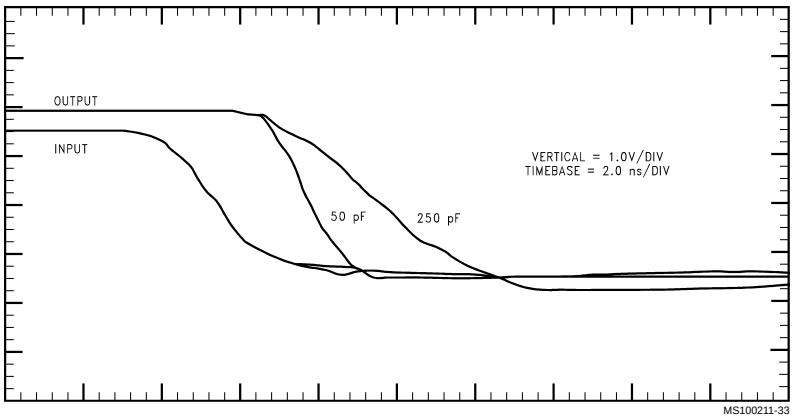


FIGURE 24. Single Output Switching, HL, 50 pF, 250 pF Capacitive Loading
74ABT244, V_{CC} = 5.0V, T_A = 25°C

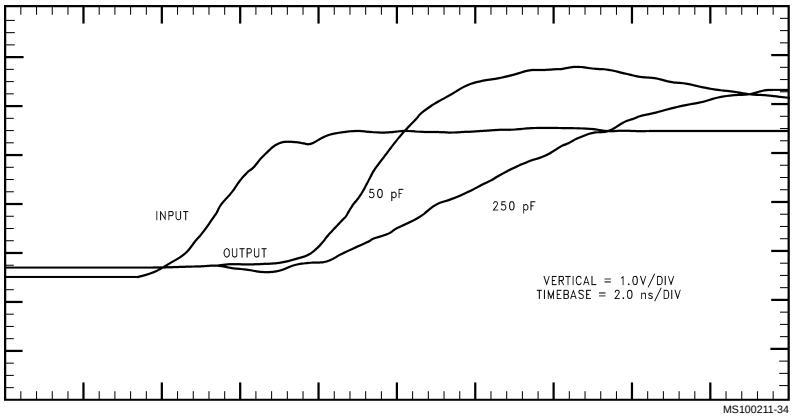


FIGURE 25. Multiple Outputs Switching (8) LH, 50 pF, 250 pF Capacitive Loading 74ABT244, V_{CC} 5.0V, T_A = 25˚C

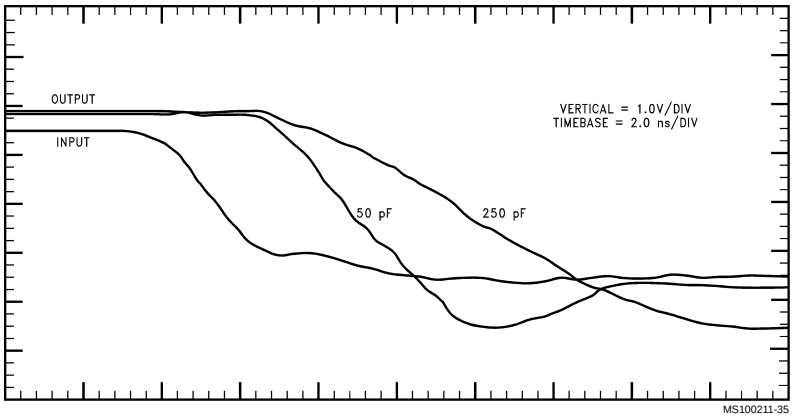


FIGURE 26. Multiple Output Switching (8) HL, 50 pF, 250 pF Capacitive Loading 74ABT244, V_{CC} = 5.0V, T_A = 25˚C

SKEW

Skew specifications provide a system designer with up front critical timing information to speed design cycle time. Skew measurements are derived from MOS propagation delay data rather than SOS propagation delay data. The advantage of MOS skew from a design engineer's viewpoint, is that MOS is a more realistic condition under which skew becomes critical.

Three modes of skew testing are published for each device in the ABT product family. Each skew mode describes a variance either within a pin (i.e. duty cycle), across to pins or across parts (i.e. process) for a given device function.

Within-a-Pin Skew, t_{PS}

Within-a-pin skew is designated by t_{PS} (pin skew), and describes each pin on a part and its ability to maintain 50% duty cycle. Pin skew is a calculation from the MOS propagation delays, t_{PLH} and t_{PHL} on each pin.

Across-Pin Skew, t_{OS}

Across-pin skew is designated by t_{OS} (output skew), and describes the MOS output edge difference across all output pins on a part. Across-pin skew can be broken down further into t_{OSLH}, t_{OSHL} and t_{OST}. The ($_{LH}$) indicates that output skew is measured across all outputs while switching low-to-high. The ($_{HL}$) indicates output skew measured on the high-to-low transition. The (t) infers that skew is measured across the outputs independent of a low-to-high or high-to-low edge or total output skew. Total output skew is calculated from the MOS propagation delays, t_{PLH} and t_{PHL}, across all pins.

Across-Part Skew, t_{PV}

Across-part skew is designated by t_{PV} (part variation), and describes the MOS output edge difference across all output pins on all parts in the population. Across-part skew is calculated from the MOS propagation delays, t_{PLH} and t_{PHL}, across all pins and all parts.

The plots in *Figure 27* and *Figure 28* describe skew performance in a 50 pF, 500Ω environment.

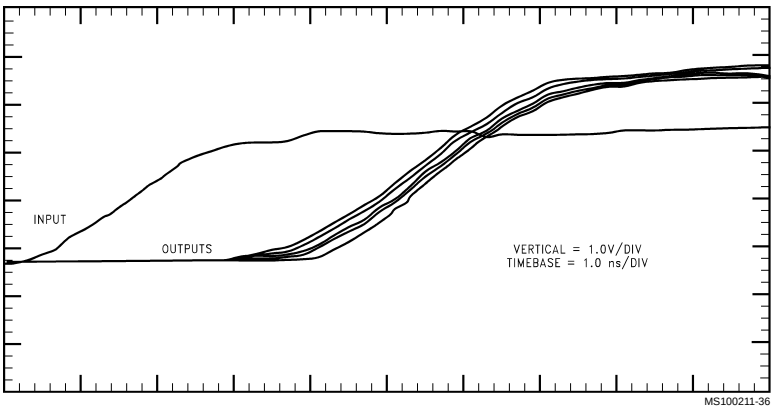


FIGURE 27. Skew 8 Outputs Switching, LH
74ABT244, V_{CC} = 5.0V, T_A = 25°C

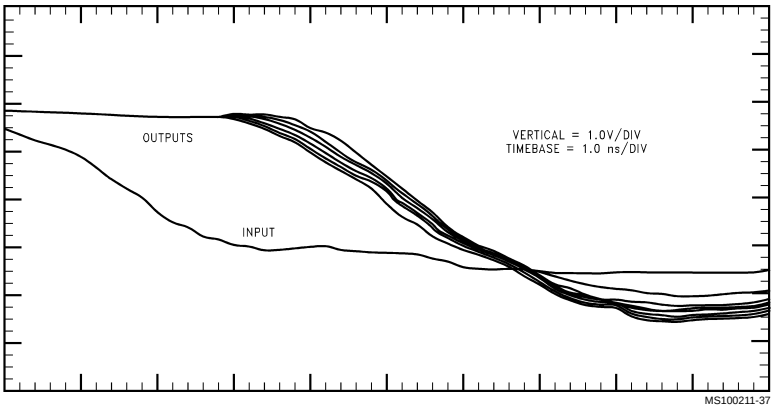


FIGURE 28. Skew 8 Outputs Switching, HL
74ABT244, V_{CC} = 5.0V, T_A = 25°C

QUIET OUTPUT SWITCHING

Quiet output switching, (QOS), specifications provide the system designer quantification of ABT's effective control of noise and performance to threshold specifications. The QOS specification is a representation of the resultant shift of an output voltage, either from a static high or low level on a single bit, while the other bits switch simutaneously in phase. The voltage shift from a quiet output is specified through four parameters.

- V_{OLP} and V_{OLV} describe the peak or valley of a voltage shift for a quiet output low level.
- V_{OHP} and V_{OHV} describe the peak or valley of a voltage shift for a quiet output high level.

The concern for the system designer evolves from the possiblity that the quiet output voltage shift could impact attached circuitry. V_{OLP} values on some product families peak above threshold high and become recognized as a logic HIGH. The period of time the voltage shift spends in the opposite state is short, in the neighborhood of 10–100 pS, and may not disrupt sequencial circuitry if it is level sensing. If the attached circuitry needs a rising edge, such as a clock input, the sequencial circuitry may take the inadvertent deflection and interpret it. National provides the QOS specification to assist in noise margin planning.

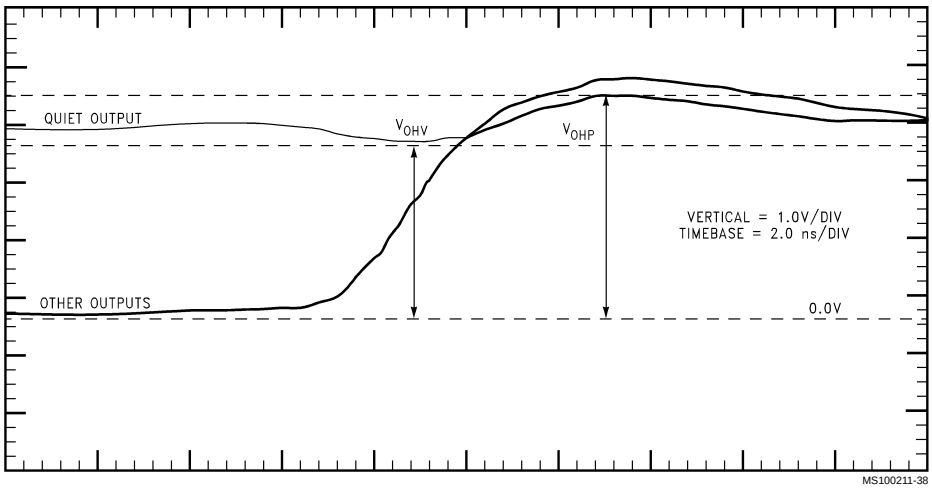


FIGURE 29. V_{OHV}, V_{OHP}
LH Transition 74ABT244, V_{CC} = 5.0V, T_A = 25˚C

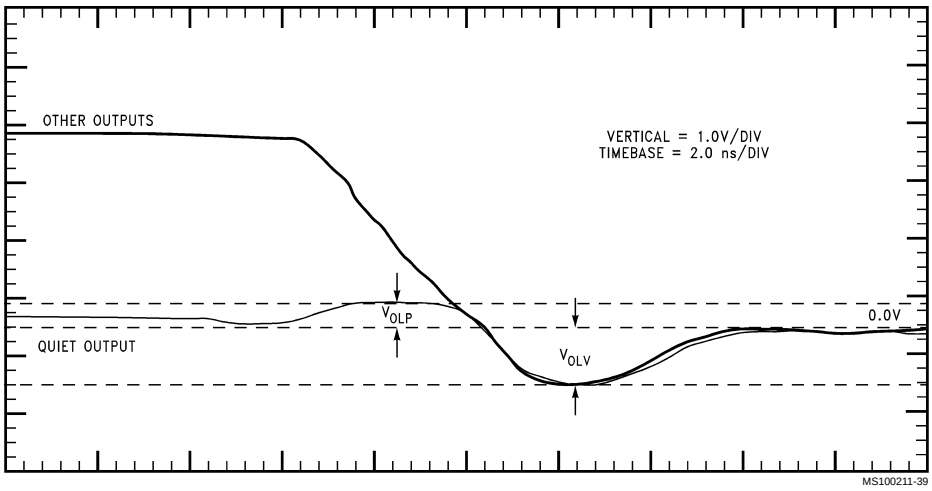


FIGURE 30. V_{OLP}, V_{OLV} HL Transition
74ABT244, V_{CC} = 5.0V, T_A = 25˚C

DYNAMIC THRESHOLD

Dynamic threshold data, (DVTH), like QOS data, provides the system designer with noise performance criteria. DVTH specifications quantify the magnitude of output voltage deflection that a logic high or low might experience under an MOS switching condition. The voltage deflection is a result of an apparent shift of an input's threshold due to noise generated from MOS switching on the internal die ground and V_{CC} busses. The phenomenon occurs during any logic state transition: LH, HL, ZL, etc. As a practice, National determines the worse case transition for each product and generates the specification based on that transition.

Dynamic threshold specifications are denoted by the nomenclature, V_{ILD} and V_{IHD}, where the "D" represents "Dynamic". The definitions for each are as follows,

- V_{ILD} - The maximum LOW input level such that normal switching/functional characteristics are observed on the output
- V_{IHD} - The minimum HIGH input level such that normal switching/functional characteristics are observed on the output

Dynamic threshold failures are bundled into five main failure modes. The most predominant failure is an output deflection in violation of an input threshold level. Others include propagation delay step out in excess of an MOS propagation delay specification, state changes and oscillations. A detailed definition of each failure can be described as follows,

1. On a low output, the LOW level will not rise above an input threshold low level of 0.8V after the transition of the output. *Figure 31* and *Figure 32*. Numbered output curve deflections are a result of 10 mV incremental changes on the low input signal level.
2. On a high output, the HIGH level will not drop below an input threshold high level of 2.0V after the transition of the output. *Figure 33* and *Figure 34*. Numbered output curve deflections are a result of 10 mV incremental changes on the high input signal level.
3. If the natural ringing, other than the initial bounce, of the output violates an input threshold level, the starting voltage level is noted and monitored until a 100 mV amplitute change towards threshold. If no amplitude change occurs, then the next peak or valley on the output is monitored for input threshold violation. *Figure 35*.
4. The propagation delay is monitored and is determined a failure when it exceeds the MOS propagation delay for that transition.
5. Gross failures including oscillation and functional state changes.

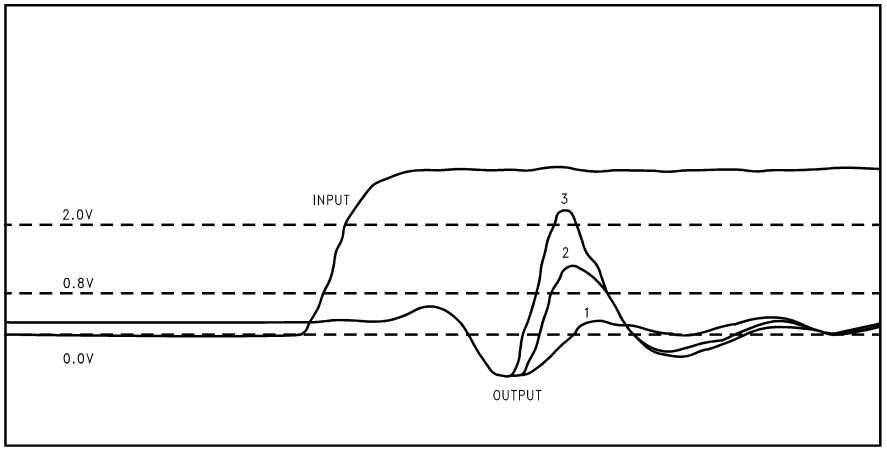


FIGURE 31. V_{ILD} 7 Outputs Switching
V_{CC} = 5.0V, T_A = 25˚C

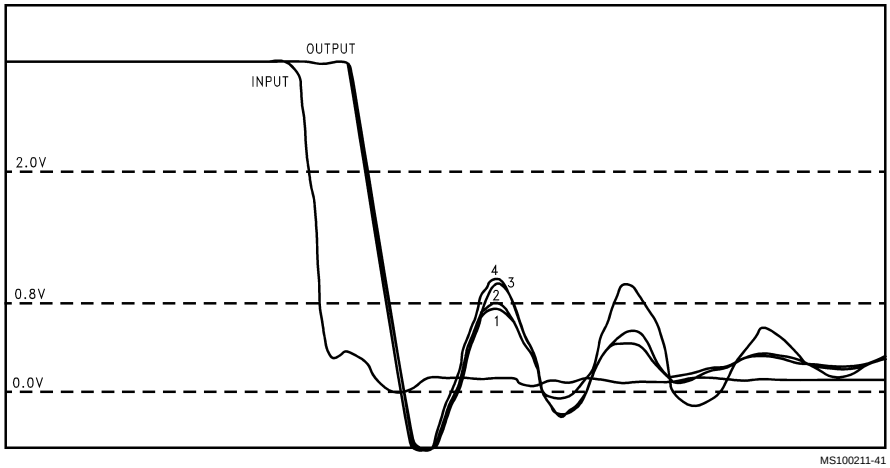


FIGURE 32. V_{ILD} 8 Outputs Switching
V_{CC} = 5.0V, T_A = 25˚C

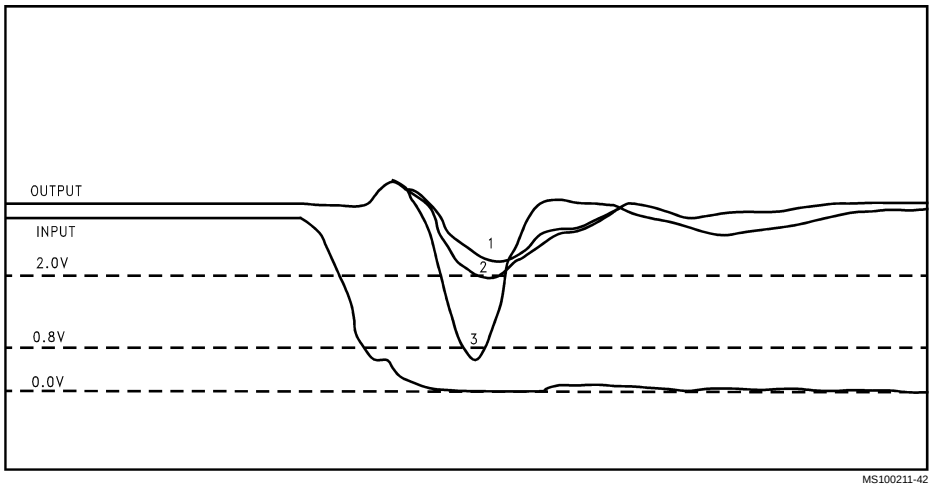


FIGURE 33. V_{IHD} 7 Outputs Switching
V_{CC} = 5.0V, T_A = 25˚C

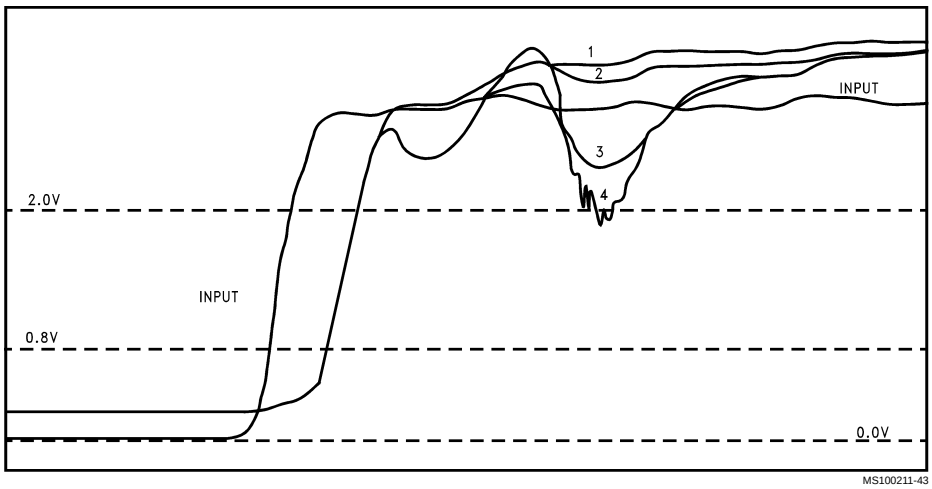


FIGURE 34. V_{IHD} 8 Outputs Switching
V_{CC} = 5.0V, T_A = 25˚C

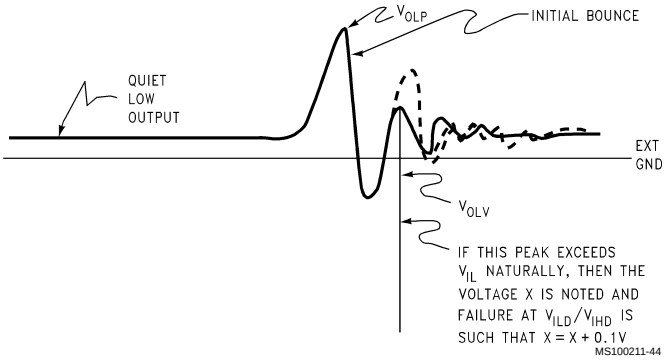


FIGURE 35.

Characterization Fixture

With the introduction of ABT product family with system level specifications that are guaranteed in a high performance AC environment, there is a necessity for a precise and repeatable test environment. Keeping in mind the defacto standards presented by Philips ABT fixture coupled with the understanding that our customers would like to correlate performance of like technologies, National reproduced an electrical equivalent AC fixture to that of the Signetics™ board documented in their Application Note 602.

To maximize correlation to National's product characterization one must match the environment in which the product was evaluated and make sure that National's implementation of load configuration, board, and DUT connection is followed as shown below.

Unique device pinouts, (20-, 24-, 48-lead, etc.) are used to obtain picosecond accuracy and repeatability. For this reason NSC recommends values of lumped and distributed capacitance used on its AC fixtures to prevent large variations in speed affected by transmission line capacitance.

Characterization Fixture (Continued)

Bare Board Front Layout Shown

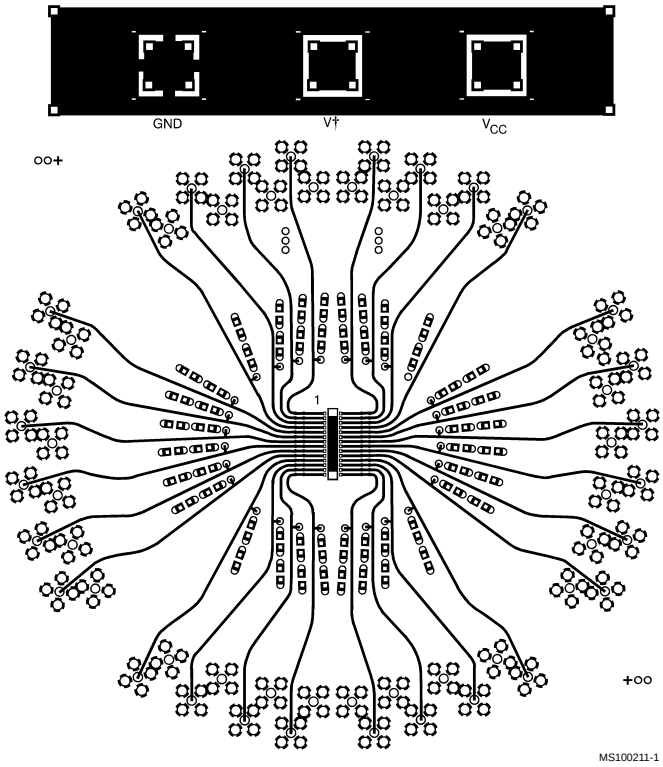


FIGURE 36. 28-Pin SOIC TOP (Viewed from Top)

Characterization Fixture (Continued)

Bare Board Back Layout Shown

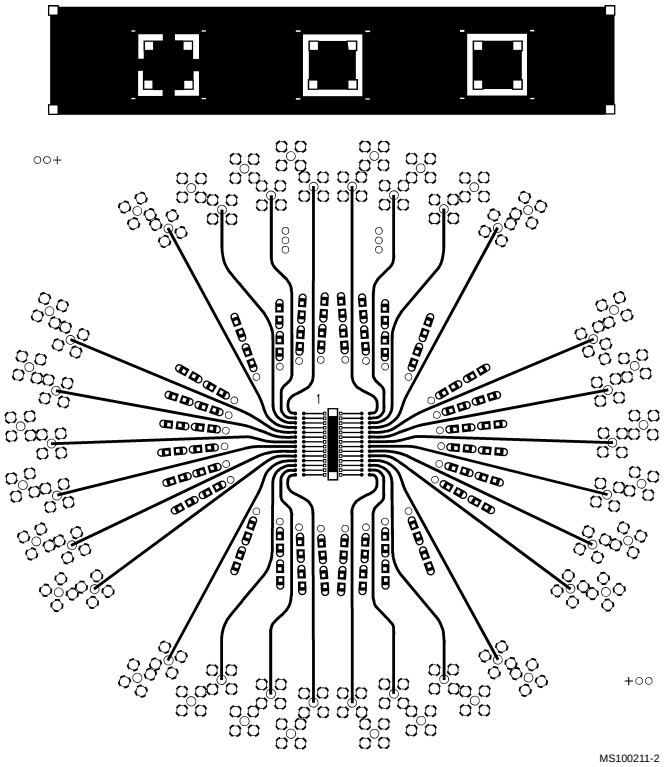
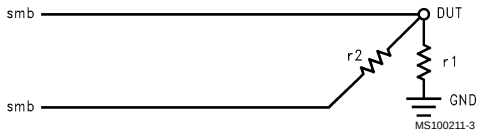


FIGURE 37. 28-Pin SOIC BOTTOM (Viewed from Top)

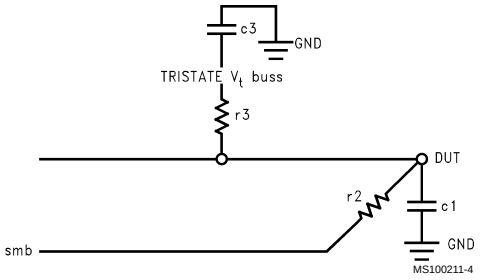
The blank AC fixture board can be used to implement the following input and output loads and terminations to provide the most repeatable environment in which to test a device.



r1 = 56Ω
r2 = 450Ω

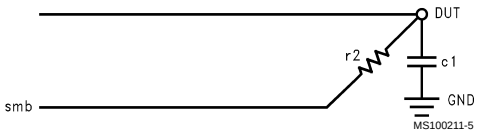
FIGURE 38. Input

Characterization Fixture (Continued)



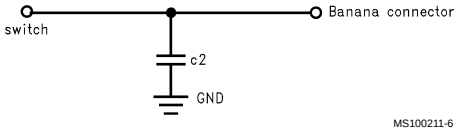
c1 = 27 pF
r2 = 450Ω
r3 = 500Ω

FIGURE 39. Output (TRI-STATE/Open Collector)



c1 = 27 pF
r2 = 450Ω
r3 = 500Ω

FIGURE 40. Output (2-State)



c2 = 0.1 µF

FIGURE 41.

Characterization Fixture (Continued)

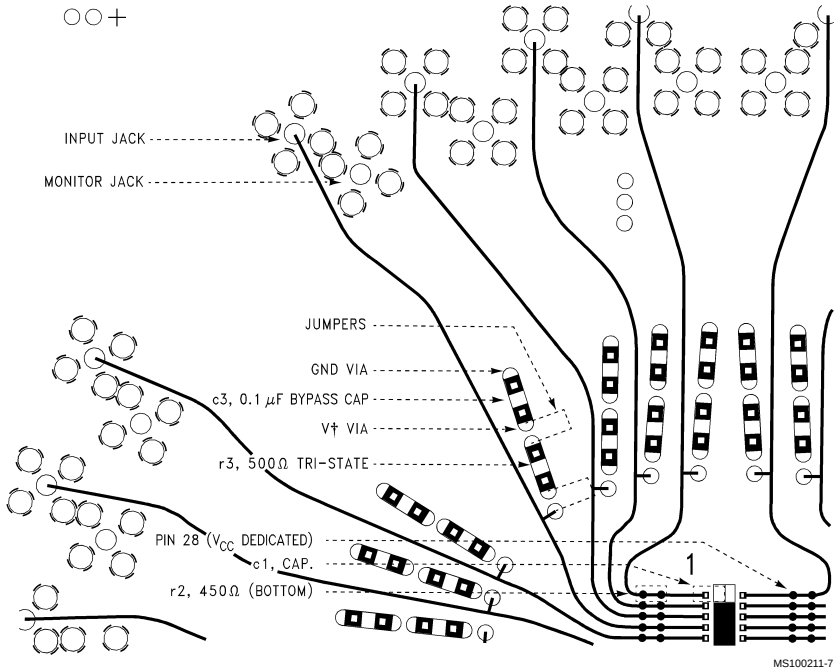


FIGURE 42. Component Placement on PC Board

National's AC fixture has the advantage of providing:

- low inductance V_{CC} and GND connections
- V_{CC} and GND planes to minimize cross talk and enhance power supply by-passing
- equal length 50Ω impedance signal and monitor lines to eliminate skew
- 50Ω input termination for ease of use
- 10:1 voltage reduction of the input and output signals to provide ease of use with standard oscilloscope inputs
- TRI-STATE load is integrated onto the same AC fixture and is connected via jumper to alleviate shunting effects when it is not required

Traces are spaced, and monitor lines are placed, on a different plane than the signal lines to reduce cross talk. *Figure 43* shows a cross section of layers used in the manufacture of National's AC test board. Vias in the signal trace are not used to ensure bandwidth. Ground connections are directly underneath the DUT to reduce the distance to the ground plane. Sense resistors are located directly adjacent to the DUT to reduce reflections.

For connection of the device to the board, a custom socket firmly presses the device against the board traces without any layers in between that add inductance or change their resitivity over temperature. The socket provides a minimum of contact resistance for the most accurate results. National designed a custom surface mount socket that provides the needed performance without damaging the device under test. Because of its shape and appearance, we call it the ferrari fixture.

In the characterization of National's product, we made efforts to correlate performance with other manufacturers. If a customer wishes to verify NSC results and requires an AC fixture, we recommend using Signetics AN-602 to build one. While the board that National uses is probably cost equivalent to the Signetics board, the socket used is expensive. If you wish to build a National fixture, please call the factory at 1-800-341-0392 and ask for applications. We can provide you with the component and manufacturer list for a National board along with a socket.

Characterization Fixture (Continued)

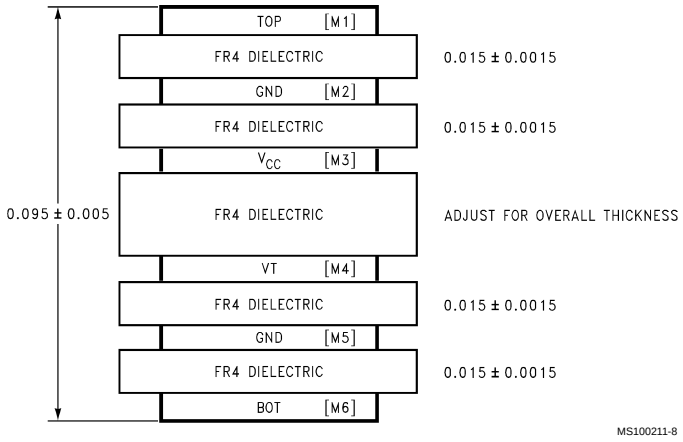


FIGURE 43. Layer Stacking Diagram

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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