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Application Report

OA-25 Stability Analysis of Current Feedback Amplifiers

ABSTRACT

High frequency current-feedback amplifiers (CFA) are finding a wide acceptance in more complicated applications from dc to high bandwidths. Often the applications involve amplifying signals in simple resistive networks for which the device-specific data sheets provide adequate information to complete the task. Too often the CFA application involves amplifying signals that have a complex load or parasitic components at the external nodes that creates stability problems.

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1 Introduction

This application report covers the discussion of using Bode analysis to determine the gain and phase margin while including external parameters. It discusses how to determine the input buffer gain and its effect on the closed-loop gain. A more appropriate mathematical model is developed for a clearer understanding of the poles and zeros of the CFA amplifier. Finally a summary of how parasitic components influence the frequency and time domain response.

2 Stability Review

Bode analysis is one of the more useful methods for determining stability for an amplifier. When an engineer selects a unity gain stable voltage-feedback amplifier, the internal compensation of the amplifier is transparent to the end user of the amplifier. If the VFA is connected to a complex load and it alters the phase margin then often the part will oscillate or peak the frequency response. Adding external compensation networks with capacitors and resistors will generally stabilize the amplifier. Of course, this is done at the expense of additional components and cost. With a CFA amplifier, stabilization is accomplished by adjusting the feedback resistor. Thus, one component, the feedback resistor, controls the phase and gain margin of the amplifier. The most practical way to determine stability of current-feedback amplifier is by Bode plots generated from computer simulations.

3 Review of Bode Analysis

Bode analysis is the easiest predictor for determining amplifier stability. The measurement is based upon creating an open-loop magnitude and phase plot to arrive at the closed-loop stability, indicators of gain and phase margin. The phase margin is derived by finding the intersection of the closed-loop unity gain frequency response curve to the open-loop response curve as shown in Figure 1. At this frequency the phase is read from the phase plot. This value is subtracted from 180° to arrive at the desired phase margin. Similarly the frequency at 180° is used to determine the gain margin in the magnitude plot shown in Figure 1. A recommended phase margin is at least 60° with gain margin of 12 dB.
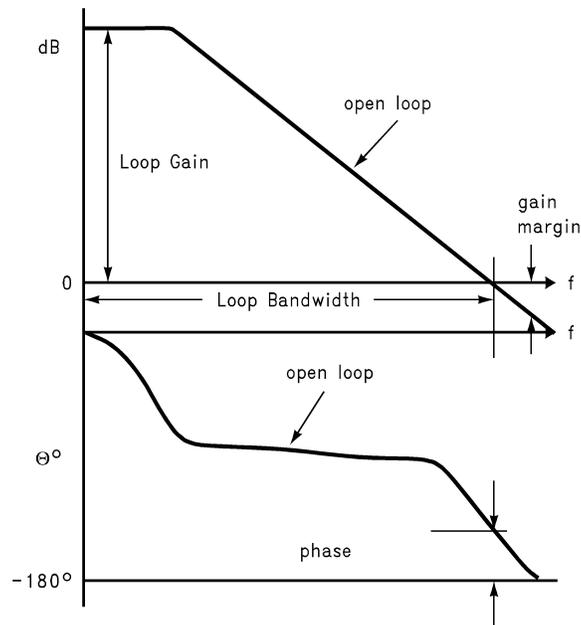

Figure 1. Bode Analysis

4   A Better Model

A practical voltage follower has output resistance that creates a need for a more comprehensive model. That model is developed in Figure 2 and allows us to mathematically model the effects of critical parameters. For example, if an application consists of amplifying continuous waveforms, then this model allows us to determine gain-accuracy, stability, impedances, frequency response and output swing for a particular load requirement.
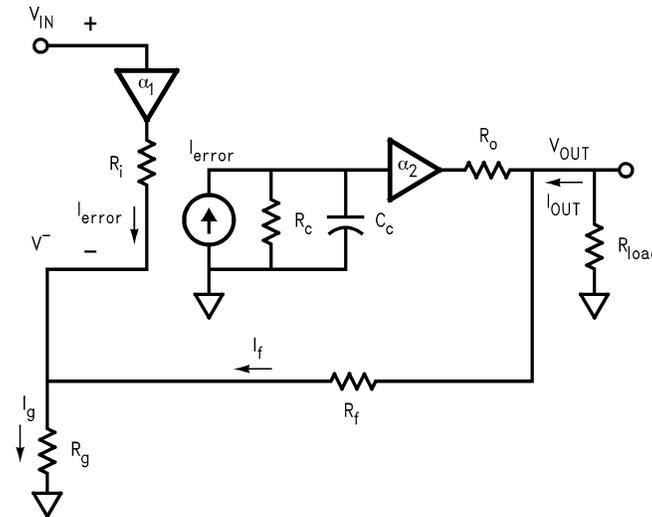

Figure 2. Practical Model

5   Mathematical Justification

Our first task is to derive a transfer function by nodal analysis for an infinite load condition.

$$I_{error} = I_g - I_f$$

$$I_{error} = \frac{V^-}{R_g} - \frac{V_{OUT} - V^-}{R_f}$$

$$V_{OUT} = I_{error}(\alpha_2 \cdot Z(s)) - I_f \cdot R_o$$

$$V^- = \alpha_1 \cdot V_{IN} - I_{error} \cdot R_i$$

Equation 1

(1)

After combining and eliminating the terms V^- and I_{error} in Equation 1, a transfer function is derived by dividing V_{OUT} by V_{IN} as seen in Equation 2.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \cdot A_v\left(1 + \dfrac{R_o}{A_v \cdot \alpha_2 \cdot Z(s)}\right)}{1 + \dfrac{R_f + R_i \cdot A_v + R_o\left(1 + \dfrac{R_i}{R_g}\right)}{\alpha_2 \cdot Z(s)}}$$

$$A_v = 1 + \frac{R_f}{R_g}$$

Equation 2

(2)

The $Z(s)$ in Equation 2 is the open-loop transimpedance gain and its value is derived by dividing the output voltage V_{OUT} by the current through V_{IN}, shown in the schematic of Figure 3. The terms "α_1 and α_2" are the buffer gains while R_o is the open loop output resistance.

Although this equation has many variables, most of the terms are reduced by the open-loop response $Z(s)$. The gain bandwidth independence for CFA is still true when $Z(s)$ approaches infinity and the gain A_v remains small. The denominator term, "R_i" is multiplied by closed-loop gain A_v, and is small with a range of 16Ω to 490Ω for current feedback amplifiers. For a CLC406 R_i is 60Ω. The series output resistance R_o in the denominator is scaled by the ratio of the R_i and gain setting resistor R_g. While the R_o in the numerator is divided by the gain A_v, α_2, and $Z(s)$. Typically, the open-loop R_o will vary from 5Ω to 25Ω.

The closed-loop output resistance approaches zero at dc, and is a function of the open-loop $Z(s)$ frequency response. This is an important point when matching an output impedance by a back matching resistor. Typically back matching consists of placing a resistor that matches the characteristic impedance of a coaxial cable or specific devices input impedance, such as 50Ω.

The denominator term:

$$\frac{\alpha_2 \cdot Z(s)}{R_f + R_i \cdot A_v + R_o \left(1 + \dfrac{R_i}{R_g}\right)} \tag{3}$$

is referred to as the loop gain, and its closed-loop bandwidth is determined by denominator:

$$R_f + R_i \cdot A_v + R_o \left(1 + \dfrac{R_i}{R_g}\right) \tag{4}$$

As you increase gain A_v, you need to decrease R_f to maintain the largest possible −3 dB bandwidth. Manufacturers of CFA amplifiers specify a gain of 1 or 2 at a recommended R_f in the data sheet. For large gain changes the designer can select a value that best fits the desired new closed-loop gain A_v. This maximizes the bandwidth and maintains the same stability based upon maintaining the same ratio used to select the original R_f in the device-specific data sheet. For small changes in gain, using the recommended R_f while changing the gain by R_g is acceptable unless stability becomes an issue.

As R_f decreases, a fundamental limit is reached by the approximate parallel combination of R_{load} and R_f. At this new load, the output voltage limit is set by the output current capability or the maximum output voltage swing into a no load condition. An alternative is to increase R_{load} or increase R_f. A bandwidth reduction in the ratio of the open-loop to closed-loop will result. This ratio decrease results in secondary effects such as a decrease in distortion, noise, gain accuracy, and so forth. Therefore, small changes are acceptable and large ratio changes are not recommended.
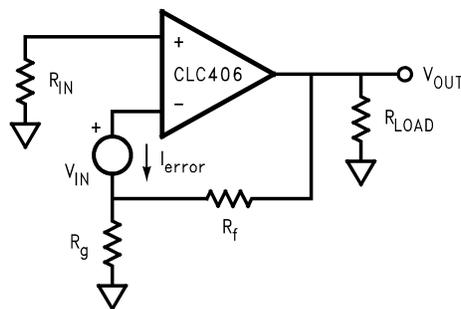

Figure 3. Simulation Method

6   Open Loop Transimpedance Plot

At first it may seem strange to determine $Z(s)$ by placing the voltage source in the inverting node of Figure 3. But this simplifies the simulation steps and has advantages for deriving the stability plot for investigating loads at the output pin.

The circuit in Figure 3 simulates the open-loop transimpedance response Plot 1, while looking at two conditions:

• Infinite load
• 100Ω load

This plot helps explain the accuracy of our spice model and its effects for a practical application. Later this transimpedance gain Z(s) is normalized to an open-loop magnitude function.
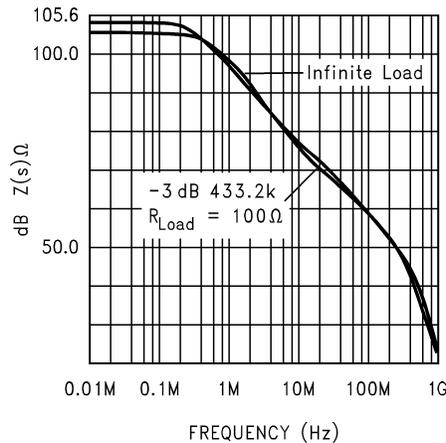

Figure 4. Plot 1: Open Loop Transimpedance

The open loop transimpedance gain Plot 1 has axis in dB ohms versus frequency, and shows an approximate first order roll off function:

$$Z(s) = \frac{R_c}{sR_cC_c + 1}$$

(5)

that includes secondary poles at the higher frequencies. To derive the value of R_c you take the inverse log of the axis:

$$10^{Z(s)/20}$$

(6)

at low frequencies while the 3 dB bandwidth gives C_c by the following:

$$\frac{1}{2\pi R_c f_{-3\,dB}}$$

(7)

Equation 3:

$$T(s) = \frac{Z(s) \cdot A_v}{R_f + R_i \cdot A_v}$$

(8)

where, Z(s) is:

$$\frac{V_{OUT}}{I(V_{IN})}$$

(9)

and, I is the current in V_{IN}.

If you plot this transfer function for a CLC406 at an $A_V = 1$ with an $R_f = 768\Omega$ and $R_g = \infty$, the magnitude and phase information is shown in Plot 2 and 3. The output R_o term is ignored since R_i is low. The gain and phase margin is now available for determining the stability of the *OA-25 Stability Analysis of Current Feedback Amplifiers* (SNOA371).

With Plot 2, you find the unity gain crossover frequency point. This frequency point determines the phase of the amplifier on Plot 3 and it is subtracted from a 180° to derive the Phase Margin. The value at 0 dB is at a frequency of 108 MHz and infers a phase margin of 62°. The gain margin is measured from the −180° phase point and is the difference between the open-loop gain intersection and the 0 dB gain line in Plot 2, which is approximately 12 dB. From control theory, these values are the indicators for optimum amplifier performance, although many designers will set the phase margin to 45° and 9 dB of gain margin. This results in 3 dB of frequency peaking or in the time domain signal preshoot and undershoot. Yet, we will still have a difference in the unity gain −3 dB frequency response of 220 MHz in simulation versus 200 MHz in an actual part. The explanation for the difference will be explained later.
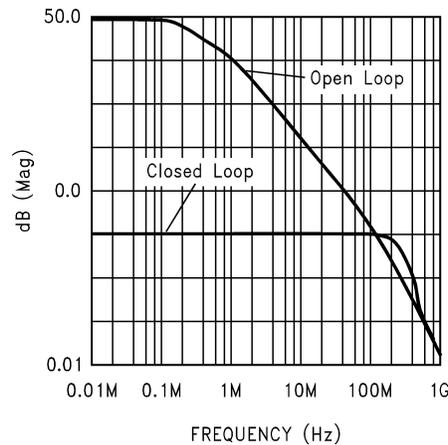
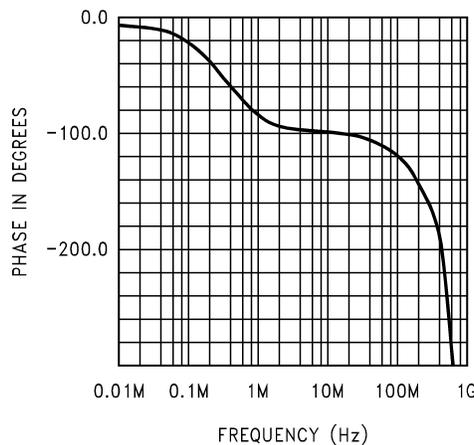**Figure 5. Plot 2: Open and Closed Loop Magnitude**

Figure 6. Plot 3: Open Loop Phase

7   Including Z(s)

The transfer function derived in Equation 2 has little meaning when looking at the poles and zeros for the amplifier without including transimpedance gain Z(s). At first let's substitute the first order pole of Z(s) into Equation 2. After some mathematical manipulation we discover a pole plus a zero as shown in. This is not intuitively obvious until you think about the amplifier's independent and dependent source and the inclusion of R_o to produce this zero.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \cdot A_v \left(1 + \dfrac{R_o}{A_v \cdot R_c} \right)}{1 + \dfrac{R_t}{R_c}} \cdot \frac{1 + s \left(\dfrac{R_o \cdot C_c}{A_v} \right)}{1 + s(R_t \| R_c \cdot C_c)}$$

Equation 3   (10)

Where the term:

$$R_t \cong R_f + A_v \cdot R_i + \left(1 + \frac{R_i}{R_g} \right) \cdot R_o \, ,$$

$$s = j\omega, \text{ and } \omega = 2\pi f.$$

(11)

At s = 0 the open-loop R_c reduces the terms in Equation 3 to the gain A_v times α_1. The zero in the numerator is an order of magnitude higher than the pole in denominator, while the pole has a new value of R_t times C_c where $R_c \gg R_t$. Yet, we have not considered the effects of "Parasites" and their influences upon the stability of the amplifier.

8   External Parasites and Complex Loads

Connecting multiple circuits that have complex values (capacitance or inductance) at the nodes often results in stability issues for all types of amplifiers. Recall the bandwidth of the CLC406 model indicated its −3 dB bandwidth to be higher than the measured unity-gain frequency. This increase bandwidth is largely the result of parasitic components of the package and evaluation board layout [1]. This adds additional zeros and poles to the equation that peaks the frequency response. Adding complex loads to various pins of our model causes stability questions that are probably more easily answered through simulation analysis rather than mathematical analysis.

If a capacitance is in parallel with the load resistance, a decrease in phase margin will result. Capacitance in parallel with R_g decreases the loop gain, while capacitance in parallel with R_f increases the loop gain. All of these effects are seen in simulations for an amplifier.

A common designed circuit is a transimpedance amplifier. The circuit in Figure 7 shows replacing the R_g resistor with the equivalent photo-diode capacitance to simulate closed-loop stability for the CFA. Using the earlier spice simulation method to generate a Bode plot that determines the stability of the design. Adding an independent current source in parallel with the diode capacitance provides a method to simulate the transimpedance gain versus frequency.
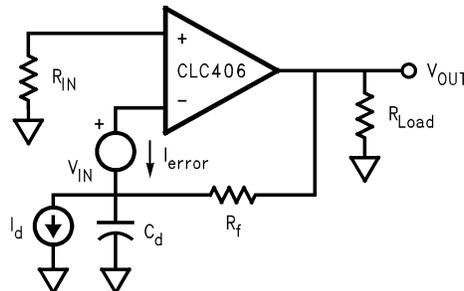
Figure 7. Photo Diode Analysis

9   Summary

Models are available from Comlinear Corporation for modeling many of the important parameters for high speed op amps. *OA-18 Simulation SPICE Models for Comlinear's Op Amps* (SNOA368) details the schematics and parameters that are modeled. Ask for Comlinear's latest spice model diskette.

10   References

1. R. Schmid, "Technique targets board parasites", EDN April 14, 1994 page 147
2. *OA-25 Stability Analysis of Current Feedback Amplifiers* (SNOA371)
3. *OA-18 Simulation SPICE Models for Comlinear's Op Amps* (SNOA368)

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