Integrated Assembly and Strip Test of Chip Scale Packages

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ABSTRACT
The Chip Scale Package (CSP) has been widely used by the Wireless and the Portable industry. With the increase demand in CSP volume ramp and the package variations, a new manufacturing strategy has been implemented.

National Semiconductor Corporation is one of the industry leader in the Wireless products. The Wireless products in general, run from 900MHz to 2.8 GHz. The package used to support the Wireless product has migrated from conventional Thin Quad Flat Pack (TQFP) and Thin Shrink Small Outline Package (TSSOP) to Fine Pitch Ball Grid Array (FBGA) and CSP. The assembly for the TQFP and TSSOP is typically done using a matrix frame. The test for TQFP and TSSOP is typically done in a singulated format. The TQFP and TSSOP can be strip tested by trimming the lead tip from the tie-bar before test. Due to the conventional substrate manufacturing process, the buss line is typically connecting the pads for plating. The FBGA and CSP (Figure 1) are typically sawn in to individual unit for test. A new substrate manufacturing process is needed to isolate pads for strip test.

The major advantages of this integrated assembly and strip test method are as follow:

- Universal platform for assembly and test regardless of package I/O counts
- Enable mapping/sorting for yield tracking during assembly and test
- Higher through-put for assembly and test

This paper will describe the migration of CSP equipment from a conventional method to a fully integration assembly and strip test manufacturing method. This paper will also present the detail program and support with test results to ensure manufacturability and reliability of the manufacturing process.

INTRODUCTION
The CSP in general is a smaller package comparing to the conventional package available in the industry. Although there are many versions of the CSP available such as mBGA (trademark for Tessera), BCC from Fujitsu and other FBGA package from various suppliers. Most of these packages are so small that after assembly and singulation, the package handling becomes extremely difficult. A slight bump or jerking in handling will result in spilling the package all over the floor. Once they are spilled, recovering the package is nearly impossible.

The conventional assembly and test involves the following **(Table 1)** major process steps:

Process Steps	PQFP & TSSOP	FBGA	CSP	Integrated CSP
1	Die Attach	Die Attach	Die Attach	Front-End Auto-Line Assembly from Die Attach to Mold Cure
2	Die Attach Cure	Die Attach Cure	Die Attach Cure	
3	Wire Bond	Plasma Clean	Plasma Clean	

4	Mold	Wire Bond	Wire Bond	
5	Mold Cure	Mold	Mold	
6	Lead Plating	Mold Cure	Mold Cure	
7	Laser Mark	Laser Mark	Laser Mark	Strip Test & Laser Mark Integraton
8	Trim and Form	Ball Attach	Saw Singulation	
9	Singulated Test	Reflow	Singulated Test	Saw Singulation, Dry Visual Inspection & Tape and Reel
10	Visual Inspection	Flux Cleaning	Visual Inspection	
11	Tray or Tape & Reel	Saw Singulation	Tape & Reel	
12		Test		
13		Visual Inspection		
14		Tape & Reel		

Table 1 *Major Process Steps for Assembly and Test*

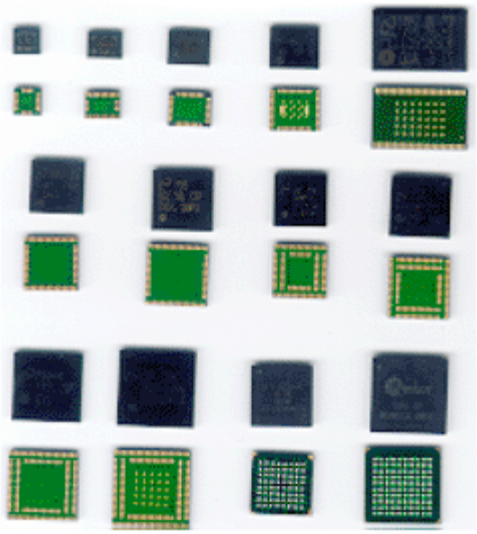

Figure 1 *NSC CSPs and FBGAs*

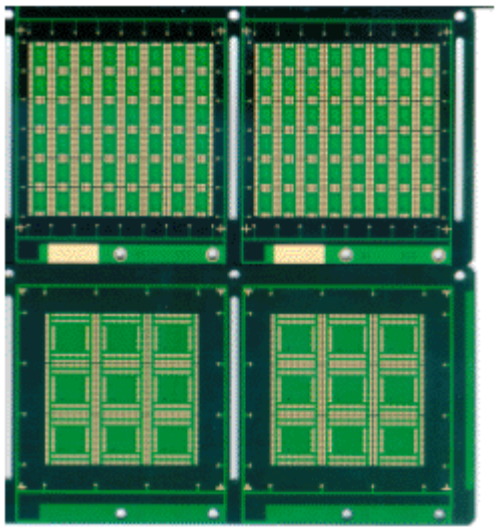

Figure 2 *Chemical Etch Back & Dual Image Substrate*

THE KEY CHALLENGES

- The substrate pad has to be isolated from adjacent pads
- The warpage for the molded panel within the strip has to be controlled to minimum
- The solder pads size and its location have to be accurate for contact consistency
- Strip test handler selection
- Contactor selection
- Concern about EDS damage during saw
- Strip 2D Cell, Sort and Mapping
- Most of all, guarantee 100% no other additional damage induced after test
- Singulated and strip test trade off analysis

The front-end assembly and back-end for test infrastructure had not been changed by much in the past 20 over years. Although the equipment for assembly and test have been improved significantly every year, the assembly and test process has been the same old thing. As Jack Kessler from Concept Unlimited has pointed out in Chip Scale Review in September/October 1999, it is certainly overdue for a change. There are not only the challenges to overcome, but most important of all is the change of our way of doing thing.

SOLUTIONS FOR THE KEY CHALLENGES

1) Substrate Design using Chemical Etched Back Process
Most substrate suppliers can supply the CSP/FBGA substrate using conventional substrate manufacturing process, in which the pads are all connected to the buss-line for Ni and Au plating. The buss-line connecting the pads has to be removed to isolate pads for strip test. Otherwise, yes, all pads will be shorted together and strip test is impossible using the electrolytic plated substrate. Certainly, other substrate manufacturing process such as gold etch or eletroless process could achieve the same isolation for strip test. The only problems are the package reliability and manufacturing consistency being compromised using the gold etch and electroless process. Gold etch substrate is using gold plating as etching resist. The problem associated with gold etch is that the adhesion between solder mask and the gold plating has been proven very poor. Gold plating surface does not adhere well with anything. Most packaging engineers know that the mold gate used for BGA and CSP substrate is gold plated for ease of degating after molding. The plating thickness control and consistency for the electroless process is not as good as electrolytic plating. Hence the problem associated with electroless plating is the poor wire bond yield.

The alternative substrate solution for strip test is achieved by using a de-bussed or chemical etched back (Figure 2, Top) substrate. The de-bussed or chemical etch back substrate is one with the buss-line removed after electrolytic plating. This is a process that has been used by a few substrate manufacturers. This is an additional process for the substrate manufacturing, however, it is one that is much more reliable than the gold etch or electroless process for strip testing of CSP.

For the dual row CSP, the dual image process (Figre 2, Bottom) is used to achieve the same results as chemical etch back process. The dual image process is selected for the dual row CSP because routing the buss line for the second row is not feasible for the fine pitch (0.5 mm) solder pads.

2) Warpage Control:
Other major design consideration is the substrate metal balancing between top and bottom metals for a 2 layers metal substrate design. The balance metal substrate design will minimize the substrate warpage during assembly. The warpage of molded substrate is primarily introduced by the mold compound selection. There are many versions of mold compounds offered by the suppliers to reduce the warpage during mold. The warpage for the molded substrate strip will create problem at strip test as well as at the saw operation. Generally, higher glass transition temperature (Tg) and lower viscosity is desirable for the panel molding of CSP substrate. Certainly, one should evaluate the available mold compounds to select the right mold compound for the CSP. The larger the mold area, will result in larger mold warpage. However, with the proper design of experiment (DOE), one could select a mold compound to achieve the desirable result. Large mold area such as full strip flood molding, approximate 200 mm x 50 mm, or panel molding exceeding 50 mm sq. have been demonstrated by many companies.

The most important thing in design is to consider manufacturing equipment constraints. There are many ways to achieve the manufacturability for strip testing of CSP. Taking too much risk may result in a major failure, but not to take risk (conservative approach) is just as bad or worse.

3) Solder Pad Design:
There are many versions of CSP available in the industry. Some CSPs are with solder balls, other CSP may be designed with land grid array. In general, the larger the solder ball or solder pads, the easier for contactor to make contact during test. Certainly, the larger the solder ball or solder pads, the better it is for the solder joint reliability. The only problem is that in the CSP arena, pad size geometry is very precious. With the continue shrinking of CSP body size and pad pitch, the solder pad size is also being reduced. This has created a major problem for contact continuity during test. The contactor selection is important, but the pad design is more important. National Semiconductor Corporation has introduced many versions of the land grid array CSP for high volume production. Two types of solder pad design are used typically in the BGA and CSP construction. The solder mask defined (SMD) pad is using solder mask opening to define the pad size. The SMD pad has created a problem for the strip test due to the solder mask registration error. Most solder mask shifting for the BGA and CSP substrate can be as much as 50 um. For small pad size, a 50 um shift can be quite significant pad shift resulting in contact problem during testing. The contactor can touch down on the solder mask resulting in continuity failure. Poor solder mask etching or cleaning during manufacturing could also resulting in contact error. The other solder pad design is non-solder mask defined (NSMD) pad (see in Figure 1), in which the pad size is defined by the actual metal size. The solder mask is typically pull back from the solder pads. The NSMD pad is a better pad design for the CSP for strip test.

4) Strip Test Handler Selection
There are several handler manufacturers that are currently working on strip test handling solutions. MCT (Figure 3), and Delta Design are actively working on an integratable handler. MCT seems to be further along the power curve at this point. One key consideration in selecting a handler for strip test is the companies willingness to work with your process considerations. They must be flexible enough to create hardware and software that can integrate smoothly with your factories upstream and downstream processes. Both MCT and Delta seem to be willing to work with their customers in this way as well as sell you a complete integration solution. Tesec is offering a handler that uses a slightly different approach that uses a wafer ring on which the strip will be tested after singulation. Parts would be removed from the wafer ring after test.

Figure 3 *MCT Strip Test Handler with Teradyne A575*

Some of the key challenges for the strip test handler for CSP are as follow:

- Alignment Technologies
- Strip Idendification
- Strip Mapping
- Temperature conditioning
- Retest capabilities
- Debussing of strips
- Index time
- Parallel Test and UPH s

Alignment Technology
Alignment technologies have been used in various parts the Semiconductor industry today ie. Wafer probers . Adapting these technologies to strip test, while being new to the companies attempting the venture, does not mean inventing the wheel.

Strip Identification
Strip Identification can be done with several methods including Bar Codes 3 of 9, 2D Cell codes ECC 200, and several others. The trick will be to find the one that best suits your operation and internal process. It must take up as little valuable space as possible, yet be readable in process plant wide.

Strip Mapping
Strip Mapping and electronic transfer of maps is probably one of the key technologies that make strip testing work. The same or similar process as wafer mapping and electronic transfer of maps to assembly sites can be done with strip map transfers tool to server to tool. Map transfer can be made throughout the assembly, test, mark, saw and TNR process .

Temperature conditioning
Temperature conditioning of strips will require new ideas in temperature control. The old method of creating a temperature chamber will no longer work because of XYZ stage issues. Therefore more localized conditioning methods must be developed. Various heat exchanging methods will work that are used on various semiconductor equipment.

Retest capabilities
Retest capabilities can be accomplished in several methods. This can be accomplished with real time yield monitoring and retest with preprogrammed yield hurdles. After all its just software.

Debussing
Debussing of strips is probably the single most important factor to enable strip testing. This goes without saying to most people in the semiconductor industry but can be overlooked or an afterthought that makes implementation difficult if not impossible. This goes for Laminate CSP, Leadframe CSP, or any type of Matrix leadframe.

Index time
Index time is one of key enhancements to testing in strip / matrix format. Minimizing X, Y, and Z motion during test will reduce index time to bare minimum. Probers have done this for years. Hopefully the strip handler players will learn from the prober manufacturers.

Parallel test
Parallel test methods for analog, mixed signal and digital products will no longer be limited in the handler domain but will only be tester resource limited. With technologies learned from the memory manufacturers and new testers with mega resources. Testing of any number of parts will be possible. UPH s in 5 figures will be possible.

5) Contactor Selection
Contacting at strip test can be one of the more challenging areas for the equipment and test engineers. The handler must be able to use a variety of contactor technologies. Johnstech, Prime Yield, Oztek, and RTI are a few of the contactors companies currently working on solutions for mulit-site contactors for strip testing. Contactor considerations are the same as singulated contacting with the exception of alignment characteristics. Alignment features must be embedded in the design that will allow the handlers vision technology to find the contactor in space. Further considerations for test development must allow for manual verification of singulated parts outside of the handler environment.

Contactor designs must be customized for the strip design. Strip designs must take into account contactability and optimum multisite test performance. Figure 4 shows two contactor designs that take advantage of the strips design for testability. This required a good working relationship between the packaging and test communities.

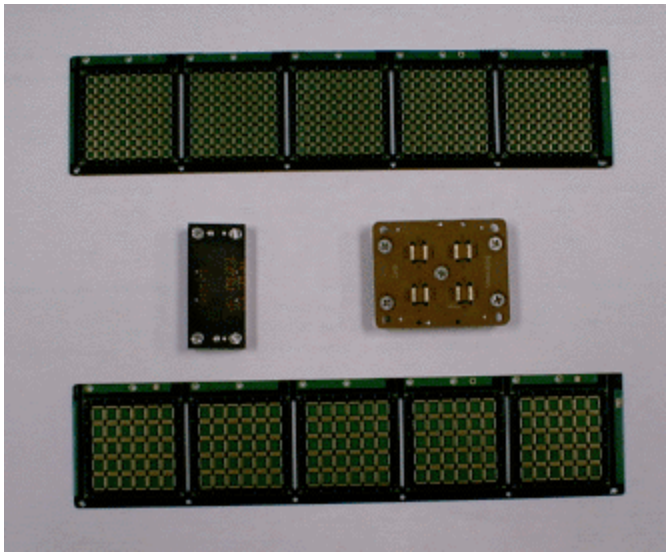

Figure 4 *CSP Strip and Contactors*

6) ESD Elimination
Taping and de-taping laminate CSP on a UV cure tape are the major areas cause ESD damage. Sawing operation and the subsequent handling process have to be controlled carefully to ensure no ESD damage is

done to the strip-tested CSP. Ionizers are installed at various critical points to eliminate ESD charges after test. Some of the new tapeless saw machines have been developed by a few suppliers, naming a few like, ASA, Towa Intercon, Motorola etc.. This is an ideal machine to eliminate ESD changes for the saw operation after strip test. The only concern is that this is a new development in the industry. Once again, we have to take some risk and prove that this equipment can support the CSP infrastructure without causing ESD damage for the tested units.

7) Strip 2D Cell, Sort and Mapping
The laminate substrate can be designed with dedicated area for a 2D cell for strip identification. Currently, we can easily create the 2D cell for strip identification using laser for strip test and mark integration block.

Preferably, we would like to promote the substrate supplier to mark the strip ID and create a inkless mapping for all the reject CSP sites. This feature can be implemented from the front end assembly all the way through tape and reel operation. The equipment infrastructure is there already. The only problem is that most substrate suppliers do not have the laser mark equipment and the read/write capability to implement the 2D cell, sorting and mapping. It is very likely this infrastructure can be developed to automate the CSP assembly and strip test in the near future.

Laser mark after test will help control quality of outgoing product by download of maps created at the strip handler and stored at a local server. The maps would then be uploaded by the laser marker and only the good parts would be marked via the strip map.

8) 100% Damage Free from Saw to Tape and Reel
Yes. This seems like an impossible mission, but once we will let the result speaks for itself. Most of the saw errors can be overcome by substrate design. Sawing through buss-line has been demonstrated for regular FBGA saw process. However, we prefer not to saw through any metal. Furthermore, metal pull back for the pads is an important feature to prevent any mistake in sawing through metal due to saw accuracy. Metal defined target mark or fuducial is another important feature to ensure sawing accuracy with respect to the CSP metal pads location. In a simple term, we should design the substrate to ensure robust design for manufacturing (DFM). Finally, we have to prove with high volume production that our DFM dose ensure damage free saw operation and the subsequent handling through tape and reel.

9) Tradeoff Analysis:

	Strip Test	**Singulated Test**
Index Time (SOT to SOT)	.3 seconds	..5 seconds
Parallel Sites	Unlimited	4 sites max
Jam Rates	1 in 500 strips (125000 units)	1 in 3k units
Sort Time	none	2 seconds / 4 sites
UPH (2.4 sec TT, 4 sites)	4.7k	3.03k
Retest capability	On the fly	Operator intervention required

Temperature	-40 to 130	Ambient to 130
Soak capability	2 strips	500 units
Site Disable	Not Practical	Can turn sites off

Table 2 *Singulated test vs. Strip test Attribute Comparison*

Strip handlers should not limit that number of parallel sites to be tested. The number of sites should only be limited by tester resources. Figure 5 shows UPH curves for a Quad site Singulated PNP handler vs. Strip handling with 4 sites and greater. The chart speaks to the advantages of strip test.

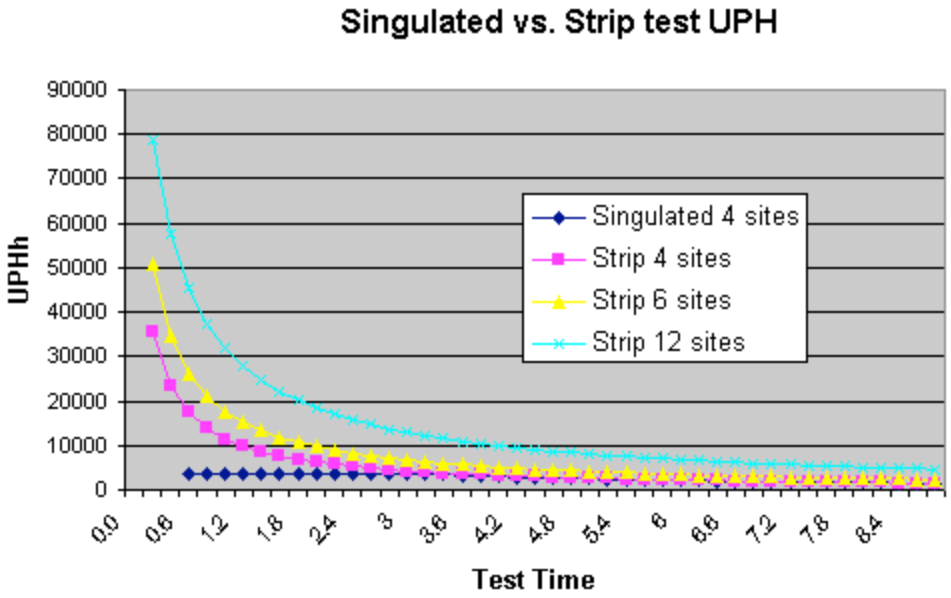

Figure 5 *UPH Comparison Strip to Singulate*

CONCLUSION

The integrated assembly and strip test of CSP have been demonstrated in the CSP development at National Semiconductor Corporation. The advantages described in this paper and the methods to achieve the strip test results have proven that the integrated assembly and strip test are reliable, manufacturable and cost effective for CSP manufacturing.

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