PowerPAD™ - A Method To Create Thermally Enhanced Plastic Package Solutions for Semiconductors

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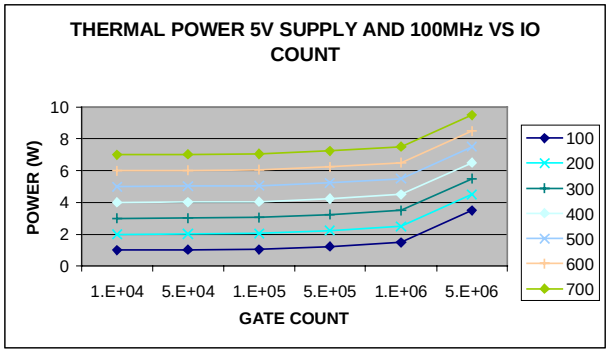
ABSTRACT

A continuing rise in the requirement for thermal power dissipation in semiconductor components due to circuit operation at higher frequencies, higher circuit gate counts per unit area, and the increased emphasis in smaller package sizes for portable and hand-held end equipment has created significant challenges to low cost plastic packages. PowerPAD™ thermally enhanced package solutions patented by Texas Instruments, provide a cost efficient method of improving traditional plastic package heat transfer from the semiconductor device junction to the printed circuit board (PCB) or system level thermal management system when compared to conventional heat spreader, heat slug, or metal package body options. The improvement in thermal efficiency is accomplished with minimal impact on PCB design, construction, or component attachment processes. This paper describes methods used for PowerPAD™ implementation in SSOP, TSSOP, MSOP, LQFP, and TQFP semiconductor package styles as examples of the general application of the technique for thermal removal. Design considerations for the implementation of the PowerPAD™ solution to plastic semiconductor packages, PCB design recommendations, measured and modeled results obtained for the packages, PCB board assembly, and component re-work guidelines are addressed.

INDUSTRY TRENDS – THERMAL POWER

Complementary Metal Oxide Semiconductor (CMOS) components have historically operated at low thermal power – typically less than 1 watt – due to the modest operating voltages, current, gate count, and operating frequency of the part. The thermal power for a component can be approximated by adding the power for the internal gates of the device to that generated in the input/output (IO) structures. Using the power approximation of a switched gate and knowing that only about 15% to 20% of the total gates of a circuit switch in any clock cycle, the internal power generated in the circuit can be easily determined. The IO power uses the same formula, adjusted by the assumption that at least 80% of the IO's will switch on each clock cycle.

Switched Gate Power Approximation = [(CV^2)*f]*N
Where C = capacitance in pF
V = switched voltage (V)
f = switching frequency in Hz
N = number of gates switched/clock cycle



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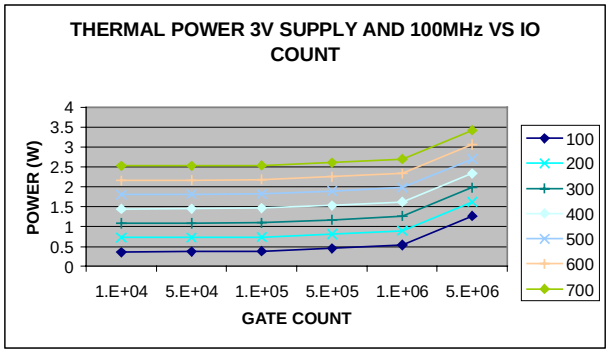

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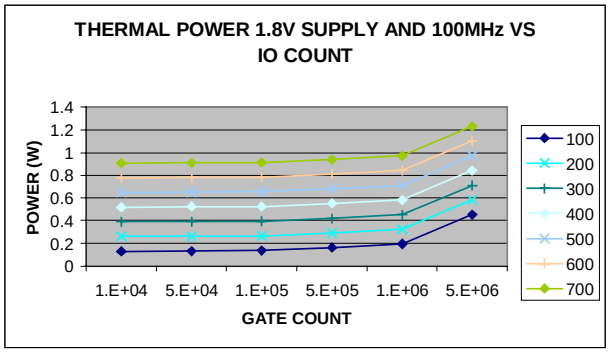
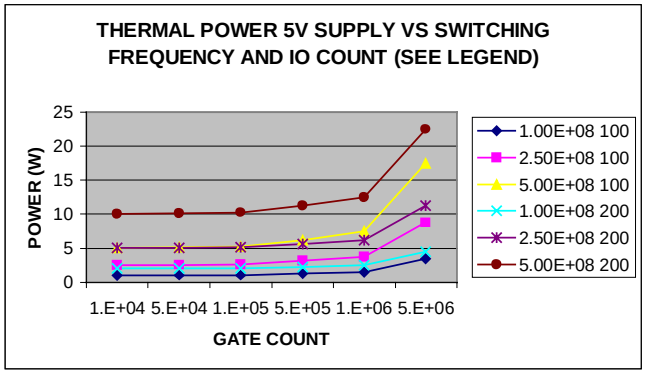


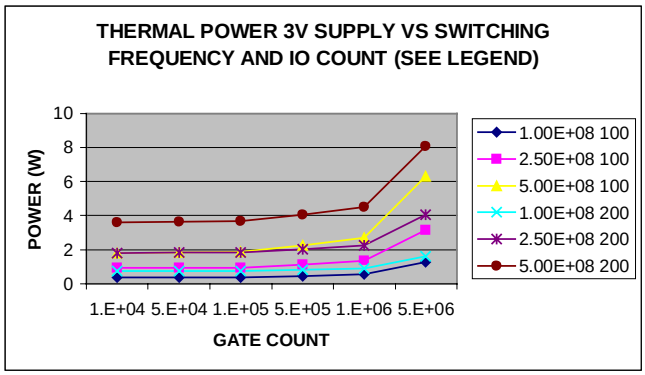
(c)

Figure 1. The impact of the IO count and the gate count of an integrated circuit operating at 100MHz on the thermal power of candidate circuits is shown with (a) being 5.0 volt bias supply, (b) at 3.0 volt bias supply, and (c) at 1.8 volt bias supply.

Results of examples created using 100 to 700 IO, 10000 to 5000000 gates, frequencies from 100MHz to 500MHz, and operating bias supply voltages from 5 volt to 1.8 volt are shown in Figure 1 and Figure 2. The significance of the number of operating IO's on thermal power must be taken into account as the major source of heat generated in an integrated circuit (IC). The switching power of the internal gates of the IC only becomes a dominating factor when a very large number of gates are used with respect to the number of IO's required.



(a)



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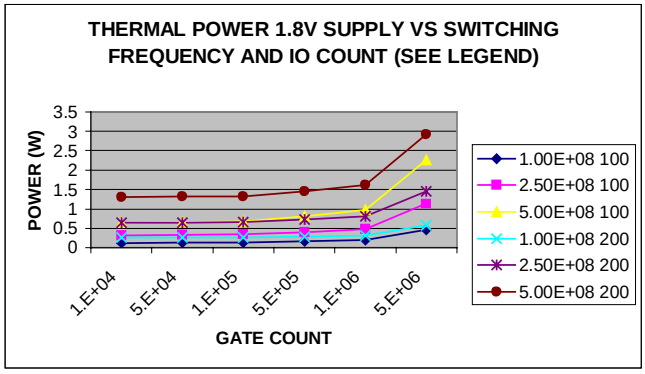


(c)

Figure 2. The reduction in thermal power at a given gate count and number of IO can result in a large reduction in system power handling requirements. (a) demonstrates 5.0 volt bias supply, (b) is 3.0 volts, and (c) is 1.8 volts.

The general trend in the industry is to reduce the operating bias voltage to get the benefit of reduced thermal and electrical power requirements for a given circuit, but in many cases, this potential saving is used to accommodate enhanced features or higher device operating frequencies. Net result of this activity is equal or higher thermal power as implemented in the system.

CONVENTIONAL PACKAGES - CONSTRUCTION

The semiconductor industry has created a number of variations in basic plastic packages to serve the various needs of the components contained within the packages and the connection to the printed circuit board (PCB) utilized in the system application. Relatively simple package cross sections can be used to understand the principles of the construction and the potential for thermal management for each of the options. The following figures represent the principles found in the majority of plastic packages ranging from the standard package with only inherent thermal capability due to the leadframe material, to the case where a copper slug is attached to the lead fingers within the package and exposed to the outside world at the bottom of the package.

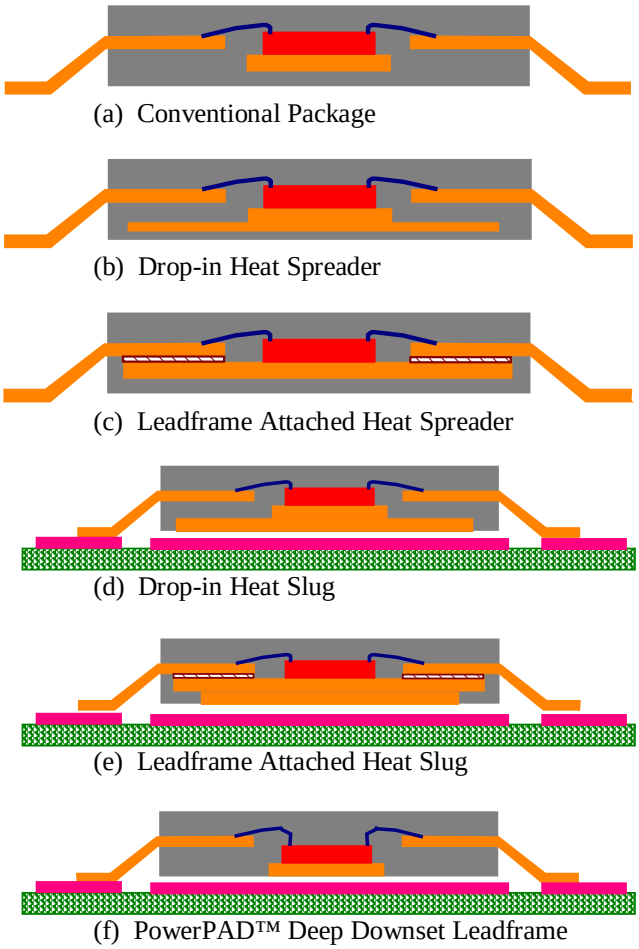


Figure 3. Simplified representations (a) through (f) of plastic semiconductor packaging methods for removal of thermal energy from the silicon chip to the outside world. The TI PowerPAD™ concept is shown for comparison.

Each of the thermally enhanced packages shown in Figure 3 take heat away from the transistor junction of the chip with the efficiency improving as you go from Figure 3(a) the standard package representation to Figure 3(f), the PowerPAD™ representation. The Drop-in Heat Spreader shown in Figure 3(b) provides improvement by adding metal within the package to help carry the heat closer to the lead fingers of the leadframe, with added improvement in Figure 3(c) – Leadframe Attached Heat Spreader – with the metal of the heat spreader replacing the conventional die pad of the leadframe and creating a very short distance between the lead fingers and this metal feature. The Drop-in Heat Slug in Figure 3(d) provides improvement by creating a path from the die pad of the leadframe to the external surface of the package with a metal (typically copper) slug, and the Leadframe Attached Heat Slug of Figure 3(e) creates an additional path for heat to the lead fingers of the leadframe. Each of these versions adds cost and complexity to the package assembly to gain the improvement in thermal removal efficiency.

The PowerPAD™ concept represented in Figure 3(f) solves the problem of heat removal without adding complexity to the package construction (heat spreaders or heat slugs), or adding the cost of the added elements. The thermal path to the outside world is the shortest possible, and results in superior package thermal efficiency with a very simple construction.

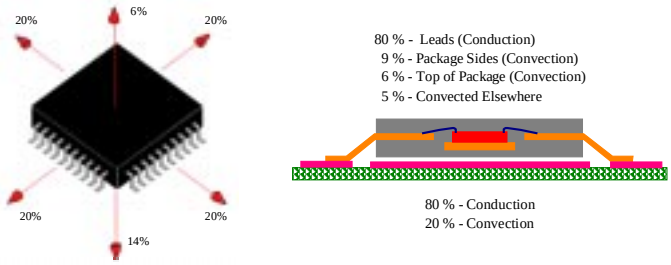


Figure 4. Representation of the path followed in removing heat from a standard package configuration. 80% of the heat is removed by conduction through the leads of the package while only 20% is removed by conduction from the body of the package.

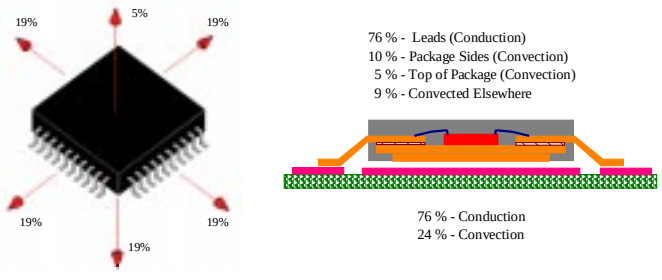


Figure 5. When a Leadframe Attached Heat Slug configuration is employed, 76% of the heat is removed through the package leads by conduction, and the remaining 24% by convection. This would be improved if the package slug can be soldered to the PCB, but most package slugs do not have a solderable surface.

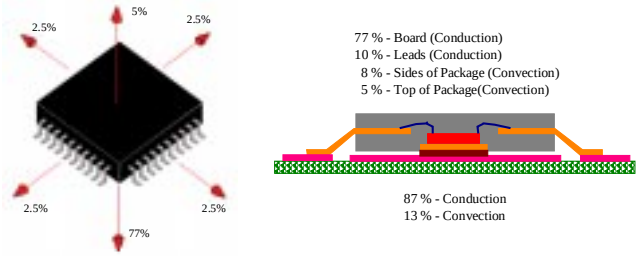


Figure 6. The advantage of the TI PowerPAD™ package is readily shown with 87% of the heat removed from the package by conduction with the remaining 13% dissipated through convection from the external surfaces. The die pad of this package is easily soldered to a thermal land on the surface of the PCB with the heat removal limited only by the efficiency of the PCB and system level thermal management process.

UNDERSTANDING HEAT REMOVAL PROCESS

The heat generated within the semiconductor device results in lower operating performance of the circuit (at higher temperatures, the transistor operation degrades due to increased resistances in material properties), and can result in reduced long term reliability of the package/circuit combination. Thus, it is important to move the heat away from the transistor junctions as efficiently as possible for best operation.

Standard plastic packages use the leads of the package as the primary heat removal mechanism, with the metal of the leadframe carrying the heat away from the internal sites to the outside world by conduction. Figure 4 provides a visual depiction of the heat removal in this style package. The traditional rule that 80% of the heat is removed through the leads with the remaining 20% removed through the package body by convection continues to be valid for this package type. Adding external heat spreaders to the package body will only impact the 20% problem, and is usually applied when only marginal improvement of heat removal is required.

The thermal efficiency of the package can be significantly improved by providing a thermal path directly to the surface of the package. This is shown in Figure 5 by the Leadframe Attached Heat Slug implementation. In this variation, a metal slug is attached to the lead fingers of the leadframe internal to the package body with an adhesive tape material. This replaces the traditional die pad of the leadframe. The chip is mounted to the metal slug with a thermally conductive adhesive material. The resulting construction provides an effective thermal path away from the chip at the cost of added materials within the package, and increased package weight – both of which are undesirable features in a

semiconductor package solution. Another limitation for this solution is the in ability to solder the exposed portion of the metal slug to a PCB thermal land since many of the viable metal slug versions do not have a solderable surface finish available for this connection.

Employment of the PowerPAD™ solution shown in Figure 6 overcomes the deficiencies of the Heat Spreader or Heat Slug packaging methodologies and results in a low cost, thermally efficient package solution. No added components are required for the implementation resulting in assembly operations equivalent to the standard package versions, and the thermal path length is reduced to a minimum. The bottom of the die pad is exposed at the package body surface, and can be easily soldered a thermal land on the PCB. Packages created using this methodology cover the spectrum commonly used for semiconductors, with exactly the same handling characteristics as the standard package versions that the industry commonly uses (size, weight, form factor, reliability, and etc.).

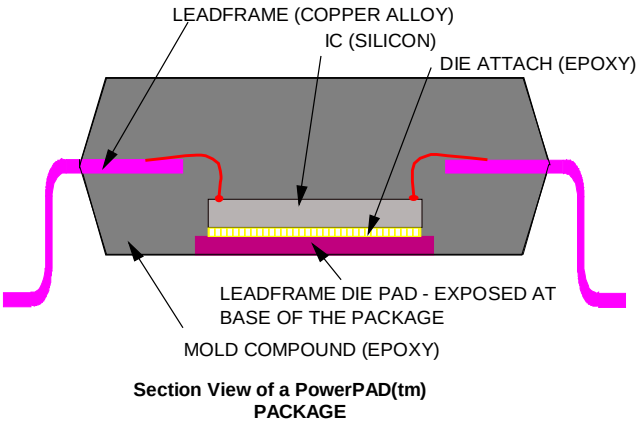


Figure 7. Enlarged pictorial cross-section of a PowerPAD™ package implementation.

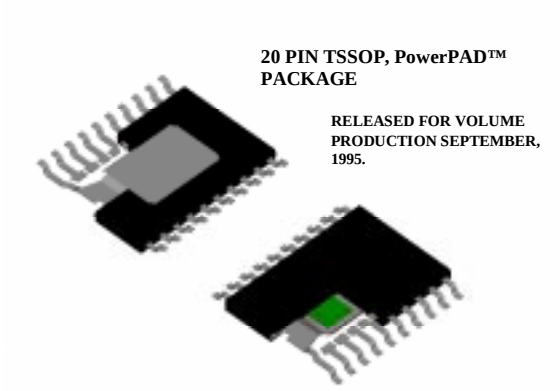


Figure 8. Top and Bottom section view of the 20 pin TSSOP PowerPAD™ package that was first introduced in 1995. This version has the 4 corner package leads tied to the die pad for enhanced thermal efficiency (a standard option in PowerPAD™ packages), in addition to the die pad exposed at the surface of the package body.

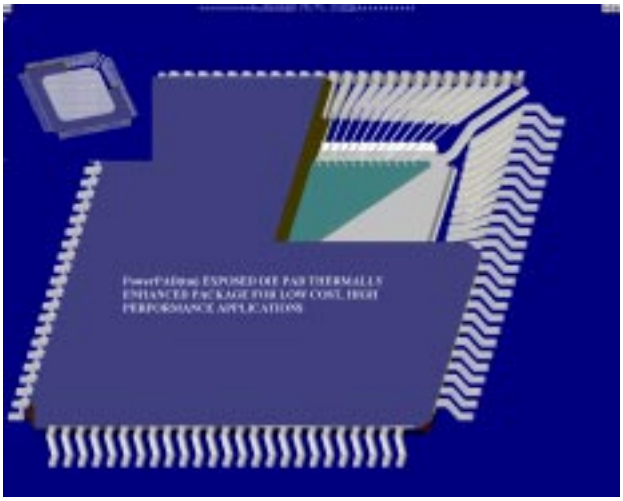


Figure 9. 100 pin TQFP PowerPAD™ implementation showing internal and bottom side features. This package has been in production since 1996.

TABLE 1. Packages available with PowerPAD™

PowerPAD™ DEEP DOWNSET/EXPOSED DIE PAD PACKAGE DESIGNATORS				
		DESIGNATOR	PowerPAD™	PowerPAD™
PACKAGE	BODY	STANDARD	NORMAL FORM	REVERSE FORM
TYPE	DESCRIPTION	PACKAGE	CHIP UP	CHIP DOWN
MSOP8	3 X 3mm 0.65P	DGK008	DGN008	N/A
MSOP10	3 X 3mm 0.50P	DGS010	DGQ010	N/A
TSSOP	225 MIL 0.65P	PW008	N/A	N/A
TSSOP	225 MIL 0.65P	PW014	PWP14	PWD14
TSSOP	225 MIL 0.65P	PW016	PWP16	PWD16
TSSOP	225 MIL 0.65P	PW020	PWP20	PWD20
TSSOP	225 MIL 0.65P	PW024	PWP24	PWD24
TSSOP	225 MIL 0.65P	PW028	PWP28	PWD28
TSSOP	225 MIL 0.50P	DBT28	DCP28	DED28
TSSOP	225 MIL 0.50P	DBT30	DCP30	DED30
TSSOP	225 MIL 0.50P	DBT38	DCP38	DED38
TSSOP	225 MIL 0.50P	DBT44	DCP44	DED44
TSSOP	225 MIL 0.50P	DBT50	DCP50	DED50
TSSOP	300 MIL 0.65P	DA030	DAP30	DAD30
TSSOP	300 MIL 0.65P	DA032	DAP32	DAD32
TSSOP	300 MIL 0.65P	DA038	DAP38	DAD38
TSSOP	300 MIL 0.50P	DGG48	DCA48	DFD48
TSSOP	300 MIL 0.50P	DGG56	DCA56	DFD56
TSSOP	300 MIL 0.50P	DGG64	DCA64	DFD64
TVSOP	225 MIL 0.40P	DGV14	N/A	N/A
TVSOP	225 MIL 0.40P	DGV16	N/A	N/A
TVSOP	225 MIL 0.40P	DGV20	DGP20	DHD20
TVSOP	225 MIL 0.40P	DGV24	DGP24	DHD24
TVSOP	225 MIL 0.40P	DGV48	DGP48	DHD48
TVSOP	225 MIL 0.40P	DGV56	DGP56	DHD56
TVSOP	300 MIL 0.40P	DBB80	DDP80	DJD80
TVSOP	300 MIL 0.40P	DBB100	DDP100	DJD100
SOP	375 MIL, 127P	DW16	DWP16	DWD16
SOP	375 MIL 1.27P	DW20	DWP20	DWD20
SOP	375 MIL 1.27P	DW24	DWP24	DWD24
SOP	375 MIL 1.27P	DW28	DWP28	DWD28
TQFP	10 X 10mm 0.8P	PGT44	PGM44	PGS44
TQFP	7 X 7mm 0.5P	PFB48	PHP48	PKD48
TQFP	10 X 10mm 0.65P	PAH52	PGP52	PLD52
TQFP	7 X 7mm 0.4P	PEG64	PVP64	PVD64
TQFP	14 X 14mm 0.8P	PBR64	PBP64	PHD64
TQFP	10 X 10mm 0.5P	PAG64	PAP64	PJD64
TQFP	12 X 12mm 0.5P	PFC80	PFP80	PMD80
TQFP	14 X 14mm 0.5P	PZT100	PZP100	PFD100
TQFP	14 X 14mm 0.4P	PDS120	PQP120	PQD120
TQFP	14 X 14mm 0.4P	PDT128	PNP128	PND128
LQFP	20 X 20mm 0.5P	PGE144	PRP144	PRD144
LQFP	24 X 24mm 0.5P	PGF176	PTP176	PTD176
LQFP	28 X 28mm 0.65P	PSF160	PSP160	PSD160
LQFP	28 X 28mm 0.5P	PDV208	PYP208	PYD208
LQFP	28 X 28mm 0.4P	PEF256	PFK256	PFL256

Package styles and lead counts available for use with PowerPAD™ features include virtually all standard leaded surface mount package types used in the semiconductor industry (see Table 1). The newer thin package versions (<2.0mm body thickness) such as MSOP (8 and 10 pins), TSSOP (8 through 100 pins), LQFP (32 through 256 pins), and TQFP (32 through 256 pins), are readily suited for use of this technology. Thinner packages in the future – VSSOP, VQFP (0.8mm body thickness), and USSOP, UQFP (<0.8mm body thickness) will easily employ the PowerPAD™ solution. Both chip-up and chip-down versions are easily implemented to support the thermal removal requirements of the component, board, and system solutions. New package versions are added as required.

CREATING A PowerPAD™ PACKAGE

Most semiconductor packages in the industry today for through hole or surface mount applications start construction with a metal (typically copper) leadframe consisting of a number of lead fingers continuing from the package external leads to the interior of the package, and a die pad that the chip attaches to. The die pad is downset to a position within the package to allow for equal mold compound flow above and below the chip/die pad combination.

The PowerPAD™ package utilizes a downset of the die pad to the point that the bottom surface of the die pad is exposed at the bottom surface of the package to create an optimum thermal path from the chip to the outside of the package body. Key attention must be paid to the leadframe material properties to allow this level of downset without cracking or breaking the tie strap that holds the die pad in position prior to the molding process. However, this simple extension of the die pad to the package surface will generally result in an unreliable package implementation.

Features must be incorporated in the die pad design to provide a highly reliable package solution. The major features include a method to prevent molding material flash or bleed from covering the exposed die pad during the molding operation (otherwise, the thermal benefits of this structure will be lost), a method to lock the die pad into the package (to prevent the chip/die pad from being pushed out of the package during temperature or power cycling), and a method to assure moisture performance of the molded plastic package (prevent popcorn effects and bond pad corrosion within the package). All of these have been included in the PowerPAD™ design to the effect that reliability and performance levels continue to meet those achieved by the low power standard configurations of the same package types.

An example of the reliability testing performed during package/production qualification is shown in Table 2 for the 80PFP (12.0 x 12.0 x 1.0mm body, 0.5mm lead pitch) TQFP package. This particular product required a moisture sensitivity level 3 for the package qualification with both conventional and flux based preconditioning. There were no failures for any test conducted during the qualification cycle.

Table 2. Qualification Results for 80PFP PowerPAD™

Test/Requirement	Conditions	Readpoints	SS/F Lot#1	SS/F Lot#2	SS/F Lot#3
*1. Steady-State Life	155C	240 Hrs	116/0	116/0	116/0
*2. Biased HAST	130C,85%RH	96 Hrs	116/0	116/0	116/0
*3. Autoclave	121C,15 PSIG	240 Hrs	76/0	76/0	76/0
*4A.Thermal Shock	-65/+150C	1000 Cyc	116/0	116/0	116/0
5. ESD:	100pF,1500 Ohms	2000 V	3/0	---	---
	200pF,0 Ohms	200 V	3/0	---	---
	CDM	1000 V	3/0	---	---
6. Solder Heat	260C,10 Sec		22/0	22/0	22/0
7. Solvent Resistance			12/0	12/0	12/0
8. Solderability	8 Hr Steam Age		22/0	22/0	22/0
9. Lead Fatigue			22/0	22/0	22/0
10. Lead Pull			22/0	22/0	22/0
11. Lead Finish Adhesion			15/0	15/0	15/0
12. Physical Dimensions			5/0	5/0	5/0
13. Flammability	Method A		5/0	5/0	5/0
	Method B		5/0	5/0	5/0
14. Thermal Impedance			Ver: WRWU 5/98		
15. Electromigration			Ver: WRWU 5/98		
16. Electrical Characterization			50	50	50
17. Bond Strength			76/0	76/0	76/0
18. Die Shear			5/0	5/0	5/0
19. Latch-Up			5/0	5/0	5/0
20. Manufacturability	(Wafer Fab)		Ver: D4NN 5/98		
	(Assembly Site)		Ver: NHUA 1/98		
25. Salt Atmosphere		24 Hrs	22/0	22/0	22/0
28. X-Ray	Top View Only		5/0	5/0	5/0
30. Visual/Mechanical			328/0	328/0	328/0
*31.Storage Life	170C	420 Hrs	45/0	45/0	45/0

* Samples used for these stresses were preconditioned with 192 hours of 30C/60%RH soak followed by three passes of VPR soldering per JEDEC A113.
* Samples used for these stresses were preconditioned with 3 cycles of flux + solder heat per QSS 009-501.

PCB ASSEMBLY CONSIDERATIONS

Assembly of PowerPAD™ components to a PCB was a priority during the development of the package concept. The goal was to utilize industry standard practices for the board design, construction, and assembly processes, and requiring changes only to incorporate thermal management features. Examples of the PCB layout are shown in Figure 10 for a single layer TSSOP style board and Figure 11 for a multi-layer LQFP/TQFP style board. The single layer PCB board case provides an illustration of the extension of the thermal land on the surface of the PCB beyond the body dimension of the semiconductor. This provides additional area for the removal of heat from the PCB by convection without having to add thermal vias within the board, or implementing features on the backside of the board.

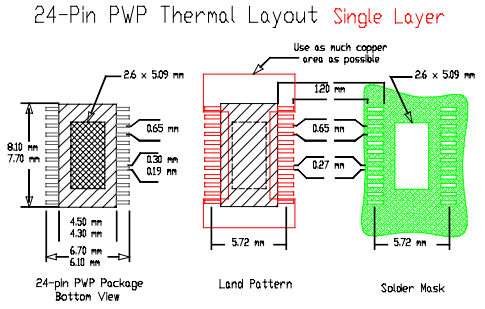


Figure 10. Example of PCB features for use of thermally enhanced packages such as the TI PowerPAD™ 24 pin TSSOP package.

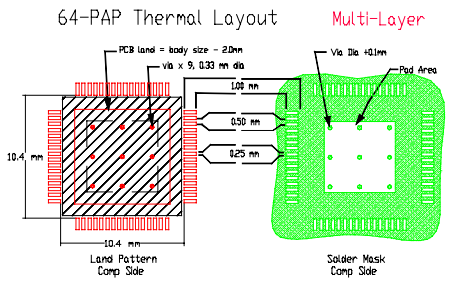


Figure 11. The PCB layout for a 64 pin PowerPAD™ TQFP package is shown indicating the thermal vias required in the board construction, and the approximate thermal land size with respect to the package body size.

A package such as the 64PAP PowerPAD™ package shown in Figure 11 normally requires a multi-layer PCB for thermal removal since device leads exist on all 4 sides of the package. The vias connect the surface thermal land to the ground plane within the PCB which will act as the thermal spreader for head removal, or may continue to features on the back side of the PCB for more efficient heat removal to other system components. Example PCB thermal lands for use with PowerPAD™ or other thermally enhanced package types are shown in Figure 12 below.

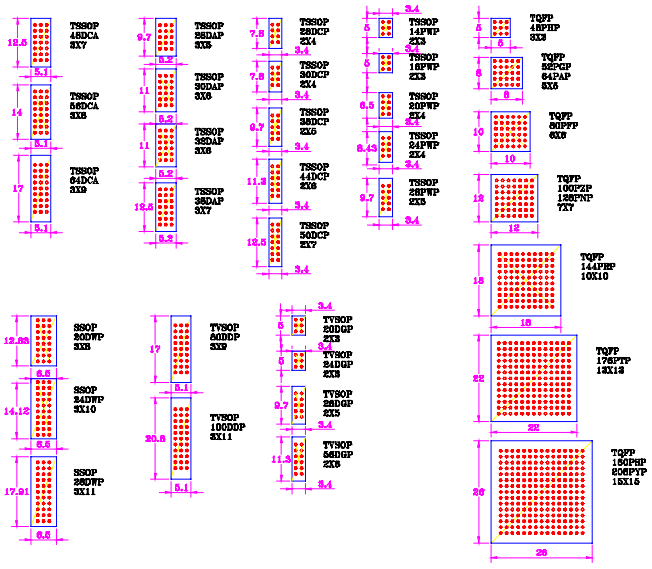


Figure 12. Typical PCB thermal land and via patterns for use with thermally enhanced packages. The number of thermal vias shown is the theoretical maximum for each land pattern based on 1.5mm via pitch. These vias connect either to an internal ground plane, or to a plane on the backside of the PCB for thermal removal.

Component assembly of PowerPAD™ packages to the PCB follows normal industry practice with no special considerations for solder paste thickness or reflow profiles required to achieve high quality attachment. Also, rework can be performed when needed after assembly using conventional component removal and replacement techniques. It should be noted that the thermally enhanced PCB normally used with thermally enhanced packages can sometimes make it difficult to re-solder a component to the board unless the whole board is reprocessed through the normal reflow. An alternative to solder attachment in this rework case is the use of thermally conductive epoxy materials (such as used with externally applied heat sinks) for the attachment of the package thermal pad to the thermal land on the PCB.

The results obtained using the recommended PCB thermal land pattern on the PCB, and with the part soldered to the PCB are shown in Attachment A. Comparison to a part mounted to the same thermally enhanced PCB without attaching the exposed die pad to the thermal land on the board is also shown, along with the thermal capability of a standard family of packages on a conventional PCB. This clearly demonstrates the advantages of the PowerPAD™ package solution.

CONCLUSION

The PowerPAD™ packages developed at Texas Instruments are low cost, high thermal performance solutions with all of the advantages of conventional plastic surface mount packages. They demonstrate applicability to most conventional surface mount types and continue to meet the handling and surface mount assembly advantages of their conventional counterparts:

- same size, weight, and form factor
- same lead configuration
- same PCB assembly processes
- superior thermal performance

REFERENCE

Additional information about the Texas Instruments PowerPAD™ package solution can be found on the TI internet web page as follows:

http://www.ti.com/sc/docs/psheets/app_msp.htm

Page down to

Audio Power Amplifiers

1. PowerPAD™ Thermally Enhanced Package slma002.pdf

Double click on slma002.pdf to view the application note.

ATTACHMENT A

Table 3. Thermal data for various PowerPAD™ packages with the TI recommended PCB having the properties of the JEDEC high thermal conductivity PCB with a) the die pad soldered to the thermal land on the board (columns 4-6), and b) the part is attached to the PCB through the leads only (columns 7-9). A standard package attached to a JEDEC low thermal conductivity board is shown for comparison to the thermally enhanced packages (data columns 10-12).

PowerPAD™ Thermal Modeling Data

Package Description			PowerPAD soldered to TI Recommended Board			PowerPAD not soldered to TI Recommended Board			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964
	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235
1	2	3	4	5	6	7	8	9	10	11	12

COLUMN NUMBERS

PowerPAD™ —A Method to Create Thermally Enhanced Plastic Package Solutions for Semiconductors

Milton L. Buschbom, Mark Peterson, Shih-Fang Chuang, David Kee, and Buford Carter

Texas Instruments
Dallas, Texas

SMI CONFERENCE
25 August 1998
San Jose, California

PRESENTATION AGENDA

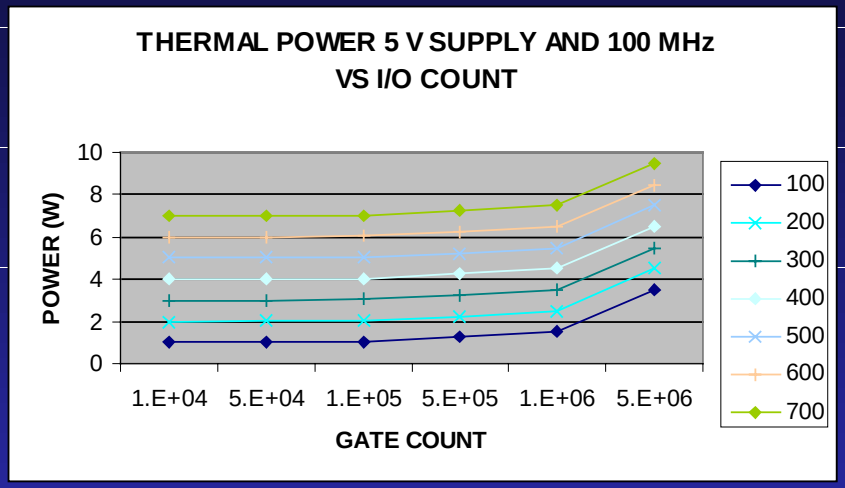
- Introduction
- Heat Generation in Semiconductor Devices
- Thermally Enhanced Plastic Package Construction
- Heat Removal in Plastic Packages
- Texas Instruments PowerPAD™ Package Implementation
- Qualification and Reliability Testing Results
- PCB Design Considerations for Thermally Enhanced Packages
- Thermal Modeling Results for PowerPAD™ Packages
- Conclusion

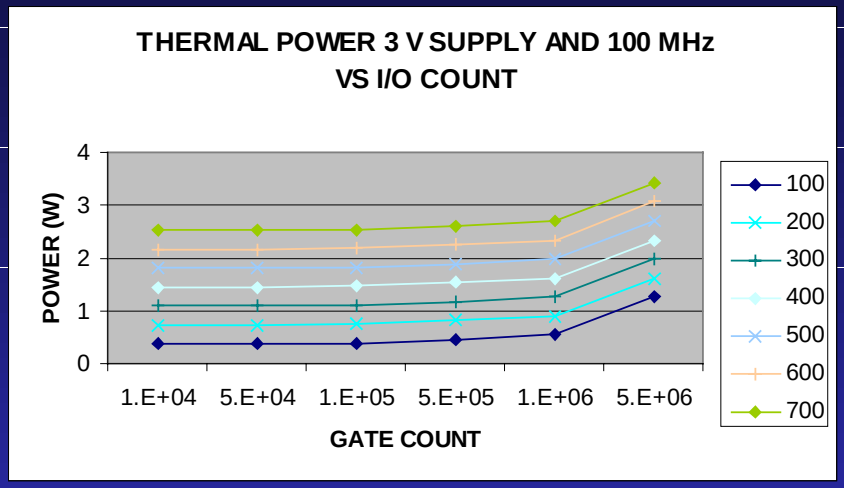
INTRODUCTION

The issue of heat generation in semiconductor components and the methods available for heat removal are increasingly important to the performance of the final product. Advances in semiconductor technology have allowed for reduced operating voltages for the circuits, but at the same time, operating frequencies and gate counts have increased dramatically. Meanwhile, the demands for smaller, thinner, and lighter weight packaged solutions are on the rise to satisfy the needs of hand-held or portable end equipment.

Package solutions available from the semiconductor industry today to satisfy the need for efficient thermal removal from the component generally fail one or more of the end user concerns. The PowerPAD™ plastic package solution from Texas Instruments addresses all of the critical issues and provides opportunity for continued application to future product generations.

THERMAL IMPACT OF SEMICONDUCTOR TECHNOLOGY

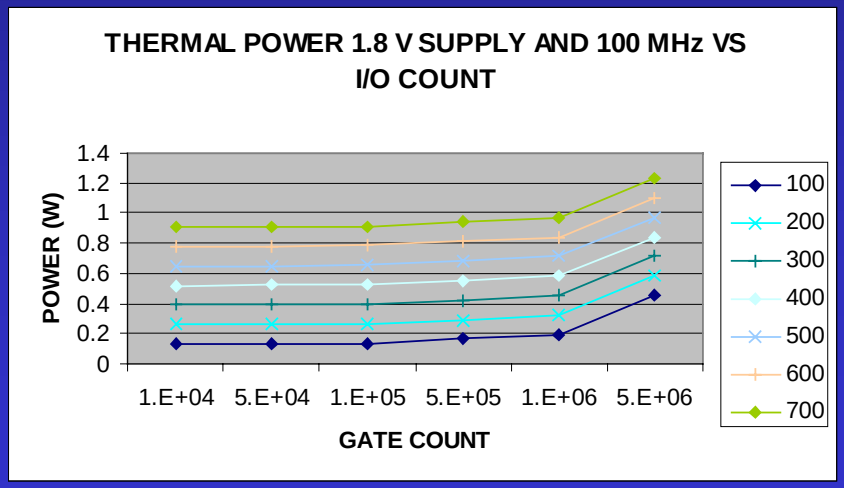




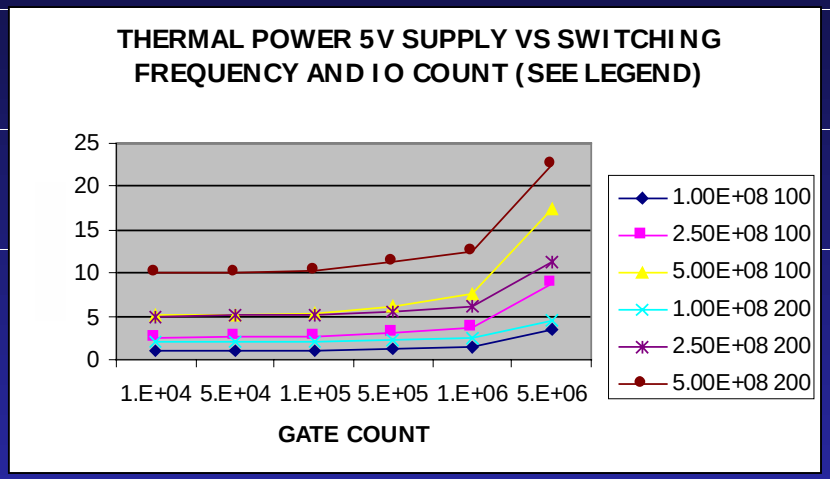
Switched Gate Power Approximation

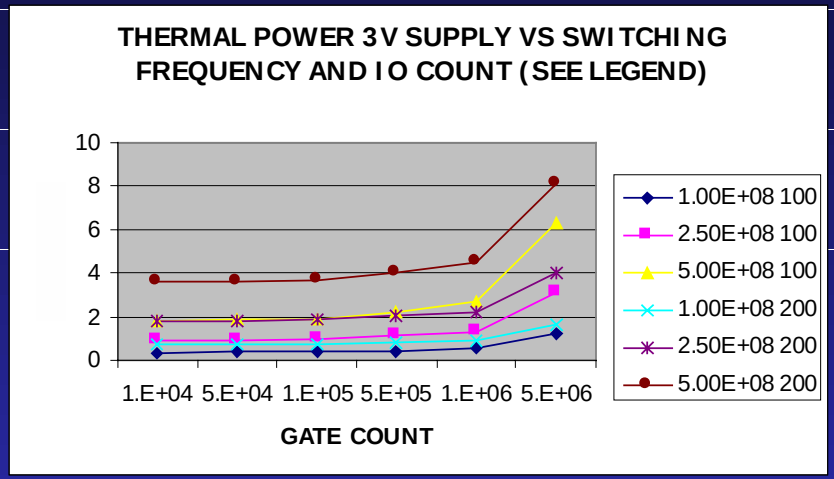
$$P = [(CV^2) \times f] \times N$$

P = Power in watts
C = Capacitance in picofarads
V = Supply voltage in volts
f = Clock frequency in hertz
N = Number of gates switched per clock



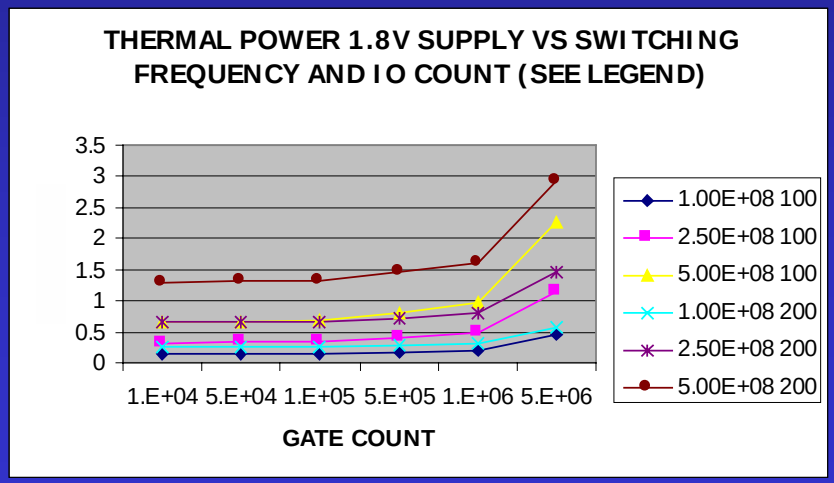
THERMAL IMPACT OF SEMICONDUCTOR TECHNOLOGY





Impact of Clock Frequency on Thermal Power of a Circuit

- Scales directly with the clock frequency
- I/O power dominates at low gate count
- Supply voltage reduction is critical
- Low gate count with high I/O can be a high thermal power option
- Dual power supply options help reduce the total power of the circuit



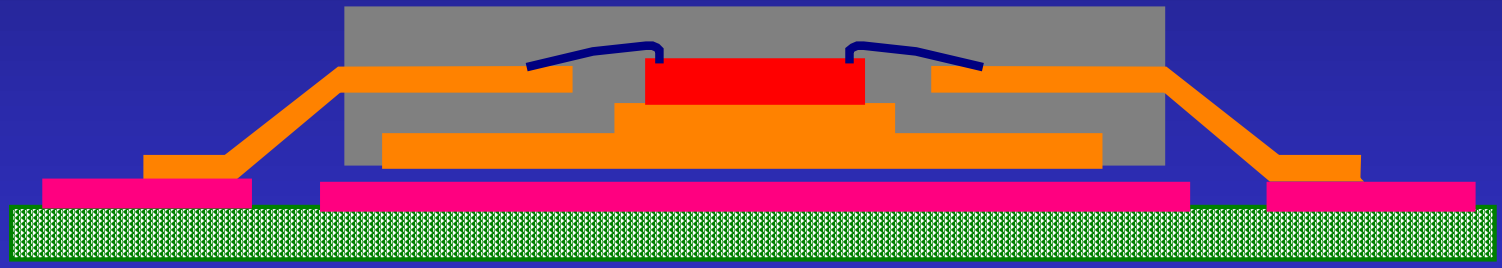
PACKAGE CONSTRUCTION VARIATIONS—PICTORIAL VIEW

Conventional Plastic Package Construction—Leadframe die pad and chip are completely surrounded by mold compound

Drop-in Heat Spreader Package—Spreader makes contact with the bottom side of the die pad and extends toward the edges of the package. All elements are surrounded by the plastic mold compound

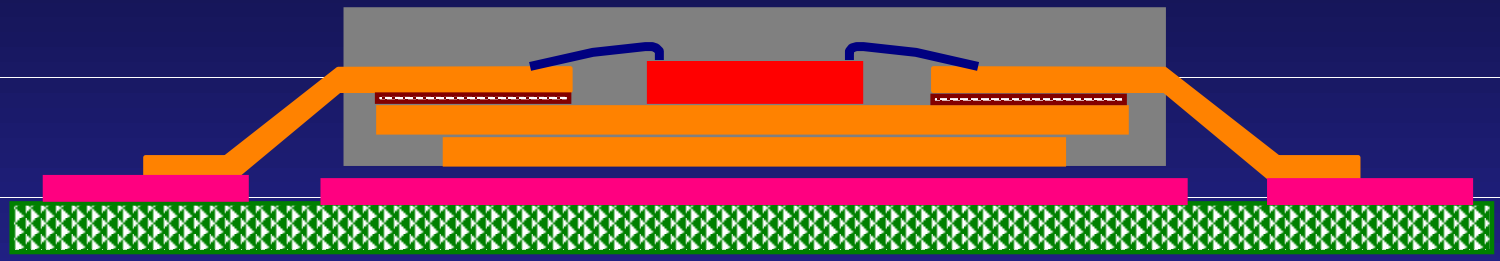
PACKAGE CONSTRUCTION VARIATIONS—PICTORIAL VIEW (Continued)

Leadframe-Attached Heat Spreader—The heat spreader becomes the die pad and is attached to the fingers of the leadframe with insulating tape

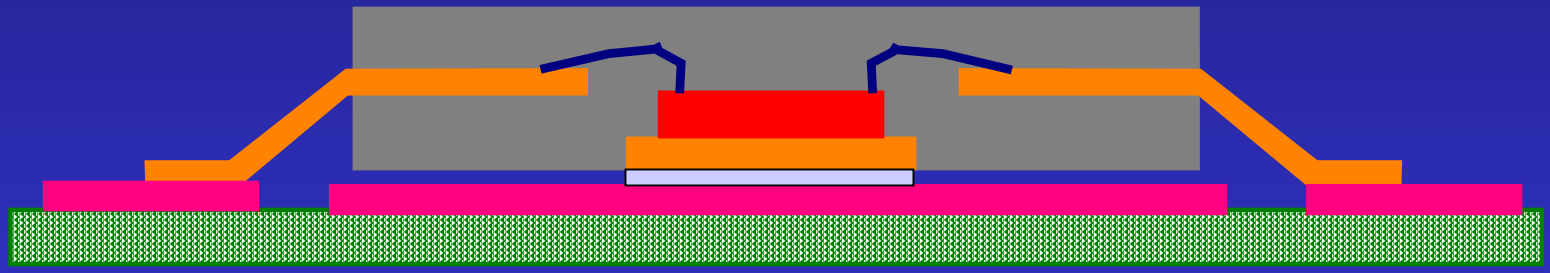


Drop-in Heat Slug Package—Heat slug makes contact with the bottom side of the die pad and extends toward the edges and is exposed at the bottom surface of the package body. Typically ≥10 mil thick

PACKAGE CONSTRUCTION VARIATIONS—PICTORIAL VIEW (Continued)

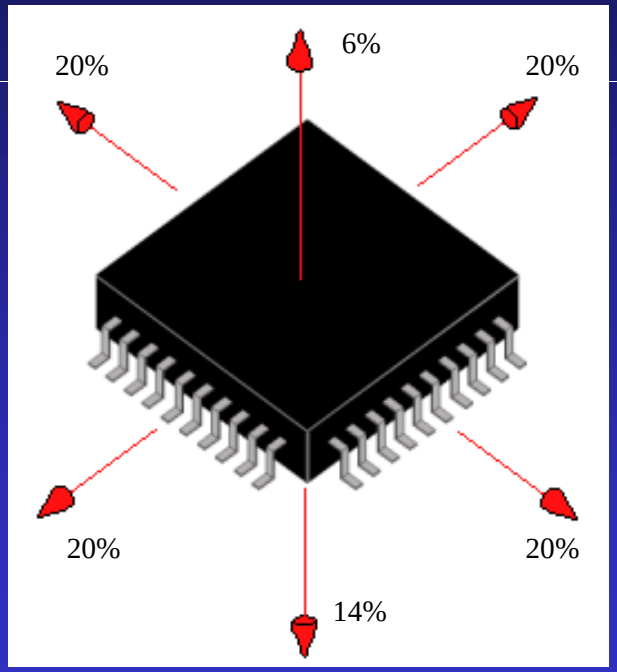


Leadframe-Attached Heat Slug—The heat slug becomes the die pad and is attached to the leadframe fingers with insulating tape. Slug is exposed.

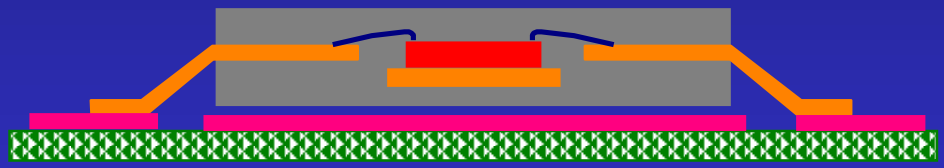


PowerPAD™ Package Configuration—The leadframe die pad is processed with a deep down-set to the point at which the bottom of the leadframe can be exposed at the surface of the package body. Thickness is same as leadframe.

HEAT FLOW IN A STANDARD CONFIGURATION
PLASTIC QUAD FLATPACK



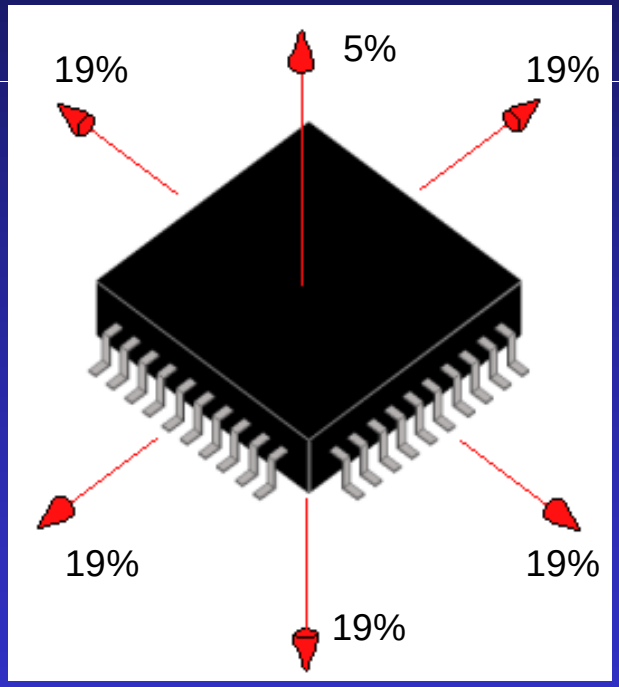
80 %	Leads (Conduction)
9 %	Package Sides (Convection)
6 %	Top of Package (Convection)
5 %	Convected Elsewhere



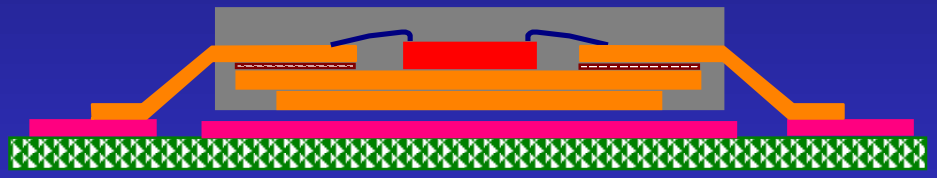
80 %	Conduction
20 %	Convection

Standard Package Configuration

HEAT FLOW IN AN ATTACHED HEAT SLUG CONFIGURATION PLASTIC QUAD FLATPACK



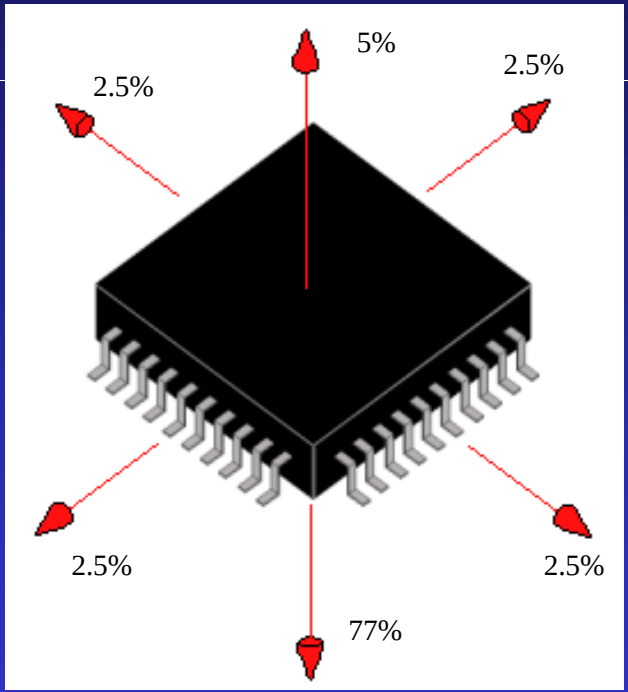
76 %	Leads (Conduction)
10 %	Package Sides (Convection)
5 %	Top of Package (Convection)
9 %	Convected Elsewhere



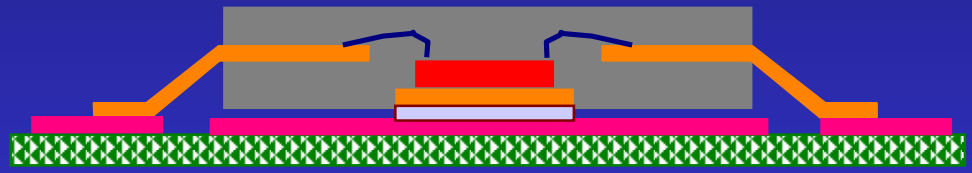
76 %	Conduction
24 %	Convection

Leadframe-Attached Heat Slug Package Configuration

HEAT FLOW IN A PowerPAD™ CONFIGURATION PLASTIC QUAD FLATPACK



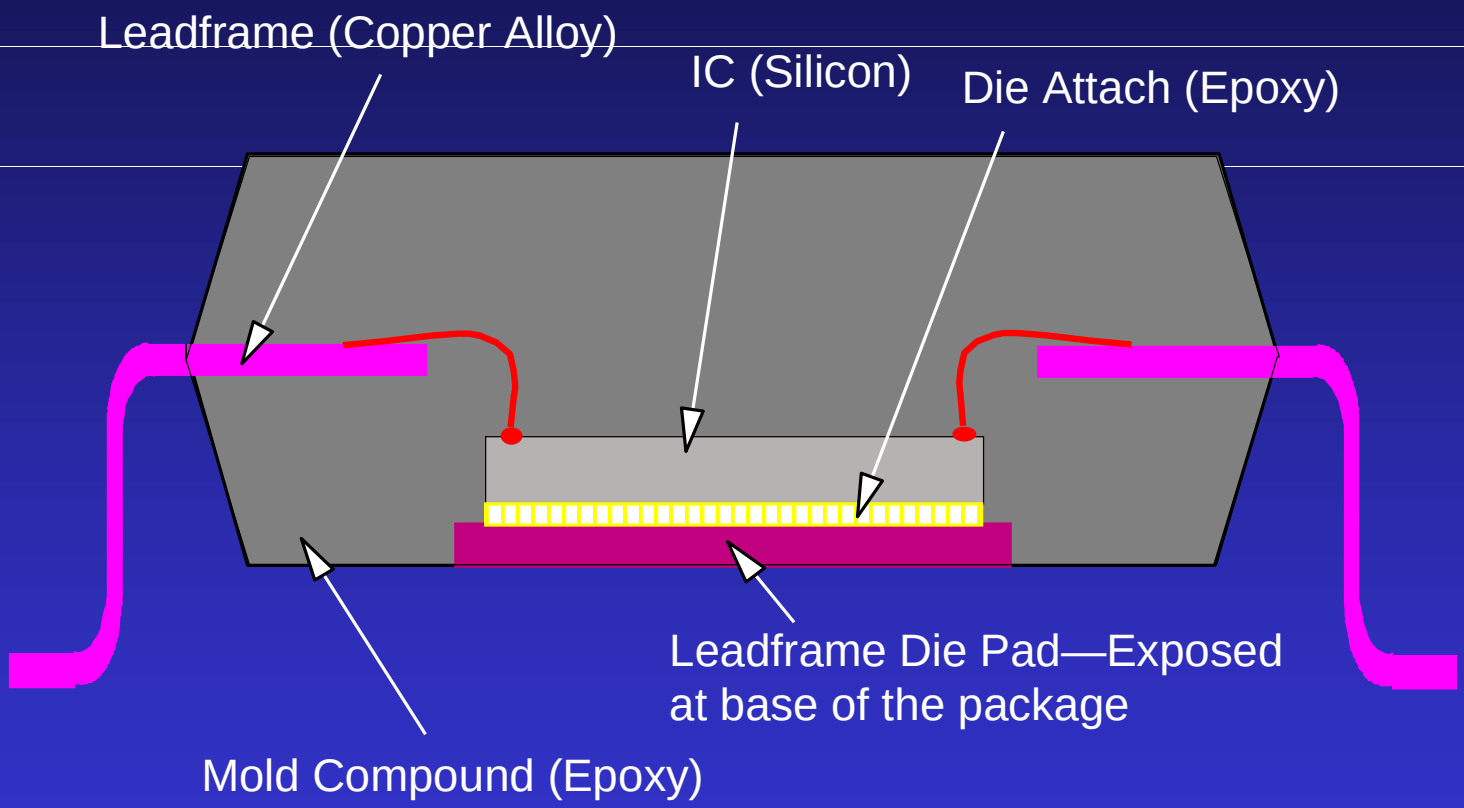
77 %	Board (Conduction)
10 %	Leads (Conduction)
8 %	Sides of Package (Convection)
5 %	Top of Package(Convection)



87 %	Conduction
13 %	Convection

PowerPAD™ Package Configuration

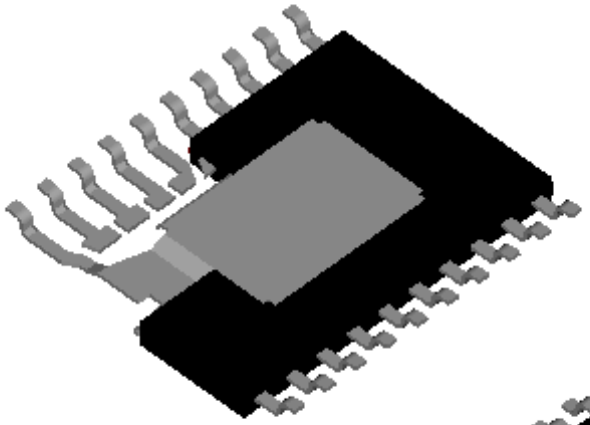
SCHEMATIC CROSS SECTION OF A PowerPAD™ CONFIGURATION PLASTIC QUAD FLATPACK



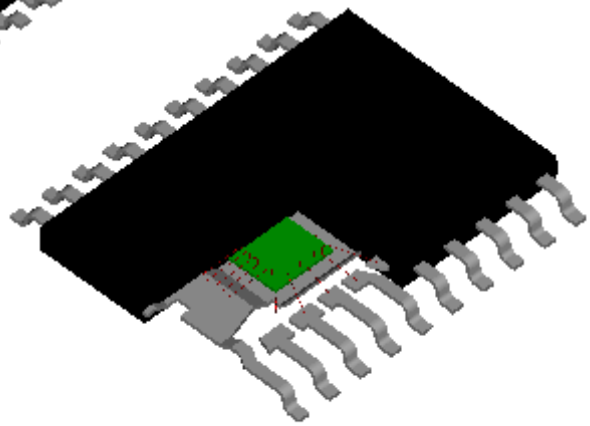
Section View of a PowerPAD™ Package

TOP AND BOTTOM VIEW OF A PowerPAD™ CONFIGURATION PLASTIC TSSOP

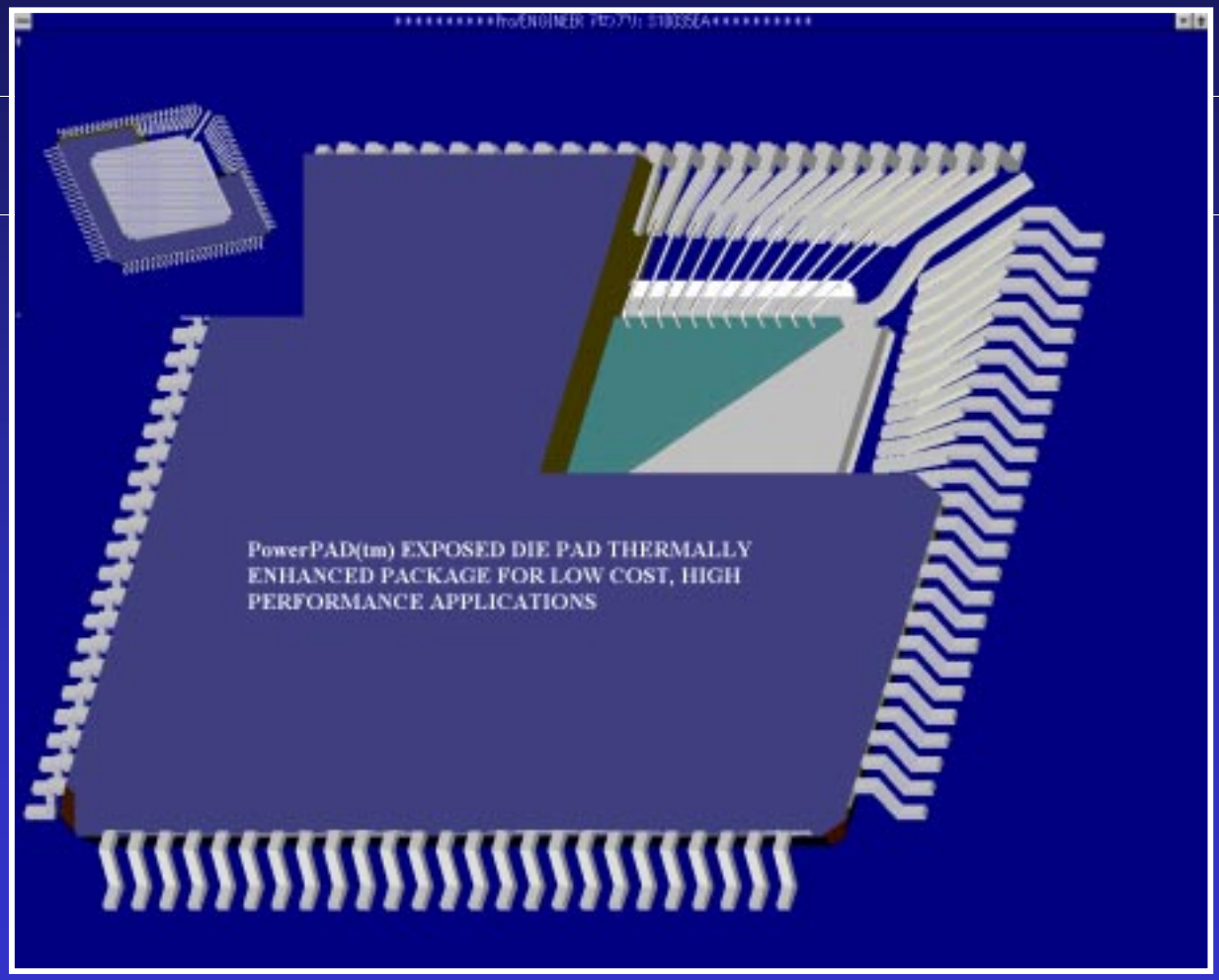
20 PIN TSSOP
PowerPAD™ PACKAGE



Released for Volume Production
September 1995



TOP AND BOTTOM VIEW OF A PowerPAD™ CONFIGURATION 100 PIN PLASTIC TQFP



TEXAS INSTRUMENTS

PowerPAD™ DEEP DOWNSET/EXPOSED DIE PAD PACKAGE DESIGNATORS

PACKAGE	BODY	BODY X	BODY Y	BODY Z	LEAD PITCH	DESIGNATOR STANDARD	PowerPAD™ NORMAL FORM	PowerPAD™ REVERSE FORM
TYPE	DESCRIPTION	mm	mm	mm	mm	PACKAGE	CHIP UP	CHIP DOWN
MSOP8	3 X 3mm 0.65P	3	3	1	0.65	DGK008	DGN008	N/A
MSOP10	3 X 3mm 0.50P	3	3	1	0.5	DGS010	DGQ010	N/A
TSSOP	225 MIL 0.65P	3	4.4	1	0.65	PW008	N/A	N/A
TSSOP	225 MIL 0.65P	5	4.4	1	0.65	PW014	PWP14	PWD14
TSSOP	225 MIL 0.65P	5	4.4	1	0.65	PW016	PWP16	PWD16
TSSOP	225 MIL 0.65P	6.5	4.4	1	0.65	PW020	PWP20	PWD20
TSSOP	225 MIL 0.65P	7.8	4.4	1	0.65	PW024	PWP24	PWD24
TSSOP	225 MIL 0.65P	9.7	4.4	1	0.65	PW028	PWP28	PWD28
TSSOP	225 MIL 0.50P	7.8	4.4	1	0.5	DBT28	DCP28	DED28
TSSOP	225 MIL 0.50P	7.8	4.4	1	0.5	DBT30	DCP30	DED30
TSSOP	225 MIL 0.50P	9.7	4.4	1	0.5	DBT38	DCP38	DED38
TSSOP	225 MIL 0.50P	11.3	4.4	1	0.5	DBT44	DCP44	DED44
TSSOP	225 MIL 0.50P	12.5	4.4	1	0.5	DBT50	DCP50	DED50
TSSOP	300 MIL 0.65P	9.7	6.1	1	0.65	DA030	DAP30	DAD30
TSSOP	300 MIL 0.65P	11	6.1	1	0.65	DA032	DAP32	DAD32
TSSOP	300 MIL 0.65P	12.5	6.1	1	0.65	DA038	DAP38	DAD38
TSSOP	300 MIL 0.50P	12.5	6.1	1	0.5	DGG48	DCA48	DFD48
TSSOP	300 MIL 0.50P	14	6.1	1	0.5	DGG56	DCA56	DFD56
TSSOP	300 MIL 0.50P	17	6.1	1	0.5	DGG64	DCA64	DFD64
TVSOP	225 MIL 0.40P	3.6	4.4	1	0.4	DGV14	N/A	N/A
TVSOP	225 MIL 0.40P	3.6	4.4	1	0.4	DGV16	N/A	N/A
TVSOP	225 MIL 0.40P	5	4.4	1	0.4	DGV20	DGP20	DHD20
TVSOP	225 MIL 0.40P	5	4.4	1	0.4	DGV24	DGP24	DHD24

PowerPAD™ DEEP DOWNSET/EXPOSED DIE PAD PACKAGE DESIGNATORS - CONTINUED

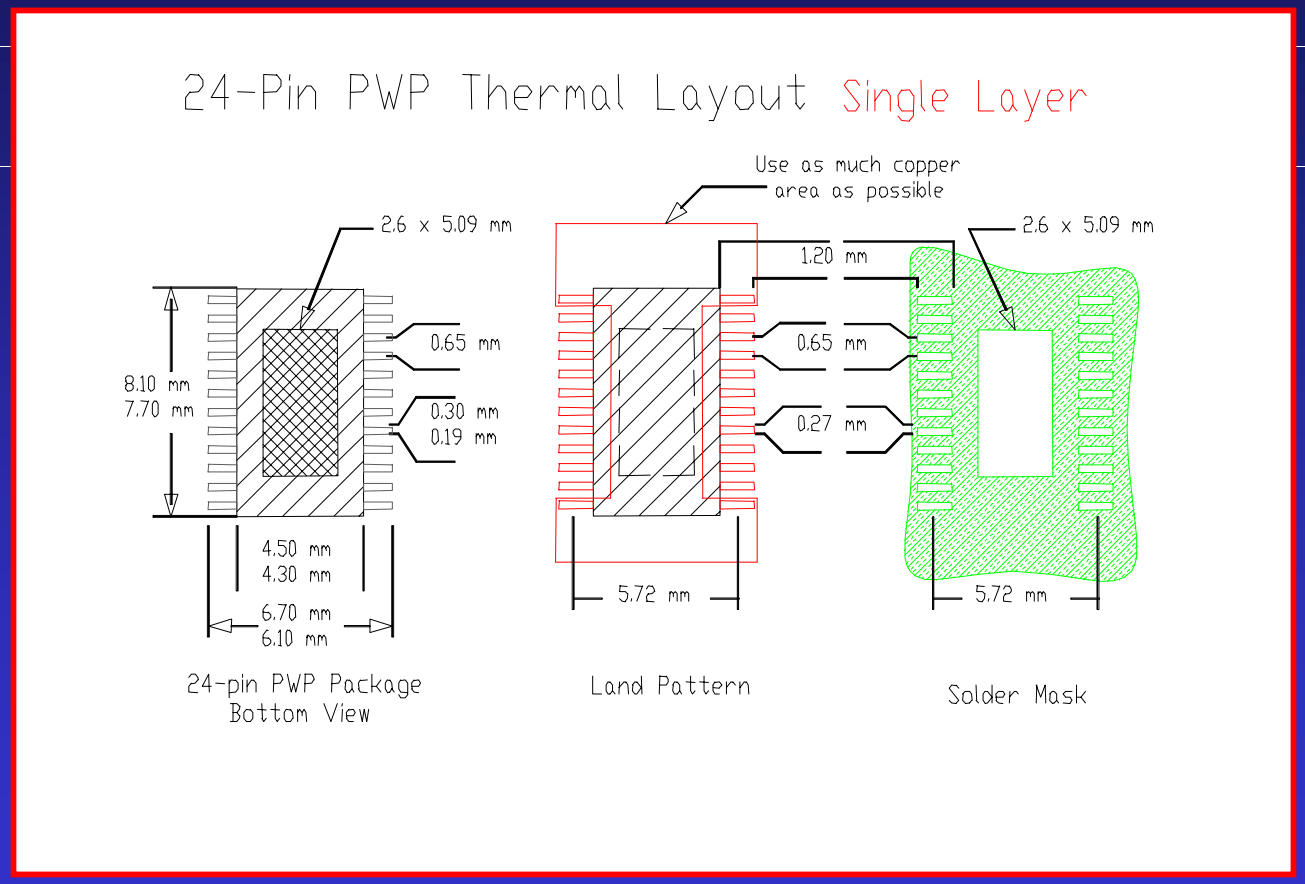
PACKAGE	BODY	BODY X	BODY Y	BODY Z	LEAD PITCH	DESIGNATOR STANDARD	PowerPAD™ NORMAL FORM	PowerPAD™ REVERSE FORM
TYPE	DESCRIPTION	mm	mm	mm	mm	PACKAGE	CHIP UP	CHIP DOWN
TVSOP	225 MIL 0.40P	9.7	4.4	1	0.4	DGV48	DGP48	DHD48
TVSOP	225 MIL 0.40P	11.3	4.4	1	0.4	DGV56	DGP56	DHD56
TVSOP	300 MIL 0.40P	17	6.1	1	0.4	DBB80	DDP80	DJD80
TVSOP	300 MIL 0.40P	20.8	6.1	1	0.4	DBB100	DDP100	DJD100
SOP	375 MIL, 127P	12.8	7.5	2.3	1.27	DW16	DWP16	DWD16
SOP	375 MIL 1.27P	12.8	7.5	2.3	1.27	DW20	DWP20	DWD20
SOP	375 MIL 1.27P	15.3	7.5	2.3	1.27	DW24	DWP24	DWD24
SOP	375 MIL 1.27P	17.8	7.5	2.3	1.27	DW28	DWP28	DWD28
TQFP	10 X 10mm 0.8P	10	10	1	0.8	PGT44	PGM44	PGS44
TQFP	7 X 7mm 0.5P	7	7	1	0.5	PFB48	PHP48	PKD48
TQFP	10 X 10mm 0.65P	10	10	1	0.65	PAH52	PGP52	PLD52
TQFP	7 X 7mm 0.4P	7	7	1	0.4	PEG64	PVP64	PVD64
TQFP	14 X 14mm 0.8P	14	14	1	0.8	PBR64	PBP64	PHD64
TQFP	10 X 10mm 0.5P	10	10	1	0.5	PAG64	PAP64	PJD64
TQFP	12 X 12mm 0.5P	12	12	1	0.5	PFC80	PFP80	PMD80
TQFP	14 X 14mm 0.5P	14	14	1	0.5	PZT100	PZP100	PFD100
TQFP	14 X 14mm 0.4P	14	14	1	0.4	PDS120	PQP120	PQD120
TQFP	14 X 14mm 0.4P	14	14	1	0.4	PDT128	PNP128	PND128
LQFP	20 X 20mm 0.5P	20	20	1.4	0.5	PGE144	PRP144	PRD144
LQFP	24 X 24mm 0.5P	24	24	1.4	0.5	PGF176	PTP176	PTD176
LQFP	24 X 24mm 0.4P	24	24	1.4	0.4	PDQ216	RBP216	RBD216
LQFP	28 X 28mm 0.65P	28	28	1.4	0.65	PSF160	PSP160	PSD160
LQFP	28 X 28mm 0.5P	28	28	1.4	0.5	PDV208	PYP208	PYD208
LQFP	28 X 28mm 0.4P	28	28	1.4	0.4	PEF256	PFK256	PFL256

QUALIFICATION TESTING RESULTS FOR PowerPAD™ CONFIGURATION 100 PIN PLASTIC TQFP

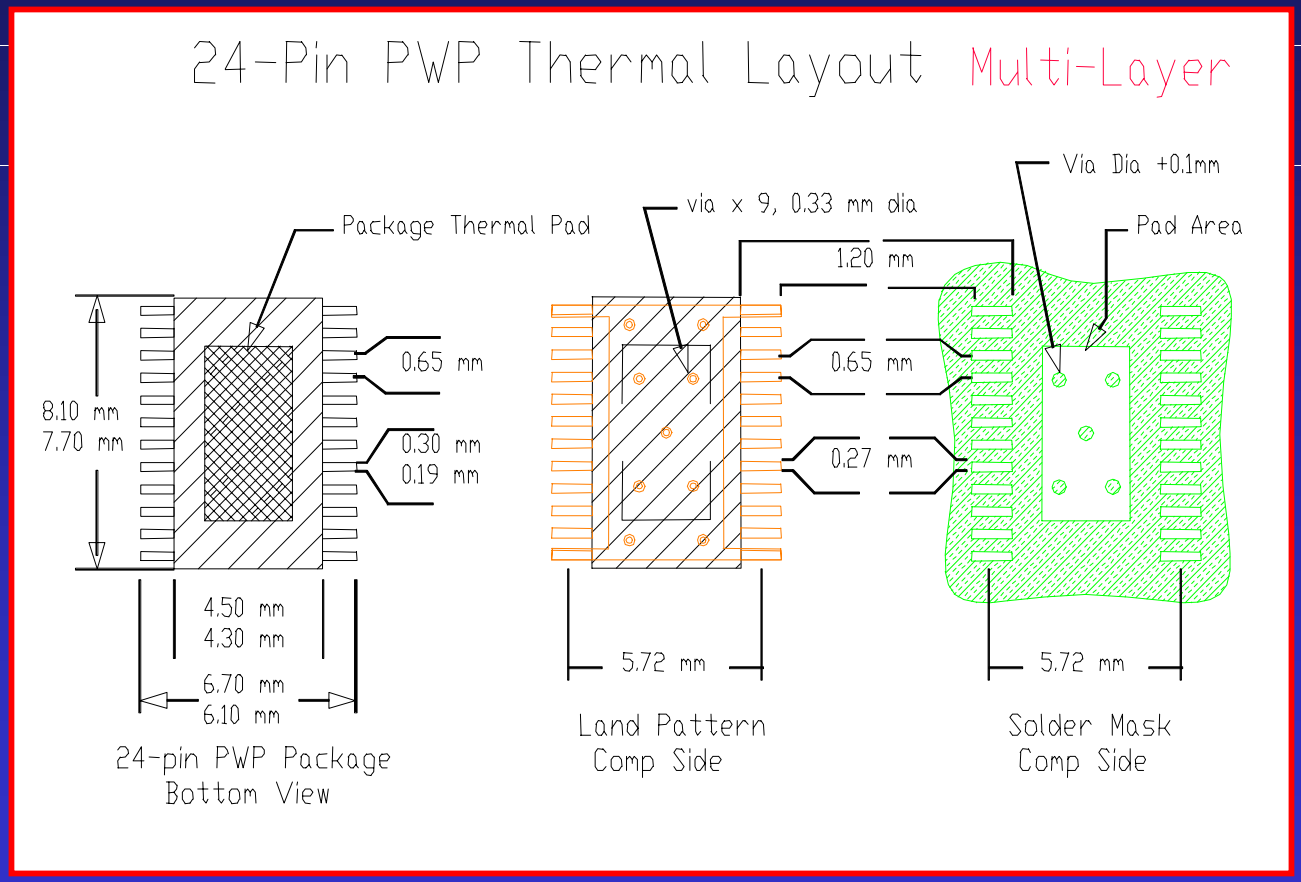
Test/Requirement	Conditions	Readpoints	SS/F Lot#1	Lot#2	Lot#3
*1. Steady-State Life	155C	240 Hrs	116/0	116/0	116/0
*2. Biased HAST	130C,85%RH	96 Hrs	116/0	116/0	116/0
*3. Autoclave	121C,15 PSIG	240 Hrs	76/0	76/0	76/0
*4A.Thermal Shock	-65/+150C	1000 Cyc	116/0	116/0	116/0
5. ESD:	100pF,1500 Ohms	2000 V	3/0	---	---
	200pF,0 Ohms	200 V	3/0	---	---
	CDM	1000 V	3/0	---	---
6. Solder Heat	260C,10 Sec		22/0	22/0	22/0
7. Solvent Resistance			12/0	12/0	12/0
8. Solderability	8 Hr Steam Age		22/0	22/0	22/0
9. Lead Fatigue			22/0	22/0	22/0
10. Lead Pull			22/0	22/0	22/0
11. Lead Finish Adhesion			15/0	15/0	15/0
12. Physical Dimensions			5/0	5/0	5/0
13. Flammability	Method A		5/0	5/0	5/0
	Method B		5/0	5/0	5/0
14. Thermal Impedance			Ver: WRWU 5/98		
15. Electromigration			Ver: WRWU 5/98		
16. Electrical Characterization			50	50	50
17. Bond Strength			76/0	76/0	76/0
18. Die Shear			5/0	5/0	5/0
19. Latch-Up			5/0	5/0	5/0
20. Manufacturability	(Wafer Fab)		Ver: D4NN 5/98		
	(Assembly Site)		Ver: NHUA 1/98		
25. Salt Atmosphere		24 Hrs	22/0	22/0	22/0
28. X-Ray	Top View Only		5/0	5/0	5/0
30. Visual/Mechanical			328/0	328/0	328/0
*31.Storage Life	170C	420 Hrs	45/0	45/0	45/0

* Samples used for these stresses were preconditioned with 192 hours of 30C/60%RH soak followed by three passes of VPR soldering per JEDEC A113.
* Samples used for these stresses were preconditioned with 3 cycles of flux + solder heat per QSS 009-501.

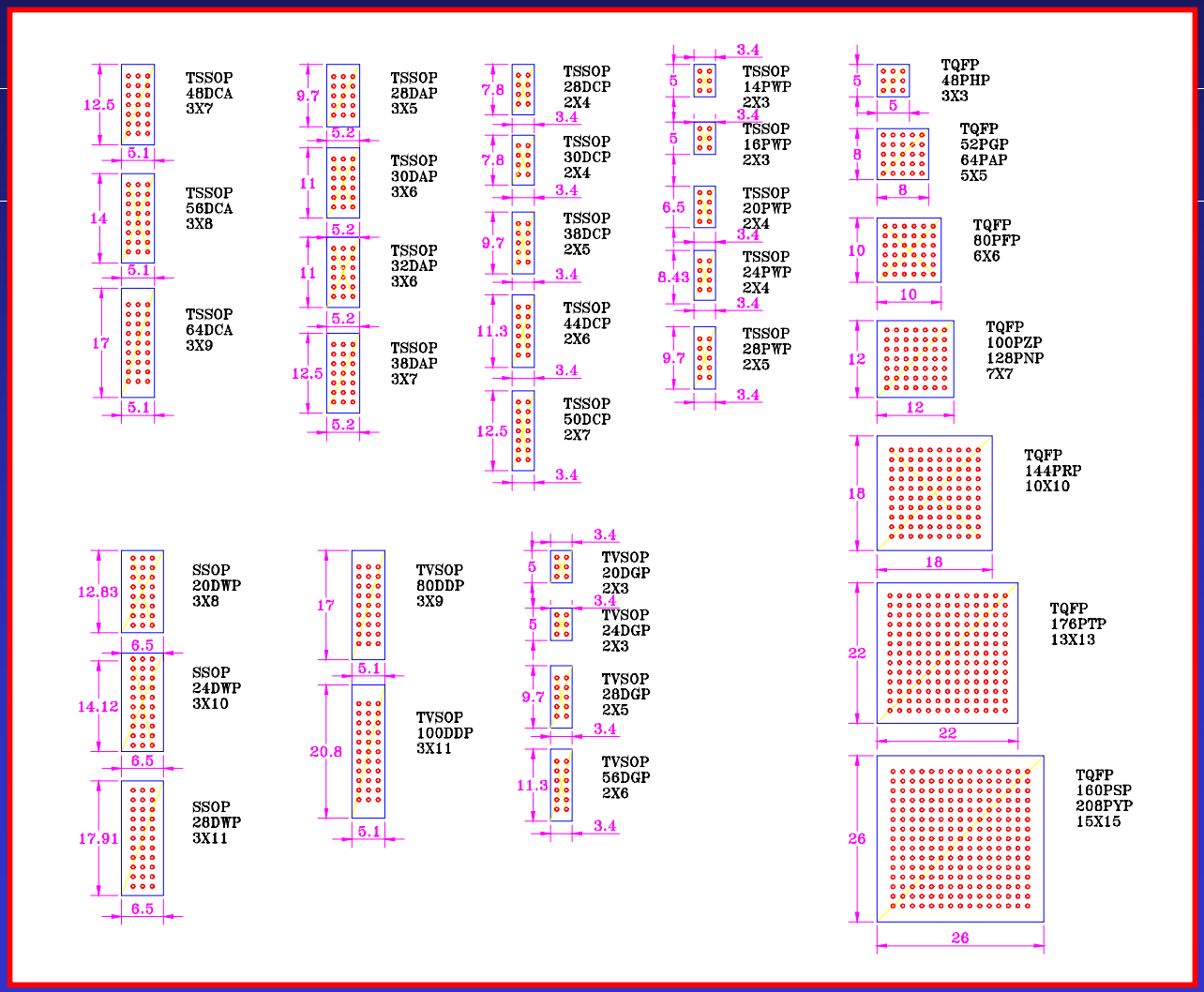
PCB LAYOUT FOR PowerPAD™ CONFIGURATION 24 PIN PLASTIC TSSOP WHERE ONLY TOP METAL LAYER IS USED FOR THERMAL REMOVAL



PCB LAYOUT FOR PowerPAD™ CONFIGURATION 24 PIN PLASTIC TSSOP WHERE MULTILAYER BOARD IS USED FOR THERMAL REMOVAL



PCB VIA LAYOUT FOR STANDARD PowerPAD™ PACKAGES WHERE MULTILAYER BOARD IS USED FOR THERMAL REMOVAL



THERMAL MODELING RESULTS FOR STANDARD PowerPAD™ PACKAGES vs CONVENTIONAL PACKAGES AND WITH/WITHOUT PCB ATTACHMENT

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
SSOP	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
SSOP	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
TVSOP	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
TVSOP	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
TVSOP	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
TVSOP	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
TVSOP	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
TSSOP	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
TSSOP	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
TSSOP	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
TSSOP	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
TSSOP	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
TSSOP	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
TSSOP	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
TSSOP	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
TSSOP	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
TSSOP	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
TSSOP	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
TSSOP	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
TSSOP	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964

THERMAL MODELING RESULTS FOR STANDARD PowerPAD™ PACKAGES vs CONVENTIONAL PACKAGES AND WITH/WITHOUT PCB ATTACHMENT (Continued)

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)	Theta Ja (C/W)	Theta Jc (C/W)	Psi Jt (C/W)
TSSOP	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
TSSOP	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
TSSOP	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
TQFP	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
TQFP	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
TQFP	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
TQFP	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
TQFP	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
TQFP	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
LQFP	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
LQFP	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
LQFP	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235

CONCLUSION

- Thermal power for semiconductor components will continue to rise
- Thermal management for plastic packages can meet the product needs
- PowerPAD™ packages provide superior, low-cost thermal solutions
  - Applicable to LQFP, TQFP, VQFP, SSOP, TSSOP, and VSSOP
  - Low mass of thermal pad provides advantages to hand-held needs
  - Conventional high-volume assembly equipment in place
  - Standard PCB assembly processes and flows
  - Minimum cost for PCB design implementation
  - High quality and reliability equivalent to standard plastic packages
  - Appropriate for both “chip up” and “chip down” configurations
- PowerPAD™ may be the enabler for next-generation “thin” packages

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