User's Guide

TPS40345 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS40345EVM-353 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.2-V output at up to 20 A from a 12-V input bus. The EVM is designed to start-up from a single supply, which means no additional bias voltage is required for start-up. The module uses the TPS40345 high-performance, mid-input voltage synchronous buck controller and TI's NexFET™ high performance MOSFETs.

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Trademarks

NexFET™ is a trademark of TI.
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1 Description

The TPS40345EVM-353 is designed to use a regulated 12 V (8 V – 14 V) bus voltage to provide a regulated 1.2-V output at up to 20 A of load current. The TPS40345EVM-353 is designed to demonstrate the TPS40345 controller and TI NexFETs in a typical 12-V bus to low-voltage application while providing a number of non-invasive test points to evaluate the performance of the TPS40345 and TI NexFETs in a given application.

1.1 Applications

- High-current, low-voltage FPGA or microcontroller core supplies
- High-current point of load modules
- Telecommunications equipment
- Computer peripherals

1.2 Features

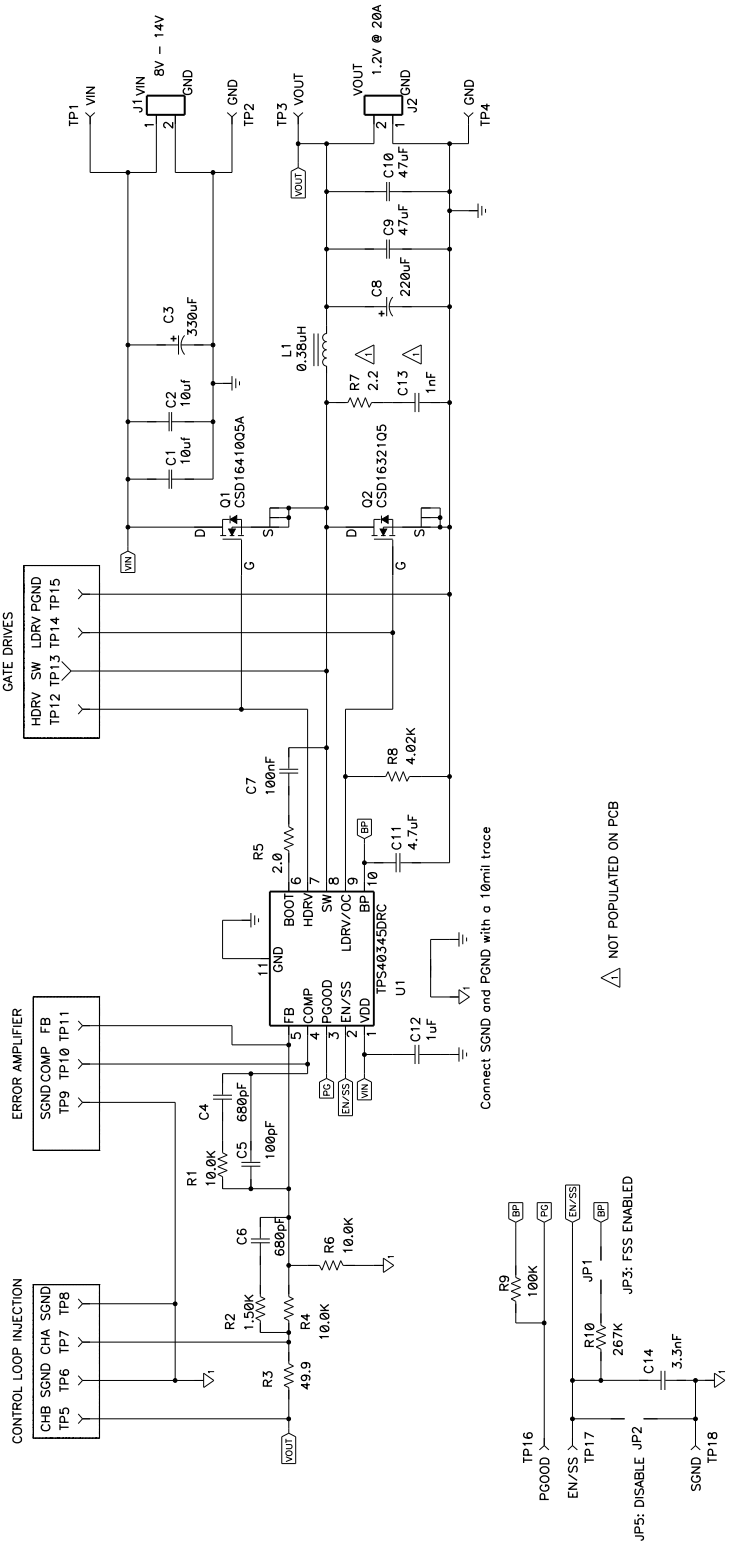
- 8-V to 14-V input voltage rating
- 1.2-V ± 2% output voltage rating
- 20-A steady state load current
- 600-kHz switching frequency
- Simple access to IC features including power good, enable, soft start, and error amplifier
- Convenient test points for simple, non-invasive measurements of converter performance

2 TPS40345EVM-353 Electrical Performance Specifications

Table 2-1. TPS40345EVM-353 Electrical and Performance Specifications

PARAMETER		NOTES AND CONDITIONS	MIN	TYP	MAX	UNIT
INPUTS CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = Nom, I_{OUT} = Max		2.3	2.5	A
	No load input current	V_{IN} = Nom, I_{OUT} = 0A		40	50	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 10 A		3.0		V
OUTPUTS CHARACTERISTICS						
V_{OUT1}	Output voltage 1	V_{IN} = 12 V, I_{OUT} = 20 A	1.17	1.2	1.23	V
	Line regulation	V_{IN} = 8 V to 14 V			0.5%	
	Load regulation	I_{OUT} = 0 A to 20 A			0.5%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 20 A			24	mVpp
I_{OUT1}	Output current 1	V_{IN} = 8 V to 14 V	0		20	A
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency		540	600	660	kHz
ηpk	Peak efficiency	V_{IN} = 12 V		88%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 20 A		86%		

3 TPS40345EVM-353 Schematic



For reference only, See Table 8-1 for specific values

Figure 3-1. TPS40345EVM-353 Schematic

4 Connector and Test Point Descriptions

4.1 Enable Jumper (JP2)

The TPS40345EVM-353 is designed with a Disable Jumper (JP2) using a 0.1-inch spacing header and shunt. Installing a shunt in the JP2 position connects the EN/SS pin to GND, discharges the soft-start capacitor, and disables the TPS40304 controller. This forces the output into a high-impedance state (approximately 20kΩ to GND).

4.2 Frequency Spread Spectrum – FSS Jumper (JP1)

The TPS40345EVM-353 is designed with a frequency spread spectrum (FSS) enable jumper (JP1) using a 0.1-inch spacing header and shunt. Installing a shunt in the JP1 position connects the EN/SS pin to BP via a 267-kΩ resistor (R10) to enable frequency spread spectrum.

FSS modulates the switching frequency to ±10% of the nominal value at 30 kHz to reduce EMI at the switching frequency and its harmonics, however there may be a 30-kHz component to the output ripple (see Figure 6-6).

The TPS40345EVM-353 does not dynamically monitor the JP1 status for programming FSS. The TPS40345EVM-353 must be disabled via JP2 or powered down by reducing VIN to less than 3 V to remove or install JP1.

4.3 Test Point Descriptions

Table 4-1. Test Point Descriptions

TEST POINT	LABEL	USE	SECTION
TP1	VIN	Measurement test point for input voltage	4.3.1
TP2	GND	Ground test point for input voltage	4.3.1
TP3	VOUT	Measurement test point for output voltage	4.3.1
TP4	GND	Ground test point for output voltage	4.3.2
TP5	CHB	Measurement test point for channel B of loop response	4.3.3
TP6	SGND	Ground test point for channel B of loop response	4.3.3
TP7	CHA	Measurement test point for channel A of loop response	4.3.3
TP8	SGND	Ground test point for channel A of loop response	4.3.3
TP9	SGND	Ground test point for error amplifier measurements	4.3.4
TP10	COMP	Measurement test point for error amplifier output voltage	4.3.4
TP11	FB	Measurement test point for error amplifier input voltage	4.3.4
TP12	HDRV	Measurement test point for high-side gate driver voltage	4.3.5
TP13	SW	Measurement test point for switching node voltage	4.3.5
TP14	LDRV	Measurement test point for low-side gate driver voltage	4.3.5
TP15	PGND	Ground test point for switch node and gate drive voltages	4.3.5
TP16	PGOOD	Measurement test point for power good	4.3.6
TP17	EN/SS	Measurement test point for enable / soft start	4.3.7
TP18	SGND	Ground test point for power good and enable / soft start	4.3.6 and 4.3.7

4.3.1 Input Voltage Monitoring (TP1 and TP2)

The TPS40345EVM-353 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and input terminal to TP2.

4.3.2 Output Voltage Monitoring (TP3 and TP4)

The TPS40345EVM-353 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module output voltage without losses from input cables and connectors. All input voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive input to TP3 and negative input to TP4.

4.3.3 Loop Response Testing (TP5, TP6, TP7, TP8, and R3)

The TPS40345EVM-353 provides four test points (2 signal and 2 ground) for measuring the control loop frequency response. This allows the user to measure the actual module loop response without modifying the evaluation board. A transformer isolated signal up to 30 mV can be injected between TP5 and TP7. The injected signal amplitude can be measured by the ac coupled amplitude at CHA (TP7) and the resulting output voltage deviation can be measured at CHB (TP5). See Figure 5-3 for additional detail.

4.3.4 Error Amplifier Voltage Monitoring (TP9, TP10, and TP11)

The TPS40345EVM-353 provides three test points for measuring the error amplifier input and output voltages. This allows the user to directly measure the feedback and control voltages of the TPS40304 controller. The control voltage (TP10) can also be used to measure the control to output or power-stage frequency response or output to control or error amplifier frequency response. See *Section 5.5* for additional details.

4.3.5 Switching Waveform Monitoring (TP12, TP13, TP14, and TP15)

The TPS40345EVM-353 provides three test points and a local power ground for measuring the switching waveforms of the module power stage. This allows the user to monitor actual switching waveforms during operation. TP13 is a 0.040-inch square pad of exposed PCB copper to minimize EMI radiation from the high transient voltages on the switch node. Switching waveform measurements should be made using power ground (TP15) as the ground reference for more accurate measurements.

4.3.6 Power-Good Voltage Monitoring (TP16 and TP18)

The TPS40345EVM-353 provides a test point and local ground for measuring the power good output voltage. A 100-kΩ resistor pullup to BP (R9) is included to allow the power-good signal to be monitored without requiring an external pull-up. For true open-drain operation with no pullup, remove R9. With R9 removed, TP16 can be connected to TP17 of another TPS40345EVM-353 to provide sequential start-up of the two TPS40345EVM-353 converters.

4.3.7 Enable and Soft-Start Voltage Monitoring (TP17 and TP18)

The TPS40345EVM-353 provides a test point and local ground for measuring the enable and soft-start voltage. TP17 and TP18 or JP2 can be used to provide an external enable signal. Due to the nature of the soft-start function, the external signal must be open-collector or open-drain without pullup.

5 Test Setup

5.1 Equipment

5.1.1 Voltage Source

V_{IN} — The input voltage source (V_{IN}) must be a 0-V to 15-V variable DC source capable of supplying 5 Adc.

5.1.2 Meters

A1: — Input current meter. 0 Adc – 5 Adc ammeter

V1: — Input voltage meter. 0 V – 15 V voltmeter

V2: — Output voltage meter. 0 V – 2 V voltmeter

5.1.3 Load

LOAD1: — Output load. Electronic load set for constant current or constant resistance capable of 0 Adc – 20 Adc at 1.2-Vdc.

5.1.4 Oscilloscope

For output voltage ripple: — Oscilloscope must be an analog or digital oscilloscope set for ac-coupled measurement with 20-MHz bandwidth limiting. Use 20 mV/division vertical resolution, 1-µs/division horizontal resolution.

For switching waveforms: — Oscilloscope shall be an analog or digital oscilloscope set for dc coupled measurement with 20-MHz bandwidth limiting. Use 2 V/division or 5V/division vertical resolution and 1-µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

VIN to J1: — The connection between the source voltage (V_{IN}) and J1 of TPS40345EVM-353 can carry as much as 3.5 Adc of current. The minimum recommended wire size is AWG #16 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

J2 to LOAD1: — The connection between the source voltage (V_{IN}) and J1 of TPS40345EVM-353 can carry as much as 20 Adc of current. The minimum recommended wire size is AWG #12 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

5.1.6 Other

FAN: — The TPS40345EVM-353 evaluation module includes components that can get hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, TI recommends a small fan capable of 200 lfm – 400 lfm to reduce component temperatures when operating.

5.2 Equipment Setup

Shown in Figure 5-1 is the basic test set up recommended to evaluate the TPS40345EVM-353. Note that although the return for J1 and JP2 are the same system ground, the connections should remain separate as shown in Figure 5-1.

5.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 4 A, maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 5-1.
3. Connect VIN to J1 as shown in Figure 5-1.
4. Connect ammeter A1 between VIN and J1 as shown in Figure 5-1.
5. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 5-1.
6. Connect voltmeter V2 to TP3 and TP4 as shown in Figure 5-1.
7. Connect oscilloscope probes to desired test points per Table 4-1.
8. Place fan as shown in Figure 5-1 and turn on making sure to blow air directly across the evaluation module.

5.2.2 Diagram

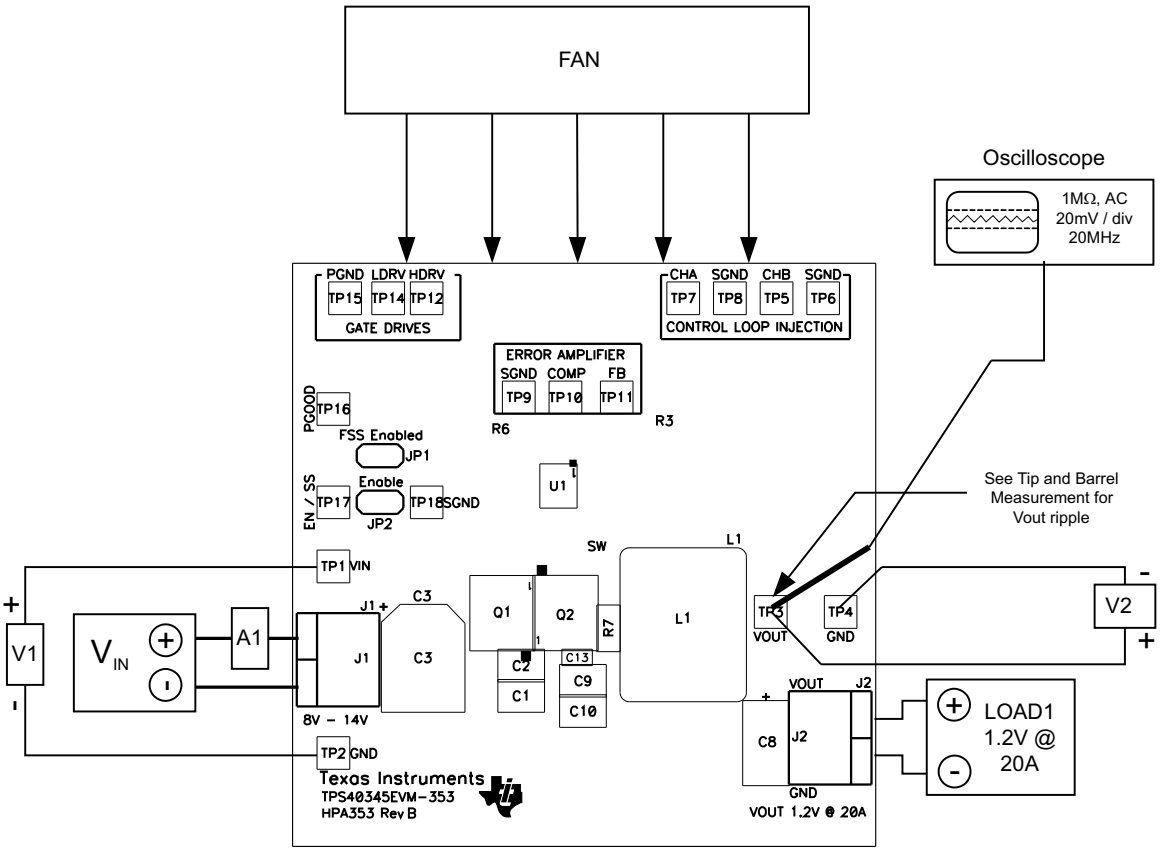


Figure 5-1. TPS40345EVM-353 Recommended Test Set-Up

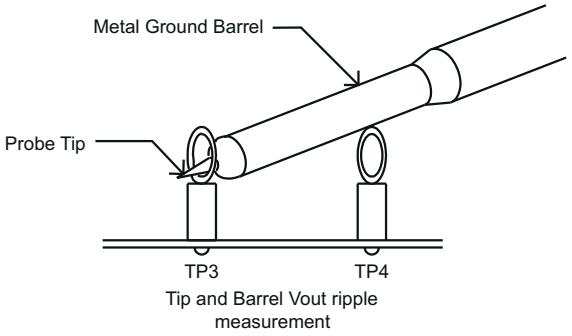


Figure 5-2. Output Ripple Measurement – Tip and Barrel using TP3 and TP4

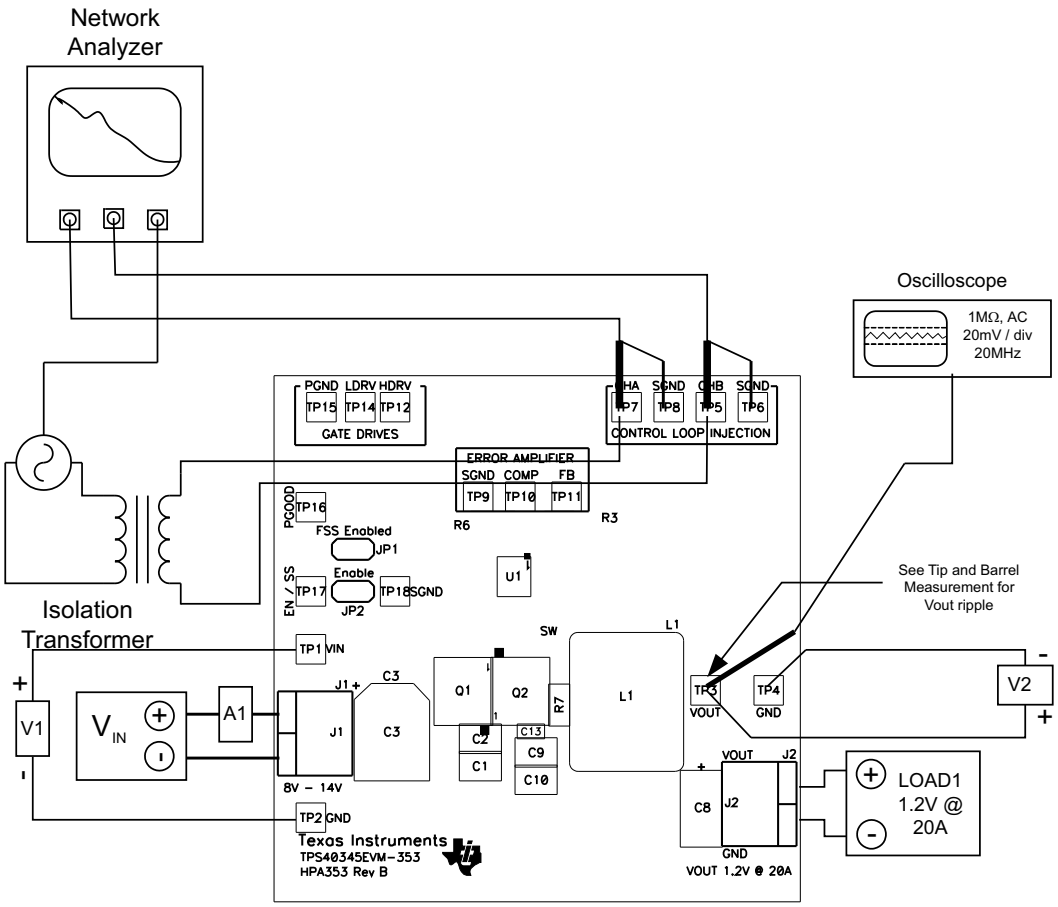


Figure 5-3. Control Loop Measurement Setup

5.3 Start-Up/Shutdown Procedure

1. Verify shunt position for JP1 for desired FSS status per Section 4.2.
2. Remove shunt from JP2 location if present.
3. Increase V_{IN} from 0 Vdc to 12 Vdc.
4. Vary LOAD1 from 0 Adc to 20 Adc.
5. Vary V_{IN} from 8 V to 14 V.
6. Decrease V_{IN} to 0 V.
7. Decrease LOAD1 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

1. Follow *Section 5.3* steps 1 – 5 to set V_{IN} and LOAD1 to the desired operating condition.
2. Connect oscilloscope probe with exposed metal barrel to TP3 and TP4 per Figure 5-2.
3. Set oscilloscope per oscilloscope for output voltage ripple measurement in *Section 5.1.4*.
4. Follow Section 5.3 steps 6 and 7 to power down.

5.5 Control Loop Gain and Phase Measurement Procedure

1. Follow Section 5.3 steps 1 – 5 to set V_{IN} and LOAD1 to the desired operating condition:
   a. If JP1 is installed (FSS enabled), loop response data about the modulation frequency (30 kHz) may be affected.
2. Connect a 1-kHz – 1-MHz isolation transformer to TP5 and TP7 as shown in Figure 5-3.
3. Connect input signal amplitude measurement probe (channel A) to TP7 as shown in Figure 5-3.
4. Connect output signal amplitude measurement probe (channel B) to TP5 as shown in Figure 5-3.
5. Connect ground lead of channel A and channel B to TP6 and TP8 as shown in Figure 5-3.
6. Inject 30 mV or less signal across R3 through isolation transformer.
7. Sweep frequency from 1 kHz to 1 MHz with 10-Hz or lower post filter.

8. Control loop gain can be measured by $20 \times \mathrm{LOG}\left(\frac{\text{Channel B}}{\text{Channel A}}\right)$
9. Control loop phase can be measured by the phase difference between channel A and channel B.
10. Control to output response (power stage transfer function) can be measured by connecting channel A probe to TP10 (COMP) and channel B probe to TP5 (CHB).
11. Output to control response (compensated error amplifier transfer function) can be measured by connecting channel A probe to TP7 (CHA) and channel B probe to TP10 (COMP).
12. Follow Section 5.3 steps 6 and 7 to power down.

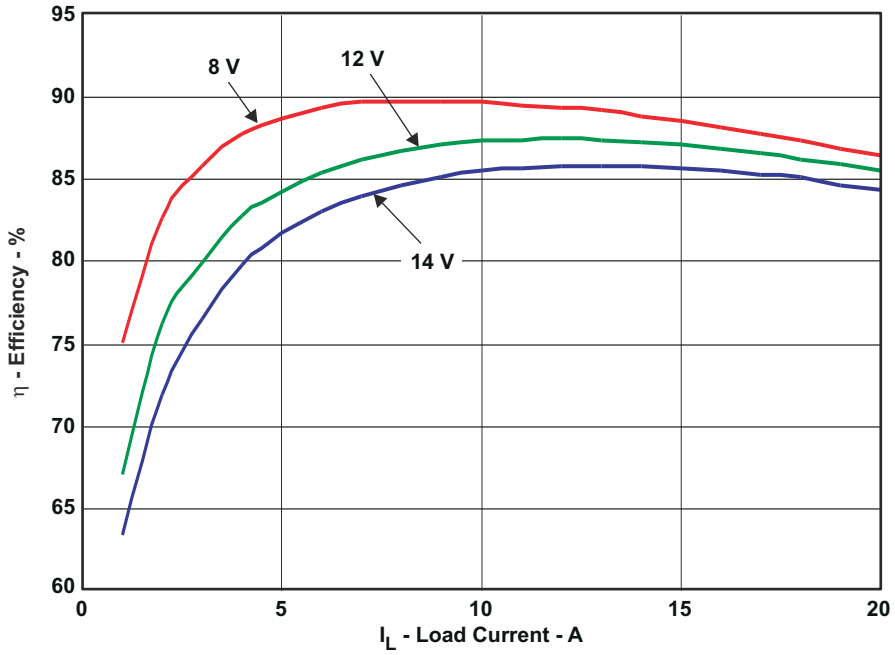
5.6 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD1
3. Shut down V_{IN}
4. Shut down fan

6 TPS40345EVM-353 Test Data

Figure 6-1 through Figure 6-6 present typical performance curves for the TPS40345EVM-353. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

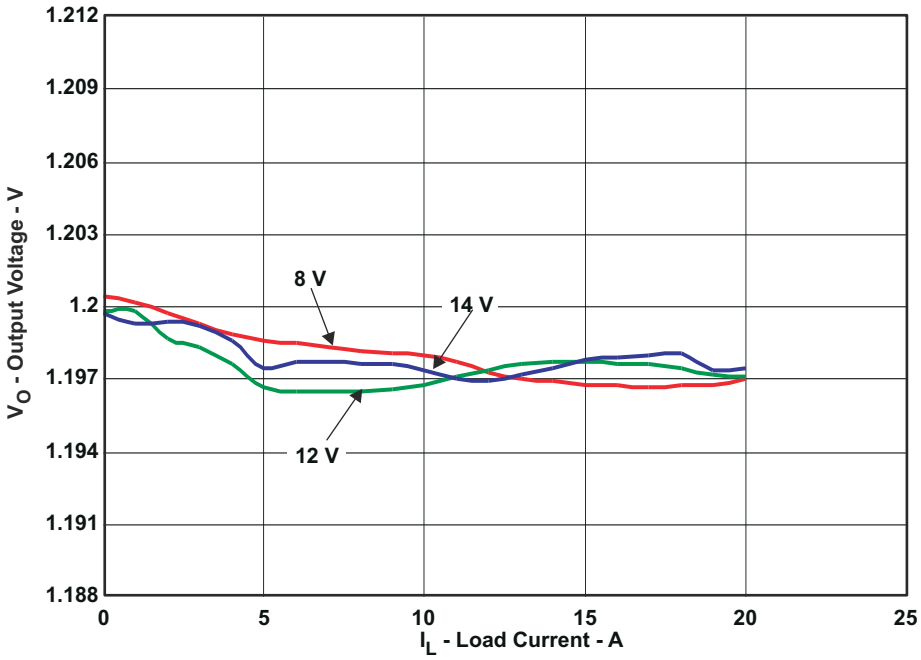
6.1 Efficiency



V_{IN} = 8.0V – 14V, V_{OUT} = 1.2V, I_{OUT} = 0A – 20A

Figure 6-1. TPS40345EVM-353 Efficiency vs Load Current

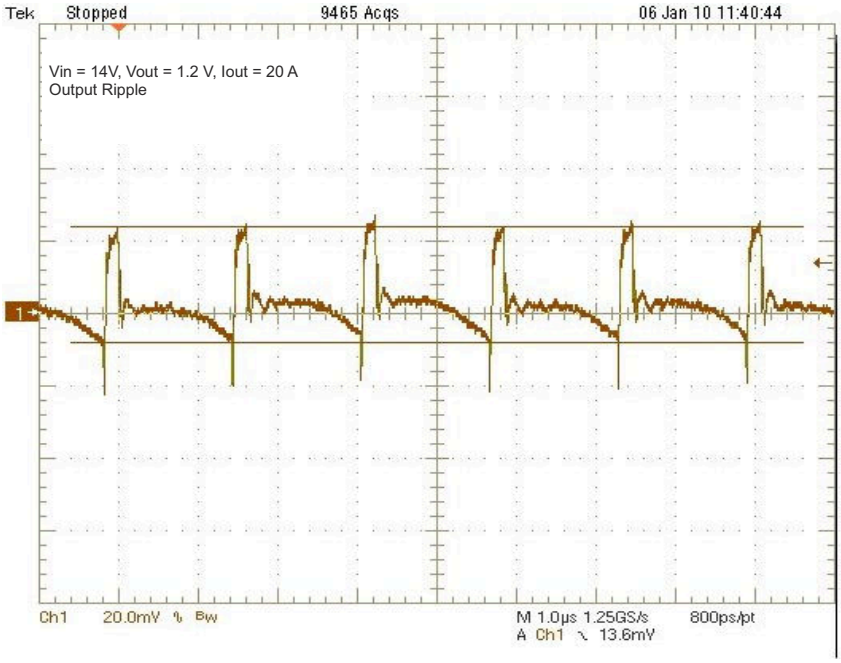
6.2 Line and Load Regulation



V_{IN} = 8.0V – 14V, V_{OUT} = 1.2V, I_{OUT} = 0A – 20A

Figure 6-2. TPS40345EVM-353 Output Voltage vs Load Current

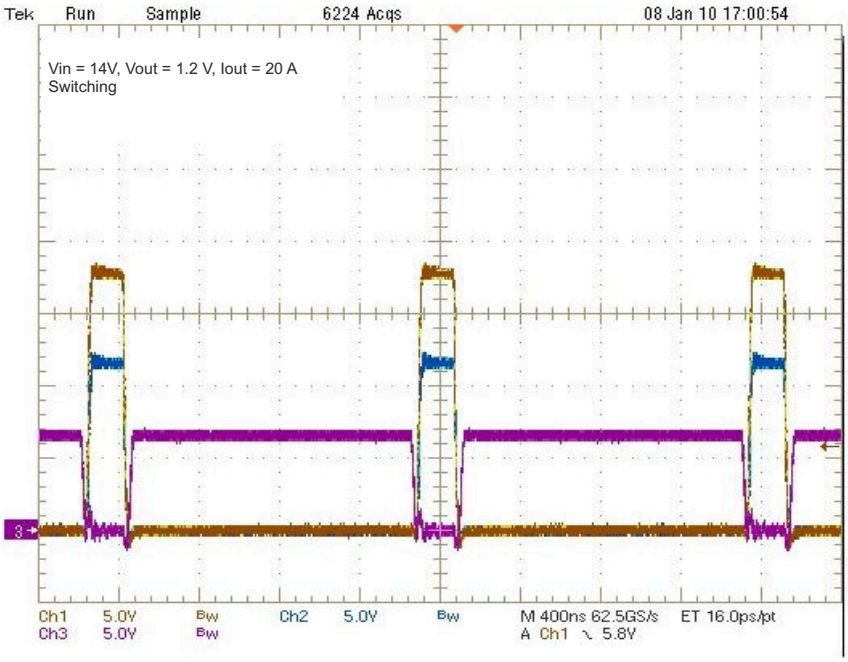
6.3 Output Voltage Ripple



V_{IN} = 14V, V_{OUT} = 1.2V, I_{OUT} = 20A

Figure 6-3. TPS40345EVM-353 Output Voltage Ripple

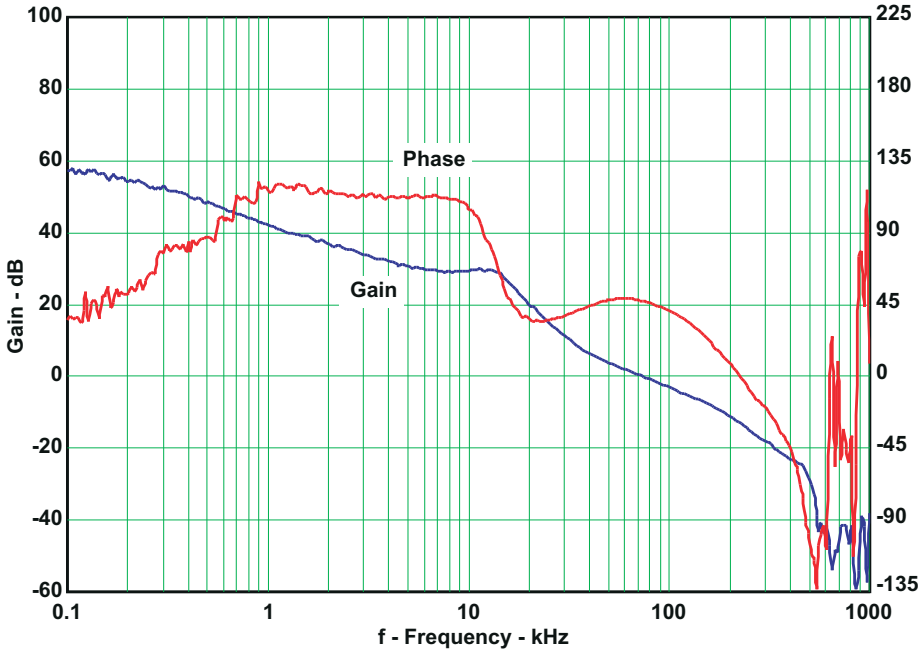
6.4 Switch Node



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 20 A Ch1: TP12 (HDRV), Ch2:13 TP (SW), Ch3: TP14 (LDRV)

Figure 6-4. TPS40345EVM-353 Switching Waveforms

6.5 Control Loop Bode Diagram



V_{IN} = 14V, V_{OUT} = 1.2V, I_{OUT} = 20A, Bandwidth: 73kHz, Phase Margin: 47°

Figure 6-5. TPS40345EVM-353 Gain and Phase vs Frequency

6.6 Additional Waveforms

6.6.1 Output Ripple With Frequency Spread Spectrum (FSS) Enabled

FSS varies the output switching frequency. This change in switching frequency can produce a small change in the output voltage at the modulation frequency. Figure 6-6 shows the approximately 10-mV modulation of the output voltage generated when FSS is enabled.

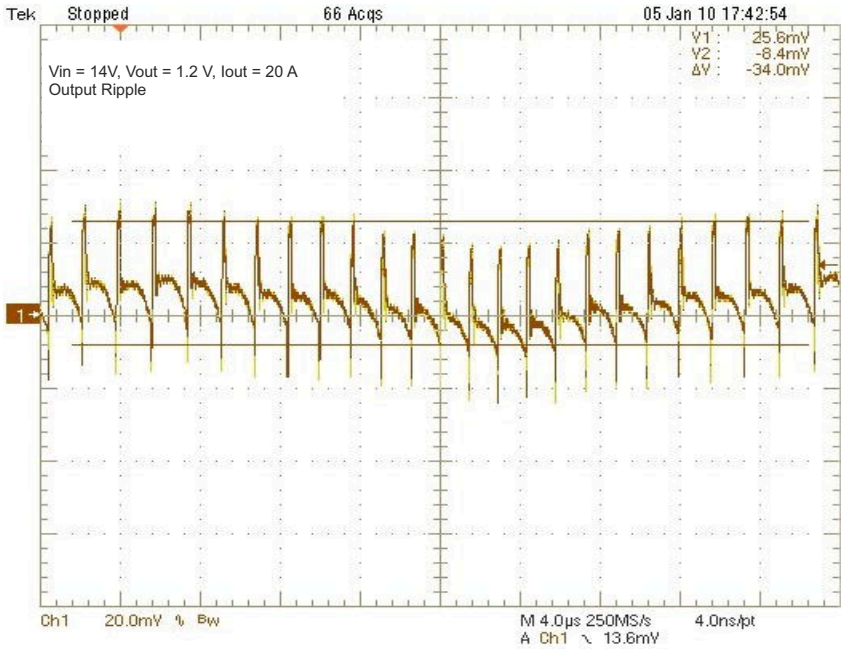


Figure 6-6. TPS40345EVM-353 Output Ripple With FSS Enabled

7 TPS40345EVM-353 Assembly Drawings and Layout

The following figures (Figure 7-1 through Figure 7-6) show the design of the TPS40345EVM-353 printed circuit board. The EVM has been designed using a 4-layer, 2-oz. copper-clad circuit board 3-inch × 3-inch with all components on the top to allow the user to easily view, probe, and evaluate the TPSxxxxx control IC in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

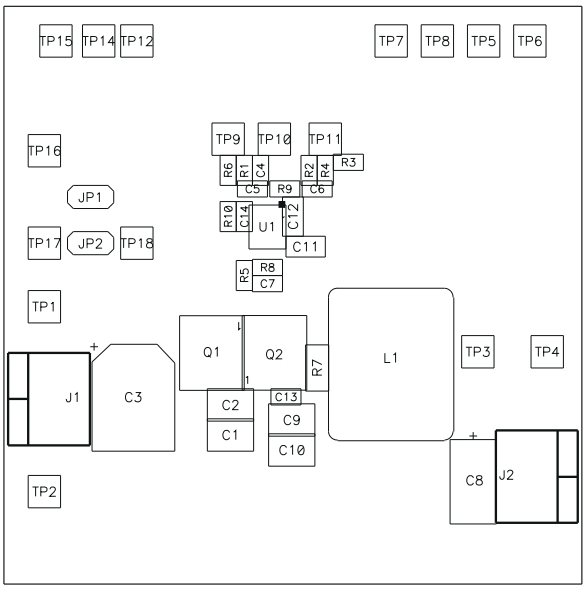


Figure 7-1. TPS40345EVM-353 Component Placement (Top View)

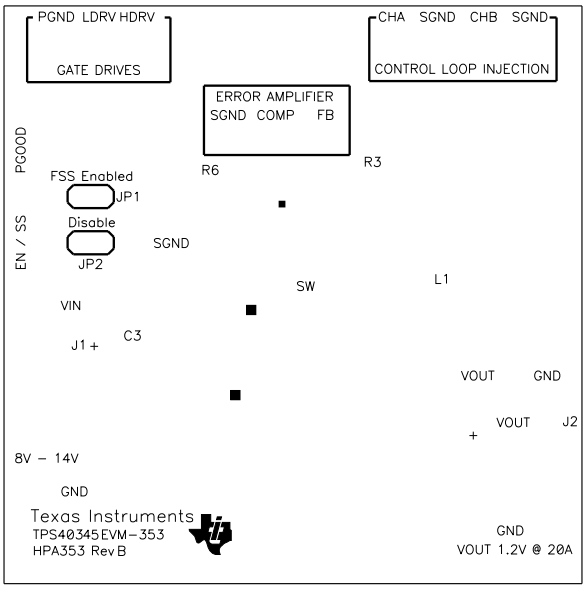


Figure 7-2. TPS40345EVM-353 Silk Screen (Top View)

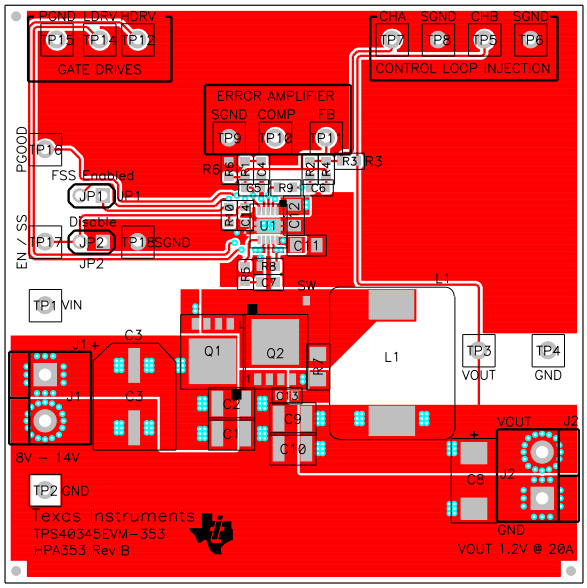


Figure 7-3. TPS40345EVM-353 Top Copper (Top View)

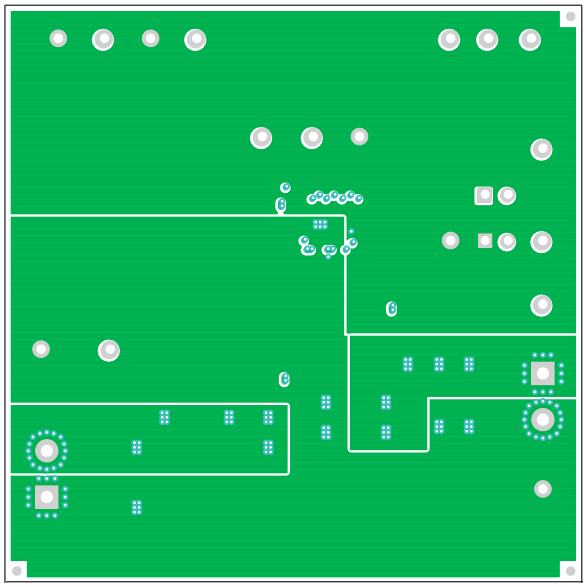


Figure 7-4. TPS40345EVM-353 Bottom Copper (Top View)

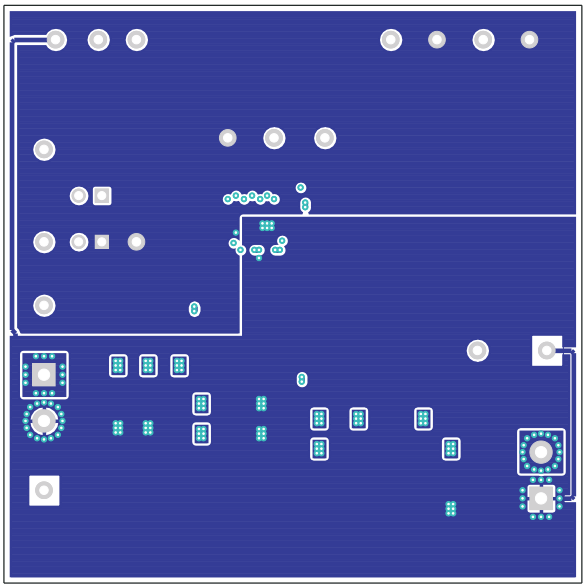


Figure 7-5. TPS40345EVM-353 Internal 1 (X-Ray Top View)

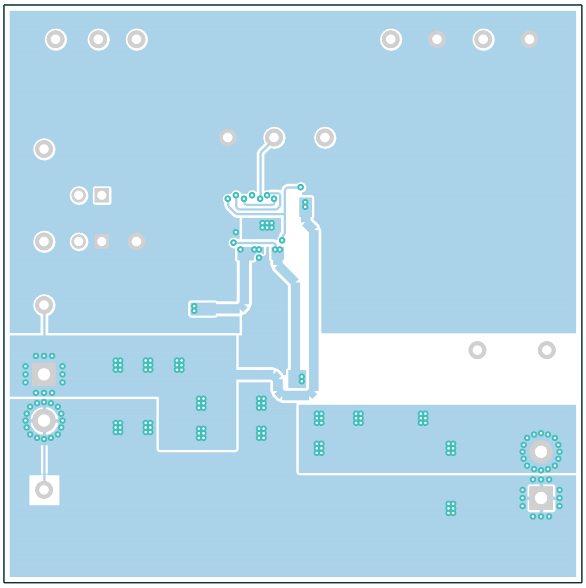


Figure 7-6. TPS40345EVM-353 Internal 2 (X-Ray Top View)

8 TPS40345EVM-353 Bill of Materials

Table 8-1. TPS40345EVM-353 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	10µF	Capacitor, Ceramic, 25V, X7R, 10%	1210	Std	Std
1	C11	4.7µF	Capacitor, Ceramic, 10V, X7R, 20%	0805	Std	Std
1	C12	1µF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
0	C13	1nF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std	Std
1	C14	3.3nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
1	C3	330µF	Capacitor, Aluminum, 25V, ±20%, 160mΩ	0.328 x 0.390 inch	EEEFK1E331P	Panasonic
2	C4, C6	680pF	Capacitor, Ceramic, 25V, COG, 10%	0603	Std	Std
1	C5	100pF	Capacitor, Ceramic, 25V, COG, 10%	0603	Std	Std
1	C7	100nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
1	C8	220µF	Capacitor, POSCAP, 6.3V, 25mΩ, 105C, 20%	7343(D)	6TPE220M	Sanyo
2	C9, C10	47µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
2	J1, J2	ED120/2DS	Terminal Block, 2-pin, 15A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
2	JP1, JP2	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	0.38µH	Inductor, SMT, 35A	0.512 x 0.571 inch	PG0077.401NLT	Pulse
1	Q1*	CSD16410Q5A	MOSFET, N-Chan, 25V, 59A, 9.6mΩ	QFN-8 POWER	CSD16410Q5A	TI
1	Q2*	CSD16321Q5	MOSFET, N-Chan, 25V, 31A	QFN-8 POWER	CSD16321Q5	TI
3	R1, R4, R6	10.0kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	267kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	1.50kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	49.9Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	2Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7	2.2Ω	Resistor, Chip, 1/8W, 5%	1206	Std	Std
1	R8	4.02kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	100kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	TP1, TP3	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
0	TP13	N/A	Test Point, SM, 2x3mm	0.118 x 0.079 inch		
6	TP2, TP4, TP6, TP8, TP15, TP18	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
9	TP5, TP7, TP9–TP12, TP14, TP16, TP17	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	U1*	TPS40345DRC	IC, 3V – 20V sync. Buck controller/Enable Light Load/Fq Spread Spectrum	DRC10	TPS40345DRC	TI
2	–		Shunt, 100-mil, Black	0.1	929950-00	3M
1	–		PCB, 2.5 In x 2.5 In x 0.062 In		HPA353	Any

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2017) to Revision A (August 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated user's guide title..... 2

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