User's Guide

LM5013-Q1EVM User's Guide

ABSTRACT

The LM5013-Q1EVM has a 100-V DC/DC buck regulator that employs asynchronous rectification and achieves high conversion efficiency. The EVM operates over a wide input voltage range of 15-V to 100-V to provide a regulated 12-V output at 300-kHz switching frequency. The module design uses the LM5013-Q1 asynchronous buck converter with wide input voltage (wide V_{IN}) range, wide duty-cycle range, integrated high-side power MOSFET, cycle-by-cycle overcurrent protection, and precision enable. With AEC-Q100 grade 1 automotive qualification, the LM5013-Q1 is rated to operate over a junction temperature range of –40°C to +150°C. The LM5013-Q1 is available in an 8-pin SO PowerPAD™ package to enable high density, low component count DC/DC solutions.

Use the LM5013-Q1 with *WEBENCH® Power Designer* LM5013-Q1 with *WEBENCH® Power Designer* to create a custom regulator design.

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Trademarks

1 General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support.ti.com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed-circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area.
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**

  As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.

- **Personal Safety:**
  - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact may cause burns. Do not touch! A fan should be utilized if full-power operation is done. The EVM was constructed to highlight the small solutize size and as a result, is not as thermally optimized as typical application PCB.

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board should be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Overview

2.1 LM5013-Q1 Asynchronous Buck Converter

The LM5013-Q1 step-down switching converter features all the functions needed to implement a low-cost, high-efficiency buck regulator capable of supplying 3.5-A load current. An adaptive constant on-time (COT) control scheme and PFM at light loads enables low standby current. Various features incorporated for enhanced reliability and safety include cycle-by-cycle peak current limit, thermal shutdown protection, internal output voltage soft-start timer, precision enable , and an open-drain PGOOD indicator for sequencing and fault reporting.

Figure 2-1 shows the pin configuration of the LM5013-Q1. Figure 2-2 presents the regulator schematic for quick reference.

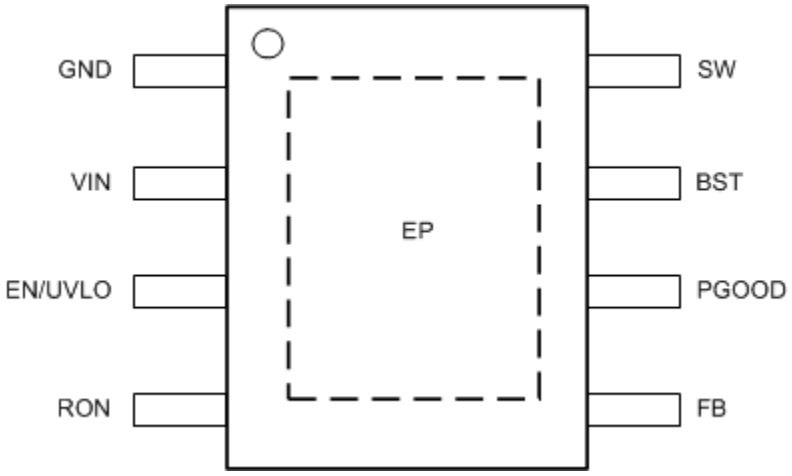

Figure 2-1. LM5013-Q1 Pin Configuration (8-Pin SO Package with PowerPAD, Top View)

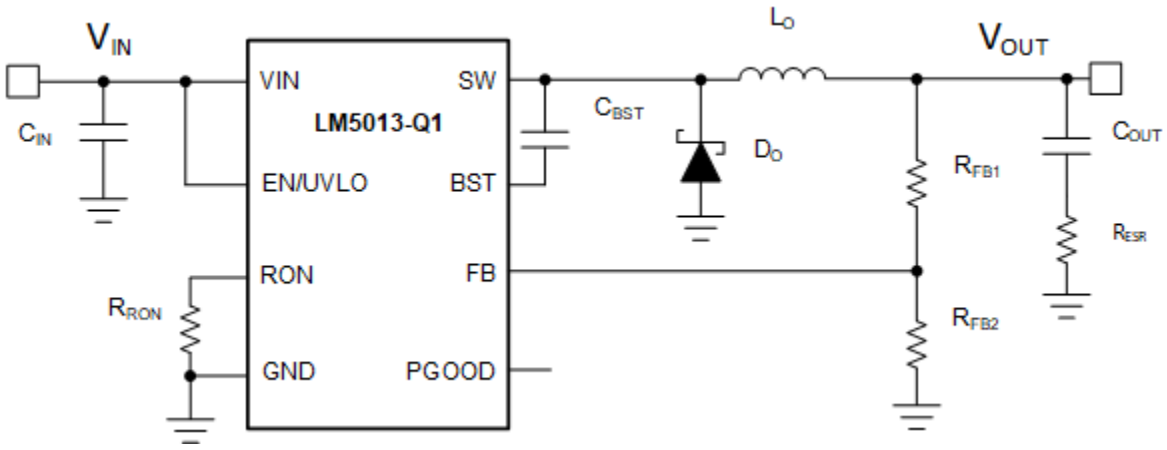

Figure 2-2. LM5013-Q1 Buck Regulator Simplified Schematic

3 LM5013-Q1 Evaluation Module

The LM5013-Q1EVM is configured to deliver 12-V at up to 3.5-A at a switching frequency of 300-kHz. As shown in LM5013-Q1EVM schematic, a type 3 ripple generation circuit is used to generate the appropriate voltage ripple on FB. This circuit uses an RC network (consisting of "R4" and "C4") between SW and V_{OUT} to create a triangular ramp. This triangular ramp is then AC coupled into the feedback node with capacitor "C16." This method is best suited for applications where low output voltage ripple is required and where ceramic output capacitors are used (since it is not using the output voltage to generate the ripple signal). If additional output ripple can be managed, a possibility for reduced BOM count can be achieved with type 1 or type 2 compensation. Reference the data sheet for these implementations.

3.1 Quick Start Procedure

1. Connect the voltage supply between VIN and GND connectors using short wires.
2. Connect the load of the converter between VOUT and GND connectors using short wires.
3. Set the supply voltage (V_{VIN}) at an appropriate level between 15-V to 100-V. Set the current limit of the supply to an appropriate level as well.
4. Turn on the power supply. The EVM powers up and provides V_{OUT} = 12-V.
5. Monitor the output voltage while increasing the load current to max.

   See Figure 3-1 for the location of the connectors.

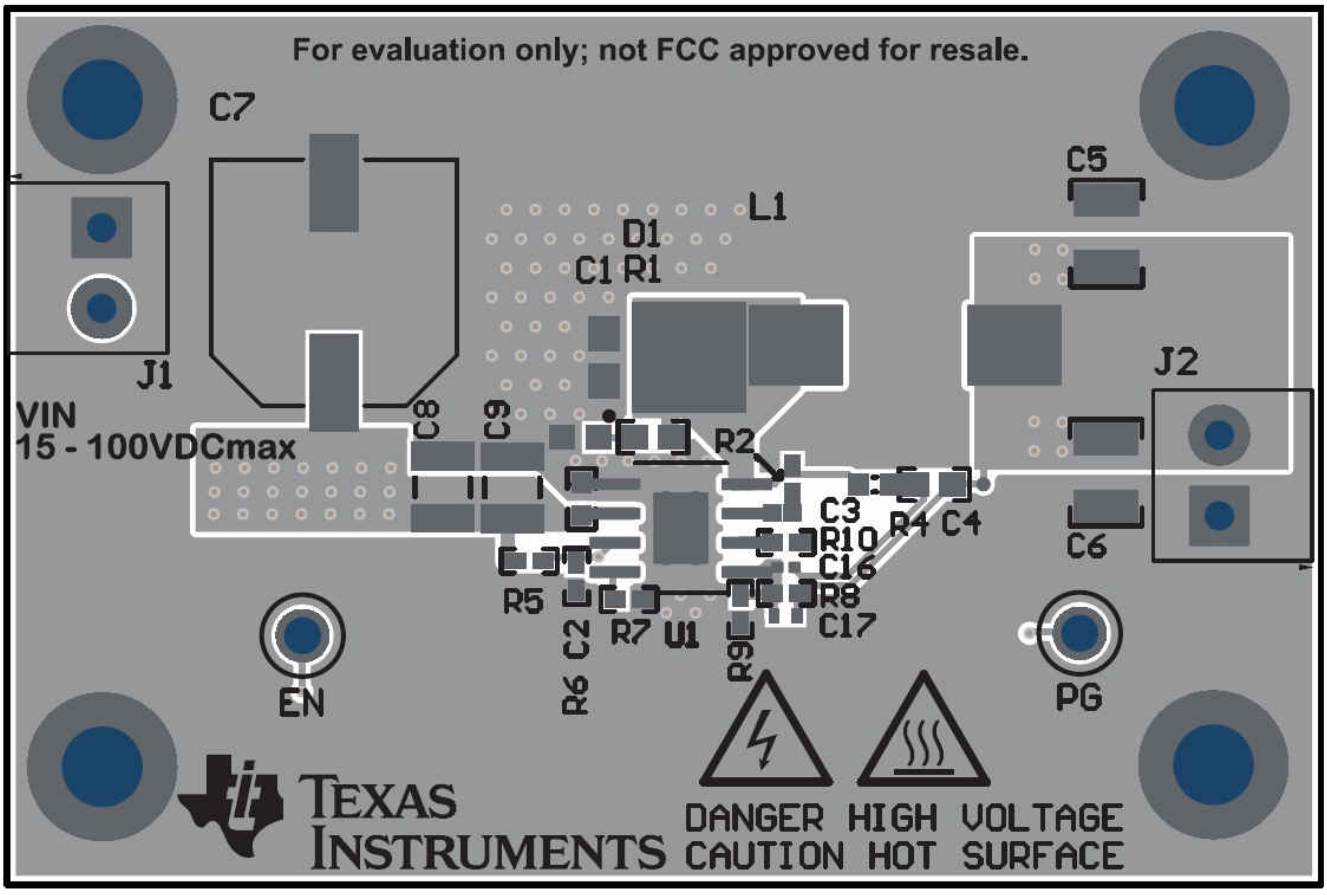

Figure 3-1. LM5013-Q1 EVM Top View

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

3.2 Detailed Descriptions

This section describes the connectors and the test points on the EVM and how to properly connect, set up and use the LM5013-Q1EVM. See Figure 3-1 for a top view of the EVM.

VOUT Output voltage of the converter.

VOUT connector and test point connected to the power inductor and the output capacitors. Connect the loading device between VOUT and GND connectors to provide loading to the regulator. Connect the loading device to the board with short wires to handle the DC output current.

GND Ground of the converter.

It is connected to the GND as well as the return terminals of the input and output capacitors. GND is the current return path for both supply voltage and load. Connect to supply and load grounds with short wires.

VIN Input voltage to the converter.

VIN connector and test point connects to the input capacitors and the VIN pin of the LM5013-Q1. Connect the supply voltage from a power supply or a battery between the VIN and GND connectors. The voltage range should be higher than 6 V for the device to be active. V_{VIN} higher than 15-V provides a regulated 12-V output voltage. To avoid damaging the device V_{VIN} should be no greater than 100-V. The current limit on the supply should be high enough to provide the needed supply current when the output is fully loaded. The supply voltage should be connected to the board with short wires. C_7 is populated to avoid oscillation between the cable parasitic inductance and the low-ESR input ceramic capacitors.

VIN-EMI Input voltage to input filter of the converter.

The supply voltage should be connected to the board with short wires.

The inductor/ferrite in series with input path have some DCR associated with them. Verifying datasheet specification should be done by shorting these components.

GND-EMI Ground connection near the input filter.

This is the current return path for the supply connected to VIN-EMI. It provides a direct connection to the input filter capacitors to filter conducted noise generated by the converter. Use VIN-EMI and GND-EMI connections at the input filter to minimize EMI.

Input Filter EMI mitigation.

The input filter consists of a filter inductor, ferrite bead and ceramic capacitors. An electrolytic capacitor is included for bulk energy storage and input parallel damping.

EN/UVLO Test point to monitor the EN/UVLO pin of the device.

This test point is to monitor the voltage on the device EN/UVLO pin.

EN/UVLO Set EN/UVLO

By default, device is hard-enabled. Device enable/disable voltage would correspond to typical $V_{EN\text{-}RISING}$ and $V_{EN\text{-}FALLING}$ datasheet specification.

The enable/disable voltage can be varied by calculating for bottom UVLO resistor R_{UV2}.

Calculate the lower UVLO resistor, R_{UV2} (R6), based on the desired turn-on voltage of 6 V and the selected upper UVLO resistor, R_{UV1} (R5) , of 1 MΩ using Equation 1.

$$R_{UV2} = \frac{1.5\,V}{V_{IN(on)} - 1.5\,V} \cdot R_{UV1} = \frac{1.5\,V}{6\,V - 1.5\,V} \cdot 1\,M\Omega = 332k\Omega \quad (1)$$

PGOOD PGOOD

This flag indicates whether the output voltage has reached its regulation level. LM5013-Q1 PGOOD is an open-drain output that is tied to V_{OUT} through pull-up resistor.

4 Schematic

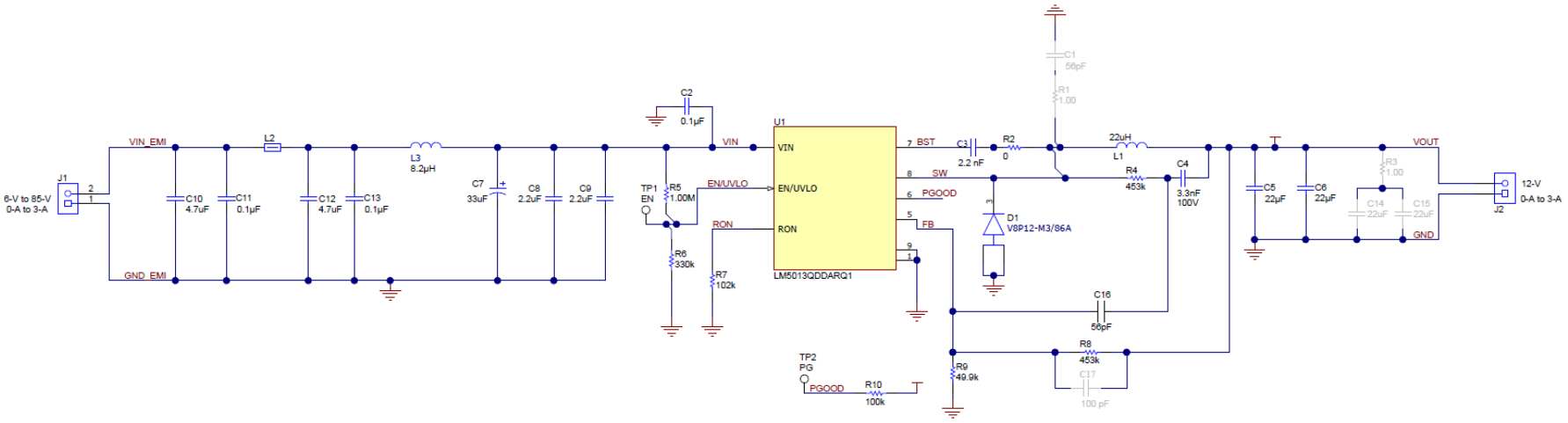

Figure 4-1. LM5013-Q1 EVM Schematic

Note the ripple injection circuit was designed for minimum ripple at the nominal input voltage of the design of 48 V. The circuit should be re-designed if the nominal voltage is lower, or make sure ensure there is sufficient ripple injection for stability at lower input voltages (< 30 V).

5 PCB Layout

Top Layer and Silkscreen Layer through Bottom Layer Routing show the board layout for the LM5013-Q1EVM. The EVM offers resistors, capacitors, and test points to configure the output voltage, precision enable, and switching frequency.

The 8-pin SO PowerPAD package offers an exposed thermal pad, which must be soldered to the copper landing on the PCB for optimal thermal performance. The PCB consists of a 4-layer design. There are 2-oz copper planes on the top and bottom and 1-oz copper mid-layer planes to dissipate heat with an array of thermal vias under the thermal pad to connect to all four layers.

Test points have been provided for ease of use to connect the power supply, required load, and to monitor critical signals.

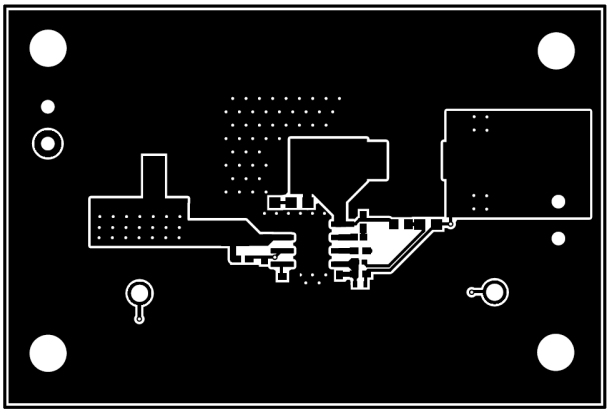

Figure 5-1. Top Layer and Silkscreen Layer

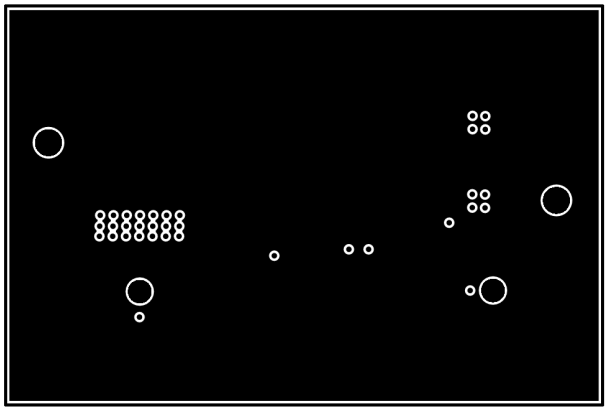

Figure 5-2. Mid-Layer 1 Ground Plane

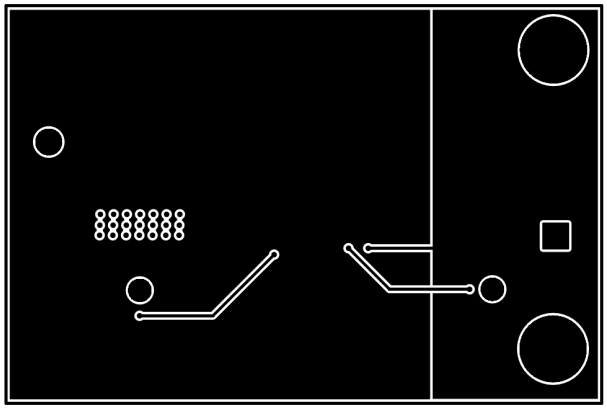

Figure 5-3. Mid-Layer 2 Routing

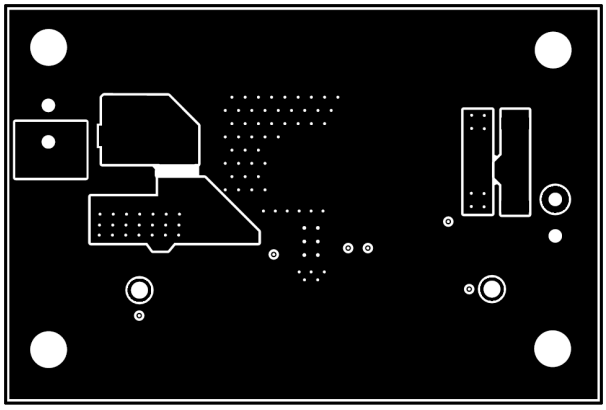

Figure 5-4. Bottom Layer Routing

6 Bill of Materials

Designator	Quantity	Description	PartNumber
C2, C11, C13	3	CAP, CERM, 0.1 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	HMK107B7104KAHT
C3	1	Chip Capacitor, 2.2 nF, +/- 10%, 50 V, -55 to 125 degC, 0402 (1005 Metric), RoHS, Tape and Reel	GRM155R71H222KA01D
C4	1	CAP, CERM, 3300 pF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CEU3E2X7R2A332K080AE
C5, C6	2	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	CL32B226KAJNFNE
C7	1	CAP, AL, 33 uF, 100 V, +/- 20%, 0.7 ohm, AEC-Q200 Grade 2, SMD	EEE-FK2A330P
C8, C9	2	CAP, CERM, 4.7 uF, 100 V, +/- 10%, X7S, 1210	C3225X7S2A475K200AE
C10, C12	2	CAP, CERM, 4.7 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1210	CGA6M3X7S2A475K200AB
C16	1	Cap Ceramic 56pF 50V C0G 5% SMD 0402 125C Paper T/R	CL05C560JB5NNNC
D1	1	Diode Schottky 120V 8A 3-Pin(2+Tab) SMPC T/R	V8P12-M3/86A
J1, J2	2	Terminal Block, 3.5mm Pitch, 2x1, TH	ED555/2DS
L1	1	22µH Shielded Molded Inductor 3.5A 74mOhm Max Nonstandard	74437368220
L2	1	Ferrite Bead, 220 ohm @ 100 MHz, 4 A, 1206	FBMH3216HM221NTV
L3	1	Shielded Power Inductors	XGL4020-822MEC
R2	1	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP
R4	1	RES, 453 k, 1%, 0.1 W, 0603	RC0603FR-07453KL
R5	1	RES, 1.00 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021M00FKED
R6	1	RES, 330 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402330KFKED
R7	1	RES, 102 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402102KFKED
R8	1	RES, 453 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402453KFKED
R9	1	RES, 49.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040249K9FKED
R10	1	RES, 100 k, 1%, 0.063 W, 0402	RC1005F104CS
TP1, TP2	2	Test Point, Multipurpose, White, TH	5012
U1	1	100-V Input, 3.5-A Non-Synchronous Buck DC/DC Converter with Ultra-low IQ	LM5013QDDARQ1
C1	0	CAP, CERM, 56 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A560JA01D
C14, C15	0	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1210	TMK325B7226KMHT
C17	0	Chip Capacitor, 100 pF, +/- 10%, 50 V, -55 to 125 degC, 0402 (1005 Metric), RoHS, Tape and Reel	C1005C0G1H101K050BA
R1, R3	0	RES, 1.00, 0.5%, 0.1 W, 0603	RT0603DRE071RL

7 Performance Curves

For performance curves, in addition to those shown in Figure 7-1, please visit LM5013-Q1 data sheet's application section. Applications curves would be taken on LM5013-Q1 EVM unless otherwise specified.

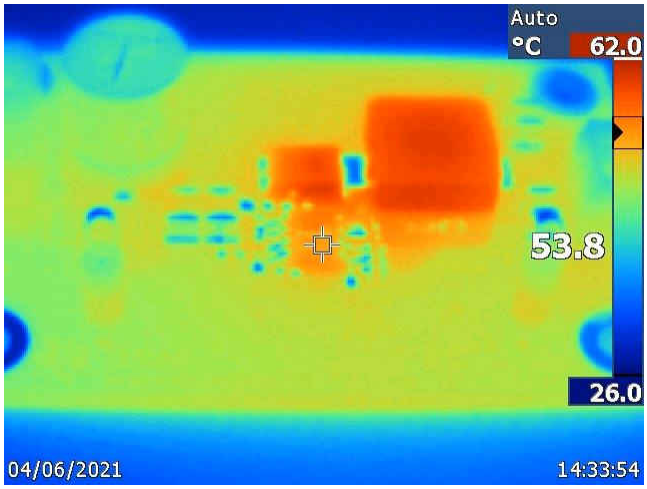

Figure 7-1. Thermal Capture of EVM: V_{IN} = 48-V, V_{OUT} = 12-V, I_{OUT}= 1.5-A

Note the design was optimized for small size and as a result, the thermal performance of the EVM does not reflect expected system performance with larger copper area. If continuous evaluation is to be done at higher input voltage, load current, or both, a fan must be used to make sure the IC does not hit its thermal limit.

Ensure the hot temperature identifiers are noticed on the PCB and care is taken in the handling of the PCB.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2021) to Revision A (November 2021)	Page
• Updated Section 4	8
• Updated Section 7	11

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