Product Bulletin

AC7 ADSL Infrastructure Chipset

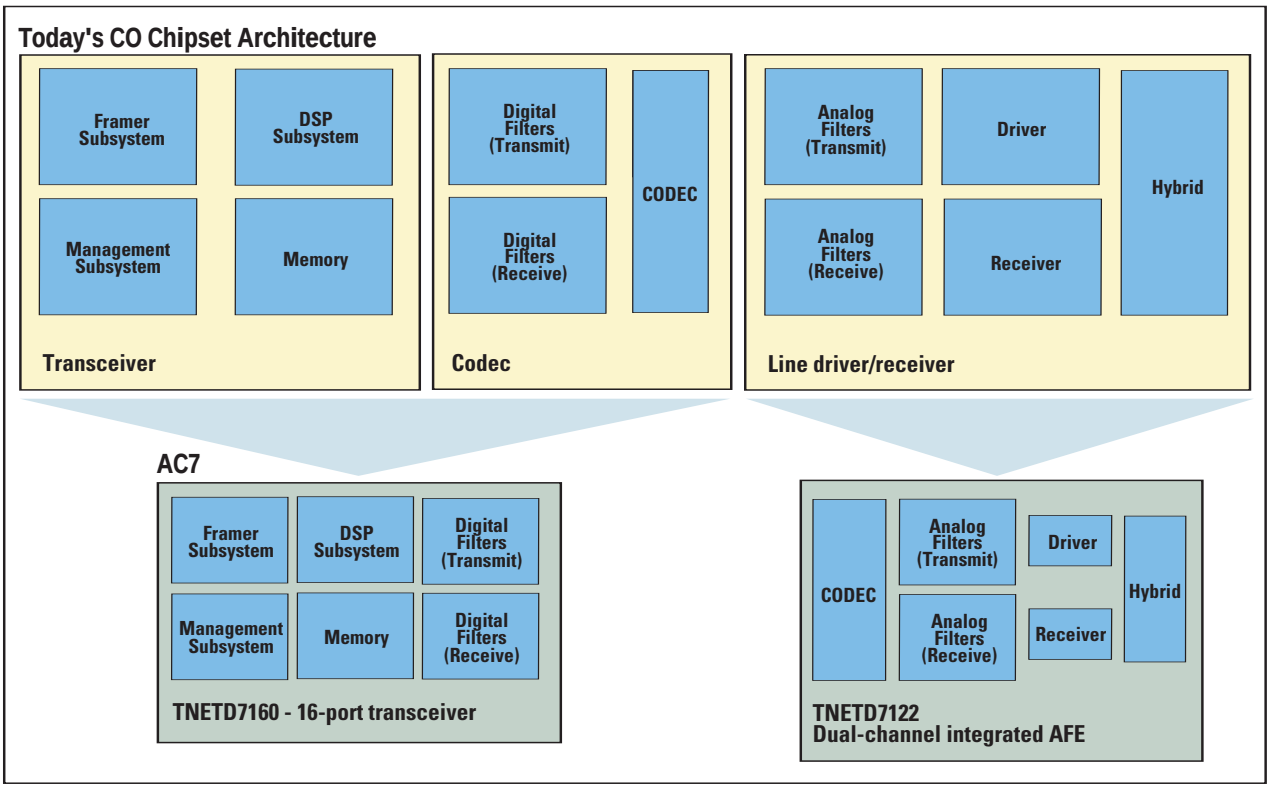
The 16-port AC7 Infrastructure chipset from Texas Instruments (TI) supports all new ADSL standards and establishes a new baseline of integration that enables a much lower system cost—two key considerations for next-generation DSLAMs, IP-DSLAMs, mini-DSLAMs, and DLCs.

The AC7 offers manufacturers low power per port operation compared to competitive solutions. This translates into significantly improved cabinet-level power consumption and dissipation, overall system quality reliability, and network level electricity usage.

Through complete ownership of the DSL signal chain, TI has established a new system architecture that offers distinct cost advantages versus current three-chip solutions. By integrating the traditional codec functionality, the AC7 is a true two-chip solution. By eliminating all cumbersome and noise prone analog signal traces between chipset devices, AC7

Key Features

- 16-port, two-chip design significantly reduces component count, stream lining layout and manufacturing
- "Any Service/Any Port" architecture protects existing ADSL installed base with support of current standards while also supporting the latest ADSL2, ADSL2+, enhanced upstream and extended reach standards
- Two-chip solution integrates all intra-chipset analog signal traces to reduce PCB costs and simplify board layout
- AC7 reduces bill-of-materials (BOM) costs by eliminating the number of devices needed when compared to competitive solutions



simplifies board designs and layouts and reduces overall PCB costs.

Unmatched Interoperability

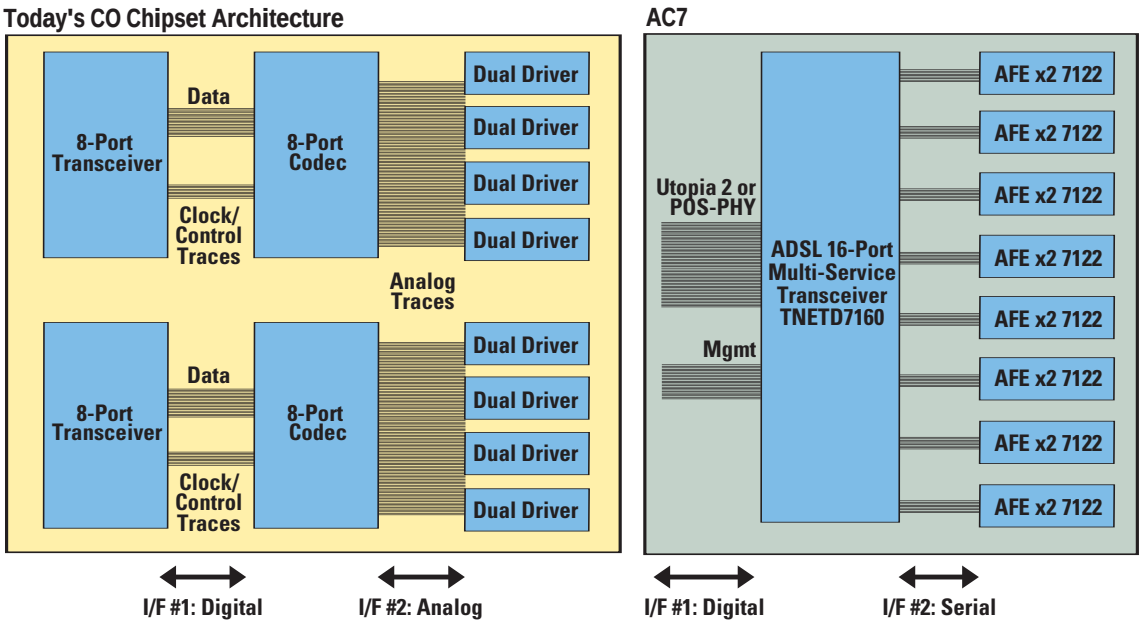
Since the beginning of the ADSL market, TI has built a solid reputation for industry leading interoperability performance. The significant investments TI has made in the capital equipment needed to establish a leading interoperability lab and the extensive man-hours devoted to testing and pre-qualification of its chipsets helps manufacturers achieve the best possible interoperability performance, enhancing network qualification success.

The cumulative effect of the many years that TI has devoted to ADSL interoperability is an extensive database of knowledge and human expertise that is readily applied to new generations of ADSL infrastructure technology. As such, the AC7 leverages this expertise as well as the experience gained from shipping over 50 million ports worldwide.

Development Support

The support provided with the AC7 accelerates the development process and shortens a new system's time-to-market. The full package of support includes an evaluation board, reference design, a hardware design kit (HDK) and a software design kit (SDK).

TI also offers a full range of brick and discrete board-level power solutions that are specifically matched to support the AC7 chipset in typical configurations. This reduces the development time for customers to bring a complete board to market.



AC7 Hardware Design Kit

- Design manual
- Application notes
- Datasheets
- Schematics in OrCAD™ and PDF files
- Layout example in PowerPCB™, Gerber and PDF files
- Example splitter design for Annex A
- Full bill of materials
- Evaluation module (EVM) motherboard reference schematics
- Boundary scan (JTAG) diagnostics files for Annex A

AC7 Software Design Kit

- Management access users guide
- Management presentation
- Management port interface example code
- Description and example code source files
- OAM code module
- Software release notes
- Modem diagnostic code module
- Modem datapump code

Devices in the AC7 Chipset

TNETD7160 ADSL Transceiver

The TNETD7160 embeds an ARM7 processor for all real-time modem operation and maintenance (OAM) control, extensively uses TI programmable DSP capability for transceiver training and steady-state functions, and includes all necessary program, data, interleaver memory, and interprocessor communications paths to reduce bill-of-materials costs. Each modem port can be configured dynamically to support ADSL, ADSL2, ADSL2+ (up to 24 Mbps), extended reach and enhanced upstream (up to 3.5 Mbps) with the same software load.

- Single chip integrates all digital functions for 16 Asymmetric Digital Subscriber Line (ADSL) ATU-C modems including digital section of the codec function
- Supports:
  - 16 ADSL modems
  - ANSI T1.413, Issue 2
  - ITU-T G.992.1 G.dmt (s=1/2 framing)
  - ITU-T G.992.3 G.dmt.bis (ADSL2–Annex A)
  - ITU-T G.992.3 (Annex I, J, M) Enhanced Upstream
  - ITU-T G.992.3 (Annex L) Extended Reach
  - ITU-T G.992.5 (ADSL2+ –Annex A)
  - ITU-T G.992.5 (Annex M) Enhanced Upstream
  - ITU-T G.994.1 G.hs
  - ITU-T G.997.1 G.ploam
  - ADSL2 Packet transfer mode (PTM)
  - ADSL2+ s=1/4 framing
- Data interfaces include:
  - UTOPIA 2
  - Packet over Sonet (POS-PHY)
- Optional in-band management eliminates need for local microcontroller
- Glueless interface to TNETD7122 dual channel AFE line interface
- On chip:
  - ARM processor and memory
  - Interleaving memory compliant to all ANSI and ITU standards
  - Two bit error rate tester (BERT) modules
- OAM register interface compatible with AC5 and AC6 for easy software migration
- Operating free-air temperature range -40°C to 85°C
- Packaged in a 480-terminal ball grid array with 1-mm Pitch for easy mounting

TNETD7122 Dual Channel Analog Front End (AFE)

The TNETD7122, used in plain old telephone service (POTS) implementations, is a dual low-power differential ADSL central-office (CO) front end containing line driver/receiver, codec, analog filters and hybrid used in conjunction with the TNETD7160. These devices feature active-termination drivers that eliminate the matching resistors required with traditional ADSL line drivers. The transmitter and receiver have full-bandwidth access, allowing for SELT/DELT capability and line characterization. The selectable integrated hybrid optimizes performance over different loop impedances.

- Designed for use with TNETD7160
- Integrates codec functionality to reduce chip count
- Low-power dual-channel zero-overhead Class-G design
- ±5-V power rails
- Active termination differential driver/receiver
- Bypassable filters allow full bandwidth access for SELT/DELT
- Programmable integrated hybrid for enhanced upstream performance
- Multiple power-saving modes to support L0–L3 ITU specifications
- 64-terminal PowerPAD™ Plastic Quad Flatpack (PAP)

For More Information

For more information on the AC7 ADSL infrastructure chipset, please contact the local TI field sales office or visit www.ti.com/ac7

TI Worldwide Technical Support

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TI Semiconductor KnowledgeBase Home Page
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