Product Bulletin

IP Phone Solution

TNETV1001

Texas Instruments' TNETV1001 IP Phone Solution is comprised of an integrated silicon platform, featuring the market leading programmable DSP, an ARM processor and a dual Ethernet interface combined with the market leading Telogy Software™ for Voice over IP (VoIP).

TI's IP phone solution leverages the success of the widely deployed TI silicon architecture for wireless phones; a low power, low cost platform supporting rapid implementation of differentiated features.

One of the unique features of our IP phone solution is the accompanying starter's kit. The starter's kit includes the software development license, software training and complete IP phone reference design for immediate demonstration and development.

Telogy Software™ for IP Phone Applications

Telogy Software provides an efficient framework for real-time voice processing that has been pre-integrated and thoroughly tested. The complete DSP solution features include PCM reception, tone generation, acoustic echo suppression/cancellation, voice activity detection, voice playout, and a variety of voice compression options. The solutions are provided in several packages to allow customization for a full range of phone products.

The Telogy microprocessor software, along with third party components, offers a toolkit with a variety of functions to support enterprise IP phone implementations. This includes voice applications services that access DSP services and support APIs necessary for implementation of call processing features. Sample code for device drivers and network management is provided. Additional packages include full signaling services with standard network protocols, H.323, MGCP and Megaco. Figure 1 shows the IP phone software architecture.

The Basic IP phone product provides the functionality required for today's typical desktop speaker phones. It includes acoustic echo suppression and a low bit rate codec. The Deluxe product is intended for executive phone implementations. The Deluxe product includes all of the features of the Basic product *plus* acoustic echo cancellation for full duplex speakerphone capability, three way conferencing and a wideband codec. All products include RTOS run-time licenses.

Silicon Solution

The TNETV1001 IP phone solution includes the TI C54xx based programmable DSP for optimal IP phone voice processing and signal processing features. The ARM processor provides a standard based RISC architecture for customer ease in feature development and integration with Telogy Software services. The Dual Ethernet MAC provides support for IP phone and PC connectivity to the Ethernet LAN.

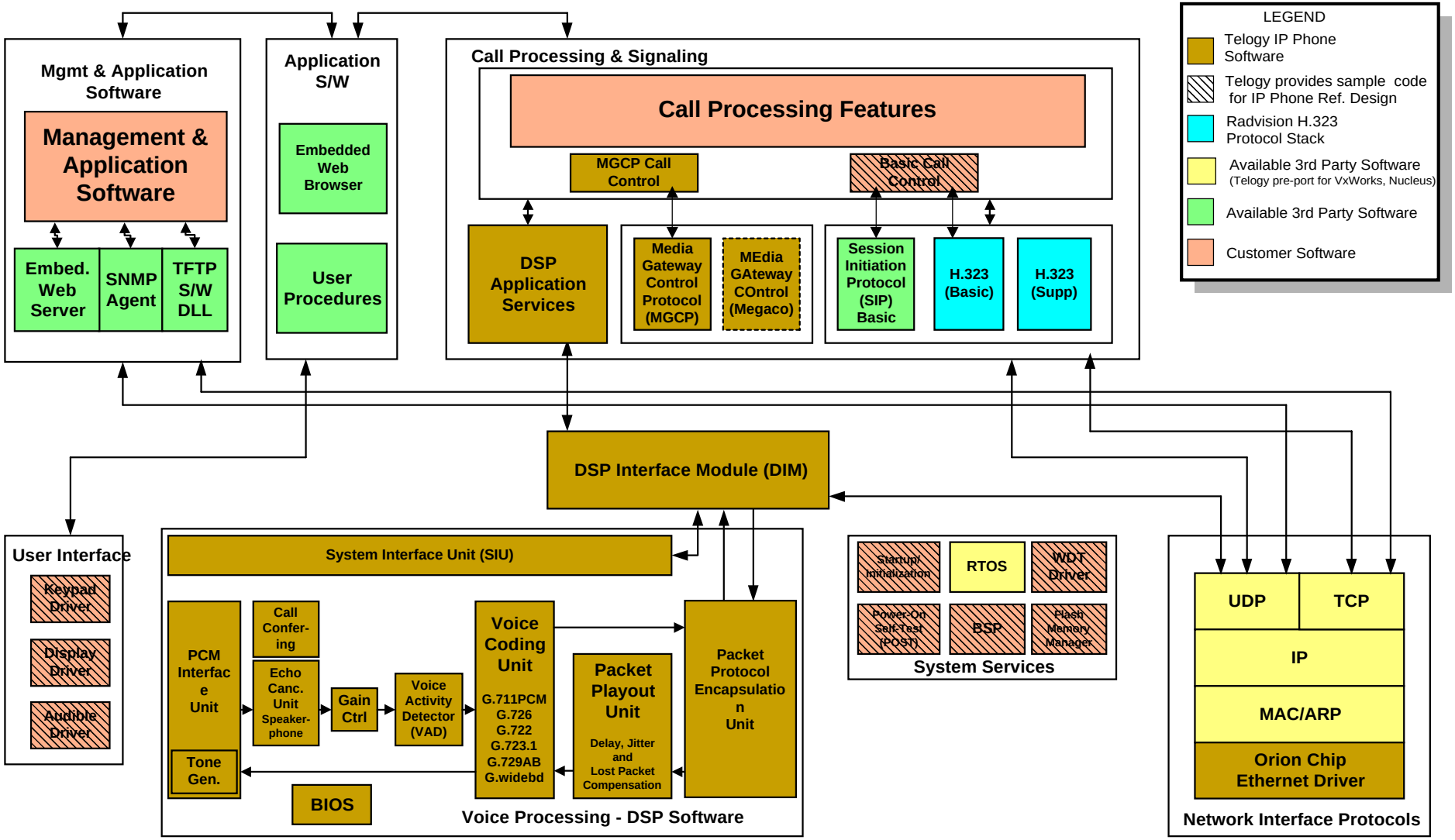
Key Benefits

- Optimal silicon/software platform supporting a variety of IP phone solutions
- Rapid implementation of customer unique features and services
- Field proven software with emphasis on QOS, interoperability, and remote monitoring
- Most comprehensive range of features
- Largest installed base of solutions
- Industry leader in DSP
  - Committed roadmap
  - Code compatibility
  - Process technology
  - Production facilities
- World class technical support
- Industry leader in indemnification with broad patent portfolio

The TNETV1001 silicon integrates a TMS320C54x™ DSP subsystem with its program and data memories (all RAM) and a RISC Micro-Controller core with emulation facilities (ARM7). A dual port Ethernet 10/100 Base-T interface is supported for connection to the Ethernet physical layer (PHY) via two MII interfaces (Media Independent Interface).

- The V1001 implements all features for the structural

Figure 1: IP Phone Software Architecture

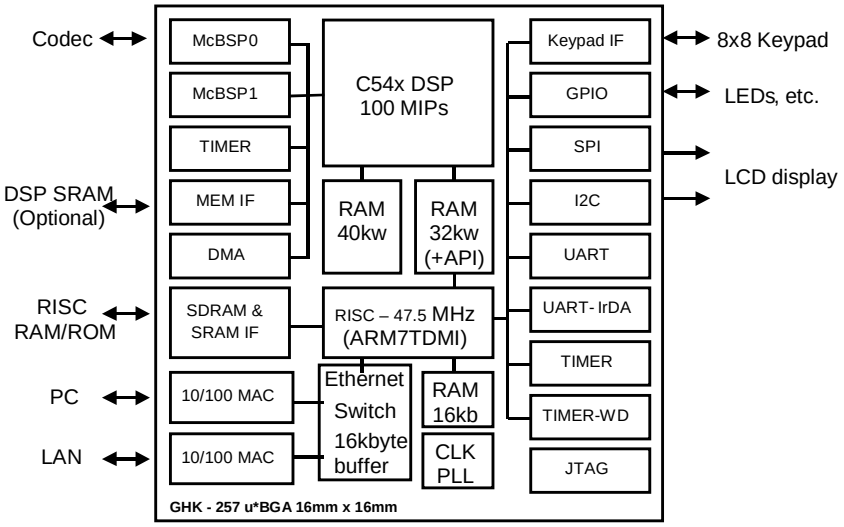


test of the logic (full scan, built in self- test, parallel multiplexed test, JTAG boundary scan). This device is implemented in 0.18μm (L_{eff}) CMOS technology. The nominal supply voltage for the device core logic is 1.8V; it is 3.3V for I/O.

The V1001 includes the following features:

- Dual CPU processor integrating TMS320C54x™ DSP core and an ARM7TDMI RISC MCU
- DSP - 100MHz, low power, TMS320C54x™ 16-bit core with 72k × 16 on-chip SRAM
- DSP on-chip Peripherals
  - Two high-speed, full-duplex multi-channel buffered serial ports (McBSPs) allowing the DSP core to interface directly with codecs and other devices in the system.
  - A six-channel Direct Memory Access (DMA) Controller enabling six independent block transfers with no intervention from the CPU.
  - ARM Port Interface shared memory interface for efficient information exchange between the ARM and the DSP CPUs.
  - External Memory Interface.
  - Software Programmable Wait-State Generator capable of extending external bus cycles by up to fourteen machine cycles.
  - One independent software programmable Hardware Timer for control operations.
- RISC – 47.5MHz ARM7TDMI Micro-Controller core with 16kByte on-chip SRAM.
- RISC Peripherals.
  - Dual port Ethernet Interface Module with two 10/100Mbps IEEE 802.3 Ethernet MACs
  - Universal Asynchronous Receiver/Transmitter (UART) compatible with NS 16C750 compliant devices
  - NS 16C750 compliant UART/IrDA interface allowing the connection through an infra-red transmitter to any external data peripherals using the Slow Infra-Red (SIR) protocol
  - Serial Port Interface (SPI™)
  - 36 general purpose I/O pins configurable in read or write mode by internal registers
  - I^2C Interface connecting ARM to I^2C compliant devices
  - 3 on-chip MCU Timers (one timer configurable as a Watchdog by default and two general purpose timers)
  - Interrupt Handler managing prioritized and maskable interrupts for both internal modules and external devices
  - Memory Interface between ARM CPU and its internal peripherals, external Flash and SRAM memories
  - SDRAM Memory Interface between the ARM CPU and external SDRAM memories
  - Clock Management Module controlling clock generation and activity for the DSP, MCU and peripherals
- JTAG (Joint Test Action Group) interface
- Ice Crusher module for emulation of both the DSP and RISC CPUs
- 257-pin 16mm x16mm Plastic Ball Grid Array (MicroStar BGA) Packaging
- Smart Power Management and Low-Power Modes:
  - DSP Low-Power Mode
  - ARM Low-Power Mode
  - Peripherals Low-Power Mode
- Advanced high-performance 0.18μm (L_{eff}) CMOS Technology
- 1.8V normal supply voltage for device core logic
- 3.3V normal supply voltage for device I/O

Figure 2: The C5472 Functional Block Diagram



IP Phone Processor Software Product Specifications

BASIC AND DELUXE FEATURES – MICROPROCESSOR
IP Phone Platform
DSP Interface Module
Voice Applications Services
APIs to access DSP Services
APIs needed to setup DSP for basic and supplementary services
APIs to generate inband tones
Sample Display and Keypad Drivers
Sample Network Management Module
VxWorks and Nucleus RTOS support
RTOS Run-Time licenses provided with complete solution.
Development and any related tools must be obtained via RTOS vendors
Signaling Services Package (In addition to the IP Phone Platform features above)
Sample Basic Call Control
Supports setup of basic calls
MGCP Protocol - Basic call support
OR
H.323 Protocol support - Stack available via Radvision, third party partner

** Please consult your sales representative for latest product features and availability.

Specifications: Telogy Software™ for IP Phone Processor

BASIC PHONE FEATURES - DSP
PCM Voice Mode
G.711 Codec
Gain Control
Transmit and Receive ranging from –14dB to 14dB
Voice Activity Detection
Adaptive Voice Activity Detection (VAD)
Configurable Hangover Period
Useable with any Codec (disabled w/ codec internal VAD)
Bi-Directional Silence Detection
Silence Insertion Descriptor (SID) Support
Voice Playout
Noise Level Matching
Adaptive Pink Comfort Noise Generation
Configurable, Adaptive Jitter Buffer
Lost Packet Compensation
Echo Cancellation
Acoustic Echo Suppression for Half Duplex Speakerphone
Doubletalk Detection
Packet Protocol
VoIP (RTP) Packet Format
Real Time Diagnostics
PCM Pattern Detection
Signal Level Measurement and Report
Jitter Statistics
Transmit, Receive, Lost Packet Counts
Loopback Mode
Codec Options*
G.711 Codec plus G.729AB (CS-ACELP) Codec or G.723.1A Codec
Advanced Power Management
ADDITIONAL DELUXE FEATURES
3-Way Conferencing
Codec Options
Deluxe Solution includes G.711 plus choice of two of the following codecs; G.729AB (CS-ACELP) Codec ,G.723.1A Codec or G.722 Wideband Codec
Full Duplex Speakerphone Support
G.167 Acoustic Echo Cancellation**

* A single low bit rate codec may be utilized with the product in addition to the G.711 PCM.

** Please consult your sales representative for latest product features and availability.

General Description of the V1001

The V1001 is composed of the following modules:

DSP Sub System
TMS320C54x™ DSP core with 72k words (16-bit) of RAM data/program.
DSP peripherals:
ARM Port Interface
2 McBSPs (Multi-channel Buffered Serial Port)
PLL (Phase-Locked Loop)
Timer
DMA (Direct Memory Access Controller)
Programmable Wait State Generator
External Memory Interface
RISC Micro-Controller ARM7
ARM7TDMI CPU core (32/16 bit RISC processor) + ARM IceCrusher for emulation purposes
ARM peripherals:
ARM Memory Interface for external SRAM, Flash or ROM and SDRAM.
On-chip 16kByte (32 x 4096) zero wait-state SRAM.
ARM General Purpose I/Os with 8x8 keyboard interface.
3 Timers (2 generic, 1 watchdog)
UART 16C750 interface (UART_IRDA) with
– IRDA control capabilities (SIR)
– supports only the SW flow control (UART mode)
UART 16C750 interface (UART) with
– hardware flow protocol (DCD, CTS/RTS)
– autobaud function
ARM Interrupt Handler (INTH).
Clock generator & control (CLKM)
Dual port Ethernet 10/100Base-T Interface (EIM)
I^2C “master-only” interface (I2C)
SPI interface
OTHER peripherals:
JTAG TAP controller.

Telogy Software is a trademark of Texas Instruments
For more information please contact your TI sales representative or call 301-515-8580.
www.ti.com/voip