Migrating from Sandstorm-Class to Fury-Class Stellaris® Microcontrollers

Application Note

Texas Instruments

Copyright

Texas Instruments
108 Wild Basin, Suite 350
Austin, TX 78746
Main: +1-512-279-8800
Fax: +1-512-279-8879
http://www.luminarymicro.com

Table of Contents

Introduction

This application note provides existing users of the Stellaris® family of microcontrollers a summary of differences between existing and new members of the family.

The existing members of the family are part of the Stellaris Sandstorm class, and the new members of the family are part of the Stellaris Fury class of microcontrollers.

The new Fury class of devices introduces many new features and interfaces, including:

■ 10/100 Mb/s Ethernet with integrated PHY

■ Controller area network (CAN)

■ IrDA support for the UARTs

■ Additional instances of existing interfaces (UART, SSI, I2C, and QEI)

■ Improved power management

For more information on these new interfaces, refer to the Fury device data sheets. The scope of this application note covers changes to the system features with which an existing user is already familiar, as well as other key changes.

This document covers the following differences between the classes of devices:

■ Identifying the new devices from existing devices

■ Reset sequence differences

■ Pin differences

■ Register differences

Device Identification

Devices are easily identified visually. All new Stellaris family devices are packaged in 100-pin LQFP packages and are marked with a four-digit part number of the form LM3S*nnnn*, where *nnnn* is the part number. This includes the devices listed in Table 1-1.

Table 1-1. Stellaris Fury-class devices

LM3S2110	LM3S2620	LM3S2948	LM3S6422	LM3S6938
LM3S2139	LM3S2637	LM3S2950	LM3S6432	LM3S6952
LM3S2410	LM3S2651	LM3S2965	LM3S6610	LM3S6965
LM3S2412	LM3S2730	LM3S6100	LM3S6633	
LM3S2432	LM3S2739	LM3S6110	LM3S6637	
LM3S2533	LM3S2939	LM3S6420	LM3S6730	

The existing members are packaged in either a 28-pin SOIC package or a 48-pin LQFP package and are marked with a three-digit part number of the form LM3S*xxx*, where *xxx* is the part number. This includes the devices listed in Table 1-2.

Table 1-2. Stellaris Sandstorm-class devices

LM3S101	LM3S315	LM3S601	LM3S613	LM3S628	LM3S815
LM3S102	LM3S316	LM3S610	LM3S615	LM3S801	LM3S817
LM3S301	LM3S317	LM3S611	LM3S617	LM3S811	LM3S818
LM3S310	LM3S328	LM3S612	LM3S618	LM3S812	LM3S828

The device is identified in software via the Device Identification 0 (**DID0**) register. The two classes of devices differ in two fields of the **DID0** register: the VER field and the CLASS field.

■ The VER field provides software an indication of the format version of the register. Existing devices use the initial version of the register; therefore, the VER field value is 0. New members use a modified format; therefore, the VER field value is 1.

■ The CLASS field is defined in the new format and is intended to serve as a means to distinguish the classes within the family. The CLASS field value for the Sandstorm devices is 0. The CLASS field value for the Fury devices is 1.

Note that the new format of the **DID0** register is backwards-compatible with the initial format. The new field, CLASS, is created from reserved bits whose reserved value matches the class of the existing devices.

Hibernation Module

Some Fury class of devices add a new, optional, power-saving mode that improves battery-powered operation. This module provides three interfaces:

■ A battery-power input (VBAT) that is automatically switched with VDD. The higher supply provides power to the hibernation module.

■ An oscillator interface. A 4.194301-MHz crystal can be attached and a 32.768-kHz clock is internally derived by dividing the crystal frequency by 128. Alternatively, a 32.768-kHz oscillator may be directly connected to the input pin.

■ A two-pin power-control interface (see "$\overline{\text{HIB}}$" and "$\overline{\text{WAKE}}$" on page 9). Note that the oscillator must be attached and enabled in order for this interface to function.

Reset Differences

Boot Clock

Out of power-on reset, the Fury class of devices boot internally from the internal oscillator (IOSC). Unlike Sandstorm class devices, the microcontroller does not power up the main oscillator (MOSC) during a power-on reset sequence. Rather, the new devices require firmware to enable the MOSC source for applications that require the time accuracy the MOSC source provides.

The reset state of the **RCC** register is different in the Fury class of devices. In particular, the MOSCDIS bit is set and the OSCSRC field is set to the value 1 (use IOSC) as the result of a power-on reset.

Enabling the MOSC source is accomplished using the following steps:

1. Write the value 0 into the **RCC** register MOSCDIS bit.

2. Write the value 0 into the **RCC** register OSCSRC field. The value 0 selects the MOSC as the source of oscillator reference for the device.

This change requires a small change to the reset sequence of existing software in order to function on the new devices.

GPIO Reset

In the Sandstorm class of devices, the power-on reset state of most[1] GPIO pins is as an enabled input with the weak pull up device enabled. The Fury class of devices initialize the GPIO pins differently, resulting in an undriven (tristate) pin; the digital function of the pin is disabled and the pull up is not enabled.

The difference is in the reset value of two registers:

Table 1-3. GPIO Pin Reset Value

Class	GPIOPUR	GPIODEN
Sandstorm	1 (ENABLED)	1 (ENABLED)
Fury	0 (DISABLED)	0 (DISABLED)

To use the GPIO pins in a digital capacity, the GPIO pins must, therefore, have their corresponding **GPIODEN** register's DEN bit set before they may be used. Note that this is true if the GPIO pin operates as *an input or an output*. The DEN bit should not be set when using the pin as an analog comparator input.

The Stellaris peripheral driver library (PDL) GPIO module contains functions that configure a GPIO pin for operation as a specified peripheral. These functions configure the specified GPIO pins for operation for both classes of device, and their use is highly encouraged. This includes the function calls:

■ GPIOPinTypeComparator()

■ GPIOPinTypeI2C()

■ GPIOPinTypePWM()

■ GPIOPinTypeQEI()

---

1. The exception is the GPIO pins that involve the JTAG/SWD functions. These GPIOs are configured per the debug interface's functionality requirements.

- GPIOPinTypeSSI()

- GPIOPinTypeTimer()

- GPIOPinTypeUART()

- GPIOPinTypeGPIO()

Hibernate/Wake-Up Check

If the system uses hibernate mode, in the power-on-reset handler the Reset Cause (**RESC**) register does not provide enough information to indicate that the power-on reset sequence is due to a first-time sequence or a sequence due to a wake-up event. The distinction may be important to system software that must restore state.

Following a wake event, the **RESC** register indicates the power-on reset by setting the POR bit. This should be further qualified by first checking the hibernation module is active by checking the **HIBCTL** register CLK32EN bit is set, and then checking the hibernation module's **HIBMIS** register's value. If the **HIBMIS** register value is non-zero, the hibernation module generated a wake-up event.

The Stellaris peripheral driver library (PDL) GPIO module provides a function, HibernateIsActive(), that returns the active status of the hibernation module.

Pin and Hardware Differences

The Fury class introduces some additional system hardware and control pins. These must be correctly connected in order for the microcontroller to operate correctly. This section provides detail with regard to these new pins.

Power

The Fury class devices provide some enhancements to the Sandstorm class devices.

VDD/GND

Additional VDD/GND pin pairs improved noise immunity.

Core Power and the LDO Regulator

The largest change with respect to power connectivity between the classes in the way that the core power is supplied to the devices. In the Sandstorm class, the core power is connected internally with a single pin that provides a mechanism for decoupling. In most Sandstorm class devices, the internal low-dropout (LDO) regulator is connected directly to the internal power grid.

In the Fury class, the internal LDO regulator does not connect directly to the internal core power grid. Instead, the output of the LDO regulator is connected to the LDO pin. The LDO pin is connected to the VDD25 pins that then connects to the internal core power grid. Figure 1 shows the differences between these two methods.

The advantages of the Fury-class method are:

■ Better power distribution

■ Customers may supply their own externally adjustable regulators—provided that the core voltage specifications are met

Figure 1. Core Power

Fury Class of Devices

Sandstorm Class of Devices
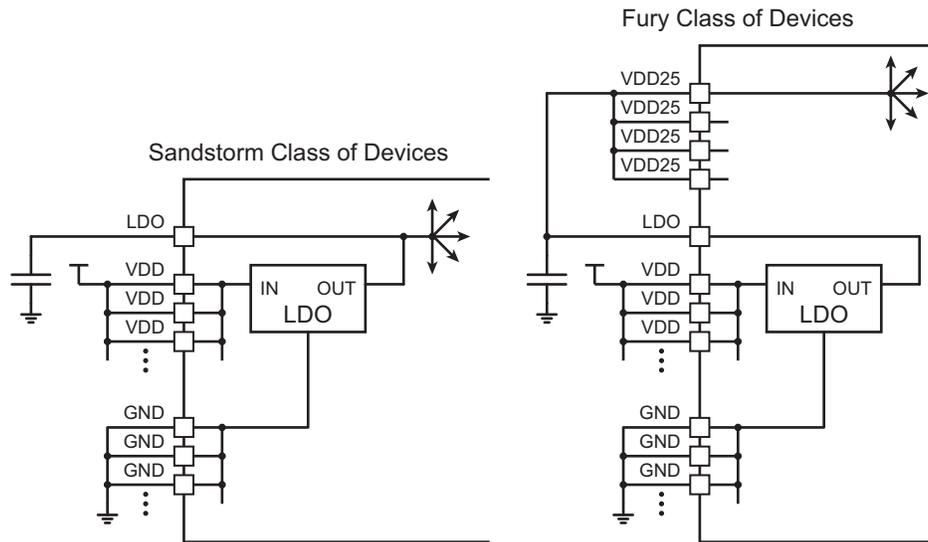
Analog power and ground
The Fury class of devices separates the analog circuitry power input from the input/output (VDD) power input. Two pairs of analog power and ground pins, VDDA and GNDA respectively, are added.

These pins may be used, depending on the application's electrical environment, to reduce noise in the analog components of the device by filtering the analog power supply. Otherwise, they should be connected directly to VDD and GND respectively.

Test Mode Control
Two pins, CMOD0 and CMOD1, are defined for use by Texas Instruments for testing the devices during manufacture. They have no end-user function and should not be used. The CMOD pins should be connected to ground.

Hibernation Module
The Fury class of devices introduces an optional, aggressive low-power mode, called hibernate mode, that is intended to provide the capability of running the microcontroller from battery power for extended periods of time. During this time, the majority of the microcontroller is unpowered. A small amount of hardware provides a mechanism to save state and re-establish powered operation. The hibernation module provides 256 bytes of non-volatile memory, a real-time clock, and a power control interface. The real-time clock and power control interface are both capable of bringing the microcontroller out of hibernate mode and back to run mode through a power-on reset sequence.

VBAT

In applications that use hibernate mode, the VBAT pin connects to a 3-V battery or an auxillary power supply. The hibernation module's power is drawn from either the VDD pins or the VBAT pin based on the state of the microcontroller and the voltage applied to the VDD and VBAT pins.

If hibernate mode is not used, the real-time clock logic in the hibernation module may still be used, provided that the VBAT pin is connected to a 3.3-V source on the circuit board. Otherwise, the VBAT pin may be disconnected.

Note that if VBAT is connected, the voltage level of VBAT should be lower than VDD otherwise the hibernation module will consume VBAT current before VDD current. The hibernation module uses the higher of the VBAT or VDD supply in deciding which pin to draw power.

$\overline{\text{HIB}}$

The $\overline{\text{HIB}}$ pin is used to control the power provided to the microcontroller by connecting to the enable input of an external voltage regulator. The low power consumption of hibernate mode is achieved only when the power supplied to the device is turned off.

$\overline{\text{HIB}}$ is driven by an open-drain driver, and asserts (low) when the microcontroller enters hibernate mode, and remains asserted for the duration. The assertion of $\overline{\text{HIB}}$ pulls the enable input of the voltage regulator low, turning it off. When $\overline{\text{HIB}}$ is not asserted, the voltage regulator enable input is pulled high through a resistor connected to the voltage regulator's input, turning it on. The power-on reset state of $\overline{\text{HIB}}$ is deasserted. Figure 2 shows the connection between the $\overline{\text{HIB}}$ pin and an external voltage regulator.

Figure 2. $\overline{\text{HIB}}$ to External Voltage Regulator Connection
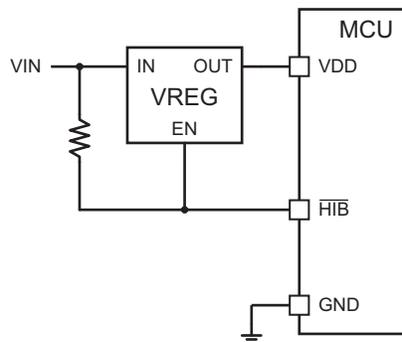
$\overline{\text{WAKE}}$

The $\overline{\text{WAKE}}$ pin is used by external circuitry to signal the hibernation module interface to restore power to the microcontroller and initiate a power-on sequence. This is accomplished by asserting $\overline{\text{WAKE}}$ (low).

XOSC0/XOSC1

These pins are the real-time clock oscillator interface. They may be connected either a crystal or a single-ended clock source.

The crystal option uses the following components: a 4.194304-MHz crystal and parallel 1-MΩ resistor connected across the pins and compensation capacitors connected from each pin to ground.

The single-ended option uses a 32.768-kHz clock source driven into the XOSC0 pin.

A real-time clock circuit is provided for optional use in periodically generating interrupts (if not hibernating) or genreating wake-up events (if hibernating) based on programmable match registers. See the product data sheet for additional details.

Note that in order to use the $\overline{\text{HIB}}/\overline{\text{WAKE}}$ interface, the oscillator must be enabled since the oscillator is used in the hibernation module's circuitry as the clock source.

Register Differences

There are a number of changes made regarding existing registers or new registers.

System Control Registers

This section details changes made to system control registers.

DID0 Register

As outlined in a previous section, the Device Identification 0 (**DID0**) register is updated. The VER field has changed to reflect the definition of a new CLASS field.

DID1 Register

The Device Identification 1 (**DID1**) register includes changes to the following fields:

■ VER field is updated to the value 1 to reflect the changes to the register format.

■ The PKG field is redefined. In the Sandstorm class of devices, the PKG field is a two-bit field that indicates the package type and number of package pins. In the Fury class of devices, the PKG field indicates only the package type. Currently two encodings are provided: one for SOIC and one for LQFP.

■ A new PINCOUNT field is provided to encode the number of pins present on the package. Currently, the defined encodings support 28, 48, and 100 pins.

RCC Register and the New RCC2 Register

The **RCC** register is unchanged in the Fury class of devices. However; a new register, **RCC2**, is defined to override some of the fields of the **RCC** register.

If the **RCC2** register's USERCC2 bit is set, all defined fields in the **RCC2** register override their **RCC** register counterparts. Register fields that exist in the **RCC** register that are not defined in the **RCC2** register are unaffected.

The specific fields and bits defined in the **RCC2** register are as follows:

■ USERCC2—If set, the **RCC2** register fields are used instead of their counterparts in the **RCC** register.

■ SYSDIV2—This field provides an increase in the number of system clock divisors. The maximum system clock divisor increases from 16 to 64. The minimum system clock divisor is unchanged at 4.

■ PWRDN2—This bit behaves exactly as the **RCC** register PWRDN bit.

■ BYPASS2—This bit behaves exactly as the **RCC** register BYPASS bit.

■ OSCSRC2—This field provides additional oscillator source options. In particular, this field adds the options of using the low-speed internal 30-kHz oscillator and the hibernation module's 32.768-kHz oscillator.

The PWRDN2 and BYPASS2 bits are present so that all PLL function may be modified in a single register access, rather than having to modify both the **RCC** and **RCC2** registers.

PLLCFG Register
The PLL was changed from the Sandstorm class of devices to the Fury class. Accordingly, the **PLLCFG** register generates different values.

The PLL frequency of a Sandstorm class device is calculated using the PLLCFG field values, as follows:

$$PLLFreq = OSCFreq * (F + 2) / (R + 2);$$

The PLL frequency of a Fury class device is calculated using the PLLCFG field values, as follows:

$$PLLFreq = OSCFreq * F / (R + 1);$$

The PDL function SysCtlClockGet() function returns the correct PLL VCO frequency regardless of the class of device being used.

Peripheral Driver Library Support

The Stellaris® peripheral driver library (PDL) is a set of drivers for controlling the peripherals found on the Stellaris family, as well as providing support in managing the changes to the affected registers. The PDL is shipped as part of Stellaris evaluation and development kits and available as a free download from the http://www.luminarymicro.com web site.The use of the code, either directly or as an example incorporated in other software, is encouraged. The PDL functions are intended for use across devices and provide an additional layer of compatibility.

Conclusion

The new Fury class devices introduce important new capabilities to the Stellaris family of ARM® Cortex™-M3 microcontrollers, including CAN, Ethernet MAC and PHY, more serial interfaces (UARTs, I^{2}C, and SSI/SPI), and more GPIO. Knowing the differences outlined in this application note, users of existing Stellaris microcontrollers can easily and rapidly take advantage of the new capabilities in their applications.

The latest version of the PDL is available for download from the http://www.luminarymicro.com/products/software_updates.html web site.

References

Documents used in the generation of this application note include:

■ Stellaris® microcontroller data sheet, Publication Number DS-LM3S*nnn* (where *nnn* is the part number for that specific Stellaris family device)

■ StellarisWare® Driver Library, Order number SW-DRL

■ *StellarisWare® Driver Library User's Manual*, publication number SW-DRL-UG

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		