User's Guide
LMK3H2104A10 Register Map

TEXAS INSTRUMENTS

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Read This First

About This Manual

This document is the configuration summary and register guide specific to the LMK3H2104A10 configuration. For the configuration summaries of the other LMK3H2104xyy configurations, refer to the appropriate configuration addendum on the LMK3H2104 product page.

Fields that are marked as read-only can differ from the default values listed.

Notational Conventions

This document uses the following conventions.
- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

Related Documentation

For more information about usage of the LMK3H2104 device, please refer to the LMK3H2104 and LMK3H2108 data sheet.

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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1 Configuration Overview

1.1 LMK3H2104A10 Configuration Information

Table 1-1. Frequency Configuration

OTP Page	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	REF0 (MHz)	REF1 (MHz)
OTP Page 0	24	24	24	50	50	50
OTP Page 1	24	24	24	50	50	50
OTP Page 2	24	24	24	50	50	50
OTP Page 3	24	24	24	50	50	50

Table 1-2. I2C Configuration

OTP Page	I2C Configuration
OTP Page 0	I2C Address: 0x68 1 Byte Register Adderssing
OTP Page 1	I2C Address: 0x68 1 Byte Register Adderssing
OTP Page 2	I2C Address: 0x68 1 Byte Register Adderssing
OTP Page 3	I2C Address: 0x68 1 Byte Register Adderssing

OTP Page 0

Table 1-3. GPI Settings, OTP Page 0

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled

Table 1-4. GPIO Settings, OTP Page 0

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-5. Input Settings, OTP Page 0

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC

Table 1-6. Output Settings, OTP Page 0

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT1	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT2	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT3	50	In-Phase LVCMOS	PATH1	Enabled	No OE Group	Disabled
REF0	50	N/A	PATH1	Enabled	No OE Group	Disabled
REF1	50	N/A	PATH1	Enabled	No OE Group	Disabled

OTP Page 1

Table 1-7. GPI Settings, OTP Page 1

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled

Table 1-8. GPIO Settings, OTP Page 1

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-9. Input Settings, OTP Page 1

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC

Table 1-10. Output Settings, OTP Page 1

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	24	In-Phase LVCMOS	PATH0	Disabled	No OE Group	Disabled
OUT1	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT2	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT3	50	In-Phase LVCMOS	PATH1	Enabled	No OE Group	Disabled
REF0	50	N/A	PATH1	Enabled	No OE Group	Disabled
REF1	50	N/A	PATH1	Enabled	No OE Group	Disabled

OTP Page 2

Table 1-11. GPI Settings, OTP Page 2

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled

Table 1-12. GPIO Settings, OTP Page 2

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-13. Input Settings, OTP Page 2

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC

Table 1-14. Output Settings, OTP Page 2

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT1	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT2	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT3	50	In-Phase LVCMOS	PATH1	Disabled	No OE Group	Disabled
REF0	50	N/A	PATH1	Enabled	No OE Group	Disabled
REF1	50	N/A	PATH1	Disabled	No OE Group	Disabled

OTP Page 3

Table 1-15. GPI Settings, OTP Page 3

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Enabled	Disabled
GPI1	GPI	Normal	Enabled	Disabled
GPI2	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled

Table 1-16. GPIO Settings, OTP Page 3

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Alternate OE, Alternate Mapping 1	Normal	Enabled	Disabled
GPIO1	GPI	Normal	Enabled	Disabled

Table 1-17. Input Settings, OTP Page 3

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	N/A (IN0 Unused)	None, DC

Table 1-18. Output Settings, OTP Page 3

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	24	In-Phase LVCMOS	PATH0	Disabled	No OE Group	Disabled
OUT1	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT2	24	In-Phase LVCMOS	PATH0	Enabled	No OE Group	Disabled
OUT3	50	In-Phase LVCMOS	PATH1	Disabled	No OE Group	Disabled
REF0	50	N/A	PATH1	Enabled	No OE Group	Disabled
REF1	50	N/A	PATH1	Disabled	No OE Group	Disabled

2 Device Register Map

Table 2-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 2-1 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. Register Map

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
0x0	R0	VENDOR_ID[7:0]							
0x1	R1	VENDOR_ID[15:8]							
0x2	R2	RES	FLOAT_VDDO_3	FLOAT_VDDO_2	FLOAT_VDDO_1	FLOAT_VDDO_0	RES		OTP_BURNT
0x3	R3	RES					OTP_SEL_1_PU_RB	OTP_SEL_0_PU_RB	RES
0x4	R4	RES					REF0_CTRL_PU_RB	RES	
0x5	R5	RES					OTP_PAGE_SEL_DYN_DEBOUNCE	RES	
0x6	R6	I2C_REG_ADDR_FMT	I2C_TRGT_ADDR						
0x8	R8	PWRGD_SAMPLE_TMR							
0x9	R9	RES	SUP_LVL_RAMP_TMR						PWRGD_SAMPLE_TMR_EN
0xA	R10	GLOBAL_SUP_DET_TMR							
0xB	R11	FOD0_PD	BAW_PD	AUTO_FOD_PD_EN	CRC_IGNORE	PIN_RESAMPLE_DIS	OTP_AUTOLOAD_DIS	PDN	GLOBAL_SUP_DET_TMR_EN
0xC	R12	RES						IN0_PD	FOD1_PD
0xD	R13	PWRGD_PWRDN_PIN_SEL				RES			
0xE	R14	RES				GPI0_FUNC			
0xF	R15	RES				GPI1_FUNC			
0x10	R16	RES				GPI2_FUNC			
0x11	R17	RES			OE_GLOBAL	RES			
0x15	R21	RES				GPIO0_FUNC			
0x19	R25	RES				GPIO1_FUNC			
0x1A	R26	RES				GPIO0_OUT_SRC_SEL			
0x1C	R28	RES	GPI2_POLARITY	GPI1_POLARITY	GPI0_POLARITY	GPIO1_OUT_SRC_SEL			
0x1D	R29	GPI0_PULL_DN_EN	GPIO1_POLARITY	RES			GPIO0_POLARITY	RES	
0x1E	R30	RES	GPI2_PULL_UP_EN	GPI2_PULL_DN_EN	RES		GPI1_PULL_UP_EN	GPI1_PULL_DN_EN	GPI0_PULL_UP_EN
0x1F	R31	RES	GPIO0_PULL_UP_EN	GPIO0_PULL_DN_EN	RES				
0x20	R32	RES	GPIO1_PULL_UP_EN	GPIO1_PULL_DN_EN	RES				
0x21	R33	RES	GPI2_LIVE_RB	GPI1_LIVE_RB	GPI0_LIVE_RB	RES			
0x22	R34	RES				GPIO0_LIVE_RB		RES	
0x23	R35	RES	GPIO1_GPO_VAL	RES			GPIO0_GPO_VAL	GPIO1_LIVE_RB	RES
0x24	R36	RES		GPI1_OE_GRP_SEL			GPI0_OE_GRP_SEL		
0x25	R37	RES					GPI2_OE_GRP_SEL		

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	7	6	5	4	3	2	1	0
0x27	R39	RES						GPIO0_OE_GRP_SEL	
0x29	R41	GPIO1_OUT_SIG_TYPE	RES			GPIO0_OUT_SIG_TYPE	GPIO1_OE_GRP_SEL		
0x2A	R42	RES							IN0_RCVR_FMT
0x2B	R43	RES						IN0_TERMINATION_SEL	
0x2C	R44	RES	IN0_LOS_THRESH	RES		IN0_LOS_EN	RES		
0x2D	R45	PERST_BUF_IN0_STS	RES					PERST_BUF_IN0	RES
0x2E	R46	RES					PERST_BUF_IN0_LOS_EN	RES	
0x2F	R47	RES	FOD0_N_DIV						
0x30	R48	RES	FOD1_N_DIV						
0x31	R49	FOD0_NUM[7:0]							
0x32	R50	FOD0_NUM[15:8]							
0x33	R51	FOD0_NUM[23:16]							
0x34	R52	FOD1_NUM[7:0]							
0x35	R53	FOD1_NUM[15:8]							
0x36	R54	FOD1_NUM[23:16]							
0x37	R55	FOD1_CFG_UPDATE	FOD0_CFG_UPDATE	PATH1_DIV			PATH0_DIV		
0x39	R57	RES	FOD_PH_OFFSET_N_DIV						
0x3A	R58	FOD_PH_OFFSET_NUM[7:0]							
0x3B	R59	FOD_PH_OFFSET_NUM[15:8]							
0x3C	R60	RES	FOD0_SSC_CONFIG_SEL			FOD0_SSC_MOD_TYPE	FOD0_SSC_EN	FOD_PH_OFFSET_FOD_SEL	FOD_PH_OFFSET_SHIFT_NOW
0x3D	R61	FOD0_SSC_STEPS[7:0]							
0x3E	R62	RES			FOD0_SSC_STEPS[12:8]				
0x3F	R63	FOD0_DCO_STEP_SIZE[7:0]							
0x40	R64	FOD0_DCO_STEP_SIZE[15:8]							
0x41	R65	RES			FOD1_SSC_CONFIG_SEL			FOD1_SSC_MOD_TYPE	FOD1_SSC_EN
0x42	R66	FOD1_SSC_STEPS[7:0]							
0x43	R67	RES			FOD1_SSC_STEPS[12:8]				
0x44	R68	FOD1_DCO_STEP_SIZE[7:0]							
0x45	R69	FOD1_DCO_STEP_SIZE[15:8]							
0x46	R70	RES		FOD1_DCO_DEC	FOD1_DCO_INC	FOD1_DCO_EN	FOD0_DCO_DEC	FOD0_DCO_INC	FOD0_DCO_EN
0x47	R71	FOD0_DCO_STEPS_STAT[7:0]							
0x48	R72	FOD0_DCO_STEPS_STAT[15:8]							
0x49	R73	FOD1_DCO_STEPS_STAT[7:0]							
0x4A	R74	FOD1_DCO_STEPS_STAT[15:8]							
0x4B	R75	RES	FOD0_DCO_N_DIV_STAT						
0x4C	R76	FOD0_DCO_NUM_STAT[7:0]							

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4D	R77	FOD0_DCO_NUM_STAT[15:8]							
0x4E	R78	FOD0_DCO_NUM_STAT[23:16]							
0x4F	R79	RES	FOD1_DCO_N_DIV_STAT						
0x50	R80	FOD1_DCO_NUM_STAT[7:0]							
0x51	R81	FOD1_DCO_NUM_STAT[15:8]							
0x52	R82	FOD1_DCO_NUM_STAT[23:16]							
0x53	R83	BANK1_CLK_SEL			BANK0_CLK_SEL			PATH1_EDGE_COMB_EN	PATH0_EDGE_COMB_EN
0x54	R84	RES		BANK3_CLK_SEL			BANK2_CLK_SEL		
0x55	R85	RES		BANK5_CLK_SEL			BANK4_CLK_SEL		
0x56	R86	BANK0_CH_DIV[7:0]							
0x57	R87	BANK0_CH_DIV[15:8]							
0x58	R88	BANK2_CH_DIV				BANK1_CH_DIV			
0x59	R89	RES							IN0_LOS
0x5A	R90	BANK4_CH_DIV				BANK3_CH_DIV			
0x5B	R91	PERST_BUF_BANK1		PERST_BUF_BANK0		BANK5_CH_DIV			
0x5C	R92	PERST_BUF_BANK5		PERST_BUF_BANK4		PERST_BUF_BANK3		PERST_BUF_BANK2	
0x5D	R93	BANK1_AUTO_CLK_SWITCHBACK_EN	BANK0_AUTO_CLK_SWITCHBACK_EN	BANK5_AUTO_CLK_SWITCHOVER_EN	BANK4_AUTO_CLK_SWITCHOVER_EN	BANK3_AUTO_CLK_SWITCHOVER_EN	BANK2_AUTO_CLK_SWITCHOVER_EN	BANK1_AUTO_CLK_SWITCHOVER_EN	BANK0_AUTO_CLK_SWITCHOVER_EN
0x5E	R94	BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK5_AUTO_CLK_SWITCHBACK_EN	BANK4_AUTO_CLK_SWITCHBACK_EN	BANK3_AUTO_CLK_SWITCHBACK_EN	BANK2_AUTO_CLK_SWITCHBACK_EN
0x5F	R95	BANK5_CLK_SWITCHOVER_TYPE	BANK4_CLK_SWITCHOVER_TYPE	BANK3_CLK_SWITCHOVER_TYPE	BANK2_CLK_SWITCHOVER_TYPE	BANK1_CLK_SWITCHOVER_TYPE	BANK0_CLK_SWITCHOVER_TYPE	BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL	BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL
0x60	R96	BANK1_SWITCHOVER_FRC_CLK_EN	BANK0_SWITCHOVER_FRC_CLK_EN	BANK5_CLK_DIS_ON_LOS	BANK4_CLK_DIS_ON_LOS	BANK3_CLK_DIS_ON_LOS	BANK2_CLK_DIS_ON_LOS	BANK1_CLK_DIS_ON_LOS	BANK0_CLK_DIS_ON_LOS
0x61	R97	OUT1_SLEW_RATE		OUT0_SLEW_RATE		BANK5_SWITCHOVER_FRC_CLK_EN	BANK4_SWITCHOVER_FRC_CLK_EN	BANK3_SWITCHOVER_FRC_CLK_EN	BANK2_SWITCHOVER_FRC_CLK_EN
0x62	R98	OUT3_SLEW_RATE		OUT2_SLEW_RATE		RES			
0x63	R99	OUT1_CMOS_SLEW_RATE		OUT0_CMOS_SLEW_RATE		RES			
0x64	R100	OUT3_CMOS_SLEW_RATE		OUT2_CMOS_SLEW_RATE		RES			
0x65	R101	OUT1_DIS_STATE		OUT0_DIS_STATE		RES			
0x66	R102	OUT3_DIS_STATE		OUT2_DIS_STATE		RES			
0x67	R103	OUT0_FMT		REF1_DIS_STATE	REF0_DIS_STATE	RES			
0x68	R104	OUT2_FMT			RES			OUT1_FMT	
0x69	R105	RES							IN1_LOS
0x6A	R106	OUT1_CMOS_1P2V_EN	OUT0_CMOS_1P2V_EN	RES				OUT3_FMT	
0x6B	R107	RES				OUT3_CMOS_1P2V_EN	OUT2_CMOS_1P2V_EN	RES	
0x6C	R108	OUT1_OE_GRP				OUT0_OE_GRP			
0x6E	R110	OUT3_OE_GRP				OUT2_OE_GRP			
0x6F	R111	REF1_OE_GRP				REF0_OE_GRP			

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	7	6	5	4	3	2	1	0
0x70	R112	OUT1_LPHCSL_VOD_SEL				OUT0_LPHCSL_VOD_SEL			
0x72	R114	OUT3_LPHCSL_VOD_SEL				OUT2_LPHCSL_VOD_SEL			
0x74	R116	RES				OUT1_SYNC_MODE		OUT0_SYNC_MODE	
0x75	R117	REF1_SYNC_MODE		REF0_SYNC_MODE		OUT3_SYNC_MODE		OUT2_SYNC_MODE	
0x76	R118	RES			OUT1N_OE_CMOS	OUT1P_OE_CMOS	OUT0N_OE_CMOS	OUT0P_OE_CMOS	SINGLE_CMOS_EN_SYNC
0x77	R119	RES			OUT3N_OE_CMOS	OUT3P_OE_CMOS	OUT2N_OE_CMOS	OUT2P_OE_CMOS	RES
0x78	R120	RES	OUT3_FREQ_DET_EN	OUT2_FREQ_DET_EN	RES		OUT1_FREQ_DET_EN	OUT0_FREQ_DET_EN	RES
0x7A	R122	OUT2_FREQ_DET_THRESH	RES		OUT1_FREQ_DET_THRESH	OUT0_FREQ_DET_THRESH	REF1_FREQ_DET_EN	REF0_FREQ_DET_EN	RES
0x7B	R123	RES	OUT1_AMP_DET_EN	OUT0_AMP_DET_EN	REF1_FREQ_DET_THRESH	REF0_FREQ_DET_THRESH	RES		OUT3_FREQ_DET_THRESH
0x7C	R124	OUT_AMP_DET_THRESH	RES				OUT3_AMP_DET_EN	OUT2_AMP_DET_EN	RES
0x7D	R125	CRC_ERROR_EVT_INTR_EN	RES		IN0_LOS_LMT_EVT_INTR_EN	RES		IN0_LOS_EVT_INTR_EN	DEV_INTR
0x7E	R126	RES				OUT1N_FREQ_ERR_EVT_INTR_EN	OUT1P_FREQ_ERR_EVT_INTR_EN	OUT0N_FREQ_ERR_EVT_INTR_EN	OUT0P_FREQ_ERR_EVT_INTR_EN
0x7F	R127	RES				OUT3N_FREQ_ERR_EVT_INTR_EN	OUT3P_FREQ_ERR_EVT_INTR_EN	OUT2N_FREQ_ERR_EVT_INTR_EN	OUT2P_FREQ_ERR_EVT_INTR_EN
0x80	R128	RES		OUT1N_AMP_ERR_EVT_INTR_EN	OUT1P_AMP_ERR_EVT_INTR_EN	OUT0N_AMP_ERR_EVT_INTR_EN	OUT0P_AMP_ERR_EVT_INTR_EN	REF1_FREQ_ERR_EVT_INTR_EN	REF0_FREQ_ERR_EVT_INTR_EN
0x81	R129	RES		OUT3N_AMP_ERR_EVT_INTR_EN	OUT3P_AMP_ERR_EVT_INTR_EN	OUT2N_AMP_ERR_EVT_INTR_EN	OUT2P_AMP_ERR_EVT_INTR_EN	RES	
0x82	R130	RES			IN0_LOS_EVT	RES			
0x83	R131	RES			IN0_LOS_CNTR				
0x84	R132	LOS_LMT				RES			
0x85	R133	OUT0N_FREQ_GOOD	OUT0P_FREQ_GOOD	CRC_ERROR_EVT	CRC_ERROR	CRC_DONE	RES		IN0_LOS_LMT_EVT
0x86	R134	OUT2N_FREQ_GOOD	OUT2P_FREQ_GOOD	RES				OUT1N_FREQ_GOOD	OUT1P_FREQ_GOOD
0x87	R135	REF1_FREQ_GOOD	REF0_FREQ_GOOD	RES				OUT3N_FREQ_GOOD	OUT3P_FREQ_GOOD
0x88	R136	RES				OUT1N_FREQ_ERR_EVT	OUT1P_FREQ_ERR_EVT	OUT0N_FREQ_ERR_EVT	OUT0P_FREQ_ERR_EVT
0x89	R137	RES				OUT3N_FREQ_ERR_EVT	OUT3P_FREQ_ERR_EVT	OUT2N_FREQ_ERR_EVT	OUT2P_FREQ_ERR_EVT
0x8A	R138	RES		OUT1N_AMP_GOOD	OUT1P_AMP_GOOD	OUT0N_AMP_GOOD	OUT0P_AMP_GOOD	REF1_FREQ_ERR_EVT	REF0_FREQ_ERR_EVT
0x8B	R139	RES		OUT3N_AMP_GOOD	OUT3P_AMP_GOOD	OUT2N_AMP_GOOD	OUT2P_AMP_GOOD	RES	
0x8C	R140	OUT1N_AMP_ERR_EVT	OUT1P_AMP_ERR_EVT	OUT0N_AMP_ERR_EVT	OUT0P_AMP_ERR_EVT	RES			
0x8D	R141	OUT3N_AMP_ERR_EVT	OUT3P_AMP_ERR_EVT	OUT2N_AMP_ERR_EVT	OUT2P_AMP_ERR_EVT	RES			
0x8F	R143	RES				PROD_REV_ID			

Table 2-1. Register Map (continued)

Offset (Hex)	Register Acronym	Bit							
		7	6	5	4	3	2	1	0
0x90	R144	OTP_ID							
0x93	R147	UNLOCK_PROTECTED_REG							
0x94	R148	RES				VDDD_SUP_LVL_DET_RB		VDDA_SUP_LVL_DET_RB	
0x95	R149	VDDO_3_SUP_LVL_DET_RB		VDDO_2_SUP_LVL_DET_RB		VDDO_1_SUP_LVL_DET_RB		VDDO_0_SUP_LVL_DET_RB	
0x96	R150	RES		VDD_REF_SUP_LVL_DET_RB		RES			
0xBB	R187	CRC_COMPUTED							
0xBC	R188	RES						BOOTOSC_CLK_DIS	RES
0xFD	R253	RES						PAGE_SEL_0	
0x13F	R319	RES							CLK_READY
0x240	R576	RES							OUT0_DIS
0x244	R580	RES							OUT1_DIS
0x250	R592	RES							OUT2_DIS
0x254	R596	RES							OUT3_DIS
0x258	R600	RES							REF0_DIS
0x25C	R604	RES							REF1_DIS
0x270	R624	RES						PATH1_FOD_SEL	RES
0x2E9	R745	RES	OUT1P_INV_POL	OUT0P_INV_POL	RES				
0x2EA	R746	RES	OUT1N_INV_POL	OUT0N_INV_POL	RES		OUT3P_INV_POL	OUT2P_INV_POL	RES
0x2EB	R747	RES					OUT3N_INV_POL	OUT2N_INV_POL	RES
0x2FA	R762	DIE_ID_1[7:0]							
0x2FB	R763	RES	DIE_ID_1[14:8]						
0x2FC	R764	DIE_ID_2[7:0]							
0x2FE	R766	DIE_ID_2[15:8]							
0x2FF	R767	DIE_ID_3[7:0]							
0x300	R768	DIE_ID_3[15:8]							
0x301	R769	RES							ALTERNATE_OE_SEL
0x302	R770	STORED_CRC							

3 Device Registers

Table 3-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. DEVICE Registers

Offset	Acronym	Register Name
0x0	R0	
0x1	R1	
0x2	R2	
0x3	R3	
0x4	R4	
0x5	R5	
0x6	R6	
0x8	R8	
0x9	R9	
0xA	R10	
0xB	R11	
0xC	R12	
0xD	R13	
0xE	R14	
0xF	R15	
0x10	R16	
0x11	R17	
0x15	R21	
0x19	R25	
0x1A	R26	
0x1C	R28	
0x1D	R29	
0x1E	R30	
0x1F	R31	
0x20	R32	
0x21	R33	
0x22	R34	
0x23	R35	
0x24	R36	
0x25	R37	
0x27	R39	
0x29	R41	
0x2A	R42	
0x2B	R43	
0x2C	R44	
0x2D	R45	
0x2E	R46	
0x2F	R47	
0x30	R48	
0x31	R49	
0x32	R50	
0x33	R51	
0x34	R52	

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name
0x35	R53	
0x36	R54	
0x37	R55	
0x39	R57	
0x3A	R58	
0x3B	R59	
0x3C	R60	
0x3D	R61	
0x3E	R62	
0x3F	R63	
0x40	R64	
0x41	R65	
0x42	R66	
0x43	R67	
0x44	R68	
0x45	R69	
0x46	R70	
0x47	R71	
0x48	R72	
0x49	R73	
0x4A	R74	
0x4B	R75	
0x4C	R76	
0x4D	R77	
0x4E	R78	
0x4F	R79	
0x50	R80	
0x51	R81	
0x52	R82	
0x53	R83	
0x54	R84	
0x55	R85	
0x56	R86	
0x57	R87	
0x58	R88	
0x59	R89	
0x5A	R90	
0x5B	R91	
0x5C	R92	
0x5D	R93	
0x5E	R94	
0x5F	R95	
0x60	R96	
0x61	R97	
0x62	R98	
0x63	R99	
0x64	R100	

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name
0x65	R101	
0x66	R102	
0x67	R103	
0x68	R104	
0x69	R105	
0x6A	R106	
0x6B	R107	
0x6C	R108	
0x6E	R110	
0x6F	R111	
0x70	R112	
0x72	R114	
0x74	R116	
0x75	R117	
0x76	R118	
0x77	R119	
0x78	R120	
0x7A	R122	
0x7B	R123	
0x7C	R124	
0x7D	R125	
0x7E	R126	
0x7F	R127	
0x80	R128	
0x81	R129	
0x82	R130	
0x83	R131	
0x84	R132	
0x85	R133	
0x86	R134	
0x87	R135	
0x88	R136	
0x89	R137	
0x8A	R138	
0x8B	R139	
0x8C	R140	
0x8D	R141	
0x8F	R143	
0x90	R144	
0x93	R147	
0x94	R148	
0x95	R149	
0x96	R150	
0xBB	R187	
0xBC	R188	
0xFD	R253	
0x13F	R319	

Table 3-1. DEVICE Registers (continued)

Offset	Acronym	Register Name
0x240	R576	
0x244	R580	
0x250	R592	
0x254	R596	
0x258	R600	
0x25C	R604	
0x270	R624	
0x2E9	R745	
0x2EA	R746	
0x2EB	R747	
0x2FA	R762	
0x2FB	R763	
0x2FC	R764	
0x2FE	R766	
0x2FF	R767	
0x300	R768	
0x301	R769	
0x302	R770	

Complex bit access types are encoded to fit into small table cells. Table 3-2 shows the codes that are used for access types in this section.

Table 3-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

3.1 R0 Register (Offset = 0x0) [Reset = 0x8B]

R0 is shown in Table 3-3.

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Table 3-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID[7:0]	R	0x8B	Vendor ID, two bytes total. Complete Value: 0x038B

3.2 R1 Register (Offset = 0x1) [Reset = 0x03]

R1 is shown in Table 3-4.

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Table 3-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID[15:8]	R	0x3	Vendor ID, two bytes total. Complete Value: 0x038B

3.3 R2 Register (Offset = 0x2) [Reset = 0x00]

R2 is shown in Table 3-5.

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Table 3-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	FLOAT_VDDO_3	R/W	0x0	Float VDDO_3 Supply. Determines whether or not the VDDO_3 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT3. If not expected, the device will ignore the VDDO_3 pin. 0x0 = Used; The device assumes that VDDO_3 is present, and VDDO_3 must be connected for proper operation 0x1 = Floating; The device assumes that VDDO_3 is not present, and VDDO_3 may be floating (unconnected)
5	FLOAT_VDDO_2	R/W	0x0	Float VDDO_2 Supply. Determines whether or not the VDDO_2 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT2. If not expected, the device will ignore the VDDO_2 pin. 0x0 = Used; The device assumes that VDDO_2 is present, and VDDO_2 must be connected for proper operation 0x1 = Floating; The device assumes that VDDO_2 is not present, and VDDO_2 may be floating (unconnected)
4	FLOAT_VDDO_1	R/W	0x0	Float VDDO_1 Supply. Determines whether or not the VDDO_1 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT1. If not expected, the device will ignore the VDDO_1 pin. 0x0 = Used; The device assumes that VDDO_1 is present, and VDDO_1 must be connected for proper operation 0x1 = Floating; The device assumes that VDDO_1 is not present, and VDDO_1 may be floating (unconnected)
3	FLOAT_VDDO_0	R/W	0x0	Float VDDO_0 Supply. Determines whether or not the VDDO_0 power supply will be expected. If expected, the pin's supply level will be analyzed to determine when it is safe to enable OUT0. If not expected, the device will ignore the VDDO_0 pin. 0x0 = Used; The device assumes that VDDO_0 is present, and VDDO_0 must be connected for proper operation 0x1 = Floating; The device assumes that VDDO_0 is not present, and VDDO_0 may be floating (unconnected)
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	OTP_BURNT	R	0x0	Indicates whether or not the OTP has been programmed, and controls whether or not the OTP data will be loaded into the registers during the power-up sequence. Note: This field will be loaded from the OTP at power-up, regardless of the value of OTP_BURNT.

3.4 R3 Register (Offset = 0x3) [Reset = 0x00]

R3 is shown in Table 3-6.

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Table 3-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OTP_SEL_1_PU_RB	R	0x0	OTP_SEL_1 Pin Power-up Value Readback 0x0 = Low 0x1 = High
1	OTP_SEL_0_PU_RB	R	0x0	OTP_SEL_0 Pin Power-up Value Readback 0x0 = Low 0x1 = High
0	RESERVED	R	0x0	Reserved

3.5 R4 Register (Offset = 0x4) [Reset = 0x00]

R4 is shown in Table 3-7.

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Table 3-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	REF0_CTRL_PU_RB	R	0x0	REF0_CTRL Pin Power-up Value Readback 0x0 = Low 0x1 = High
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.6 R5 Register (Offset = 0x5) [Reset = 0x00]

R5 is shown in Table 3-8.

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Table 3-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OTP_PAGE_SEL_DYN_DEBOUNCE	R/W	0x0	OTP Page Selection (Dynamic) Debounce Interval. Sets the amount of time that all dynamic OTP page selection pins must be stable before the device responds to a level change on any dynamic OTP page selection pin. Once all active dynamic OTP page selection pins have been stable for the selected amount of time, the resulting OTP Page Selection Code is registered and the selected page is loaded into the device registers. Any dynamic OTP page selection pin level changes that occur between the expiration of the debounce interval and completion of OTP autoload will be ignored until OTP autoload finishes. If the registered OTP Page Selection Code matches the current OTP Page Selection Code (for example, a short pulse was observed on the pin) or if the registered OTP Page Selection Code is invalid, no OTP autoload will occur. 0x0 = 133ns 0x1 = 4.2us
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.7 R6 Register (Offset = 0x6) [Reset = 0x68]

R6 is shown in Table 3-9.

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Table 3-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_REG_ADDR_FMT	R/W	0x0	I2C Register Address Format. Selects between 1-Byte Addressing and 2-Byte Addressing. In 1-Byte Addressing, only one byte of register address (the lower 8 bits) must be transmitted. The upper 2 bits are controlled by the PAGE_SEL_x register fields. In 2-Byte Addressing, two bytes of register address (all 10 bits) must be transmitted. The PAGE_SEL_x register fields are ignored. The required value of this field should be loaded from OTP. 0x0 = 1-Byte Addressing; The upper 2 bits of the register address must be written to the PAGE_SEL field. 0x1 = 2-Byte Addressing; The PAGE_SEL field is not used. Instead, all ten register bits are acces through two subsequent 8-bit I2C accesses.
6:0	I2C_TRGT_ADDR	R/W	0x68	I2C target address 7 bits, does not include R/W bit. This field is locked, and requires unlocking UNLOCK_PROTECTED_REG before using.

3.8 R8 Register (Offset = 0x8) [Reset = 0x00]

R8 is shown in Table 3-10.

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Table 3-10. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PWRGD_SAMPLE_TMR	R/W	0x0	PWRGD Function Sampling Timer. The value of this field sets the earliest time that the GPIO pin assigned with the PWRGD/PWRDN# function will be sampled for use with the PWRGD function. This timer exists to ensure that the pin is not sampled before it is stable. This timer starts once the voltages of both VDDA and VDDD reach 1.62V. When the timer expires, the value of the pin starts being evaluated for use with the PWRGD function. If PWRGD is asserted before the timer expires, the PWRGD function is seen to be asserted upon timer expiration. If PWRGD is asserted after the timer expires, the PWRGD function is seen to be asserted as the pin value changes. The timer is enabled/disabled using PWRGD_SAMPLE_TMR_EN. The timer is ignored if no pin is assigned with the PWRGD/PWRDN# function (for that case, see SUP_LVL_RAMP_TMR and GLOABL_SUP_DET_TMR). The timer duration, which can range from 0.1ms to 25.6ms, is configured using the following equation: PWRGD_SAMPLE_TMR = 10 * timer_duration (ms) - 1

3.9 R9 Register (Offset = 0x9) [Reset = 0x12]

R9 is shown in Table 3-11.

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Table 3-11. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:1	SUP_LVL_RAMP_TMR	R/W	0x9	Supply Level Ramp-up Timer. The value of this field controls the duration of the Supply Level Ramp-up Timer. For each power supply pin (VDDA, VDDD, VDDX, VDDR, VDDO_*, VDD_REF), a timer exists to ensure that the device does not begin operation until the power supply pin has ramped up to its final voltage. For each pin, this timer starts once the pin voltage reaches 1.62V. When the timer expires, the device assumes that the power supply is fully ramped up, and supply detection for that pin no longer gates device operation. The user must set this field according to the longest expected power supply ramp-up time, measured from 1.62V to the final voltage. This timer is ignored if a GPIO pin is assigned with the PWRGD/PWRDN# function (for that case, see PWRGD_SAMPLE_TMR). The timer duration, which can range from 0.1ms to 6.4ms, is configured using the following equation: SUP_LVL_RAMP_TMR = 10 * timer_duration (ms) - 1
0	PWRGD_SAMPLE_TMR_EN	R/W	0x0	PWRGD Function Sampling Timer Enable. When set to 0x1, the PWRGD Functrion Sampling Timer is used to delay sampling of the GPIO pin assigned with the PWRGD/PWRDN# function. See PWRGD_SAMPLE_TMR for further details. When set to 0x0, timer is not used, and the pin begins getting sampled immediately after pin functions are loaded from the OTP.

3.10 R10 Register (Offset = 0xA) [Reset = 0x2C]

R10 is shown in Table 3-12.

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Table 3-12. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GLOBAL_SUP_DET_TMR	R/W	0x2C	Global Supply Detect Timer. The value of this field controls the duration of the Global Supply Detect Timer. This timer exists to ensure that if one of the supply detect pins (VDDA, VDDD, VDDX, VDDR, VDDO_*, VDD_REF) fails to ramp up, the device will not hang. This timer starts once the voltages of both VDDA and VDDD reach 1.62V. Once all power supply pins that are expected to be used (FLOAT_VDDx == 0x0) reach 1.62V and their corresponding Supply Level Ramp-Up Timer expires, the device will begin all remaining power-up sequence steps and clocks will start. If this timer expires before that condition occurs, the device will stop waiting for power supply pins to ramp up, and the device will begin all remaining power-up sequence steps. While this prevents the device from hanging, it may result in unintended behavior. The user must set this field according to the longest allowable delay between core power supplies starting to ramp up, and the first output clocks starting. The timer is enabled/disabled using GLOBAL_SUP_DET_TMR_EN. This timer is ignored a GPIO pin is assigned with the PWRGD/PWRDN# function (for that case, see PWRGD_SAMPLE_TMR). The timer duration, which can range from 0.1ms to 25.6ms, is configured using the following equation: GLOBAL_SUP_DET_TMR = 10 * timer_duration (ms) - 1

3.11 R11 Register (Offset = 0xB) [Reset = 0x34]

R11 is shown in Table 3-13.

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Table 3-13. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FOD0_PD	R/W	0x0	FOD0 Power-Down. Setting this bit to 1 turns off power to FOD0. This can be used to reduce power consumption in configurations where FOD0 is not used. 0x0 = Powered Up; FOD0 is not powered down. 0x1 = Powered Down; If FOD0 is not needed (pure buffer mode operation), then FOD0 is powered down for current savings. In general, FOD0 should be used for clock generation from the BAW resonator if only one FOD is needed.
6	BAW_PD	R/W	0x0	BAW Power-Down. Setting this bit to 1 turns off power to the BAW. This can be used to reduce power consumption in configurations where the BAW is not used. 0x0 = Powered Up; The internal BAW resonator is not powered down. 0x1 = Powered Down; If the internal BAW resonator is not needed (pure buffer mode operation), then the BAW is powered down for current savings when setting this field to a 1. When powering off the BAW, both FODs should also be powered off.
5	AUTO_FOD_PD_EN	R/W	0x1	Automatic FOD Power-down Enable. When enabled, if an FOD is not selected as the source of any output clock or reference clock, that FOD will be automatically powered down. If an 0x0 = No; If an FOD is not used for any outputs, it will still be powered up (increasing current consumption and potentially FOD-FOD crosstalk) 0x1 = Yes; If an FOD is not used for any outputs, it will still be automatically powered down (reducing current consumption and potentially FOD-FOD crosstalk)
4	CRC_IGNORE	R/W	0x1	CRC Ignore. When set to 0x1 (default), if a CRC error is detected during OTP autoload, the CRC_ERROR status bit will be set, but the device will attempt to continue to power up normally with the loaded OTP data. When set to 0x0, if a CRC error is detected, the CRC_ERROR status bit will be set, and the device power-up sequence will stop. In this case, no output clocks will be generated. 0x0 = Halt; If there is a CRC error (CRC_ERROR set to 1), the device will halt the startup process. No output clocks will be generated. 0x1 = Ignore; If there is a CRC error (CRC_ERROR set to 1), it will be ignored, and the device will attempt to start up normally.
3	PIN_RESAMPLE_DIS	R/W	0x0	Pin Resample Disable. By default, when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), GPIO0, GPIO1, and GPIO2 are sampled. Each sampled value is used for OTP Page Selection (Power-Up) if the corresponding OTP_PAGE_SEL_PU_x register field is configured to use the GPIO pin. If this field has a value of 0x1 while exiting power-down mode, this pin re-sampling will not occur, and the last sampled values of the GPIO pins will be retained.
2	OTP_AUTOLOAD_DIS	R/W	0x1	OTP Autoload Disable. By default, when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), OTP data is loaded into the device registers; however, if OTP_AUTOLOAD_DIS has a value of 0x1 while exiting power-down mode, this data transfer will not occur. The OTP_AUTOLOAD_DIS register field has no effect on dynamic OTP page changes. When changing the device settings and doing a PDN toggle to recalibrate the FODs, this field should be written to a 1 before PDN is cleared to prevent reloading from OTP.

Table 3-13. R11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PDN	R/W	0x0	Power-Down. Writing this bit with 0x1, which is equivalent to asserting the PWRDN# pin, causes the device to enter a power-down mode. Writing this bit with 0x0, which is equivalent to deasserting the PWRDN# pin, casuse the device to exit power-down mode. The resulting behavior from entering/exiting power-down mode is defined by the PIN_RESAMPLE_DIS and OTP_AUTOLOAD_DIS register fields. When modifying the FOD divider values, TI recommends setting PDN to 1, setting OTP_AUTOLOAD_DIS to 1, then setting PDN to 0 to recalibrate the FODs for best performance.
0	GLOBAL_SUP_DET_TMR _EN	R/W	0x0	Global Supply Detect Timer Enable. When set to 0x1, the Global Supply Detect Timer is used to prevent the device from hanging if one of the power supply pins is slow to ramp up. See GLOBAL_SUP_DET_TMR for further details. When set to 0x0, timer is not used, and if a supply pin is slow to ramp up, the device will hang until it finishes ramping up.

3.12 R12 Register (Offset = 0xC) [Reset = 0x03]

R12 is shown in Table 3-14.

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Table 3-14. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	IN0_PD	R/W	0x1	IN0 Power-Down. Setting this bit to 1 turns off power to IN0. This can be used to reduce power consumption in configurations where IN0 is not used. 0x0 = Powered Up; IN_0 is not powered down. 0x1 = Powered Down; Setting this field to a 1 reduces power consumption in configurations where IN_0 is not used.
0	FOD1_PD	R/W	0x1	FOD1 Power-Down. Setting this bit to 1 turns off power to FOD1. This can be used to reduce power consumption in configurations where FOD1 is not used. 0x0 = Powered Up; FOD1 is not powered down. 0x1 = Powered Down; If FOD1 is not needed (pure buffer mode operation), then FOD1 is powered down for current savings. In general, FOD0 should be used for clock generation from the BAW resonator if only one FOD is needed.

3.13 R13 Register (Offset = 0xD) [Reset = 0xF0]

R13 is shown in Table 3-15.

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Table 3-15. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PWRGD_PWRDN_PIN_SEL	R/W	0xF	PWRGD/PWRDN# Pin Select. Selects which pin, if any, is used for the PWRGD/PWRDN# function. When a pin is assigned the PWRGD/PWRDN# function, the value of the corresponding GPIx_FUNC/GPIOx_FUNC field is ignored, with one exception: If a pin is assigned the PWRGD/PWRDN# function (via this field) and the OTP Page Selection (Dynamic) function (via GPIx_FUNC/GPIOx_FUNC) a hybrid function will be selected, which enables selection of functional/power-down OTP pages. Whether or not a pin is assigned with the PWRGD/PWRDN# function has an influence of the device power-up sequence (see Figure 7-3). 0x2 = 2: GPI_2 0x6 = 6: GPIO_0 0xA = 10: GPIO_1 0xF = 15: Unused
3:0	RESERVED	R	0x0	Reserved

3.14 R14 Register (Offset = 0xE) [Reset = 0x0C]

R14 is shown in Table 3-16.

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Table 3-16. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	GPI0_FUNC	R/W	0xC	GPI0 Function. Determines the function of GPI0. If "Group Output Enable" is selected, see "GPI0_OE_GRP_SEL" to select the Output Enable Group for GPI0. If "GPI" is selected, see "GPI0_LIVE_RB" for pin value readback. If GPI0 is not used, select "GPI". 0x0 = 0: Group OE 0x1 = 1: Global OE 0x3 = 3: I2C Bit 0 0x4 = 4: I2C Bit 1 0x6 = 6: PERST_IN0# 0xC = 12: GPI

3.15 R15 Register (Offset = 0xF) [Reset = 0x0C]

R15 is shown in Table 3-17.

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Table 3-17. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	GPI1_FUNC	R/W	0xC	GPI1 Function. Determines the function of GPI1. If "Group Output Enable" is selected, see "GPI1_OE_GRP_SEL" to select the Output Enable Group for GPI1. If "GPI" is selected, see "GPI1_LIVE_RB" for pin value readback. If GPI1 is not used, select "GPI". 0x0 = 0: Group OE 0x1 = 1: Global OE 0x3 = 3: I2C Bit 0 0x4 = 4: I2C Bit 1 0x6 = 6: PERST_IN0# 0xC = 12: GPI

3.16 R16 Register (Offset = 0x10) [Reset = 0x02]

R16 is shown in Table 3-18.

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Table 3-18. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	GPI2_FUNC	R/W	0x2	GPI2 Function. Determines the function of GPI2. If "Group Output Enable" is selected, see "GPI2_OE_GRP_SEL" to select the Output Enable Group for GPI2. If "GPI" is selected, see "GPI2_LIVE_RB" for pin value readback. If GPI2 is not used, select "GPI". 0x0 = 0: Group OE 0x1 = 1: Global OE 0x2 = 2: Alternate OE; When using this pin as an alternate output enable pin, set the OE Group of the output to "No OE Group" 0x3 = 3: I2C Bit 0 0x4 = 4: I2C Bit 1 0x6 = 6: PERST_IN0# 0xC = 12: GPI

3.17 R17 Register (Offset = 0x11) [Reset = 0x10]

R17 is shown in Table 3-19.

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Table 3-19. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	OE_GLOBAL	R/W	0x1	Global Output Enable. When set to 0, all outputs are disabled. When set to 1, all other contributors are considered to determine if each output is enabled. 0x0 = Outputs Disabled; When set to a 0, all outputs will be disabled. 0x1 = Other Logic for OE; When set to 1, all other contributors are considered to determine if each output is enabled.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.18 R21 Register (Offset = 0x15) [Reset = 0x02]

R21 is shown in Table 3-20.

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Table 3-20. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	GPIO0_FUNC	R/W	0x2	GPIO0 Function. Determines the function of GPIO0. If "Group Output Enable" is selected, see "GPIO0_OE_GRP_SEL" to select the Output Enable Group for GPIO0. If "GPI" is selected, see "GPIO0_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO0_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO0_GPO_VAL" to set the output value. If GPIO0 is not used, select "GPI". 0x0 = 0: Group OE 0x1 = 1: Global OE 0x2 = 2: Alternate OE; When using this pin as an alternate output enable pin, set the OE Group of the output to "No OE Group" 0x3 = 3: I2C Bit 0 0x4 = 4: I2C Bit 1 0x6 = 6: PERST_IN0# 0xC = 12: GPI 0x10 = 16: Status Output 0x11 = 17: GPO

3.19 R25 Register (Offset = 0x19) [Reset = 0x0C]

R25 is shown in Table 3-21.

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Table 3-21. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	GPIO1_FUNC	R/W	0xC	GPIO1 Function. Determines the function of GPIO1. If "Group Output Enable" is selected, see "GPIO1_OE_GRP_SEL" to select the Output Enable Group for GPIO1. If "GPI" is selected, see "GPIO1_LIVE_RB" for pin value readback. If "Status Output" is selected, see "GPIO1_OUT_SRC_SEL" to select the status output signal. If "GPO" is selected, see "GPIO1_GPO_VAL" to set the output value. If GPIO1 is not used, select "GPI". 0x0 = 0: Group OE 0x1 = 1: Global OE 0x3 = 3: I2C Bit 0 0x4 = 4: I2C Bit 1 0x6 = 6: PERST_IN0# 0xC = 12: GPI 0x10 = 16: Status Output 0x11 = 17: GPO

3.20 R26 Register (Offset = 0x1A) [Reset = 0x00]

R26 is shown in Table 3-22.

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Table 3-22. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	GPIO0_OUT_SRC_SEL	R/W	0x0	GPIO0 Output Source Select. Determines which signal is selected for output when GPIO0_FUNC is set to "Status Output". If GPIO0_FUNC is set to any other function, the value of this field is ignored. 0x0 = 0: IN0_LOS 0x3 = 3: IN0_LOS_EVT 0x6 = 6: IN0_LOS_LMT_EVT 0x9 = 9: CLK_READY 0xA = 10: IN0_PERST_BUF_MODE_STAT 0xD = 13: DEV_INTR

3.21 R28 Register (Offset = 0x1C) [Reset = 0x09]

R28 is shown in Table 3-23.

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Table 3-23. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPI2_POLARITY	R/W	0x0	GPI2 Polarity. Selects between normal and inverted polarity for the GPI2 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0x0 = Normal 0x1 = Inverted
5	GPI1_POLARITY	R/W	0x0	GPI1 Polarity. Selects between normal and inverted polarity for the GPI1 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0x0 = Normal 0x1 = Inverted
4	GPI0_POLARITY	R/W	0x0	GPI0 Polarity. Selects between normal and inverted polarity for the GPI0 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. 0x0 = Normal 0x1 = Inverted
3:0	GPIO1_OUT_SRC_SEL	R/W	0x9	GPIO1 Output Source Select. Determines which signal is selected for output when GPIO1_FUNC is set to "Status Output". If GPIO1_FUNC is set to any other function, the value of this field is ignored. 0x0 = 0: IN0_LOS 0x3 = 3: IN0_LOS_EVT 0x6 = 6: IN0_LOS_LMT_EVT 0x9 = 9: CLK_READY 0xA = 10: IN0_PERST_BUF_MODE_STAT 0xD = 13: DEV_INTR

3.22 R29 Register (Offset = 0x1D) [Reset = 0x80]

R29 is shown in Table 3-24.

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Table 3-24. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI0_PULL_DN_EN	R/W	0x1	GPI0 Internal Pull-down Resistor Enable
6	GPIO1_POLARITY	R/W	0x0	GPIO1 Polarity. Selects between normal and inverted polarity for the GPIO1 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0x0 = Normal 0x1 = Inverted
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	GPIO0_POLARITY	R/W	0x0	GPIO0 Polarity. Selects between normal and inverted polarity for the GPIO0 pin. For 'Normal' polarity, functions ending with '#' are active-low, and functions ending without '#' are active-high. For 'Inverted' polarity, functions ending with '#' are active-high, and functions ending without '#' are active-low. This value affects both input and output functions. 0x0 = Normal 0x1 = Inverted
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.23 R30 Register (Offset = 0x1E) [Reset = 0x22]

R30 is shown in Table 3-25.

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Table 3-25. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPI2_PULL_UP_EN	R/W	0x0	GPI2 Internal Pull-up Resistor Enable
5	GPI2_PULL_DN_EN	R/W	0x1	GPI2 Internal Pull-down Resistor Enable
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	GPI1_PULL_UP_EN	R/W	0x0	GPI1 Internal Pull-up Resistor Enable
1	GPI1_PULL_DN_EN	R/W	0x1	GPI1 Internal Pull-down Resistor Enable
0	GPI0_PULL_UP_EN	R/W	0x0	GPI0 Internal Pull-up Resistor Enable

3.24 R31 Register (Offset = 0x1F) [Reset = 0x20]

R31 is shown in Table 3-26.

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Table 3-26. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO0_PULL_UP_EN	R/W	0x0	GPIO0 Internal Pull-up Resistor Enable
5	GPIO0_PULL_DN_EN	R/W	0x1	GPIO0 Internal Pull-down Resistor Enable
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.25 R32 Register (Offset = 0x20) [Reset = 0x20]

R32 is shown in Table 3-27.

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Table 3-27. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_PULL_UP_EN	R/W	0x0	GPIO1 Internal Pull-up Resistor Enable
5	GPIO1_PULL_DN_EN	R/W	0x1	GPIO1 Internal Pull-down Resistor Enable
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.26 R33 Register (Offset = 0x21) [Reset = 0x00]

R33 is shown in Table 3-28.

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Table 3-28. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPI2_LIVE_RB	R	0x0	GPI2 Pin Live Value Readback
5	GPI1_LIVE_RB	R	0x0	GPI1 Pin Live Value Readback
4	GPI0_LIVE_RB	R	0x0	GPI0 Pin Live Value Readback
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.27 R34 Register (Offset = 0x22) [Reset = 0x00]

R34 is shown in Table 3-29.

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Table 3-29. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:2	GPIO0_LIVE_RB	R	0x0	GPIO0 Pin Live Value Readback 0x0 = 0: LOW 0x3 = 3: HIGH
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.28 R35 Register (Offset = 0x23) [Reset = 0x00]

R35 is shown in Table 3-30.

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Table 3-30. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_GPO_VAL	R/W	0x0	GPIO1 GPO Output Value. When GPIO1 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO1 is not configured for the "GPO" function, this register field is ignored. 0x0 = LOW 0x1 = HIGH
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	GPIO0_GPO_VAL	R/W	0x0	GPIO0 GPO Output Value. When GPIO0 is configured for the "GPO" function, the value in this register field determines whether the pin is driven LOW or HIGH. When GPIO0 is not configured for the "GPO" function, this register field is ignored. 0x0 = LOW 0x1 = HIGH
1	GPIO1_LIVE_RB	R	0x0	GPIO1 Pin Live Value Readback 0x0 = 0: LOW 0x1 = 1: HIGH
0	RESERVED	R	0x0	Reserved

3.29 R36 Register (Offset = 0x24) [Reset = 0x08]

R36 is shown in Table 3-31.

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Table 3-31. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	GPI1_OE_GRP_SEL	R/W	0x1	GPI1 Output Enable Group Select. When GPI1 is configured for the "Group Output Enable" function, this field determines which output enable group GPI1 will control. If GPI1 is not configured for the "Group Output Enable" function, this field is ignored. 0x0 = OE_GROUP_0 0x1 = OE_GROUP_1 0x2 = OE_GROUP_2 0x3 = OE_GROUP_3 0x4 = OE_GROUP_4
2:0	GPI0_OE_GRP_SEL	R/W	0x0	GPI0 Output Enable Group Select. When GPI0 is configured for the "Group Output Enable" function, this field determines which output enable group GPI0 will control. If GPI0 is not configured for the "Group Output Enable" function, this field is ignored. 0x0 = OE_GROUP_0 0x1 = OE_GROUP_1 0x2 = OE_GROUP_2 0x3 = OE_GROUP_3 0x4 = OE_GROUP_4

3.30 R37 Register (Offset = 0x25) [Reset = 0x02]

R37 is shown in Table 3-32.

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Table 3-32. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	GPI2_OE_GRP_SEL	R/W	0x2	GPI2 Output Enable Group Select. When GPI2 is configured for the "Group Output Enable" function, this field determines which output enable group GPI2 will control. If GPI2 is not configured for the "Group Output Enable" function, this field is ignored. 0x0 = OE_GROUP_0 0x1 = OE_GROUP_1 0x2 = OE_GROUP_2 0x3 = OE_GROUP_3 0x4 = OE_GROUP_4

3.31 R39 Register (Offset = 0x27) [Reset = 0x03]

R39 is shown in Table 3-33.

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Table 3-33. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	GPIO0_OE_GRP_SEL	R/W	0x3	GPIO0 Output Enable Group Select. When GPIO0 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO0 will control. If GPIO0 is not configured for the "Group Output Enable" function, this field is ignored. 0x0 = OE_GROUP_0 0x1 = OE_GROUP_1 0x2 = OE_GROUP_2 0x3 = OE_GROUP_3 0x4 = OE_GROUP_4

3.32 R41 Register (Offset = 0x29) [Reset = 0x04]

R41 is shown in Table 3-34.

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Table 3-34. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_OUT_SIG_TYPE	R/W	0x0	GPIO1 Output Signal Type. When GPIO1 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO1 is used as an input, the value of this field is ignored. 0x0 = LVCMOS 0x1 = Open-Drain
6:4	RESERVED	R	0x0	Reserved
3	GPIO0_OUT_SIG_TYPE	R/W	0x0	GPIO0 Output Signal Type. When GPIO0 is used as an output, this field selects between CMOS and Open-Drain output signal types. When GPIO0 is used as an input, the value of this field is ignored. 0x0 = LVCMOS 0x1 = Open-Drain
2:0	GPIO1_OE_GRP_SEL	R/W	0x4	GPIO1 Output Enable Group Select. When GPIO1 is configured for the "Group Output Enable" function, this field determines which output enable group GPIO1 will control. If GPIO1 is not configured for the "Group Output Enable" function, this field is ignored. 0x0 = OE_GROUP_0 0x1 = OE_GROUP_1 0x2 = OE_GROUP_2 0x3 = OE_GROUP_3 0x4 = OE_GROUP_4

3.33 R42 Register (Offset = 0x2A) [Reset = 0x00]

R42 is shown in Table 3-35.

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Table 3-35. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	IN0_RCVR_FMT	R/W	0x0	IN0 Input Receiver Format. This field configures the IN0 receiver for a specific input clock format, with options of: N/A, LVCMOS IN0_P, LVCMOS IN0_N, and Differential IN0. 0x0 = N/A (IN0 Unused) 0x1 = LVCMOS IN0_P 0x2 = LVCMOS IN0_N 0x3 = Differential IN0

3.34 R43 Register (Offset = 0x2B) [Reset = 0x00]

R43 is shown in Table 3-36.

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Table 3-36. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	IN0_TERMINATION_SEL	R/W	0x0	IN0 Termination Select. 0x0 = None, DC; No termination, no internal bias (LVCMOS inputs, LP-HCSL inputs, and other DC-coupled inputs that do not require integrated input termination) 0x1 = None, AC; No termination, with internal bias (AC-coupled inputs that do not require integrated input termination) 0x2 = 50 Ω to GND; 50 Ω to GND on both P and N (HCSL inputs that require 100 Ω differential impedance and other DC-coupled inputs that require 50 Ω to GND) 0x3 = 42.5 Ω to GND; 42.5 Ω to GND on both P and N (HCSL inputs that require 85 Ω differential impedance and other DC-coupled inputs that require 42.5 Ω to GND) 0x4 = 100 Ω P to N; 100 Ω between P and N (DC-LVDS) 0x5 = 50 Ω to bias; 50 Ω to internal bias on both P and N (AC-LVDS and other AC-coupled inputs that require 50 Ω to AC-GND) 0x6 = 50 Ω to DC and GND; 50 Ω to DC on both P and N. DC is 50 Ω to GND. (DC-LVPECL) 0x7 = 42.5 Ω to bias; 42.5 Ω to internal bias on both P and N (AC-coupled inputs that require 42.5 Ω to AC-GND)

3.35 R44 Register (Offset = 0x2C) [Reset = 0x08]

R44 is shown in Table 3-37.

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Table 3-37. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	IN0_LOS_THRESH	R/W	0x0	IN0 Loss of Signal Detector Threshold. Selects the minimum valid frequency for IN0. If IN0 is below this frequency, LOS will be asserted. 0x0 = 1 MHz 0x1 = 25 MHz
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	IN0_LOS_EN	R/W	0x1	0x0 = Disables Loss-Of-Signal 0x1 = Enables Loss-Of-Signal detector
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.36 R45 Register (Offset = 0x2D) [Reset = 0x00]

R45 is shown in Table 3-38.

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Table 3-38. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PERST_BUF_IN0_STS	R	0x0	IN0 Buffer Mode Status. This field indicates whether or not one or more output banks are currently using Buffer Mode with IN0. 0x0 = Inactive 0x1 = Active
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2:1	PERST_BUF_IN0	R/W	0x0	IN0 Buffer Mode Select. Selects if and how Buffer Mode with IN0 is activated. For "Disabled", IN0 is unavailable for clock source selection by banks using Buffer Mode. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", the normal clock selection (BANKx_CLK_SEL) will be used instead. For "Edge-Triggered (Enabled on PERST_IN0# Deassertion)", Buffer Mode with IN0 is activated on the first deassertion of the PERST_IN0# signal. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected when Buffer Mode becomes active. Until that point, the normal clock selection (BANKx_CLK_SEL) will be used. For "Level-Triggered (Enable/Disable Follows PERST_IN0#)", Buffer Mode with IN0 is activate whenever the PERST_IN0# signal is deasserted. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected whenever Buffer Mode is active. At all other times, the normal clock selection (BANKx_CLK_SEL) will be used. For "Always On", Buffer Mode with IN0 is always active. For any bank where BANKx_BUF_MODE_CLK_SEL is set to "Enabled, Select IN0", IN0 will be selected at all times. 0x0 = Disabled 0x1 = Edge; Edge-Triggered (PERST_IN0# Deassertion) 0x2 = Level; Level-Triggered (Follows PERST_IN0#) 0x3 = Enabled
0	RESERVED	R	0x0	Reserved

3.37 R46 Register (Offset = 0x2E) [Reset = 0x00]

R46 is shown in Table 3-39.

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Table 3-39. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	PERST_BUF_IN0_LOS_EN	R/W	0x0	IN0 Buffer Mode, Loss-of-Signal Enable. This field determines whether or not clock selection for banks using Buffer Mode with IN0 is dependent on the selected the IN0_LOS status. When set to 0, Buffer Mode with IN0 can become and remain active, regardless of the IN0_LOS status. When set to 1, Buffer Mode with IN0 can only become active while IN0_LOS is deasserted, and if IN0_LOS is asserted while Buffer Mode with IN0 is already active, Buffer Mode with IN0 will be deactivated, and all deactivated banks will switch back to the normal clock selection (BANKx_CLK_SEL).
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.38 R47 Register (Offset = 0x2F) [Reset = 0x0C]

R47 is shown in Table 3-40.

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Table 3-40. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	FOD0_N_DIV	R/W	0xC	FOD0 Divide Ratio, Integer Part. This field, along with FOD0_NUM, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.39 R48 Register (Offset = 0x30) [Reset = 0x0C]

R48 is shown in Table 3-41.

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Table 3-41. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	FOD1_N_DIV	R/W	0xC	FOD1 Divide Ratio, Integer Part. This field, along with FOD1_NUM, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.40 R49 Register (Offset = 0x31) [Reset = 0x8F]

R49 is shown in Table 3-42.

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Table 3-42. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_NUM[7:0]	R/W	0x8F	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.41 R50 Register (Offset = 0x32) [Reset = 0xC2]

R50 is shown in Table 3-43.

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Table 3-43. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_NUM[15:8]	R/W	0xC2	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.42 R51 Register (Offset = 0x33) [Reset = 0x55]

R51 is shown in Table 3-44.

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Table 3-44. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_NUM[23:16]	R/W	0x55	FOD0 Divide Ratio, Fractional Part. This field, along with FOD0_N_DIV, sets the divide ratio of FOD0, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD0_CFG_UPDATE to 0x1 for this value to take effect.

3.43 R52 Register (Offset = 0x34) [Reset = 0x8F]

R52 is shown in Table 3-45.

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Table 3-45. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_NUM[7:0]	R/W	0x8F	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.44 R53 Register (Offset = 0x35) [Reset = 0xC2]

R53 is shown in Table 3-46.

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Table 3-46. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_NUM[15:8]	R/W	0xC2	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.45 R54 Register (Offset = 0x36) [Reset = 0x55]

R54 is shown in Table 3-47.

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Table 3-47. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_NUM[23:16]	R/W	0x55	FOD1 Divide Ratio, Fractional Part. This field, along with FOD1_N_DIV, sets the divide ratio of FOD1, which divides the BAW oscillator clock down to a clock with a frequency ranging between 100MHz and 400MHz. This is the first of up to three stages of clock division for output clocks originating from the BAW oscillator. Write FOD1_CFG_UPDATE to 0x1 for this value to take effect.

3.46 R55 Register (Offset = 0x37) [Reset = 0x08]

R55 is shown in Table 3-48.

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Table 3-48. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FOD1_CFG_UPDATE	R/W	0x0	FOD1 Configuration Update. To change the frequency of FOD1, first write FOD1_N_DIV and FOD1_NUM with the desired values (writing these fields does not cause the new values to take effect). Then, when ready for the new frequency configuration to take effect, write this field with 0x1.
6	FOD0_CFG_UPDATE	R/W	0x0	FOD0 Configuration Update. To change the frequency of FOD0, first write FOD0_N_DIV and FOD0_NUM with the desired values (writing these fields does not cause the new values to take effect). Then, when ready for the new frequency configuration to take effect, write this field with 0x1.
5:3	PATH1_DIV	R/W	0x1	FOD PATH1 Post-divider Divide Ratio. This field sets the divide ratio of the FOD PATH1 Post-divider, which divides an FOD clock down to a clock with a frequency ranging between 2.5MHz and 200MHz. This is the second of up to three stages of clock division for output clocks originating from the BAW oscillator. When PATH1_EDGE_COMB_EN is set to 0x1 (FOD PATH1 is configured for the using the Edge Combiner), this field must be set to 0x0. 0x0 = Disabled; When using the edge combiner, set this field to Disabled 0x1 = FOD / 2 0x2 = FOD / 4 0x3 = FOD / 6 0x4 = FOD / 8 0x5 = FOD / 10 0x6 = FOD / 20 0x7 = FOD / 40
2:0	PATH0_DIV	R/W	0x0	FOD PATH0 Post-divider Divide Ratio. This field sets the divide ratio of the FOD PATH0 Post-divider, which divides an FOD clock down to a clock with a frequency ranging between 2.5MHz and 200MHz. This is the second of up to three stages of clock division for output clocks originating from the BAW oscillator. When PATH0_EDGE_COMB_EN is set to 0x1 (FOD PATH0 is configured for the using the Edge Combiner), this field must be set to 0x0. 0x0 = Disabled; When using the edge combiner, set this field to Disabled 0x1 = FOD / 2 0x2 = FOD / 4 0x3 = FOD / 6 0x4 = FOD / 8 0x5 = FOD / 10 0x6 = FOD / 20 0x7 = FOD / 40

3.47 R57 Register (Offset = 0x39) [Reset = 0x00]

R57 is shown in Table 3-49.

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Table 3-49. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	FOD_PH_OFFSET_N_DIV	R/W	0x0	FOD Phase Offset, Integer Part. The full phase offset (delay) of the FOD indicated by FOD_PH_OFFSET_FOD_SEL (FODx) with respect to the other FOD, is defined through 2 fields: FOD_PH_OFFSET_N_DIV and FOD_PH_OFFSET_NUM. The values of these fields are determined through the follwoing equation: 400ps * (FOD_PH_OFFSET_N_DIV + (FOD_PH_OFFSET_NUM / 2^{16})) = FODx Offset (ps) Phase offsets are applied at power-up, and subsequently upon writing FOD_PH_OFFSET_SHIFT_NOW with 0x1.

3.48 R58 Register (Offset = 0x3A) [Reset = 0x00]

R58 is shown in Table 3-50.

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Table 3-50. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD_PH_OFFSET_NUM[7:0]	R/W	0x0	FOD Phase Offset, Fractional Part (Byte 0). See FOD_PH_OFFSET_N_DIV.

3.49 R59 Register (Offset = 0x3B) [Reset = 0x00]

R59 is shown in Table 3-51.

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Table 3-51. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD_PH_OFFSET_NUM[15:8]	R/W	0x0	FOD Phase Offset, Fractional Part (Byte 0). See FOD_PH_OFFSET_N_DIV.

3.50 R60 Register (Offset = 0x3C) [Reset = 0x00]

R60 is shown in Table 3-52.

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Table 3-52. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	FOD0_SSC_CONFIG_SEL	R/W	0x0	FOD0 SSC Setting. Selects between custom SSC control and 4 different SSC presets. 0x0 = Custom 0x1 = -0.1% Down-spread 0x2 = -0.25% Down-spread 0x3 = -0.3% Down-spread 0x4 = -0.5% Down-spread
3	FOD0_SSC_MOD_TYPE	R/W	0x0	FOD0 SSC Modulation Type. Selectable between down-spread and center-spread 0x0 = Down-spread 0x1 = Center-spread
2	FOD0_SSC_EN	R/W	0x0	FOD0 SSC Enable. Enables SSC on output clocks sourced from FOD0.
1	FOD_PH_OFFSET_FOD_SEL	R/W	0x0	FOD Phase Offset FOD Select. Determines which FOD will be delayed in order to produce a phase offset between the two FODs. 0x0 = FOD0 0x1 = FOD1
0	FOD_PH_OFFSET_SHIFT_NOW	R/W	0x0	FOD Phase Offset Shift Now. When written with 0x1, the FOD indicated by FOD_PH_OFFSET_FOD_SEL will be delayed with respect to the other FOD, according to the values of FOD_PH_OFFSET_N_DIV and FOD_PH_OFFSET_NUM.

3.51 R61 Register (Offset = 0x3D) [Reset = 0x00]

R61 is shown in Table 3-53.

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Table 3-53. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_SSC_STEPS[7:0]	R/W	0x0	FOD0 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD0 frequency and the desired SSC modulation freqency.

3.52 R62 Register (Offset = 0x3E) [Reset = 0x00]

R62 is shown in Table 3-54.

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Table 3-54. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	FOD0_SSC_STEPS[12:8]	R/W	0x0	FOD0 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD0 frequency and the desired SSC modulation freqency.

3.53 R63 Register (Offset = 0x3F) [Reset = 0x00]

R63 is shown in Table 3-55.

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Table 3-55. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_STEP_SIZE[7:0]	R/W	0x0	FOD0 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD0 frequency and the desired PPM change per DCO adjustment.

3.54 R64 Register (Offset = 0x40) [Reset = 0x00]

R64 is shown in Table 3-56.

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Table 3-56. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_STEP_SIZE[15:8]	R/W	0x0	FOD0 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD0 frequency and the desired PPM change per DCO adjustment.

3.55 R65 Register (Offset = 0x41) [Reset = 0x00]

R65 is shown in Table 3-57.

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Table 3-57. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	FOD1_SSC_CONFIG_SEL	R/W	0x0	FOD1 SSC Setting. Selects between custom SSC control and 4 different SSC presets. 0x0 = Custom 0x1 = -0.1% Down-spread 0x2 = -0.25% Down-spread 0x3 = -0.3% Down-spread 0x4 = -0.5% Down-spread
1	FOD1_SSC_MOD_TYPE	R/W	0x0	FOD1 SSC Modulation Type. Selectable between down-spread and center-spread 0x0 = Down-spread 0x1 = Center-spread
0	FOD1_SSC_EN	R/W	0x0	FOD1 SSC Enable. Enables SSC on output clocks sourced from FOD1.

3.56 R66 Register (Offset = 0x42) [Reset = 0x00]

R66 is shown in Table 3-58.

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Table 3-58. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_SSC_STEPS[7:0]	R/W	0x0	FOD1 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD1 frequency and the desired SSC modulation freqency.

3.57 R67 Register (Offset = 0x43) [Reset = 0x00]

R67 is shown in Table 3-59.

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Table 3-59. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	FOD1_SSC_STEPS[12:8]	R/W	0x0	FOD1 SSC Steps, Byte 0. Sets the number of frequency steps in each segment of the triangular modulation profile. For down-spread, this is the number of frequency steps between the nominal frequency and maximum down-spread. For center-spread, this is the number of frequency steps between the nominal frequency and both maximum down-spread and maximum up-spread. This should be calculated based on the FOD1 frequency and the desired SSC modulation freqency.

3.58 R68 Register (Offset = 0x44) [Reset = 0x00]

R68 is shown in Table 3-60.

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Table 3-60. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_STEP_SIZE[7:0]	R/W	0x0	FOD1 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD1 frequency and the desired PPM change per DCO adjustment.

3.59 R69 Register (Offset = 0x45) [Reset = 0x00]

R69 is shown in Table 3-61.

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Table 3-61. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_STEP_SIZE[15:8]	R/W	0x0	FOD1 DCO Step Size, Byte 0. Sets the size of the FOD0 frequency steps used for both SSC and DCO. For SSC, this should be calculated based on the number of SSC steps, the SSC modulation type, and the desired SSC magnitude. For DCO, this should be calculated based on the FOD1 frequency and the desired PPM change per DCO adjustment.

3.60 R70 Register (Offset = 0x46) [Reset = 0x00]

R70 is shown in Table 3-62.

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Table 3-62. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	FOD1_DCO_DEC	R/W1C	0x0	FOD1 DCO Increment. With FOD1_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD1 frequency to increase. If FOD1_DCO_EN is set to 0x1, any writes to this field will be ignored.
4	FOD1_DCO_INC	R/W1C	0x0	FOD1 DCO Increment. With FOD1_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD1 frequency to increase. If FOD1_DCO_EN is set to 0x1, any writes to this field will be ignored.
3	FOD1_DCO_EN	R/W	0x0	FOD1 DCO Enable. Enables DCO on output clocks driven by FOD1.
2	FOD0_DCO_DEC	R/W1C	0x0	FOD0 DCO Increment. With FOD0_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD0 frequency to increase. If FOD0_DCO_EN is set to 0x1, any writes to this field will be ignored.
1	FOD0_DCO_INC	R/W1C	0x0	FOD0 DCO Increment. With FOD0_DCO_EN set to 0x1, writing a 1 to this field will cause the FOD0 frequency to increase. If FOD0_DCO_EN is set to 0x1, any writes to this field will be ignored.
0	FOD0_DCO_EN	R/W	0x0	FOD0 DCO Enable. Enables DCO on output clocks driven by FOD0.

3.61 R71 Register (Offset = 0x47) [Reset = 0x00]

R71 is shown in Table 3-63.

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Table 3-63. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_STEPS_STAT[7:0]	R	0x0	FOD0 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD0 frequency has been adjusted by.

3.62 R72 Register (Offset = 0x48) [Reset = 0x00]

R72 is shown in Table 3-64.

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Table 3-64. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_STEPS_STAT[15:8]	R	0x0	FOD0 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD0 frequency has been adjusted by.

3.63 R73 Register (Offset = 0x49) [Reset = 0x00]

R73 is shown in Table 3-65.

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Table 3-65. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_STEPS_STAT[7:0]	R	0x0	FOD1 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD1 frequency has been adjusted by.

3.64 R74 Register (Offset = 0x4A) [Reset = 0x00]

R74 is shown in Table 3-66.

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Table 3-66. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_STEPS_STAT[15:8]	R	0x0	FOD1 DCO Steps Status, Byte 0. Reading this field returns the numer of steps that the FOD1 frequency has been adjusted by.

3.65 R75 Register (Offset = 0x4B) [Reset = 0x00]

R75 is shown in Table 3-67.

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Table 3-67. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	FOD0_DCO_N_DIV_STAT	R	0x0	FOD0 DCO Integer Readback. Reading this value returns the value of the FOD0 divisor's integer portion, after it has been adjusted by the DCO logic.

3.66 R76 Register (Offset = 0x4C) [Reset = 0x00]

R76 is shown in Table 3-68.

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Table 3-68. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_NUM_STAT[7:0]	R	0x0	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.67 R77 Register (Offset = 0x4D) [Reset = 0x00]

R77 is shown in Table 3-69.

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Table 3-69. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_NUM_STAT[15:8]	R	0x0	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.68 R78 Register (Offset = 0x4E) [Reset = 0x00]

R78 is shown in Table 3-70.

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Table 3-70. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD0_DCO_NUM_STAT[23:16]	R	0x0	FOD0 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD0 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.69 R79 Register (Offset = 0x4F) [Reset = 0x00]

R79 is shown in Table 3-71.

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Table 3-71. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	FOD1_DCO_N_DIV_STAT	R	0x0	FOD1 DCO Integer Readback. Reading this value returns the value of the FOD1 divisor's integer portion, after it has been adjusted by the DCO logic.

3.70 R80 Register (Offset = 0x50) [Reset = 0x00]

R80 is shown in Table 3-72.

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Table 3-72. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_NUM_STAT[7:0]	R	0x0	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.71 R81 Register (Offset = 0x51) [Reset = 0x00]

R81 is shown in Table 3-73.

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Table 3-73. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_NUM_STAT[15:8]	R	0x0	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.72 R82 Register (Offset = 0x52) [Reset = 0x00]

R82 is shown in Table 3-74.

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Table 3-74. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FOD1_DCO_NUM_STAT[23:16]	R	0x0	FOD1 DCO Numerator Readback, Byte 0. Reading this value returns the value of the FOD1 divisor's fractional portion, after it has been adjusted by the DCO logic.

3.73 R83 Register (Offset = 0x53) [Reset = 0x90]

R83 is shown in Table 3-75.

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Table 3-75. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	BANK1_CLK_SEL	R/W	0x4	BANK1 Clock Selection. Selects the clock source for BANK1 (OUT1, OUT2). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1
4:2	BANK0_CLK_SEL	R/W	0x4	BANK0 Clock Selection. Selects the clock source for BANK0 (OUT0). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1
1	PATH1_EDGE_COMB_EN	R/W	0x0	FOD PATH1 Edge Combiner Enable. This field determines whether output clock banks that select FOD PATH1 as their clock source will be driven by the output of the Edge Combiner or by the output of FOD PATH1 Post-divider. When set to 1, the Edge Combiner will be enabled, and the two FODs will both generate clocks with a frequency determined by the FOD0 Divide Ratio settings. TI recommends not modifying the value of this field. 0x0 = PATH1_DIV 0x1 = Edge Combiner
0	PATH0_EDGE_COMB_EN	R/W	0x0	FOD PATH0 Edge Combiner Enable. This field determines whether output clock banks that select FOD PATH0 as their clock source will be driven by the output of the Edge Combiner or by the output of FOD PATH0 Post-divider. When set to 1, the Edge Combiner will be enabled, and the two FODs will both generate clocks with a frequency determined by the FOD0 Divide Ratio settings. 0x0 = PATH0_DIV 0x1 = Edge Combiner

3.74 R84 Register (Offset = 0x54) [Reset = 0x24]

R84 is shown in Table 3-76.

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Table 3-76. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	BANK3_CLK_SEL	R/W	0x4	BANK3 Clock Selection. Selects the clock source for BANK3 (OUT5). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1
2:0	BANK2_CLK_SEL	R/W	0x4	BANK2 Clock Selection. Selects the clock source for BANK2 (OUT3, OUT4). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1

3.75 R85 Register (Offset = 0x55) [Reset = 0x24]

R85 is shown in Table 3-77.

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Table 3-77. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	BANK5_CLK_SEL	R/W	0x4	BANK5 Clock Selection. Selects the clock source for BANK5 (OUT7). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1
2:0	BANK4_CLK_SEL	R/W	0x4	BANK4 Clock Selection. Selects the clock source for BANK4 (OUT6). For FOD0, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x0. For FOD1, select "PATH1". For the Edge Combiner, select "PATH0" and set PATH0_EDGE_COMB_EN to 0x1. Manual Clock Switchover can be achieved by writing to this field while clocks are active. 0x0 = 0: IN_0 0x3 = 3: PATH0 0x4 = 4: PATH1

3.76 R86 Register (Offset = 0x56) [Reset = 0x01]

R86 is shown in Table 3-78.

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Table 3-78. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BANK0_CH_DIV[7:0]	R/W	0x1	Divisor for the BANK0 (OUT0) channel divider (Byte 0). For a divisor of 65536, value = 0. For any other divisor, value = divisor.

3.77 R87 Register (Offset = 0x57) [Reset = 0x00]

R87 is shown in Table 3-79.

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Table 3-79. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BANK0_CH_DIV[15:8]	R/W	0x0	Divisor for the BANK0 (OUT0) channel divider (Byte 0). For a divisor of 65536, value = 0. For any other divisor, value = divisor.

3.78 R88 Register (Offset = 0x58) [Reset = 0x11]

R88 is shown in Table 3-80.

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Table 3-80. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	BANK2_CH_DIV	R/W	0x1	Divisor for the BANK2 (OUT3, OUT4) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.
3:0	BANK1_CH_DIV	R/W	0x1	Divisor for the BANK1 (OUT1, OUT2) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.79 R89 Register (Offset = 0x59) [Reset = 0x01]

R89 is shown in Table 3-81.

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Table 3-81. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	IN0_LOS	R/W	0x1	IN0 Loss-of-Signal. This is set to 1 to indicate that IN0 is currently invalid. 0x0 = IN_0 Valid 0x1 = IN_0 Invalid

3.80 R90 Register (Offset = 0x5A) [Reset = 0x41]

R90 is shown in Table 3-82.

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Table 3-82. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	BANK4_CH_DIV	R/W	0x4	Divisor for the BANK4 (OUT6) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.
3:0	BANK3_CH_DIV	R/W	0x1	Divisor for the BANK3 (OUT5) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.81 R91 Register (Offset = 0x5B) [Reset = 0x04]

R91 is shown in Table 3-83.

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Table 3-83. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PERST_BUF_BANK1	R/W	0x0	BANK1 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK1 and selects the clock source to be used for BANK1 when Buffer Mode is active. For "Disabled" BANK1 will defer to the normal clock selection (BANK1_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK1 will defer to the normal clock selection (BANK1_CLK_SEL). 0x0 = BANK1_CLK_SEL 0x1 = IN_0
5:4	PERST_BUF_BANK0	R/W	0x0	BANK0 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK0 and selects the clock source to be used for BANK0 when Buffer Mode is active. For "Disabled" BANK0 will defer to the normal clock selection (BANK0_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK0 will defer to the normal clock selection (BANK0_CLK_SEL). 0x0 = BANK0_CLK_SEL 0x1 = IN_0
3:0	BANK5_CH_DIV	R/W	0x4	Divisor for the BANK5 (OUT7) channel divider. For a divisor of 16, value = 0. For any other divisor, value = divisor.

3.82 R92 Register (Offset = 0x5C) [Reset = 0x00]

R92 is shown in Table 3-84.

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Table 3-84. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PERST_BUF_BANK5	R/W	0x0	BANK5 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK5 and selects the clock source to be used for BANK5 when Buffer Mode is active. For "Disabled" BANK5 will defer to the normal clock selection (BANK5_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK5 will defer to the normal clock selection (BANK5_CLK_SEL). 0x0 = BANK5_CLK_SEL 0x1 = IN_0
5:4	PERST_BUF_BANK4	R/W	0x0	BANK4 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK4 and selects the clock source to be used for BANK4 when Buffer Mode is active. For "Disabled" BANK4 will defer to the normal clock selection (BANK4_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK4 will defer to the normal clock selection (BANK4_CLK_SEL). 0x0 = BANK4_CLK_SEL 0x1 = IN_0
3:2	PERST_BUF_BANK3	R/W	0x0	BANK3 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK3 and selects the clock source to be used for BANK3 when Buffer Mode is active. For "Disabled" BANK3 will defer to the normal clock selection (BANK3_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK3 will defer to the normal clock selection (BANK3_CLK_SEL). 0x0 = BANK3_CLK_SEL 0x1 = IN_0
1:0	PERST_BUF_BANK2	R/W	0x0	BANK2 Buffer Mode Clock Selection. This field enables/disables Buffer Mode for BANK2 and selects the clock source to be used for BANK2 when Buffer Mode is active. For "Disabled" BANK2 will defer to the normal clock selection (BANK2_CLK_SEL). If this field selects a clock source that is unavailable or not active, BANK2 will defer to the normal clock selection (BANK2_CLK_SEL). 0x0 = BANK2_CLK_SEL 0x1 = IN_0

3.83 R93 Register (Offset = 0x5D) [Reset = 0x00]

R93 is shown in Table 3-85.

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Table 3-85. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK1_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK1 Automatic Clock Switchback Enable. When enabled, after BANK1 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK1 will immediately switch back to it. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1.
6	BANK0_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK0 Automatic Clock Switchback Enable. When enabled, after BANK0 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK0 will immediately switch back to it. This bit is ignored unless BANK0_AUTO_CLK_SWITCHOVER_EN is set to 1.
5	BANK5_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK5 Automatic Clock Switchover Enable. Assuming that BANK5 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK5 will automatically switch its clock source to the FOD-generated clock selected by the BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK5_CLK_DIS_ON_LOS or BANK5 Buffer Mode.
4	BANK4_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK4 Automatic Clock Switchover Enable. Assuming that BANK4 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK4 will automatically switch its clock source to the FOD-generated clock selected by the BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK4_CLK_DIS_ON_LOS or BANK4 Buffer Mode.
3	BANK3_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK3 Automatic Clock Switchover Enable. Assuming that BANK3 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK3 will automatically switch its clock source to the FOD-generated clock selected by the BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK3_CLK_DIS_ON_LOS or BANK3 Buffer Mode.
2	BANK2_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK2 Automatic Clock Switchover Enable. Assuming that BANK2 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK2 will automatically switch its clock source to the FOD-generated clock selected by the BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK2_CLK_DIS_ON_LOS or BANK2 Buffer Mode.
1	BANK1_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK1 Automatic Clock Switchover Enable. Assuming that BANK1 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK1 will automatically switch its clock source to the FOD-generated clock selected by the BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK1_CLK_DIS_ON_LOS or BANK1 Buffer Mode.
0	BANK0_AUTO_CLK_SWITCHOVER_EN	R/W	0x0	BANK0 Automatic Clock Switchover Enable. Assuming that BANK0 is sourced by an input clock, if the input clock is determined to be invalid (LOS), BANK0 will automatically switch its clock source to the FOD-generated clock selected by the BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL. Cannot be enabled simultaneously with BANK0_CLK_DIS_ON_LOS or BANK0 Buffer Mode.

3.84 R94 Register (Offset = 0x5E) [Reset = 0xF0]

R94 is shown in Table 3-86.

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Table 3-86. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK3_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK3 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK3 clock source is determined to be invalid. This bit is ignored unless BANK3_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1
6	BANK2_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK2 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK2 clock source is determined to be invalid. This bit is ignored unless BANK2_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1
5	BANK1_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK1 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK1 clock source is determined to be invalid. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1
4	BANK0_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK0 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK0 clock source is determined to be invalid. This bit is ignored unless BANK0_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1
3	BANK5_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK5 Automatic Clock Switchback Enable. When enabled, after BANK5 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK5 will immediately switch back to it. This bit is ignored unless BANK5_AUTO_CLK_SWITCHOVER_EN is set to 1.
2	BANK4_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK4 Automatic Clock Switchback Enable. When enabled, after BANK4 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK4 will immediately switch back to it. This bit is ignored unless BANK4_AUTO_CLK_SWITCHOVER_EN is set to 1.
1	BANK3_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK3 Automatic Clock Switchback Enable. When enabled, after BANK3 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK3 will immediately switch back to it. This bit is ignored unless BANK3_AUTO_CLK_SWITCHOVER_EN is set to 1.
0	BANK2_AUTO_CLK_SWITCHBACK_EN	R/W	0x0	BANK2 Automatic Clock Switchback Enable. When enabled, after BANK2 undergoes a Automatic Clock Switchover, if the original clock source is re-validated, BANK2 will immediately switch back to it. This bit is ignored unless BANK2_AUTO_CLK_SWITCHOVER_EN is set to 1.

3.85 R95 Register (Offset = 0x5F) [Reset = 0xFF]

R95 is shown in Table 3-87.

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Table 3-87. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK5_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK5 Clock Switchover Type. Selects whether BANK5 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0x0 = Immediate 0x1 = Glitchless
6	BANK4_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK4 Clock Switchover Type. Selects whether BANK4 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0x0 = Immediate 0x1 = Glitchless
5	BANK3_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK3 Clock Switchover Type. Selects whether BANK3 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0x0 = Immediate 0x1 = Glitchless
4	BANK2_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK2 Clock Switchover Type. Selects whether BANK2 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0x0 = Immediate 0x1 = Glitchless
3	BANK1_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK1 Clock Switchover Type. Selects whether BANK1 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. This bit is ignored unless BANK1_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = Immediate 0x1 = Glitchless
2	BANK0_CLK_SWITCHOVER_TYPE	R/W	0x1	BANK0 Clock Switchover Type. Selects whether BANK0 Automatic Clock Switchover/Switchback, Manual Clock Switchover via I2C, and PERST#-triggered Buffer Mode clock switching, are glitchless or not. 0x0 = Immediate 0x1 = Glitchless
1	BANK5_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK5 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK5 clock source is determined to be invalid. This bit is ignored unless BANK5_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1
0	BANK4_AUTO_CLK_SWITCHOVER_CLK_SEL	R/W	0x1	BANK4 Automatic Clock Switchover Clock Select. Selects the clock source that is switched to if the original BANK4 clock source is determined to be invalid. This bit is ignored unless BANK4_AUTO_CLK_SWITCHOVER_EN is set to 1. 0x0 = PATH0 0x1 = PATH1

3.86 R96 Register (Offset = 0x60) [Reset = 0xC0]

R96 is shown in Table 3-88.

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Table 3-88. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BANK1_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK1 Switchover. When enabled, changing BANK1_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK1_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK1_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK1_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK1_CLK_SEL through OTP page changing will not work. Changing the value of BANK1_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK1_CLK_SEL through OTP page changing will work. Changing the value of BANK1_CLK_SEL through I2C will not have an impact.
6	BANK0_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK0 Switchover. When enabled, changing BANK0_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK0_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK0_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK0_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK0_CLK_SEL through OTP page changing will not work. Changing the value of BANK0_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK0_CLK_SEL through OTP page changing will work. Changing the value of BANK0_CLK_SEL through I2C will not have an impact.
5	BANK5_CLK_DIS_ON_LOS	R/W	0x0	BANK5 Clock Disable on Loss-of-Signal. When enabled, if BANK5 is sourced by an input clock, and that input clock is determined to be invalid, BANK5 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK5_AUTO_CLK_SWITCHOVER_EN or BANK5 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS
4	BANK4_CLK_DIS_ON_LOS	R/W	0x0	BANK4 Clock Disable on Loss-of-Signal. When enabled, if BANK4 is sourced by an input clock, and that input clock is determined to be invalid, BANK4 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK4_AUTO_CLK_SWITCHOVER_EN or BANK4 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS
3	BANK3_CLK_DIS_ON_LOS	R/W	0x0	BANK3 Clock Disable on Loss-of-Signal. When enabled, if BANK3 is sourced by an input clock, and that input clock is determined to be invalid, BANK3 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK3_AUTO_CLK_SWITCHOVER_EN or BANK3 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS
2	BANK2_CLK_DIS_ON_LOS	R/W	0x0	BANK2 Clock Disable on Loss-of-Signal. When enabled, if BANK2 is sourced by an input clock, and that input clock is determined to be invalid, BANK2 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK2_AUTO_CLK_SWITCHOVER_EN or BANK2 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS

Table 3-88. R96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BANK1_CLK_DIS_ON_LOS	R/W	0x0	BANK1 Clock Disable on Loss-of-Signal. When enabled, if BANK1 is sourced by an input clock, and that input clock is determined to be invalid, BANK1 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK1_AUTO_CLK_SWITCHOVER_EN or BANK1 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS
0	BANK0_CLK_DIS_ON_LOS	R/W	0x0	BANK0 Clock Disable on Loss-of-Signal. When enabled, if BANK0 is sourced by an input clock, and that input clock is determined to be invalid, BANK0 clocks will be automatically disabled. Cannot be enabled simultaneously with BANK0_AUTO_CLK_SWITCHOVER_EN or BANK0 Buffer Mode. 0x0 = No LOS Disable 0x1 = Disabled on LOS

3.87 R97 Register (Offset = 0x61) [Reset = 0x0F]

R97 is shown in Table 3-89.

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Table 3-89. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT1_SLEW_RATE	R/W	0x0	OUT1 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT1. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT1 clock format and the VDDO_1_2 supply level. If OUT1 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT1_CMOS_SLEW_RATE). 0x0 = 2.4 V/ns - 3.7 V/ns 0x1 = 2.2 V/ns - 3.4 V/ns 0x2 = 2.0 V/ns - 3.1 V/ns 0x3 = 1.8 V/ns - 2.8 V/ns
5:4	OUT0_SLEW_RATE	R/W	0x0	OUT0 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT0. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT0 clock format and the VDDO_0 supply level. If OUT0 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT0_CMOS_SLEW_RATE). 0x0 = 2.4 V/ns - 3.7 V/ns 0x1 = 2.2 V/ns - 3.4 V/ns 0x2 = 2.0 V/ns - 3.1 V/ns 0x3 = 1.8 V/ns - 2.8 V/ns
3	BANK5_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK5 Switchover. When enabled, changing BANK5_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK5_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK5_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK5_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK5_CLK_SEL through OTP page changing will not work. Changing the value of BANK5_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK5_CLK_SEL through OTP page changing will work. Changing the value of BANK5_CLK_SEL through I2C will not have an impact.
2	BANK4_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK4 Switchover. When enabled, changing BANK4_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK4_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK4_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK4_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK4_CLK_SEL through OTP page changing will not work. Changing the value of BANK4_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK4_CLK_SEL through OTP page changing will work. Changing the value of BANK4_CLK_SEL through I2C will not have an impact.

Table 3-89. R97 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BANK3_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK3 Switchover. When enabled, changing BANK3_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK3_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK3_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK3_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK3_CLK_SEL through OTP page changing will not work. Changing the value of BANK3_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK3_CLK_SEL through OTP page changing will work. Changing the value of BANK3_CLK_SEL through I2C will not have an impact.
0	BANK2_SWITCHOVER_FRC_CLK_EN	R/W	0x1	Force BANK2 Switchover. When enabled, changing BANK2_CLK_SEL on OTP pages allows for switching between FODs and inputs, but changing BANK2_CLK_SEL via I2C will not change the active clock source. When disabled, changing BANK2_CLK_SEL on OTP pages does not allow for switching between FODs and inputs, but changing BANK2_CLK_SEL via I2C will change the active clock source. 0x0 = Switchover through I2C; Changing the value of BANK2_CLK_SEL through OTP page changing will not work. Changing the value of BANK2_CLK_SEL through I2C will have an impact. 0x1 = Switchover through OTP; Changing the value of BANK2_CLK_SEL through OTP page changing will work. Changing the value of BANK2_CLK_SEL through I2C will not have an impact.

3.88 R98 Register (Offset = 0x62) [Reset = 0x00]

R98 is shown in Table 3-90.

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Table 3-90. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT3_SLEW_RATE	R/W	0x0	OUT3 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT3. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT3 clock format and the VDDO_3 supply level. If OUT3 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT3_CMOS_SLEW_RATE). 0x0 = 2.4 V/ns - 3.7 V/ns 0x1 = 2.2 V/ns - 3.4 V/ns 0x2 = 2.0 V/ns - 3.1 V/ns 0x3 = 1.8 V/ns - 2.8 V/ns
5:4	OUT2_SLEW_RATE	R/W	0x0	OUT2 Slew Rate (differential and 1.2V LVCMOS). Controls the slew rate for OUT2. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the OUT2 clock format and the VDDO_2 supply level. If OUT2 is set for LVCMOS (except for 1.2V LVCMOS), this field will be ignored (see OUT2_CMOS_SLEW_RATE). 0x0 = 2.4 V/ns - 3.7 V/ns 0x1 = 2.2 V/ns - 3.4 V/ns 0x2 = 2.0 V/ns - 3.1 V/ns 0x3 = 1.8 V/ns - 2.8 V/ns
3:0	RESERVED	R	0x0	Reserved

3.89 R99 Register (Offset = 0x63) [Reset = 0x00]

R99 is shown in Table 3-91.

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Table 3-91. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT1_CMOS_SLEW_RATE	R/W	0x0	OUT1 Slew Rate (CMOS). Controls the slew rate for OUT1. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_1 supply level. If OUT1 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT1 is not configured for LVCMOS, this field will be ignored (see OUT1_SLEW_RATE). 0x0 = 3.1 V/ns - 5.2 V/ns 0x1 = 2.6 V/ns - 5 V/ns 0x2 = 1.7 V/ns - 4.0 V/ns 0x3 = 1.3 V/ns - 3.5 V/ns
5:4	OUT0_CMOS_SLEW_RATE	R/W	0x0	OUT0 Slew Rate (CMOS). Controls the slew rate for OUT0. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_0 supply level. If OUT0 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT0 is not configured for LVCMOS, this field will be ignored (see OUT0_SLEW_RATE). 0x0 = 3.1 V/ns - 5.2 V/ns 0x1 = 2.6 V/ns - 5 V/ns 0x2 = 1.7 V/ns - 4.0 V/ns 0x3 = 1.3 V/ns - 3.5 V/ns
3:0	RESERVED	R	0x0	Reserved

3.90 R100 Register (Offset = 0x64) [Reset = 0x00]

R100 is shown in Table 3-92.

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Table 3-92. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT3_CMOS_SLEW_RATE	R/W	0x0	OUT3 Slew Rate (CMOS). Controls the slew rate for OUT3. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_3_4 supply level. If OUT3 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT3 is not configured for LVCMOS, this field will be ignored (see OUT3_SLEW_RATE). 0x0 = 3.1 V/ns - 5.2 V/ns 0x1 = 2.6 V/ns - 5 V/ns 0x2 = 1.7 V/ns - 4.0 V/ns 0x3 = 1.3 V/ns - 3.5 V/ns
5:4	OUT2_CMOS_SLEW_RATE	R/W	0x0	OUT2 Slew Rate (CMOS). Controls the slew rate for OUT2. 0x0 is the fastest setting and 0x3 is the slowest setting. Actual slew rate depends on the VDDO_1_2 supply level. If OUT2 is set for differential or 1.2V LVCMOS, this field will be ignored. If OUT2 is not configured for LVCMOS, this field will be ignored (see OUT2_SLEW_RATE). 0x0 = 3.1 V/ns - 5.2 V/ns 0x1 = 2.6 V/ns - 5 V/ns 0x2 = 1.7 V/ns - 4.0 V/ns 0x3 = 1.3 V/ns - 3.5 V/ns
3:0	RESERVED	R	0x0	Reserved

3.91 R101 Register (Offset = 0x65) [Reset = 0xA0]

R101 is shown in Table 3-93.

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Table 3-93. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT1_DIS_STATE	R/W	0x2	OUT1 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0x0 = P/N: HIGH/LOW 0x1 = P/N: LOW/HIGH 0x2 = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 0x3 = P/N: HI-Z/HI-Z
5:4	OUT0_DIS_STATE	R/W	0x2	OUT0 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0x0 = P/N: HIGH/LOW 0x1 = P/N: LOW/HIGH 0x2 = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 0x3 = P/N: HI-Z/HI-Z
3:0	RESERVED	R	0x0	Reserved

3.92 R102 Register (Offset = 0x66) [Reset = 0x80]

R102 is shown in Table 3-94.

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Table 3-94. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT3_DIS_STATE	R/W	0x2	OUT3 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0x0 = P/N: HIGH/LOW 0x1 = P/N: LOW/HIGH 0x2 = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 0x3 = P/N: HI-Z/HI-Z
5:4	OUT2_DIS_STATE	R/W	0x0	OUT2 Disabled State. Selects the state of OUT0_P and OUT0_N when OUT0 is disabled. For AC-LVDS clocks, LOW/LOW must be selected. DC-LVDS clocks may select any disabled state. For either LVDS coupling, "LOW/LOW" is not descriptive of the output clock behavior; the output clock will instead behave as HIGH/LOW. 0x0 = P/N: HIGH/LOW 0x1 = P/N: LOW/HIGH 0x2 = P/N: LOW/LOW; For LVDS clocks, LOW/LOW is not valid, and if selected, HIGH/LOW will be used instead. 0x3 = P/N: HI-Z/HI-Z
3:0	RESERVED	R	0x0	Reserved

3.93 R103 Register (Offset = 0x67) [Reset = 0x00]

R103 is shown in Table 3-95.

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Table 3-95. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT0_FMT	R/W	0x0	OUT0 Clock Format. 0x0 = 100 Ω LP-HCSL 0x1 = 85 Ω LP-HCSL 0x2 = LVDS 0x3 = LVCMOS
5	REF1_DIS_STATE	R/W	0x0	REF1 Disabled State. Selects the state of REF1 when REF1 is disabled. 0x0 = LOW 0x1 = HI-Z
4	REF0_DIS_STATE	R/W	0x0	REF0 Disabled State. Selects the state of REF0 when REF0 is disabled. 0x0 = LOW 0x1 = HI-Z
3:0	RESERVED	R	0x0	Reserved

3.94 R104 Register (Offset = 0x68) [Reset = 0x00]

R104 is shown in Table 3-96.

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Table 3-96. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OUT2_FMT	R/W	0x0	OUT2 Clock Format. 0x0 = 100 Ω LP-HCSL 0x1 = 85 Ω LP-HCSL 0x2 = LVDS 0x3 = LVCMOS
5:2	RESERVED	R	0x0	Reserved
1:0	OUT1_FMT	R/W	0x0	OUT1 Clock Format. 0x0 = 100 Ω LP-HCSL 0x1 = 85 Ω LP-HCSL 0x2 = LVDS 0x3 = LVCMOS

3.95 R105 Register (Offset = 0x69) [Reset = 0x00]

R105 is shown in Table 3-97.

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Table 3-97. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	IN1_LOS	R/W	0x0	IN1 Loss-of-Signal. This is set to 1 to indicate that IN1 is currently invalid.

3.96 R106 Register (Offset = 0x6A) [Reset = 0x00]

R106 is shown in Table 3-98.

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Table 3-98. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1_CMOS_1P2V_EN	R/W	0x0	OUT1 1.2V CMOS Enable. When the clock format of OUT1 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_1_2 supply voltage. When the clock format of OUT1 is not configured for one of the LVCMOS options, this bit is ignored.
6	OUT0_CMOS_1P2V_EN	R/W	0x0	OUT0 1.2V CMOS Enable. When the clock format of OUT0 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_0 supply voltage. When the clock format of OUT0 is not configured for one of the LVCMOS options, this bit is ignored.
5:2	RESERVED	R	0x0	Reserved
1:0	OUT3_FMT	R/W	0x0	OUT3 Clock Format. 0x0 = 100 Ω LP-HCSL 0x1 = 85 Ω LP-HCSL 0x2 = LVDS 0x3 = LVCMOS

3.97 R107 Register (Offset = 0x6B) [Reset = 0x00]

R107 is shown in Table 3-99.

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Table 3-99. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	OUT3_CMOS_1P2V_EN	R/W	0x0	OUT3 1.2V CMOS Enable. When the clock format of OUT3 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_3_4 supply voltage. When the clock format of OUT3 is not configured for one of the LVCMOS options, this bit is ignored.
2	OUT2_CMOS_1P2V_EN	R/W	0x0	OUT2 1.2V CMOS Enable. When the clock format of OUT2 is configured for one of the LVCMOS options, this bit determines if the CMOS clock voltage will be 1.2V or if it will match the VDDO_1_2 supply voltage. When the clock format of OUT2 is not configured for one of the LVCMOS options, this bit is ignored.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.98 R108 Register (Offset = 0x6C) [Reset = 0xCC]

R108 is shown in Table 3-100.

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Table 3-100. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OUT1_OE_GRP	R/W	0xC	OUT1 Output Enable Group. This field determines whether or not OUT1 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT1 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3:0	OUT0_OE_GRP	R/W	0xC	OUT0 Output Enable Group. This field determines whether or not OUT0 is assigned to an output enable group. If is assigned to a group, this field also determines the group assignment. If not, this field also determines whether or not OUT0 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.99 R110 Register (Offset = 0x6E) [Reset = 0xCC]

R110 is shown in Table 3-101.

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Table 3-101. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OUT3_OE_GRP	R/W	0xC	OUT3 Output Enable Group. This field determines whether or not OUT3 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT3 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3:0	OUT2_OE_GRP	R/W	0xC	OUT2 Output Enable Group. This field determines whether or not OUT2 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not OUT2 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.100 R111 Register (Offset = 0x6F) [Reset = 0xCC]

R111 is shown in Table 3-102.

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Table 3-102. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REF1_OE_GRP	R/W	0xC	REF1 Output Enable Group. This field determines whether or not REF1 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not REF1 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.
3:0	REF0_OE_GRP	R/W	0xC	REF0 Output Enable Group. This field determines whether or not REF0 is assigned to an output enable group. If is assigned to an output enable group, this field also determines the output enable group assignment. If it is not assigned to an output enable group, this field also determines whether or not REF0 can be affected by a global output enable pin or the global output enable register field. 0x0 = 0: OE_GROUP_0 0x1 = 1: OE_GROUP_1 0x2 = 2: OE_GROUP_2 0x3 = 3: OE_GROUP_3 0x4 = 4: OE_GROUP_4 0xB = 11: Global OE Only; Not assigned. Affected by global output enable controls. 0xC = 12: No OE Group; Not assigned. Not affected by global output enable controls.

3.101 R112 Register (Offset = 0x70) [Reset = 0xBB]

R112 is shown in Table 3-103.

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Table 3-103. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OUT1_LPHCSL_VOD_SEL	R/W	0xB	Programmable LP-HCSL swing for channel 1 0x0 = 686 mV 0x1 = 714 mV 0x2 = 741 mV 0x3 = 768 mV 0x4 = 793 mV 0x5 = 817 mV 0x6 = 794 mV 0x7 = 820 mV 0x8 = 823 mV 0x9 = 847 mV 0xA = 872 mV 0xB = 896 mV 0xC = 921 mV 0xD = 945 mV 0xE = 969 mV 0xF = 993 mV
3:0	OUT0_LPHCSL_VOD_SEL	R/W	0xB	Programmable LP-HCSL swing for channel 0 0x0 = 686 mV 0x1 = 714 mV 0x2 = 741 mV 0x3 = 768 mV 0x4 = 793 mV 0x5 = 817 mV 0x6 = 794 mV 0x7 = 820 mV 0x8 = 823 mV 0x9 = 847 mV 0xA = 872 mV 0xB = 896 mV 0xC = 921 mV 0xD = 945 mV 0xE = 969 mV 0xF = 993 mV

3.102 R114 Register (Offset = 0x72) [Reset = 0xBB]

R114 is shown in Table 3-104.

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Table 3-104. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OUT3_LPHCSL_VOD_SEL	R/W	0xB	Programmable LP-HCSL swing for channel 3 0x0 = 686 mV 0x1 = 714 mV 0x2 = 741 mV 0x3 = 768 mV 0x4 = 793 mV 0x5 = 817 mV 0x6 = 794 mV 0x7 = 820 mV 0x8 = 823 mV 0x9 = 847 mV 0xA = 872 mV 0xB = 896 mV 0xC = 921 mV 0xD = 945 mV 0xE = 969 mV 0xF = 993 mV
3:0	OUT2_LPHCSL_VOD_SEL	R/W	0xB	Programmable LP-HCSL swing for channel 2 0x0 = 686 mV 0x1 = 714 mV 0x2 = 741 mV 0x3 = 768 mV 0x4 = 793 mV 0x5 = 817 mV 0x6 = 794 mV 0x7 = 820 mV 0x8 = 823 mV 0x9 = 847 mV 0xA = 872 mV 0xB = 896 mV 0xC = 921 mV 0xD = 945 mV 0xE = 969 mV 0xF = 993 mV

3.103 R116 Register (Offset = 0x74) [Reset = 0x00]

R116 is shown in Table 3-105.

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Table 3-105. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	OUT1_SYNC_MODE	R/W	0x0	OUT1 Synchronization Mode. Selects the output clock synchronization mode for OUT1. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved
1:0	OUT0_SYNC_MODE	R/W	0x0	OUT0 Synchronization Mode. Selects the output clock synchronization mode for OUT0. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved

3.104 R117 Register (Offset = 0x75) [Reset = 0x00]

R117 is shown in Table 3-106.

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Table 3-106. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	REF1_SYNC_MODE	R/W	0x0	REF1 Synchronization Mode. Selects the output clock synchronization mode for REF1. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved
5:4	REF0_SYNC_MODE	R/W	0x0	REF0 Synchronization Mode. Selects the output clock synchronization mode for REF0. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved
3:2	OUT3_SYNC_MODE	R/W	0x0	OUT3 Synchronization Mode. Selects the output clock synchronization mode for OUT3. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved

Table 3-106. R117 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OUT2_SYNC_MODE	R/W	0x0	OUT2 Synchronization Mode. Selects the output clock synchronization mode for OUT2. To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". For minimal delay, set this field to "No Sync Mode". 0x0 = Full Sync; To phase synchronize a group of output clocks, set the synchronization mode of each clock in the group to "Full Sync Mode", and either assign each output clock to the same output enable group or use a global output enable control. 0x1 = No Sync; For minimal delay, set this field to "No Sync Mode" 0x2 = Self Sync; If phase synchronization is not necessary, to guarantee at least 4 output clock cycles of delay between output enable assertion and the first output clock edge, set this field to "Self Sync Mode". 0x3 = Reserved

3.105 R118 Register (Offset = 0x76) [Reset = 0x1E]

R118 is shown in Table 3-107.

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Table 3-107. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT1N_OE_CMOS	R/W	0x1	OUT1N LVCMOS Output Enable. Controls whether or not OUT1N can produce an LVCMOS clock. For OUT1N to drive an LVCMOS clock, OUT1 must be enabled by all other output enable logic, OUT1 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
3	OUT1P_OE_CMOS	R/W	0x1	OUT1P LVCMOS Output Enable. Controls whether or not OUT1P can produce an LVCMOS clock. For OUT1P to drive an LVCMOS clock, OUT1 must be enabled by all other output enable logic, OUT1 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
2	OUT0N_OE_CMOS	R/W	0x1	OUT0N LVCMOS Output Enable. Controls whether or not OUT0N can produce an LVCMOS clock. For OUT0N to drive an LVCMOS clock, OUT0 must be enabled by all other output enable logic, OUT0 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
1	OUT0P_OE_CMOS	R/W	0x1	OUT0P LVCMOS Output Enable. Controls whether or not OUT0P can produce an LVCMOS clock. For OUT0P to drive an LVCMOS clock, OUT0 must be enabled by all other output enable logic, OUT0 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
0	SINGLE_CMOS_EN_SYNC	R/W	0x0	Global Single LVCMOS Enable Synchronization. Each differential output clock pair can be used as two LVCMOS clocks. These two clocks can be enabled/disabled using their respective OUTx_OE_CMOS_P or OUTx_OE_CMOS_N. This field, when set to 0x1, ensures that the enable/disable of the individual LVCMOS clocks, is synchronous with the output clock, such that there will be no runt pulses. 0x0 = Immediate; Immediately enable/disable the LVCMOS clocks, there may be runt pulses. 0x1 = Glitchless; Ensures that the enable/disable of the individual LVCMOS clocks, is synchronous with the output clock, such that there will be no runt pulses.

3.106 R119 Register (Offset = 0x77) [Reset = 0x1E]

R119 is shown in Table 3-108.

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Table 3-108. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	OUT3N_OE_CMOS	R/W	0x1	OUT3N LVCMOS Output Enable. Controls whether or not OUT3N can produce an LVCMOS clock. For OUT3N to drive an LVCMOS clock, OUT3 must be enabled by all other output enable logic, OUT3 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
3	OUT3P_OE_CMOS	R/W	0x1	OUT3P LVCMOS Output Enable. Controls whether or not OUT3P can produce an LVCMOS clock. For OUT3P to drive an LVCMOS clock, OUT3 must be enabled by all other output enable logic, OUT3 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
2	OUT2N_OE_CMOS	R/W	0x1	OUT2N LVCMOS Output Enable. Controls whether or not OUT2N can produce an LVCMOS clock. For OUT2N to drive an LVCMOS clock, OUT2 must be enabled by all other output enable logic, OUT2 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
1	OUT2P_OE_CMOS	R/W	0x1	OUT2P LVCMOS Output Enable. Controls whether or not OUT2P can produce an LVCMOS clock. For OUT2P to drive an LVCMOS clock, OUT2 must be enabled by all other output enable logic, OUT2 must be configured for an LVCMOS format that uses that pin, and this bit must be set to 0x1.
0	RESERVED	R	0x0	Reserved

3.107 R120 Register (Offset = 0x78) [Reset = 0x00]

R120 is shown in Table 3-109.

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Table 3-109. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT3_FREQ_DET_EN	R/W	0x0	OUT3 Frequency Detector Enable. Enables the frequency detectors for OUT3P and OUT3N. These detect when the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.
5	OUT2_FREQ_DET_EN	R/W	0x0	OUT2 Frequency Detector Enable. Enables the frequency detectors for OUT2P and OUT2N. These detect when the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OUT1_FREQ_DET_EN	R/W	0x0	OUT1 Frequency Detector Enable. Enables the frequency detectors for OUT1P and OUT1N. These detect when the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.
1	OUT0_FREQ_DET_EN	R/W	0x0	OUT0 Frequency Detector Enable. Enables the frequency detectors for OUT0P and OUT0N. These detect when the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
0	RESERVED	R	0x0	Reserved

3.108 R122 Register (Offset = 0x7A) [Reset = 0x00]

R122 is shown in Table 3-110.

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Table 3-110. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2_FREQ_DET_THRESH	R/W	0x0	OUT2 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT2 Frequency Detector to determine if OUT2P and OUT2N are valid or not. 0x0 = 1 MHz 0x1 = 25 MHz
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	OUT1_FREQ_DET_THRESH	R/W	0x0	OUT1 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT1 Frequency Detector to determine if OUT1P and OUT1N are valid or not. 0x0 = 1 MHz 0x1 = 25 MHz
3	OUT0_FREQ_DET_THRESH	R/W	0x0	OUT0 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT0 Frequency Detector to determine if OUT0P and OUT0N are valid or not. 0x0 = 1 MHz 0x1 = 25 MHz
2	REF1_FREQ_DET_EN	R/W	0x0	REF1 Frequency Detector Enable. Enables the frequency detector for REF1. This detects when the output clock frequency is below the threshold specified with REF1_FREQ_DET_THRESH.
1	REF0_FREQ_DET_EN	R/W	0x0	REF0 Frequency Detector Enable. Enables the frequency detector for REF0. This detects when the output clock frequency is below the threshold specified with REF0_FREQ_DET_THRESH.
0	RESERVED	R	0x0	Reserved

3.109 R123 Register (Offset = 0x7B) [Reset = 0x00]

R123 is shown in Table 3-111.

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Table 3-111. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT1_AMP_DET_EN	R/W	0x0	OUT1 Amplitude Detector Enable. Enables the amplitude detectors for OUT1P and OUT1N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
5	OUT0_AMP_DET_EN	R/W	0x0	OUT0 Amplitude Detector Enable. Enables the amplitude detectors for OUT0P and OUT0N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4	REF1_FREQ_DET_THRESH	R/W	0x0	REF1 Frequency Detector Threshold. Sets the frequency threshold that will be used by the REF1 Frequency Detector to determine if REF1 is valid or not. 0x0 = 1 MHz 0x1 = 25 MHz
3	REF0_FREQ_DET_THRESH	R/W	0x0	REF0 Frequency Detector Threshold. Sets the frequency threshold that will be used by the REF0 Frequency Detector to determine if REF0 is valid or not. 0x0 = 1 MHz 0x1 = 25 MHz
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	OUT3_FREQ_DET_THRESH	R/W	0x0	OUT3 Frequency Detector Threshold. Sets the frequency threshold that will be used by the OUT3 Frequency Detector to determine if OUT3P and OUT3N are valid or not. 0x0 = 1 MHz 0x1 = 25 MHz

3.110 R124 Register (Offset = 0x7C) [Reset = 0x00]

R124 is shown in Table 3-112.

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Table 3-112. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_AMP_DET_THRESH	R/W	0x0	OUTx Amplitude Detector Threshold. Sets the amplitude threshold that will be used by all of the output amplitude detectors. 0x0 = 100 mV/300 mV 0x1 = 150 mV / 350 mV
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OUT3_AMP_DET_EN	R/W	0x0	OUT3 Amplitude Detector Enable. Enables the amplitude detectors for OUT3P and OUT3N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1	OUT2_AMP_DET_EN	R/W	0x0	OUT2 Amplitude Detector Enable. Enables the amplitude detectors for OUT2P and OUT2N. These detect when the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
0	RESERVED	R	0x0	Reserved

3.111 R125 Register (Offset = 0x7D) [Reset = 0x00]

R125 is shown in Table 3-113.

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Table 3-113. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_ERROR_EVT_INTR_EN	R/W	0x0	OTP CRC Event Interrupt Enable. The value of this field determines whether or not the OTP CRC Error contributes to the Device Interrupt
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	IN0_LOS_LMT_EVT_INTR_EN	R/W	0x0	IN0 Loss-of-Signal Limit Event Interrupt Enable. The value of this field determines whether or not the IN0 Loss-of-Signal Limit Event contributes to the Device Interrupt
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	IN0_LOS_EVT_INTR_EN	R/W	0x0	IN0 Loss-of-Signal Event Interrupt Enable. The value of this field determines whether or not the IN0 Loss-of-Signal Event contributes to the Device Interrupt
0	DEV_INTR	R	0x0	Device Interrupt. Indicates if one or more enabled interrupts have been asserted. Once this field is set, it is cleared only when all contributing interrupt event status fields have been cleared via I2C. The enables for each of the interrupt flags are not stored in OTP, and must be set through I2C after startup for interrupt detection.

3.112 R126 Register (Offset = 0x7E) [Reset = 0x00]

R126 is shown in Table 3-114.

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Table 3-114. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT1N_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT1N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT1N_FREQ_ERR_EVT should contribute to the device interrupt signal.
2	OUT1P_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT1P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT1P_FREQ_ERR_EVT should contribute to the device interrupt signal.
1	OUT0N_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT0N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT0N_FREQ_ERR_EVT should contribute to the device interrupt signal.
0	OUT0P_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT0P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT0P_FREQ_ERR_EVT should contribute to the device interrupt signal.

3.113 R127 Register (Offset = 0x7F) [Reset = 0x00]

R127 is shown in Table 3-115.

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Table 3-115. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT3N_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT3N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT3N_FREQ_ERR_EVT should contribute to the device interrupt signal.
2	OUT3P_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT3P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT3P_FREQ_ERR_EVT should contribute to the device interrupt signal.
1	OUT2N_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT2N Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT2N_FREQ_ERR_EVT should contribute to the device interrupt signal.
0	OUT2P_FREQ_ERR_EVT_INTR_EN	R/W	0x0	OUT2P Frequency Error Event Interrupt Enable. Determines whether or not assertions of OUT2P_FREQ_ERR_EVT should contribute to the device interrupt signal.

3.114 R128 Register (Offset = 0x80) [Reset = 0x00]

R128 is shown in Table 3-116.

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Table 3-116. R128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT1N_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT1N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT1N_AMP_ERR_EVT should contribute to the device interrupt signal.
4	OUT1P_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT1P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT1P_AMP_ERR_EVT should contribute to the device interrupt signal.
3	OUT0N_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT0N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT0N_AMP_ERR_EVT should contribute to the device interrupt signal.
2	OUT0P_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT0P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT0P_AMP_ERR_EVT should contribute to the device interrupt signal.
1	REF1_FREQ_ERR_EVT_INTR_EN	R/W	0x0	REF1 Frequency Error Event Interrupt Enable. Determines whether or not assertions of REF1_FREQ_ERR_EVT should contribute to the device interrupt signal.
0	REF0_FREQ_ERR_EVT_INTR_EN	R/W	0x0	REF0 Frequency Error Event Interrupt Enable. Determines whether or not assertions of REF0_FREQ_ERR_EVT should contribute to the device interrupt signal.

3.115 R129 Register (Offset = 0x81) [Reset = 0x00]

R129 is shown in Table 3-117.

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Table 3-117. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	OUT3N_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT3N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT3N_AMP_ERR_EVT should contribute to the device interrupt signal.
4	OUT3P_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT3P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT3P_AMP_ERR_EVT should contribute to the device interrupt signal.
3	OUT2N_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT2N Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT2N_AMP_ERR_EVT should contribute to the device interrupt signal.
2	OUT2P_AMP_ERR_EVT_INTR_EN	R/W	0x0	OUT2P Amplitude Error Event Interrupt Enable. Determines whether or not assertions of OUT2P_AMP_ERR_EVT should contribute to the device interrupt signal.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.116 R130 Register (Offset = 0x82) [Reset = 0x10]

R130 is shown in Table 3-118.

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Table 3-118. R130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	IN0_LOS_EVT	R/W	0x1	IN0 Loss-of-Signal Event. Indicates whther or not IN0_LOS has been asserted since this field was last cleared. 0x0 = No LOS Event 0x1 = LOS Event Detected
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.117 R131 Register (Offset = 0x83) [Reset = 0x00]

R131 is shown in Table 3-119.

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Table 3-119. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	IN0_LOS_CNTR	R	0x0	IN0 Loss-of-Signal Counter Readback. Reading this field returns the current value of the IN0 Loss-of-Signal Counter, which represents the number of times that IN0_LOS has been asserted since IN0_LOS_LMT_EVT was cleared. After the device power-up sequence finishes (output clocks are ready to be driven out), this counter starts from 0, and is incremented by 1 each time IN0_LOS is asserted. The counter is cleared if the device is reset via the PWRGD_PWRDN# GPIO function, and when the IN0_LOS_LMT_EVT field is written with a 1.

3.118 R132 Register (Offset = 0x84) [Reset = 0x20]

R132 is shown in Table 3-120.

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Table 3-120. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	LOS_LMT	R/W	0x2	Loss-of-Signal Limit. The maximum allowable INx Loss-of-Signal events that can occur before the corresponding INx_LOS_LMT_EVT field is set.
3:0	RESERVED	R	0x0	Reserved

3.119 R133 Register (Offset = 0x85) [Reset = 0x20]

R133 is shown in Table 3-121.

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Table 3-121. R133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT0N_FREQ_GOOD	R	0x0	OUT0N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
6	OUT0P_FREQ_GOOD	R	0x0	OUT0P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT0_FREQ_DET_THRESH.
5	CRC_ERROR_EVT	R/W	0x1	OTP CRC Event. Set to 1 when CRC_ERROR transitions from 0 (CRC OK or CRC Check In Progress) to 1 (CRC Error).
4	CRC_ERROR	R	0x0	CRC Check Status 0 ==> Normal ; 1==> CRC Error (data corruption)
3	CRC_DONE	R	0x0	CRC status. 1 == > CRC computation is done
2:1	RESERVED	R	0x0	Reserved
0	IN0_LOS_LMT_EVT	R/W	0x0	IN0 Loss-of-Signal Limit Event. Indicates whether or not the number of IN0 Loss-of-Signal events has exceeded the value of LOS_LMT, since the last time this field was cleared. Write a '1' to this field to clear the IN0 LOS LMT EVENT counter. 0x0 = LOS_LMT Not Exceeded 0x1 = LOS_LMT Exceeded

3.120 R134 Register (Offset = 0x86) [Reset = 0x00]

R134 is shown in Table 3-122.

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Table 3-122. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT2N_FREQ_GOOD	R	0x0	OUT2N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
6	OUT2P_FREQ_GOOD	R	0x0	OUT2P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT2_FREQ_DET_THRESH.
5:2	RESERVED	R	0x0	Reserved
1	OUT1N_FREQ_GOOD	R	0x0	OUT1N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.
0	OUT1P_FREQ_GOOD	R	0x0	OUT1P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT1_FREQ_DET_THRESH.

3.121 R135 Register (Offset = 0x87) [Reset = 0x00]

R135 is shown in Table 3-123.

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Table 3-123. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REF1_FREQ_GOOD	R	0x0	REF1 Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with REF1_FREQ_DET_THRESH.
6	REF0_FREQ_GOOD	R	0x0	REF0 Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with REF0_FREQ_DET_THRESH.
5:2	RESERVED	R	0x0	Reserved
1	OUT3N_FREQ_GOOD	R	0x0	OUT3N Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.
0	OUT3P_FREQ_GOOD	R	0x0	OUT3P Frequency Detector Good. Live status bit that indicates whether or not the output clock frequency is below the threshold specified with OUT3_FREQ_DET_THRESH.

3.122 R136 Register (Offset = 0x88) [Reset = 0x0F]

R136 is shown in Table 3-124.

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Table 3-124. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT1N_FREQ_ERR_EVT	R/W1C	0x1	OUT1N Frequency Error Event Flag. Set to 1 when OUT1N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT1P_FREQ_ERR_EVT	R/W1C	0x1	OUT1P Frequency Error Event Flag. Set to 1 when OUT1P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT0N_FREQ_ERR_EVT	R/W1C	0x1	OUT0N Frequency Error Event Flag. Set to 1 when OUT0N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT0P_FREQ_ERR_EVT	R/W1C	0x1	OUT0P Frequency Error Event Flag. Set to 1 when OUT0P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).

3.123 R137 Register (Offset = 0x89) [Reset = 0x0F]

R137 is shown in Table 3-125.

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Table 3-125. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT3N_FREQ_ERR_EVT	R/W1C	0x1	OUT3N Frequency Error Event Flag. Set to 1 when OUT3N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
2	OUT3P_FREQ_ERR_EVT	R/W1C	0x1	OUT3P Frequency Error Event Flag. Set to 1 when OUT3P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
1	OUT2N_FREQ_ERR_EVT	R/W1C	0x1	OUT2N Frequency Error Event Flag. Set to 1 when OUT2N_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
0	OUT2P_FREQ_ERR_EVT	R/W1C	0x1	OUT2P Frequency Error Event Flag. Set to 1 when OUT2P_FREQ_GOOD transitions from 1 (Good) to 0 (Error).

3.124 R138 Register (Offset = 0x8A) [Reset = 0x03]

R138 is shown in Table 3-126.

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Table 3-126. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT1N_AMP_GOOD	R	0x0	OUT1N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4	OUT1P_AMP_GOOD	R	0x0	OUT1P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
3	OUT0N_AMP_GOOD	R	0x0	OUT0N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
2	OUT0P_AMP_GOOD	R	0x0	OUT0P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1	REF1_FREQ_ERR_EVT	R/W1C	0x1	REF1 Frequency Error Event Flag. Set to 1 when REF1_FREQ_GOOD transitions from 1 (Good) to 0 (Error).
0	REF0_FREQ_ERR_EVT	R/W1C	0x1	REF0 Frequency Error Event Flag. Set to 1 when REF0_FREQ_GOOD transitions from 1 (Good) to 0 (Error).

3.125 R139 Register (Offset = 0x8B) [Reset = 0x00]

R139 is shown in Table 3-127.

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Table 3-127. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	OUT3N_AMP_GOOD	R	0x0	OUT3N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
4	OUT3P_AMP_GOOD	R	0x0	OUT3P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
3	OUT2N_AMP_GOOD	R	0x0	OUT2N Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
2	OUT2P_AMP_GOOD	R	0x0	OUT2P Amplitude Detector Good. Live status bit that indicates whether or not the output clock amplitude is below the threshold specified with OUT_AMP_DET_THRESH.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.126 R140 Register (Offset = 0x8C) [Reset = 0xF0]

R140 is shown in Table 3-128.

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Table 3-128. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT1N_AMP_ERR_EVT	R/W1C	0x1	OUT1N Amplitude Error Event Flag. Set to 1 when OUT1N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT1P_AMP_ERR_EVT	R/W1C	0x1	OUT1P Amplitude Error Event Flag. Set to 1 when OUT1P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT0N_AMP_ERR_EVT	R/W1C	0x1	OUT0N Amplitude Error Event Flag. Set to 1 when OUT0N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT0P_AMP_ERR_EVT	R/W1C	0x1	OUT0P Amplitude Error Event Flag. Set to 1 when OUT0P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
3:0	RESERVED	R	0x0	Reserved

3.127 R141 Register (Offset = 0x8D) [Reset = 0xF0]

R141 is shown in Table 3-129.

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Table 3-129. R141 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT3N_AMP_ERR_EVT	R/W1C	0x1	OUT3N Amplitude Error Event Flag. Set to 1 when OUT3N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
6	OUT3P_AMP_ERR_EVT	R/W1C	0x1	OUT3P Amplitude Error Event Flag. Set to 1 when OUT3P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
5	OUT2N_AMP_ERR_EVT	R/W1C	0x1	OUT2N Amplitude Error Event Flag. Set to 1 when OUT2N_AMP_GOOD transitions from 1 (Good) to 0 (Error).
4	OUT2P_AMP_ERR_EVT	R/W1C	0x1	OUT2P Amplitude Error Event Flag. Set to 1 when OUT2P_AMP_GOOD transitions from 1 (Good) to 0 (Error).
3:0	RESERVED	R	0x0	Reserved

3.128 R143 Register (Offset = 0x8F) [Reset = 0x02]

R143 is shown in Table 3-130.

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Table 3-130. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PROD_REV_ID	R	0x2	4 product ID/revision ID

3.129 R144 Register (Offset = 0x90) [Reset = 0x02]

R144 is shown in Table 3-131.

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Table 3-131. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OTP_ID	R	0x2	OTP ID. Loaded from the OTP, this field is used to identify the device's OTP configuration.

3.130 R147 Register (Offset = 0x93) [Reset = 0x5B]

R147 is shown in Table 3-132.

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Table 3-132. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	UNLOCK_PROTECTED_REG	R/W	0x5B	Internal register unlock, write "0x5B" to unlock the write operation for protected registers.

3.131 R148 Register (Offset = 0x94) [Reset = 0x00]

R148 is shown in Table 3-133.

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Table 3-133. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	VDDD_SUP_LVL_DET_RB	R	0x0	VDDD Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDD. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V
1:0	VDDA_SUP_LVL_DET_RB	R	0x0	VDDA Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDA. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V

3.132 R149 Register (Offset = 0x95) [Reset = 0x00]

R149 is shown in Table 3-134.

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Table 3-134. R149 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	VDDO_3_SUP_LVL_DET_RB	R	0x0	VDDO_3 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_3. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V
5:4	VDDO_2_SUP_LVL_DET_RB	R	0x0	VDDO_2 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_2. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V
3:2	VDDO_1_SUP_LVL_DET_RB	R	0x0	VDDO_1 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_1. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V
1:0	VDDO_0_SUP_LVL_DET_RB	R	0x0	VDDO_0 Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDDO_0. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V

3.133 R150 Register (Offset = 0x96) [Reset = 0x00]

R150 is shown in Table 3-135.

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Table 3-135. R150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:4	VDD_REF_SUP_LVL_DET_RB	R	0x0	VDD_REF Supply Level Detector Readback. Reading this field returns a 2-bit code corresponding to the detected supply level for VDD_REF. 0x0 = 3.3 V 0x1 = 1.8 V 0x2 = 2.5 V 0x3 = <1.8 V
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.134 R187 Register (Offset = 0xBB) [Reset = 0x92]

R187 is shown in Table 3-136.

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Table 3-136. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC_COMPUTED	R/W	0x92	Computed CRC, calculated at startup. The computed CRC includes the stored CRC in the calculation. If the stored CRC is correct, then the computed CRC will be 0 and CRC_ERROR will be 0. Otherwise, the computed CRC will be non-zero and CRC_ERROR will be 1.

3.135 R188 Register (Offset = 0xBC) [Reset = 0x00]

R188 is shown in Table 3-137.

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Table 3-137. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	BOOTOSC_CLK_DIS	R/W	0x0	Forcibly select Boot oscillator clock as system clock
0	RESERVED	R	0x0	Reserved

3.136 R253 Register (Offset = 0xFD) [Reset = 0x00]

R253 is shown in Table 3-138.

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Table 3-138. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PAGE_SEL_0	R/W	0x0	Register Page Select. Writing this field changes the register page that is accessble via I2C. Each collection of 256 registers forms a register page. Corresponding PAGE_SEL fields exist in the same location on each register page. In other words, PAGE_SEL_0 in R253[0], PAGE_SEL_1 in R509[0], PAGE_SEL_2 in R765[0], and PAGE_SEL_3 in R1021[0]. All PAGE_SEL_x fields share the same behavior.

3.137 R319 Register (Offset = 0x13F) [Reset = 0x01]

R319 is shown in Table 3-139.

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Table 3-139. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	CLK_READY	R/W	0x1	FOD Clocks Ready. This is set to 1 to indicate that the FODs are currently ready to be used as a clock source.

3.138 R576 Register (Offset = 0x240) [Reset = 0x00]

R576 is shown in Table 3-140.

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Table 3-140. R576 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	OUT0_DIS	R/W	0x0	OUT0 Disable. When set to 0, all other contributors are considered to determine if OUT0 should be enabled. When set to 1, OUT0 is disabled.

3.139 R580 Register (Offset = 0x244) [Reset = 0x00]

R580 is shown in Table 3-141.

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Table 3-141. R580 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	OUT1_DIS	R/W	0x0	OUT1 Disable. When set to 0, all other contributors are considered to determine if OUT1 should be enabled. When set to 1, OUT1 is disabled.

3.140 R592 Register (Offset = 0x250) [Reset = 0x00]

R592 is shown in Table 3-142.

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Table 3-142. R592 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	OUT2_DIS	R/W	0x0	OUT2 Disable. When set to 0, all other contributors are considered to determine if OUT2 should be enabled. When set to 1, OUT2 is disabled.

3.141 R596 Register (Offset = 0x254) [Reset = 0x00]

R596 is shown in Table 3-143.

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Table 3-143. R596 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	OUT3_DIS	R/W	0x0	OUT3 Disable. When set to 0, all other contributors are considered to determine if OUT3 should be enabled. When set to 1, OUT3 is disabled.

3.142 R600 Register (Offset = 0x258) [Reset = 0x01]

R600 is shown in Table 3-144.

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Table 3-144. R600 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	REF0_DIS	R/W	0x1	REF0 Disable. When set to 0, all other contributors are considered to determine if REF0 should be enabled. When set to 1, REF0 is disabled.

3.143 R604 Register (Offset = 0x25C) [Reset = 0x01]

R604 is shown in Table 3-145.

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Table 3-145. R604 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	REF1_DIS	R/W	0x1	REF1 Disable. When set to 0, all other contributors are considered to determine if REF1 should be enabled. When set to 1, REF1 is disabled.

3.144 R624 Register (Offset = 0x270) [Reset = 0x00]

R624 is shown in Table 3-146.

Return to the Summary Table.

Table 3-146. R624 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	PATH1_FOD_SEL	R/W	0x0	FOD PATH1 Post-divider FOD Select. Selects the clock that is used as the input to the FOD PATH1 Post-divider. This field is locked, and requires unlocking UNLOCK_PROTECTED_REG before using. 0x0 = FOD0 0x1 = FOD1
0	RESERVED	R	0x0	Reserved

3.145 R745 Register (Offset = 0x2E9) [Reset = 0x00]

R745 is shown in Table 3-147.

Return to the Summary Table.

Table 3-147. R745 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT1P_INV_POL	R/W	0x0	OUT1P Polarity Inversion.
5	OUT0P_INV_POL	R/W	0x0	OUT0P Polarity Inversion.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3.146 R746 Register (Offset = 0x2EA) [Reset = 0x00]

R746 is shown in Table 3-148.

Return to the Summary Table.

Table 3-148. R746 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT1N_INV_POL	R/W	0x0	OUT1N Polarity Inversion.
5	OUT0N_INV_POL	R/W	0x0	OUT0N Polarity Inversion.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OUT3P_INV_POL	R/W	0x0	OUT3P Polarity Inversion.
1	OUT2P_INV_POL	R/W	0x0	OUT2P Polarity Inversion.
0	RESERVED	R	0x0	Reserved

3.147 R747 Register (Offset = 0x2EB) [Reset = 0x00]

R747 is shown in Table 3-149.

Return to the Summary Table.

Table 3-149. R747 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	OUT3N_INV_POL	R/W	0x0	OUT3N Polarity Inversion.
1	OUT2N_INV_POL	R/W	0x0	OUT2N Polarity Inversion.
0	RESERVED	R	0x0	Reserved

3.148 R762 Register (Offset = 0x2FA) [Reset = 0x00]

R762 is shown in Table 3-150.

Return to the Summary Table.

Table 3-150. R762 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DIE_ID_1[7:0]	R	0x0	X-coor [7:0], LOT ID[23:16]

3.149 R763 Register (Offset = 0x2FB) [Reset = 0x00]

R763 is shown in Table 3-151.

Return to the Summary Table.

Table 3-151. R763 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DIE_ID_1[14:8]	R	0x0	X-coor [7:0], LOT ID[23:16]

3.150 R764 Register (Offset = 0x2FC) [Reset = 0x00]

R764 is shown in Table 3-152.

Return to the Summary Table.

Table 3-152. R764 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DIE_ID_2[7:0]	R	0x0	LOT ID[15:0]

3.151 R766 Register (Offset = 0x2FE) [Reset = 0x00]

R766 is shown in Table 3-153.

Return to the Summary Table.

Table 3-153. R766 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DIE_ID_2[15:8]	R	0x0	LOT ID[15:0]

3.152 R767 Register (Offset = 0x2FF) [Reset = 0x00]

R767 is shown in Table 3-154.

Return to the Summary Table.

Table 3-154. R767 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DIE_ID_3[7:0]	R	0x0	Spare third word for DIE_ID

3.153 R768 Register (Offset = 0x300) [Reset = 0x00]

R768 is shown in Table 3-155.

Return to the Summary Table.

Table 3-155. R768 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DIE_ID_3[15:8]	R	0x0	Spare third word for DIE_ID

3.154 R769 Register (Offset = 0x301) [Reset = 0x01]

R769 is shown in Table 3-156.

Return to the Summary Table.

Table 3-156. R769 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	ALTERNATE_OE_SEL	R/W	0x1	When GPI2 and GPIO0 adopt the alternate output enable personality, this bit selects which OE table these two pins adhere to. When set to 0, these pins follow the behavior outlined in "Alternative OE Mapping 1" in the datasheet. When set to 1, these pins follow the behavior outlined in "Alternative OE Mapping 2" in the datasheet.

3.155 R770 Register (Offset = 0x302) [Reset = 0x00]

R770 is shown in Table 3-157.

Return to the Summary Table.

Table 3-157. R770 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STORED_CRC	R/W	0x0	Stored CRC

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

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