Entering Standby and Halt Mode on F05 Devices

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Abstract

This paper will explain how to enter standy and halt modes on the TMS470R1VFx family of devices. The TMS470R1VFx family of devices scheme for entering low power mode is slightly different than the scheme used for the TMS470R1Fx family of devices. This difference is in how the Flash Module is configued prior to entering the device standby or halt mode. This difference is the source for this paper. For a more detailed functional description of the Flash Module, see the *TMS470R1x F05 Flash Module Reference Guide*.

Overview

This document will explain the procedures for entering standby and halt mode on the TMS470R1VFx family of devices. There is a difference in how the TMS470R1VFx family of devices enter standby and halt mode and the way the TMS470R1Fz family of devices enter standby and sleep mode.

In the TMS470R1Fx family of devices, standby and halt mode are enter by setting the device into standby and halt mode and then executing a the IDLE instruction. On the TMS470R1VFx family of devices, the Flash Module must first be configured for sleep mode before entering device standby or halt mode.

The Flash Module consists of the flash banks, charge pump, power and mode control logic, data path, burst logic, and write/erase state machines. Flash banks are a group of flash sectors which share input/output buffers, data paths, sense amplifiers and control logic. The charge pump consists of voltage generators and associated control (logic, oscillator, bandgap, etc.).

Device Low Power Modes

There are two low power modes that can be entered on the TMS470R1VFx family of devices. They are

(1.) Standby Mode

(2.) Halt Mode

Standby Mode

When the TMS470R1VFx device is in standby mode, the oscillator, ACLK (the output clock from the oscillator/PLL prior to the prescale divider) and RTICLK (operates at the same frequency and is in phase with SYSCLK) are active. SYSCLK (provides clock to the RAM, HET, Flash Control Register, Flash, System Module and DMA), ICLK (generated from SYSCLK and provides clock to the peripheral modules) and MCLK (provides clock to the CPU) are inactive.

Halt Mode

When the TMS470R1VFx device is in halt mode, the oscillator, ACLK, RTICLK, SYSCLK, ICLK and MCLK are inactive.

Flash Sleep Mode

When the Flash Module enters sleep mode, both banks and charge pump are asleep. While the banks are asleep, both the sense reference and the sense amplifiers are disabled. While the charge pump is in sleep mode, all circuits are disabled.

Example

Register	Description	Address
e_SARSYS_ST.ClkCntl_UW	**CLKCNTL** Configures the CLKOUT pin and a bit that controls the module low power mode. See the *TMS470R1x System Module Reference Guide* (literature number SPNU189).	0xFFFFFFD0
e_SARSYS_ST.GlbCtrl_UW	**GLBCTRL** Controls the PLL and one bit configures the Flash Module. See the *TMS470R1x System Module Reference Guide* (literature number SPNU166)	0xFFFFFFDC
e_FLASH1_ST.Bac1_UN.Bac1_UW	**FMBAC1** The Bank Access Control Register 1 (BAC1) is a half-word-access only register. It controls bank standby mode wait state generation, bank fall back power mode and bank Active Grace Period (AGP) delay. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).	0xFFE88000
e_FLASH1_ST.Bac2_UN.Bac2_UW	**FMBAC2** The Bank Access Control Register 2 (BAC1) is a half-word-access only register. It controls special burst and standard read wait state generation, bank sleep delay, and OTP sector protection. There is one BAC2 register for each bank in the Flash module. The bank is selected via BANK[2:0] of the MAC2 register. Since only one bank at a time can be selected by MAC2, only the selected bank's register appears at this address. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).	0xFFE88004
e_FLASH2_ST.Mac1_UN.Mac1_UW	**FMMAC1** The Module Access Control Register 2 is a half-word-access only register. It supports Pump sleep wait state generation and Level 1 protection. MAC1 is a global register; therefore, there is only one for the entire Flash module regardless of the number of banks present. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).	0xFFE8BC00

Register	Description	Address
e_FLASH2_ST.Mac2_UN.Mac2_UW	**FMMAC2** The Module Access Control Register 2 is a half-word-access only register. It supports control port operation, pump fallback power module and pump standby wait state generation. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).	0xFFE8BC04

Halt Mode

```
/* BEGIN INITIALIZATION */
/* Enter flash configuration mode, PLL clock divider is divide-by-8 */
e_SARSYS_ST.GlbCtrl_UW = 0x1F;
/* Set bank sleep wait states (the number of wait state cycles from sleep mode to active */
/* mode), page read wait states and standard read wait states */
e_FLASH1_ST.Bac2_UN.Bac2_UW = 0x7F00;
/* Set pump sleep wait states (the number of wait state cycles from sleep mode to */
/* active mode) */
e_FLASH2_ST.Mac1_UN.Mac1_UW = 0x7FFF;
/* Clear the flash configuration bit */
e_SARSYS_ST.GlbCtrl_UW = 0x0F;
                :
                : APPLICATION CODE GOES HERE
                :
/* PUT DEVICE INTO STANDBY/HALT AND FLASH MODULE INTO SLEEP MODE */
/* Enter flash configuration mode, PLL  clock divider is divide-by-8 */
e_SARSYS_ST.GlbCtrl_UW = 0x1F;
/* Bank0 is put to sleep, set bank active grace period and bank standby wait states */
e_FLASH1_ST.Bac1_UN.Bac1_UW = 0xFFFC;
/* Pump is put to sleep, set pump standby wait states and select bank to enter */
/* sleep mode */
e_FLASH2_ST.Mac2_UN.Mac2_UW = 0xFFE0;
/* Put device into standby or halt mode */
e_SARSYS_ST.sys_clkcntl_UN.clkcntl_ST.lpm_B2 = 3;        /* 3 for Halt */
                                                         /* 2 for Standby*/
dummy = e_SARSYS_ST.sys_clkcntl_UN.clkcntl_ST.lpm_B2;    /* Perform a dummy read */
                :
                :
                :
/* UPON ANY WAKEUP, CLEAR FLASH CONFIGURATION BIT */
/* Clear the flash configuration bit */
e_SARSYS_ST.GlbCtrl_UW = 0x0F;
```

Note

If the device has more than one bank of Flash, then the user should implement the following lines of code for each bank

```
/* Bank0 is put to sleep, set bank active grace period and bank standby wait states */
e_FLASH1_ST.Bac1_UN.Bac1_UW = 0xFFFC;
/* Pump is put to sleep, set pump standby wait states and select bank to enter */
/* sleep mode */
e_FLASH2_ST.Mac2_UN.Mac2_UW = 0xFFE0;
```

To change the bank of Flash that will enter into standby or sleep mode, the three least significant bits (BANK[2:0]) of the MAC2 register need to be modified. Below is a table showing this relationship.

BANK[2]	BANK[1]	BANK[0]	Bank	Hex
0	0	0	0	0
0	0	1	1	1
0	1	0	2	2
0	1	1	3	3
1	0	0	4	3
1	0	1	5	4
1	1	0	6	6
1	1	1	7	7

IMPORTANT NOTICE