

SPI Slave Transmit Timing

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1 Introduction

Several versions of the SPI on TI TMS470 devices transmit on the receive edge of the SPI clock (SPCLK) in slave mode (SOMI). This functionality was added as an enhancement to increase the speed of SPI transfers.

Because of the design implementation, the SOMI signal is generated with enough setup and hold time relative to the SPI clock to guarantee correct data transfer at the speeds used on devices that contain a non-edge-programmable version of the SPI module.

Note:

Recent versions of the SPI contain a control bit that allows user code to program whether the SPI in slave mode transmits on the transmit or the receive edge of the SPI clock.

2 Slave Mode SPI Signals

The following are the signals the SPI outputs or takes as input:

- SPICLK—Input
- SPISIMO—Input
- SPISOMI—Output

All the timing diagrams given in the following sections are with Phase = 0 and Polarity = 0, unless explicitly stated otherwise.

3 Edge Detection of SPICLK

The SPI clock is sampled by the internal clock (ICLK), which generates an internal edge detection signal. The internal edge detection logic and the ICLK are used by the slave-mode SPI to generate the SOMI signal. Edge detection occurs on both the falling edge (Figure 1) and the rising edge (Figure 2) of ICLK.

As a consequence of edge detection, the slave's ICLK must always be faster than the SPICLK.

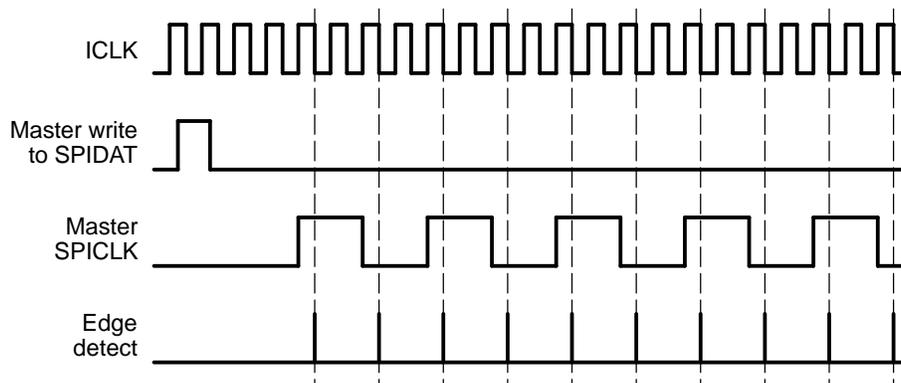


Figure 1. SPI Clock Change Detected by ICLK Falling Edge during Slave Mode

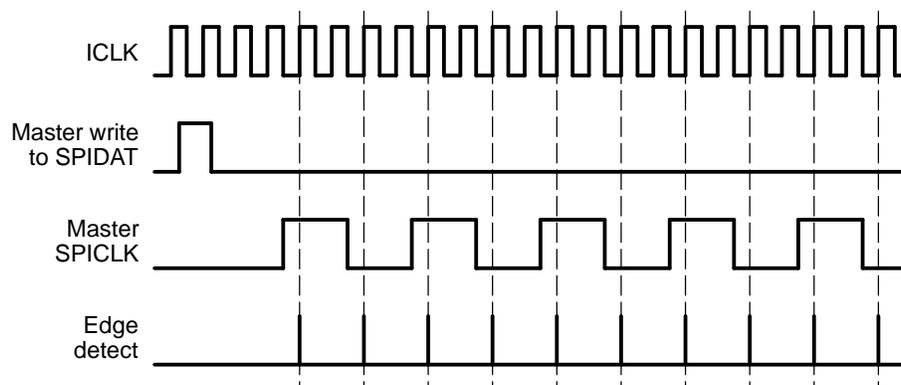


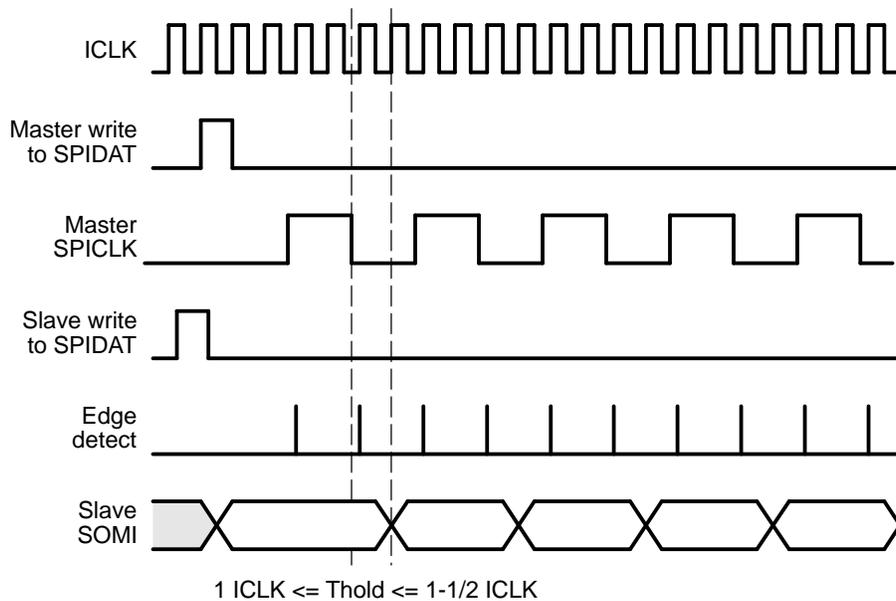
Figure 2. SPI Clock Change Detected by ICLK Rising Edge during Slave Mode

4 Generation of SOMI on Next ICLK Rising Edge

The internal clock, ICLK, is used to generate the SOMI signal. First, the clock is sampled (either on the falling edge or the rising edge of ICLK). Then, on the rising edge of ICLK, the SOMI signal is transmitted.

Figure 3 shows the worst-case hold time for the SOMI signal. That is, after the SPI clock is sampled on the falling edge of ICLK, the SOMI signal is driven on the next rising edge of ICLK.

In the worst case, the minimum hold time for the SOMI signal is given by 1/2 the period of ICLK. The maximum hold time is give by 1 period of ICLK. Buffer delays and trace delays are also added to the hold time.

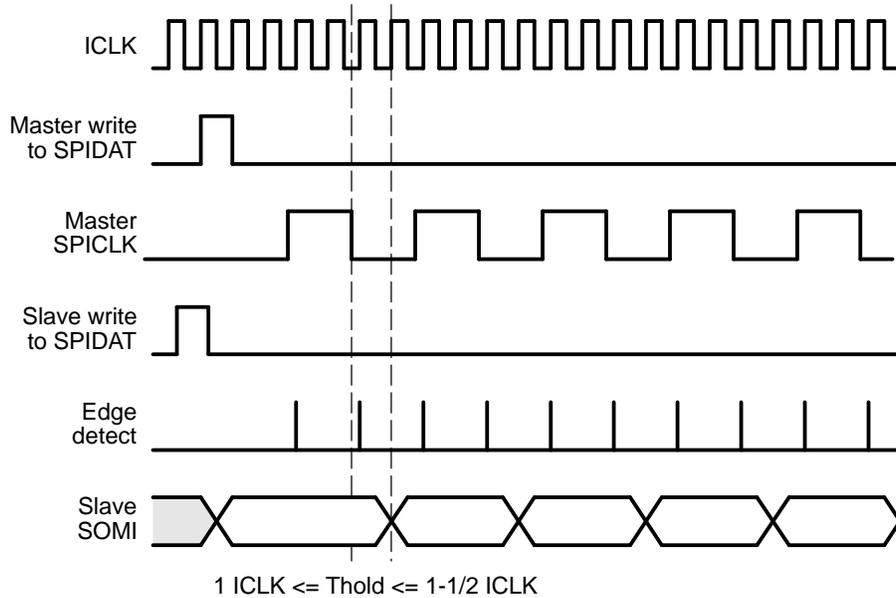


A The minimum hold time for SOMI occurs when SPICLK is sampled on the falling edge of ICLK.

Figure 3. SPICLK Sampled on ICLK Falling Edge

Generation of SOMI on Next ICLK Rising Edge

Figure 4 shows the hold time for the SOMI signal when SPICLK is sampled on the rising edge of ICLK. In this case, the SOMI signal is driven on the next rising edge of ICLK. The hold time for the SOMI signal in this case is a minimum of 1 ICLK period, up to 1-1/2 ICLK periods. Of course, any buffer delays and trace delays are also added to the hold time.



A The maximum hold time for SOMI occurs when SPICLK is sampled on the rising edge of ICLK.

Figure 4. SPICLK Sampled on ICLK Rising Edge

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