

TMS470R1x Clock Divider Module (CDM) Reference Guide

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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Contents

1	Overview	9
2	Functional Description	11
2.1	Basic Clock Module Operation	11
2.2	Module Pins	12
3	Operation	13
3.1	Resonator/Crystal Oscillato	r13
3.2	Clock Monitor	13
3.3	Clock Counter and Delay Control	14
3.4	Divide-by-R Prescale	r14
4	Control Registers	16
4.1	Global Control Register (GLBCTRL)	16
5	Application Information	19
5.1	Clock Start-up From Power Up (Non-BYPASS)	19
5.2	Clock Start-up From Exit HALT Mode (Non-BYPASS)	20
5.3	Clock Start-up from Power Up (BYPASS)	21

Contents

Figures

1	Clock Module Block Diagram	11
2	Reference Resonator / Crystal	13
3	Clock Module Control Bits and Flags	16
4	Global Control Register (GLBCTRL)	16
5	Start-up From Power Up (Non-BYPASS)	20
6	ACLK Start-up (Non-BYPASS)	21
7	Start-up From Power Up (BYPASS)	22

Clock Divider Module (CDM)

This reference guide describes the clock divider module (CDM) that provides ACLK to the clock control module (CCM) located in the system module. The CCM subsequently provides SYSCLK and ICLK for all other TMS470 modules. ACLK in this document should not be confused with the ADC internal clock, ADCLK.

Topic	Page
1 Overview.....	9
2 Functional Description	11
3 Operation	13
4 Control Registers.....	16
5 Application Information	19

1 Overview

The clock divider module generates the system clock, ACLK, from an external resonator/crystal reference. It is limited to 2.1–20 MHz crystals and resonators. The oscillator gain is inadequate to support overtone crystals with tank circuits.

This module contains a crystal oscillator, clock monitor circuit, clock enable circuit, and prescaler.

The simple oscillator's main advantage is very low jitter, simplicity of design and relative insensitivity to external noise.

Main features:

- Oscillator operates with both resonators and crystals
- Covers external OSCIN frequencies from 4 MHz to 20 MHz
- Generates ACLK frequencies from 500 kHz to 20 MHz
- $f_{\text{ACLK}} = f_{\text{OSCIN}} / \text{prescale}$
- Prescale value can be 1, 2, 3, 4, 5, 6, 7, or 8
- User option bit to reset device if resonator/crystal failure is detected
- Control/Status registers subset-compatible with APLL / ZPLL registers

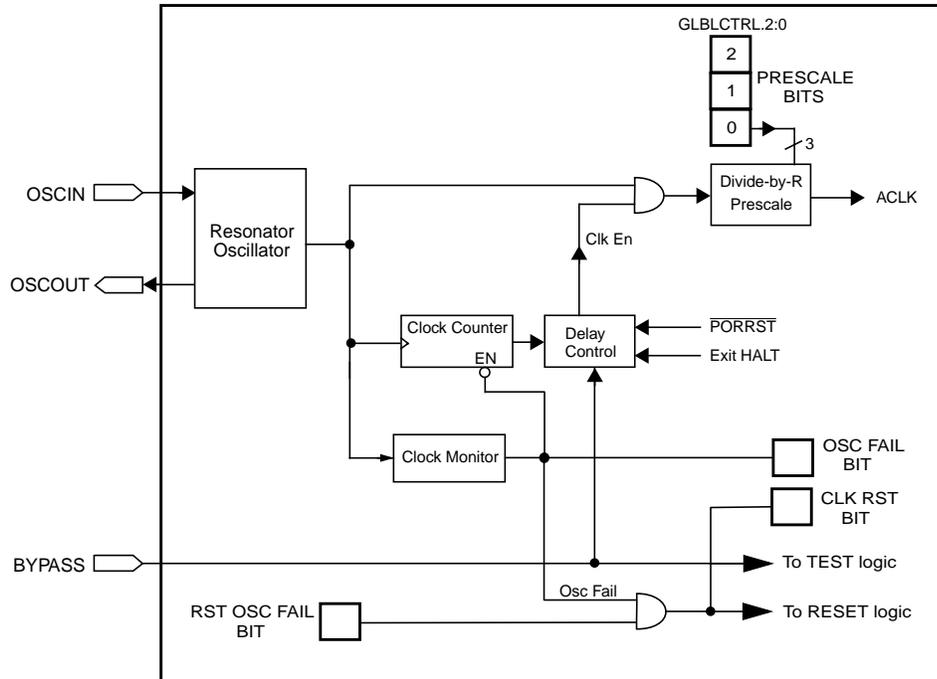
Terms used in this chapter include:

- ❑ Electromagnetic Interference (EMI): The radio frequency noise radiated by a circuit which could disturb the proper operation of other equipment, or the radio frequency noise radiated by other equipment which could disturb the proper operation of the subject circuit.
- ❑ Jitter: The maximum positive or negative deviation of a clock edge with respect to its nominal position within a single clock period, expressed in nanoseconds or in percent of one clock period.

2 Functional Description

The following section is a functional overview of the clock module. The simplified block diagram of Figure 1 shows the clock module with all of its component blocks.

Figure 1. Clock Module Block Diagram



2.1 Basic Clock Module Operation

The resonator/crystal is made to oscillate by the resonator oscillator circuit whose output is scaled by the prescaler block resulting in ACLK.

During power up or exit from HALT mode, the clock counter and delay control blocks control the release of ACLK and/or RESET. These blocks create a delay which keep the device from executing instructions until the oscillator has achieved sufficient amplitude.

The clock monitor detects some failures of the external resonator/crystal and provides a fail flag to the system module. Optionally, a system reset can be forced if such a failure is detected.

2.2 Module Pins

A total of three pins are required for the operation of the clock module shown in Figure 1. These pins are described below.

The crystal oscillator requires two pins (OSCIN and OSCOUT) for the crystal plus the external load capacitors. The load capacitors tie back to the nearest VSS pin. The oscillator's bias resistor is integrated, so no external bias resistor is needed.

The CDM has a BYPASS pin that provides compatibility for the older APLL. When the PLLDIS pin is active, the 4096-cycle delay is disabled.

Note: Replacement of APLL

If the older APLL was being used in bypass mode (no PLL frequency multiplication), then the CDM module can also be used in bypass mode as a drop-in replacement; however, the CDM module is *not* a drop-in replacement if the APLL being replaced was being operated in *non-bypass* mode.

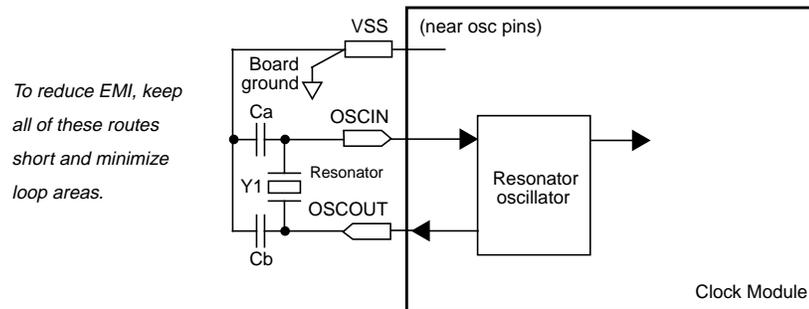
3 Operation

The paragraphs below explain the blocks found in the clock divider module and which are illustrated in Figure 1.

3.1 Resonator/Crystal Oscillator

The oscillator requires two external pins: OSCIN and OSCOUT which are connected to the resonator/crystal and load capacitors (Figure 2). The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled only during leakage test measurements.

Figure 2. Reference Resonator / Crystal



Note: Validating Resonator/Crystal Vendors

Texas Instruments strongly encourages each customer to submit samples of the microcontroller device to the resonator/crystal vendor for validation. They are equipped to determine what load capacitors will best tune their resonator/crystal to the device for optimum start-up and operation over temperature/voltage extremes. They also factor in margin for variations in the microcontroller's process variations.

The load capacitors should be grounded back to the nearest device ground pin with a private run as short as practical to minimize Electromagnetic Interference (EMI).

3.2 Clock Monitor

If the oscillator should slow to less than a hundred kilohertz or stop (including OSCIN *stuck high* or *stuck low*), the clock monitor's output will become active and set the OSC FAIL bit (see the specific device data sheet for the minimum and maximum oscillator detection frequencies).

The Clock Monitor output sets the OSC FAIL bit in the Global Status register of the System module indicating that a failure of the oscillator has been detected. Once set, this bit remains set until cleared by software or until a system reset or power-on reset.

Setting the RST OSC FAIL EN bit in the Global Control register of the System module will cause the device to undergo a system reset in the event that an oscillator failure is detected. In this case, the CLK RST flag in the System Exception Status register of the System module also becomes set and will stay set until written to a zero, or until a power-on reset ($\overline{\text{PORRST}}$) is performed.

A system reset ($\overline{\text{RESET}}$) will hold the system clocks for 4096 oscillator cycles. See Section 5.

The common failure mode of the oscillator is to stop if any of the PC board traces are opened (detectable failure); however, it is possible for the resonator to become damaged and speed up in frequency. This type of failure is *not* detected by the clock monitor circuit. If the oscillator stops, no operation will be possible except for a system reset (if the RST OSC FAIL EN bit was set before the failure occurred).

3.3 Clock Counter and Delay Control

The clock counter and delay control are used to delay the start of code execution following a power-up reset or when exiting HALT mode to allow for the oscillator to start up. The clock counter counts 4096 oscillator cycles after the oscillator monitor detects resonator/crystal oscillation.

In non-bypass mode, after $\overline{\text{PORRST}}$ occurs the timer holds off $\overline{\text{RESET}}$ until the 4096 oscillator cycles have elapsed. When exiting HALT mode, $\overline{\text{ACLK}}$ is held for 4096 oscillator cycles. Both of these mechanisms avoid code execution before good clocks are available to the system.

In bypass mode (BYPASS pin high) the 4096 clock delay is disabled during both power up and exit-HALT operations. When using the module in bypass, it is the user's responsibility to hold $\overline{\text{RESET}}$ or $\overline{\text{PORRST}}$ until the oscillator has had adequate time to start and stabilize. Also, HALT should not be used with BYPASS mode since the clocks will not be good when they are re-enabled and there is no reset during HALT.

3.4 Divide-by-R Prescaler

The user can divide the oscillator output by any integer value from 1 to 8 by programming the Clock Divider Prescale bits in the Global Control register, GLBCTRL.2:0 of the System module. Programming these bits causes a glitch-free transition from the current frequency to the frequency specified by

Operation

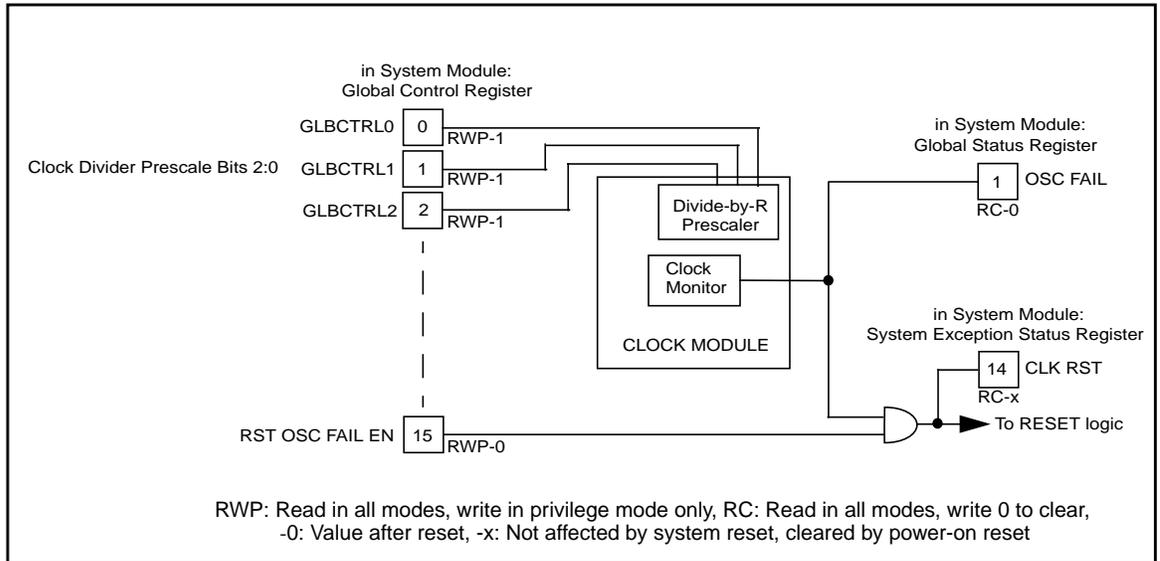
the bits. The default at power-up is divide-by-eight; therefore, the initial frequency will be equal to 1/8 the external resonator/crystal frequency.

Care must be taken with duty cycle when providing an external oscillator source if the module is to be used with a divide-by-one prescale value. If the duty cycle differs excessively from 50%, then the device may fail at higher frequencies. Refer to the specific device data sheet for minimum oscillator high and low times.

4 Control Registers

The clock module has no registers of its own; it relies on bits in three different registers within the system module. Figure 3 below shows a summary of all clock module bits.

Figure 3. Clock Module Control Bits and Flags



The Clock module generates the OSC FAIL flag. When this flag becomes set, the user has the option to cause a system reset to occur. This action is enabled by the RST OSC FAIL EN bit. When enabled and an oscillator failure is detected, the CLK RST flag is also set.

4.1 Global Control Register (GLBCTRL)

All but one bit of the Global Control register bits are reserved for the Clock module; one bit enables Flash module configuration. See Figure 4. Any write to this register asserts three wait states.

Figure 4. Global Control Register (GLBCTRL)



Control Registers

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RST OSC FAIL EN	Reserved										FL CON- FIG	Rsv	CLK DIV PRE[2:0]		
	RWP-0	U										RWP-0	U	RWP-111		

R = Read in all modes, WP = write in privilege mode only, U = Undefined; -n = Value after reset

Bits 31:16 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 15 **RST OSC FAIL EN. Reset on Oscillator Failure Enable**

When set, this bit causes a system reset to occur if a detectable oscillator failure occurs. When cleared, the status of the oscillator monitor can be checked by reading the OSC FAIL bit in the Global Status register of the System module.

Bits 14:5 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 4 **FLCONFIG. Flash Configuration Enable**

This bit enables write access to the Flash module's control registers. See the chapter on the Flash module for details of this bit's usage.

Bit 3 **Reserved**

Read values are indeterminate. Writes have no effect.

Bits 2:0 **CLK DIV PRE[2:0]: Clock Divider Prescale bits**

The Clock Divider Prescale bits determine the divisor of the VCO output. Programming these bits causes a glitch-free transition from the current frequency to the frequency specified by the bits.

The default at power-up is divide-by-eight; therefore, the initial frequency will be 1/8th the resonator/crystal frequency.

Table 1. Clock Divider Prescale Bits

GLBCTRL 2	GLBCTRL 1	GLBCTRL 0	Clock Divisor
1	1	1	8 (default at power-up)
1	1	0	7
1	0	1	6
1	0	0	5
0	1	1	4
0	1	0	3
0	0	1	2
0	0	0	1

5 Application Information

This section gives practical information about the use of the Clock module.

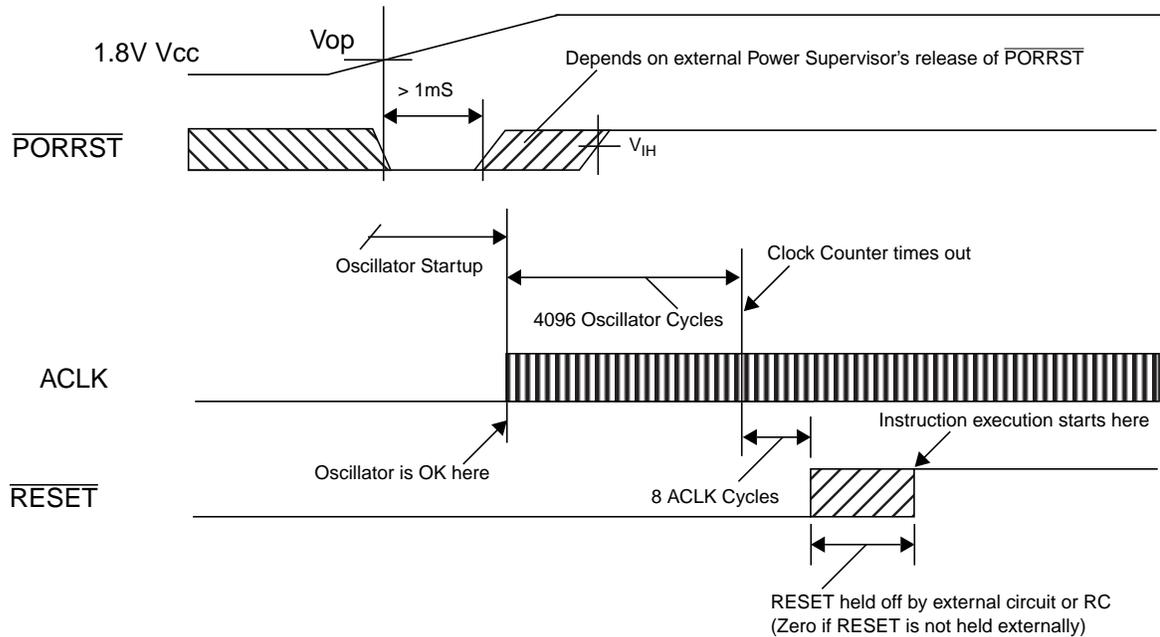
5.1 Clock Start-up From Power Up (Non-BYPASS)

With the onset of power, the following basic sequence of events occurs before the system clocks are enabled. Figure 5 highlights this timing. Note that the timing at power-on-reset is different from the timing when exiting HALT mode mainly due to no reset being performed when exiting HALT. Also, V_{cc} is already present and stable when exiting HALT.

If the RST OSC FAIL EN bit is set and an oscillator failure is detected, a reset will occur. If the oscillator condition is temporary and becomes operational again, the same basic sequence of events as described for power up will occur. See Figure 5.

- 1) **Power-up ramp:** The user supplies V_{cc} to the device along with \overline{PORRST} which needs to be valid above V_{op} (V_{op} is the V_{cc} voltage, below which the device is non-operational).
- 2) **Oscillator start-up:** As V_{cc} ramps up, the oscillator will start even before V_{op} is achieved. The oscillations will grow in amplitude with time. Once the oscillations are large enough, the oscillator output will start switching, allowing subsequent logic to start functioning.
- 3) **ACLK starts:** ACLK will start as soon as the oscillator starts. Initial clock periods may have invalid duty cycles; however, the device is still in reset so there is no ill effect.
- 4) **4096 oscillator cycles:** The clock counter will start incrementing as soon as \overline{PORRST} has been released and the oscillator has started. Once the clock counter has counted 4096 oscillator cycles, it will release the internal reset logic. If the clock monitor detects a pause in the output of the oscillator for any reason, the counter will reset and the count down of the 4096 cycles will start again.
- 5) **8 ACLK cycles:** Once the reset logic is released, the system module continues to hold internal reset as well as external \overline{RESET} active for an additional eight ACLK cycles before releasing them.
- 6) **Reset held off by external circuit:** Any external pull-downs or RC networks connected to \overline{RESET} will further delay the release of \overline{RESET} (both internally and externally).

Figure 5. Start-up From Power Up (Non-BYPASS)

**Note: Other Devices Connected to \overline{RESET} Externally**

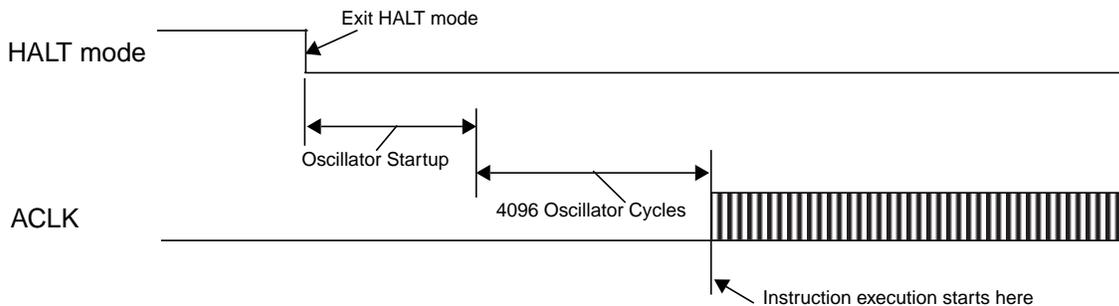
If other devices are connected to \overline{RESET} externally, keep in mind that the exact time at which internal reset is released in the TMS470R1x may differ significantly from the time when these other devices are released internally. This is due to differences in threshold levels on the reset pins of the different devices in your circuit. The time difference is made worse as the slope (rise time) of the \overline{RESET} signal is increased. While this is typically not a difficult problem to avoid, it needs to be comprehended in software when communicating to external devices immediately after power up.

5.2 Clock Start-up From Exit HALT Mode (Non-BYPASS)

During HALT mode, the oscillator is shut off. When HALT mode is exited, the following basic sequence of events occurs before the CPU can start executing instructions.

- 1) **Exit HALT mode:** Some device-level event occurs which removes the HALT signal and enables the oscillator.
- 2) **Oscillator Start-up:** The oscillations will grow in amplitude with time. Once the oscillations are large enough, the oscillator output will start switching, allowing subsequent logic to start functioning.

Figure 6. ACLK Start-up (Non-BYPASS)



- 3) **4096 Oscillator Cycles:** After the clock counter has counted 4096 cycles, it will enable ACLK. If the clock monitor detects a pause in the output of the oscillator for any reason, the counter will reset and the count down of the 4096 cycles will start again.
- 4) **ACLK Release:** ACLK will be enabled by the completion of the 4096 clock cycles. When ACLK starts, the CPU will resume instruction execution if no other modules are requesting wait states.

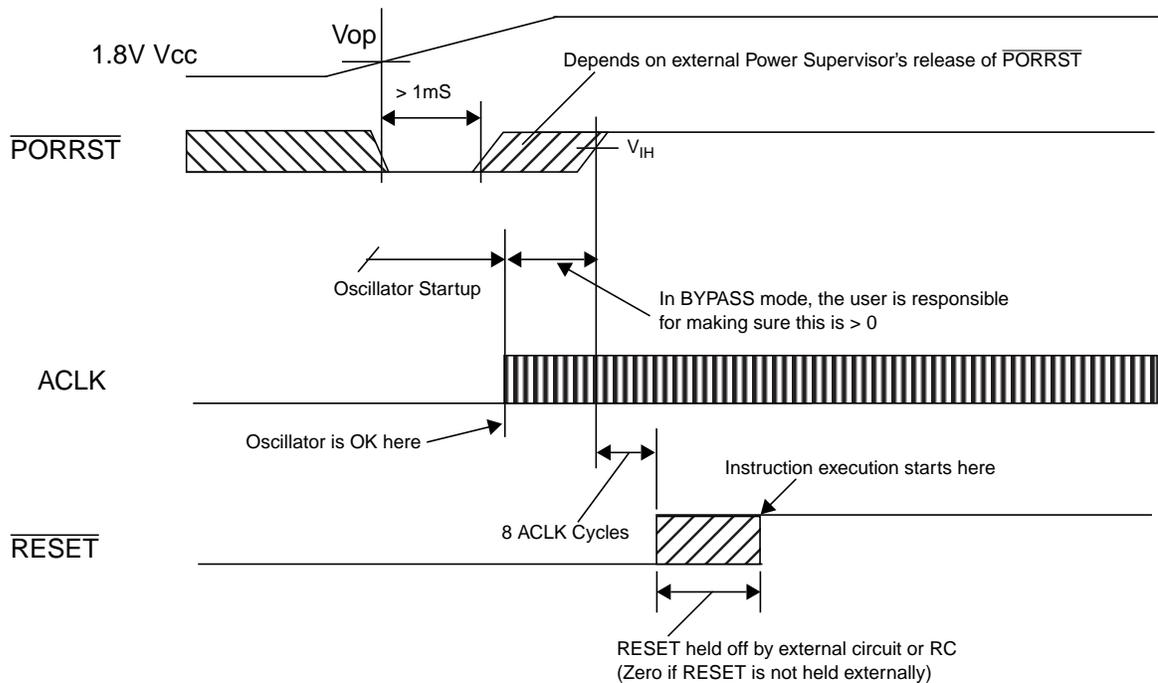
5.3 Clock Start-up from Power Up (BYPASS)

In BYPASS mode, with the onset of power, the following basic sequence of events occurs before the system clocks are enabled. Figure 7 highlights this timing.

If the RST OSC FAIL EN bit is set and an oscillator failure is detected, a reset will occur. If the oscillator condition is temporary and becomes operational again, the same basic sequence of events as described for power up will occur. See Figure 7.

- 1) **Power-up Ramp:** The user supplies V_{CC} to the device along with \overline{PORRST} which needs to be valid above V_{op} (V_{op} is the V_{CC} voltage, below which the device is non-operational).
- 2) **Oscillator Start-up:** As V_{CC} ramps up, the oscillator will start even before V_{op} is achieved. The oscillations will grow in amplitude with time. Once the oscillations are large enough, the oscillator output will start switching, allowing subsequent logic to start functioning.
- 3) **ACLK Starts:** ACLK will start as soon as the oscillator starts. Initial clock periods may have invalid duty cycles; however, if the device is still in reset, there will be no ill effect.
- 4) **Release of \overline{PORRST} :** When used in bypass mode, It is the user's responsibility to be sure that \overline{PORRST} is held off until after the oscillator amplitude is good.
- 5) **8 ACLK Cycles:** Once the reset logic is released, the system module continues to hold internal reset as well as external \overline{RESET} active for an additional eight ACLK cycles before releasing them.
- 6) **Reset held off by external circuit:** Any external pull-downs or RC networks connected to \overline{RESET} will further delay the release of \overline{RESET} (both internally and externally).

Figure 7. Start-up From Power Up (BYPASS)



Application Information
