TMS470R1VC338, TMS470R1VC348

TMS470 Microcontrollers

Silicon Errata

SPNZ128
October 2004

Contents

1 Known Design Marginality/Exceptions to Functional Specifications

The following is a list of advisories on modules in the K version of silicon. Documentation may differ from the user guide or data sheet. The advisory reference number is shown first (i.e.; CCM#1), followed by a description and any known workarounds. The reference numbers may not always be sequential for this device.

Modules include the following:

Clock control module (CCM)

ROM pipeline wrapper (RPW)

Real-time interrupt (RTI)

Standard CAN controller (SCC)

Serial peripheral interface (SPI)

Zero-pin phase-locked loop (ZPLL)

Advisory CCM#1	*ICLK Not 50% Duty Cycle*

Description: The ICLK signal output from the CCM is not a 50% duty cycle signal when the SYSCLK to ICLK divide ratio is odd. This affects the SCI and SPI modules and occurs when the divide ratio is 3 or above.

Workaround: None

Advisory RPW#1	*Wrong Opcode After Return Instruction*

Description: Under some circumstances, the ROM in pipeline mode will return the wrong opcode after executing an instruction in which the internal address bus changes during an internal CPU cycle. The instructions most likely to cause this problem are:

- LDR pc, [address]
- LDM Rd, [list of regs, ,pc]
- POP {Rlist, PC}

Workaround: Do not use the ROM in pipeline mode.

While it is possible that some codes run in pipeline mode will not contain the critical sequence of instruction and data reads that causes this problem, Texas Instruments will not generally release a ROM code on material containing this erratum.

Advisory RTI#3 — *Tap Interrupt When Clearing Counter*

Description: Write accesses to the RTICNTR register will clear the CNTR (21 bit counter), which causes a Tap interrupt if the corresponding bit switches from a “1” to a “0”.

Workaround: Disable the RTI prior to changing the RTICNTR value.

Advisory RTI#4 — *Tap Interrupt When Clearing Counter in Suspend Mode*

Description: Write accesses to the RTICNTR register will clear the CNTR (21 bit counter), which causes a Tap interrupt if the corresponding bit switches from a “1” to a “0” when the suspend signal is asserted.

Workaround: This is the same problem as RTI#3, however, on the initial fix of RTI#3, the case where the suspend signal is asserted because of an emulator breakpoint was not considered. This problem occurs when the emulator has set a breakpoint on one of the instructions closely following the instruction which writes to the counter.

Advisory SCC#4 — *Delayed Frame Error*

Description: Due to the proposed update of the ISO-WD-16485 CAN Test specification (2001−05−31), the SCC on this device has a non-conformance to the Bosch CAN Specification and the ISO-11898 Standard as described below.

If the following conditions are met, the CAN does not perform a re-synchronization as it is expected.

Conditions:

1. The node must be transmitter
2. The node must transmit a dominant bit
3. The dominant bit must be sampled back as recessive
4. A recessive to dominant edge must be detected after the sample point

But since the recessive sampling of the bit transmitted as dominant is an error anyway, an error frame will be transmitted at the beginning of the following bit.

Therefore, the effect of the non-conformance is a delay of this error frame. The maximum for this delay is five (max(SJW) + 1 Tq) time quanta.

Workaround: This non-conformance is classified as non-serious and does not have any impact on proper communication and inter-operability with other nodes. See above description.

Advisory SCC#5 — *Pins Are High Impedance in Low Power Mode*

Description: Regardless of how the CANSTX or CANSRX pins are configured, they become general purpose inputs when entering low power mode.

Workaround: If the pin is not driven externally, which is usually the case with the CANSTX pin, an external pull-up or pull-down resistor should be added to avoid consuming extra current in low power mode.

Advisory SCC#6 — *CANSRX Must be High During Self-test*

Description: The CANSRX pin must be high during self-test.

Workaround: The CANSRX pin is usually driven high by the bus transceiver. As long as there is no bus activity during the self-test, this is not a problem. If there is nothing driving the CANSRX pin, it can be configured as a digital output and set high during the self-test.

Advisory SCC#7 — *Abort Acknowledge Bit Not Set After Transmission Request Reset*

Description: After aborting a message using the Transmission Request Reset (TRR) register bit, there are some rare instances where the TRR bit will clear without setting the Abort Acknowledge (AA) bit.

In order for this rare condition to occur all the following three conditions must happen:

1. The current message has a message error or lost arbitration. This message does not need to have the same mailbox number as the following TRR bit mailbox.
2. The TRS bit of the same mailbox as the TRR mailbox must be set from either this current message, prior to the current message and still pending, or just set.
3. The TRR bit must be set in the exact ICLK cycle were the wrapper state machine is in IDLE for one cycle. (One ICLK before or after and the condition will not occur). This IDLE state can occur just after the current message. It can also occur just a few ICLKs after setting the TRS bit of any mailbox after the current message (point 1 above).

If these conditions occur then the TRR and TRS bits for the mailbox will clear t_{clr} ICLKs after the TRR bit is set where:

$$\mathbf{t_{clr} = ((16-mailbox\_number)*2)+3 \quad ICLK\ cycles}$$

The TA and AA bits will not be set if this condition occurs. Normally, either the TA or AA bit sets after TRR bit goes to zero.

Workaround: When this problem occurs, the TRR and TRS bits will clear within t_{clr} ICLK cycles. To check for this condition, first disable the interrupts. Check the TRR bits' t_{clr} ICLK cycles after setting the TRR bits to make sure that they are still set. A set TRR bit indicates the problem did not occur. If TRR is cleared, then maybe it was the normal end of a message and the TA or AA bits are set. Check both the TA and AA bits. If they are both zero, then the conditions did occur. Handle the condition like the interrupt service routine would, except that the AA bit does not need clearing now. If the TA or AA bit is set, then the normal interrupt routine will happen when the interrupt is re-enabled.

Advisory SPI#1 — *Slave Baud Rate Setting*

Description: When the SPI is operated in slave mode, the SPI clock must be configured to a baud rate less than or equal to the master SPI clock, but not so slow that there are less than two slave device ICLK cycles for each actual SPICLK period. An SPI baud rate for the slave too much slower than the actual SPI baud rate of the master will delay the assertion of the SPInENA signal from the slave, allowing for the possibility that the master will start a new SPI transmission before the slave is ready.

Workaround: The documentation will be updated to reflect this requirement. (SPNU195C, 7/2003)

Advisory SPI#2 — *Clearing, Setting SPI EN Bit Does Not Clear Internal Flag*

Description: Clearing and then setting the SPI EN bit does not clear an internal flag that indicates there is valid data in the SPI data register. This could lead to an inadvertent overrun error. The software should do a dummy read of SPIBUF after setting the SPIEN bit to clear the internal flag.

Workaround: The documentation will be update to reflect this requirement. (SPNU195C, 7/2003)

Advisory ZPLL#1 — *Clock Corruption When Changing Multiplier*

Description: All interrupt requests coming to the CIM module must be disabled when changing between multiply-by-4 and multiply-by-8.

Workaround: Disable the interrupt request at the peripheral source if possible.

Advisory ZPLL#2 — *High Halt Current*

Description: High IDDQ current consumption due to an incorrect tie-off of internal unused signals.

Workaround: None

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