TMS320FLEX Family Messaging System Solutions With Numeric Decoder Design Manual

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Preface

Read This First

About This Manual

The Texas Instruments (TI™) *TMS320FLEX Family Messaging System Solutions With Numeric Decoder Design Manual* describes the products that can be used to design embedded messaging functionality into computers, automobiles, and smart home electronics. This manual is part of a set of three manuals developed for this purpose (see *Related Documentation*).

This set of documents provides detailed information on the TLV5590 decoder and the analog-to-digital converters that enable you to develop embedded messaging functions that implement the FLEX protocol. Interfacing these components to your existing receivers and microcontrollers means that your application will required little, if any, hardware redesign.

The following decoders can be used with either the TLV5590 or TLV5592 converter to create a customized application.

- TLV5591BVF Alphanumeric Decoder
- TLV5594VF Numeric
- TLV5593VF Alphanumeric Roaming

Common features of the three decoders include:

- FLEX messaging protocol signal processor
- Decoding at 1600, 3200, or 6400 bits per second (bps)
- Real-time clock time base
- Low battery indication (external detector)
- Standard serial peripheral interface (SPI) in slave mode
- Highly programmable receiver control
- Compatible with synthesized receivers
- Low-current STOP mode operation of host processor

Features specific to each decoder include:

- ❑ TLV5591BVF Alphanumeric Decoder
  - 16 programmable user-address words
  - 16 fixed-temporary addresses
  - Any-phase decoding
- ❑ TLV5594VF Numeric
  - 4 programmable user-address words
  - Single-phase decoding
- ❑ TLV5593VF Alphanumeric Roaming
  - 16 programmable user-address words
  - 16 fixed temporary addresses
  - 16 operator messaging addresses
  - Any-phase or single-phase decoding
  - FLEX fragmentation and group messaging support
  - Real-time clock over-the-air update support
  - Simulcast system ID (SSID) and network ID (NID) roaming support
  - 28 used pins (32-pin package standard)
  - Backward-compatible to the standard FLEXchip signal processor

See Appendix C, *Mechanical Data*, for the package diagram that applies to each of the decoders.

How to Use This Manual

This manual contains the following chapters:

Chapter 1 Introduction
Presents an overview of FLEX™ messaging protocol and a general description of the TMS320FLEX Family chipset

Chapter 2 FLEX Signal Structure
Describes the TLV5594VF FLEX signal structure

Chapter 3 TLV5594VF FLEX Decoder
Describes the TLV5594VF FLEX decoder

Appendix A TLV5590 Data Sheet
Presents a complete TLV5590 converter data sheet with its own page numbering

Appendix B Timing Diagrams
Presents the timing diagrams for the TLV5594VF decoder

Appendix C Mechanical Data
Presents the mechanical data for the TLV5594VF decoder

Related Documentation From Texas Instruments

The following books describe the TMS320FLEX Family Decoders and related tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TMS320FLEX1 Messaging System Solutions Design Manual (literature number SPRA086)

TMS320FLEX Family Messaging System Solutions With Numeric Decoder Design Manual (literature number SPRA183)

TMS320FLEX Family Messaging System Solutions With Alphanumeric Roaming Decoder Design Manual (literature number SPRA193)

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Chapter 1

Introduction

The Texas Instruments (TI™) TMS320FLEX Family Chipset with Numeric Decoder simplifies implementation of the FLEX™ protocol in a messaging application by interfacing directly with most popular off-the-shelf messaging receivers and microcontrollers. You can quickly and easily develop a FLEX-compliant product by interfacing the TLV5590 converter and the TLV5594VF decoder to your existing receivers and microcontrollers with virtually no hardware redesign.

Purchase of the TMS320FLEX Family Chipset with Numeric Decoder satisfies all licensing requirements for the FLEX protocol. No separate license agreement with Motorola is required.

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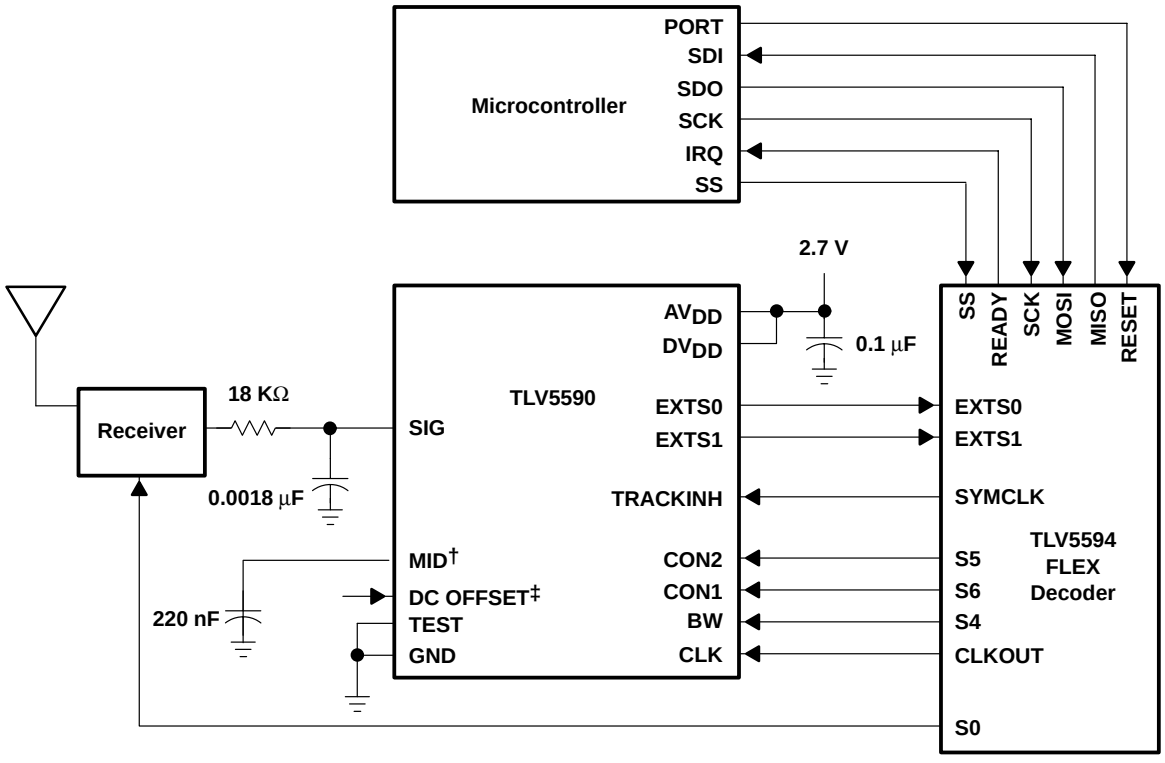
1.1 FLEX Messaging Overview

FLEX messaging protocol was developed by Motorola to provide a robust form of text and data messaging not previously available. Figure 1–1 shows a block diagram of a FLEX messaging device. The FLEX protocol brings new levels of functionality and service to pagers while providing you with the following benefits:

- ❏ Longer battery life than existing standards
- ❏ Support for numeric and alphanumeric messages
- ❏ High signal integrity for error protection and positive message termination
- ❏ Advanced features, such as group pages between systems
- ❏ Support for 1600-, 3200-, or 6400-bps transmissions
- ❏ Low upgrade costs by allowing gradual migration from FLEX 1600 to FLEX 3200 to FLEX 6400
- ❏ Increased number of subscribers per channel, thereby reducing infrastructure costs

Figure 1–1. FLEX Messaging Device



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

1.2 Chipset Description

The TMS320FLEX Family Chipset with Numeric Decoder consists of a TLV5594VF signal processor that decodes the FLEX messaging protocol transmission and the TLV5590 analog-to-digital (A/D) converter that converts the analog signal from the receiver into a digital signal for decoding by the TLV5594VF. FLEXstack™ system software to facilitate application development is also included. This software runs on a host processor and is specifically designed to support the TLV5594VF FLEX decoder. It handles communications with the TLV5590 converter and interprets the code words passed to the host from the TLV5594VF decoder.

The flexible architecture of the TMS320FLEX chipset offers a variety of possibilities in application design.

1.2.1 TLV5594VF FLEX Decoder

The TLV5594VF FLEX decoder has the following features:

- 4 programmable user-address words
- 1600, 3200, or 6400 b/s decoding
- Single-phase decoding
- Standard serial peripheral interface (SPI) in slave mode
- Low-current STOP mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- Compatibility with synthesized receivers
- Low battery indication (external detector)

1.2.2 TLV5590 A/D Converter

The TLV5590 A/D converter has the following features:

- Selectable dual-bandwidth audio filter
  - Three-pole Butterworth low-pass
  - BW 1 = 1 KHz +/–5% (–3 db)
  - BW 2 = 2 KHz +/–5% (–3 db)
- Peak and valley detectors
- Two-bit A/D converter
- Four modes of operation: fast track, slow track, hold, and standby
- Operation at 2.7-V to 3.3-V with a single power supply

See Appendix A, *TLV5590 Data Sheet*, for more information.

Chapter 2

FLEX Signal Structure

The FLEX signal transmitted on the radio channel consists of a series of four-minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames that are not assigned. The FLEX signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing, or carry-on information within the FLEX signal. This chapter discusses the FLEX signal structure.

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2.1 Synchronization

Figure 2–1 shows the FLEX signal structure.

Each FLEX frame has a synchronization portion followed by an 11-block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200, or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2-level FSK modulation and consists of a single phase of information at 1600 bps called *phase A*. The 3200 bps rate is transmitted at either 1600 sps using 4-level FSK modulation or 3200 sps using 2-level FSK modulation and consists of two concurrent phases of information at 1600 bps called *phase A* and *phase B*. The 6400 bps rate is transmitted at 3200 sps using 4-level FSK modulation and consists of four concurrent phases of information at 1600 bps called *phase A*, *phase B*, *phase C*, and *phase D*.

Each block has eight interleaved words per phase; there are 88 words, numbered 0 – 87, per phase in every frame. Each word has information contained within an error correcting code that allows for bit error correction and detection. The 88 words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field. The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of a first sync signal at 1600 bps; a Frame Information Word having the Frame Number 0 – 127 (7 bits) and the Cycle Number 0 – 14 (4 bits); and a second sync signal at the data rate of the interleaved portion.

2.1.1 Block Infomation Field

The block information field may contain block information words for determining time and date information and certain paging system information.

2.1.2 Address Field

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. An address may be either a short one-word address or a long two-word address. Information in the FLEX signal may indicate that an address is a priority address. An address may be a *tone-only* address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX signal indicates the location of the vector word in the vector field associated with the address. Short addresses have one associated vector word, and long addresses have two associated vector words. A pager may battery save at the end of the address field when its address(es) is not detected.

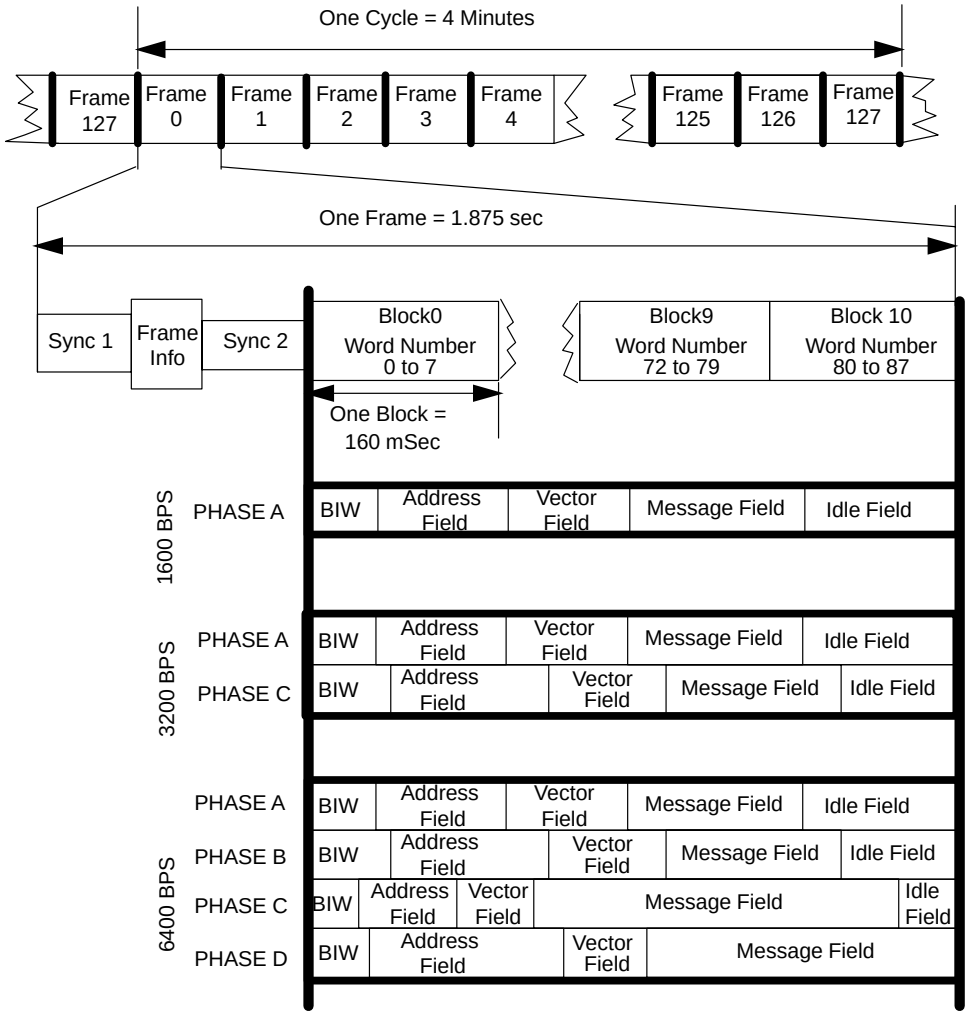
2.1.3 Vector Field

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information.

2.1.4 Message Field

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, binary coded decimal (BCD), or binary, depending upon the message type.

Figure 2–1. FLEX Signal Structure



2.2 FLEX Message Word Definitions

2.2.1 Numeric Data Message

Table 2–1 and Table 2–2 describe the bit format of the numeric messages. The 4-bit numeric characters of the message are designated as lowercase letters a, b, c, d, etc.

Table 2–1. Standard (V = 011) or Special (V = 100) Format: 4, 10, 15, 20, 25, 31, 36, or 41 Characters

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 2–2. Numbered (V = 111) Format: 2, 8, 13, 18, 23, 29, 34, or 39 Numeric Characters

Message Word	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

2.2.2 Bit Definitions

K: 6-bit Message Check Character (First 4 bits are in the vector word). This check character is calculated by initializing the message check character (**K**) to zero and summing the information bits of each code word in the message, (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: bits $\mathbf{i_0}$ through $\mathbf{i_7}$, bits $\mathbf{i_8}$ through $\mathbf{i_{15}}$, and bits $\mathbf{i_{16}}$ through $\mathbf{i_{20}}$. Bits $\mathbf{i_0}$, $\mathbf{i_8}$ and $\mathbf{i_{16}}$ are the LSBs of each group. The binary sum is calculated and the result is shortened to the 8 least significant bits. The 2 most significant bits are shifted right 6 bits and summed with the least significant 6 bits to form a new sum. This resultant sum is 1's complemented with the 6 LSBs of the result being transmitted as the message check character.

N: Message Number: When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing to a maximum of 63 in consecutive order. The actual maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) by allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (Message Retrieval Flag is equal to 0), it is not included in the missed message calculation.

R: Message Retrieval Flag: When this bit is set to 1, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with **R** = 0 is allowed to be out of order and does not cause the pager to indicate that a message has been missed.

S: Special Format: In the numbered message format, this bit set to 1 indicates that a special display format should be used.

2.2.3 Message Fill Rules

For numeric messages of 36 characters or less (34 characters if numbered), fewer than 8 code words on the channel are required. Only code words containing the numeric message can be transmitted. The space character (hexadecimal C) should be used to fill any unused 4-bit characters in the last word, and zeros should be used to fill any remaining partial characters. The check sum is correspondingly shortened to include only the code words comprising the shortened message along with the space and fill characters used to fill in the last word.

2.2.4 Special Format Numeric

Spaces and dashes as specified by the host are inserted into the received message. This feature in certain markets saves the transmission of an additional word on the channel. For example, in the U.S. market a 10-character format (area code plus telephone number) fits into two message words. If the dashes or parentheses are included in the message, three message words on the channel are required. The actual placement can be programmed into the paging device and can vary between markets.

2.3 FLEX Encoding and Decoding Rules

The encoding and decoding rules identify the minimum requirements that must be met by the paging device, paging terminal, or other encoding equipment to properly format a FLEX data stream for RF transmission and to successfully decode it. The encoding and decoding rules explained in this section pertain to the FLEX messaging capabilities of the numeric FLEX decoder.

2.3.1 FLEX Encoding Rules

- ❑ The stability of the encoder clock used to establish time positions of FLEX frames must be no worse than +/–25 ppm (including worst-case temperature and aging effects).
- ❑ A maximum of two occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for paging devices that support any-phase addressing, an any-phase address may appear only once in two different phases, in a single phase of a single multi-phase frame.
- ❑ A dynamic group address cannot be used to set up a second dynamic group.
- ❑ Messages using any of the three defined numeric vectors (011, 100, 111) cannot be fragmented, and thus must be completely contained in a single frame.
- ❑ Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- ❑ Message numbers must be assigned sequentially in ascending order.
- ❑ Message number sequences must be separately maintained for each individual and radio group address.
- ❑ When a missed page is retransmitted from message retrieval storage, the message must have R = 0 to avoid creating an out-of-sequence message that may cause the pager to indicate a missed message.

2.3.2 FLEX Decoding Rules

- ❑ FLEX decoding devices may implement either single-phase addressing or any-phase addressing.
- ❑ FLEX decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- ❑ FLEX decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode: 1600 bps, 2 level; 3200 bps, 2 level; 3200 bps, 4 level; 6400 bps, 4 level.

2.4 FLEX Numeric Character Set

Table 2–3 and Table 2–4 define the characters to be displayed in the FLEX numeric message mode.

Table 2–3. Standard Character Set (Peoples Republic of China Option Off)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
Spare	1	0	1	0
U	1	0	1	1
Space	1	1	0	0
–	1	1	0	1
]	1	1	1	0
[	1	1	1	1

Table 2–4. Alternate Character Set (Peoples Republic of China Option On)

Character	B_3	B_2	B_1	B_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
Space	1	1	0	0
C	1	1	0	1
D	1	1	1	0
E	1	1	1	1

2.5 FLEX Local Time and Date

The FLEX protocol allows for systems to transmit time information in its Block Information Field. When a system provider supports local time transmissions, the system provider is required, at a minimum, to transmit at least one time-related block information word in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of Sync 1 of Frame 0 of the current cycle. The information carried in the **s** bits of the block information word depend on the value of the **f** bits of the block information word. Table 2–5, Table 2–6, and Table 2–7 describe the bit definitions of the time-related block information words.

2.5.1 Month/Day/Year

Table 2–5. Month/Day/Year Block Information Word Definition

$f_2 f_1 f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
001	m_3 m_2, m_1 m_0 d_4 d_3 d_2 d_1 d_0 Y_4 Y_3 Y_2 Y_1 Y_0	Month/Day/Year

m: Month field. 0001 through 1100 (binary) correspond to January through December, respectively.

d: Day field. 00001 through 11111 (binary) correspond to 1 through 31, respectively.

Y: Year field. This represents the year with modulo arithmetic (00000 through 11111 (binary), representing 1994 through 2025, 2026 through 2057, etc.

2.5.2 Second/Minute/Hour

Table 2–6. Second/Minute/Hour Block Information Word Definition

$f_2 f_1 f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
010	S_5 S_4 S_3 M_5 M_4 m_3 M_2 M_1 M_0 H_4 H_3 H_2 H_1 H_0	Second/Minute/Hour

S: Second field. This represents a coarse value of the seconds field. These bits represent the seconds in 1/8 of a minute (7.5 second) increments. 000 through 111 (binary) correspond to 0 through 52.5 seconds, respectively.

M: Minute field. 000000 through 111011 (binary) correspond to 0 through 59, respectively.

H: Hour field. 00000 through 10111 (binary) correspond to 0 through 23, respectively.

2.5.3 Accurate Seconds/Daylight Savings Time/Time Zone

Table 2–7. System Message Block Information Word Definition

$f_2 f_1 f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
101	S_2 S_1 S_0 x L_0 z_4 z_3 z_2 z_1 z_0 0 1 0 X	System Message

Note: When the s3 s2 s1 s0 field is set to 0100 or 0101, the other s4 through s13 are defined as above. The system messages with the s3 s2 s1 s0 field set to some other value do not contain time-related information.

S: Accurate Seconds. This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents how much time should be added to the coarse seconds in 1/64-of-a-minute increments.

L: Daylight Savings Time. When this bit is set, the time being transmitted is Local Standard Time. When it is clear, the time being transmitted is Daylight Savings Time.

Z: Time Zone. These bits indicate the time zone for which the time is being transmitted. The offset from GMT is the offset for local standard time. Table 2–8 describes the values for z.

Table 2–8. Time Zone Values

$z_4z_3z_2z_1z_0$	Time Zone
00000	GMT
00001	GMT+0100
00010	GMT+0200
00011	GMT+0300
00100	GMT+0400
00101	GMT+0500
00110	GMT+0600
00111	GMT+0700
01000	GMT+0800
01001	GMT+0900
01010	GMT+1000

$z_4z_3z_2z_1z_0$	Time Zone
01011	GMT+1100
01100	GMT+1200
01101	GMT+0330
01110	GMT+0430
01111	GMT+0530
10000	RESERVED
10001	GMT+0545
10010	GMT+0630
10011	GMT+0930
10100	GMT–0330
10101	GMT–1100

$z_4z_3z_2z_1z_0$	Time Zone
10110	GMT–1000
10111	GMT–0900
11000	GMT–0800
11001	GMT–0700
11010	GMT–0600
11011	GMT–0500
11100	GMT–0400
11101	GMT–0300
11110	GMT–0200
11111	GMT–0100

2.6 FLEX CAPCODE

To send messages to a FLEX decoding device, the FLEX service provider must know the *device address*, *address type* (single-phase, any-phase, or all-phase), *address assigned phase*, *address assigned frame*, and the *address battery cycle*. This information is typically included in a FLEX CAPCODE. The assignment of CAPCODEs is regulated to prevent duplication of addresses on a system. Check with your FLEX service provider or other appropriate regulatory body for FLEX CAPCODE assignments. This section defines the FLEX CAPCODE parameters.

The device address consists of one or two 21-bit words. A one-word address is called a short address and a two-word address is called a long address. Address words are separated into ranges according to Table 2–9.

Table 2–9. Address Word Range Definitions

Type	Hexadecimal Value
Idle Word (Illegal Address)	000000
Long Address 1	000001 through 008000
Short Address	008001 through 1E0000
Long Address 3	1E0001 through 1E8000
Long Address 4	1E8001 through 1F0000
Short Address (Reserved)	1F0001 through 1F27FF
Information Service Address	1F2800 through 1F67FF
Network Address	1F6800 through 1F77FF
Temporary Address	1F7800 through 1F780F
Operator Messaging Address	1F7810 through 1F781F
Short Address (Reserved)	1F7820 through 1F7FFE
Long Address 2	1F7FFF through 1FFFFE
Idle Word (Illegal Address)	1FFFFF

Long addresses are grouped into sets, as shown in Table 2–10.

Table 2–10. Long Address Sets

Long Address Set	First Word	Second Word
1–2	Long Address 1	Long Address 2
1–3	Long Address 1	Long Address 3
1–4	Long Address 1	Long Address 4
2–3	Long Address 2	Long Address 3
2–4	Long Address 2	Long Address 4

The address type indicates how messages on a particular address can be delivered in multi-phase FLEX frames. Messages sent on single-phase addresses can only be delivered in a particular phase (a, b, c, or d). Messages sent on any-phase addresses can be delivered in any phase, but a single message is limited to a single phase per frame. Messages sent on all-phase addresses can be delivered in any phase, and a single message can be spread across multiple phases in a single frame. All-phase messaging is a future feature of FLEX and has not been completely defined.

The address assigned phase is required only for single-phase devices. It determines the phase (a, b, c, or d) in which the messages are sent.

The address assigned to the frame and battery cycle determines the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The address battery cycle is a number between 0 and 7 that defines how often the decoding device looks for messages on the FLEX channel. For a given battery cycle, b, the decoding device looks in every 2^b frame. Thus, an address with an assigned frame of 3 and a battery cycle of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e., frames 3, 35, 67, and 99).

The FLEX CAPCODE is defined to represent either a short or a long address. The short address is defined in the FLEX protocol as one code word on the RF channel and is represented by a 7-digit decimal field. The long address is defined in the FLEX protocol as two code words on the RF channel and is represented by a 9- or 10-digit decimal field. The long addresses in set 1–2 are represented by a 9-digit decimal field. The long addresses in sets 1–3, 1–4, 2–3, and 2–4 are represented by a 10-digit decimal field. An alphabetic character known as the *CAPCODE type* always precedes the 7-, 9-, or 10-digit decimal address field. The CAPCODE type indicates the type of address and distinguishes FLEX CAPCODEs from CAPCODEs of other paging protocols.

2.6.1 CAPCODE Type

Example CAPCODE types are shown in Table 2–11. The CAPCODE type can be any of A through L or U through Z. The CAPCODE types A through L indicate that the standard rules are used to derive the assigned frame and phase information from the address field (See subsection *2.6.2, Standard Frame and Phase Embedding Rule*). For these CAPCODE types, the battery cycle (indicated as a b in example 1) is indicated by a single decimal digit, 0 through 7, preceding the CAPCODE type. When the FLEX standard battery cycle of 4 (16 frame cycle) is used, the battery cycle digit is not required (see example 2).

The CAPCODE types U through Z indicate that the standard frame and phase embedding rules were not used and additional information is required. The phase assignment can be derived from the CAPCODE type as described in Table 2–11. The 3-digit decimal frame assignment, 000 through 127 (indicated by fff in example 3), may precede this CAPCODE type. The frame and battery

cycle fields are not required. When they are not included (see example 4), the paging device or the subscriber database must be accessed to determine the assigned frame and battery cycle.

The extended CAPCODE is a regular CAPCODE with a 10-digit address field and preceded by an extra alphabetic character, P through S. These CAPCODEs are used to provide additional information required for roaming devices.

Table 2–11. FLEX CAPCODE Examples

Example	Short	Long	Extended
1	bA1234567	bA123456789	RbA1234567890
2	A1234567	A123456789	RA1234567890
3	ffffbU1234567	ffffbU123456789	RffffbU1234567890
4	U1234567	U123456789	RU1234567890

By using the convention of 7 digits to represent short addresses, 9 digits to represent some of the long addresses in set 1–2, and 10 digits to represent the balance of long addresses, it is possible to differentiate between the different types of addresses. The range of the decimal address field consists of the numbers 1 through 5,370,810,366 where short and other single code word addresses fall below 2,031,615, and long addresses are above 2,101,248.

The goal in displaying a CAPCODE is to use the shortest form possible. Even though the nonstandard form could represent a standard assignment, the standard form is chosen to indicate that it is a standard assignment. All CAPCODE forms, except example 4 in Table 2–11, contain the information required to send a message to a subscriber unit.

2.6.2 Standard Frame and Phase Embedding Rule

Maximum battery life in a FLEX decoding device is achieved when all of the addresses assigned to a device are in the same frame. For single-phase decoding devices, all assigned addresses are required to be in the same phase.

Typically, it is desirable to spread the population of FLEX subscriber units on a system across all four phases of all 128 frames. Frame and phase spreading can be performed automatically as addresses are assigned sequentially by embedding that information into the 7-, 9-, and 10-digit decimal FLEX address.

The standard procedure for deriving the phase and frame values from the CAPCODE starts by separating the 7-, 9-, or 10-digit decimal address portion (field to the right of the CAPCODE type) and performing a decimal-to-binary conversion. The least significant bit (LSB) is labeled bit 0. The following bits 2 and 3 in order, specify phases 00, 01, 10, or 11 for phase 0,1,2,3 (a,b,c,d), and bits 4 through 10 represent frames 000 through 127.

The frame and phase can also be derived from the 7-, 9-, or 10-digit decimal address by using modulo arithmetic (base 10) where:

Phase = (Integer (Addr/4)) Modulo 4

Frame = (Integer (Addr/16)) Modulo 128

When these rules are used, and addresses are assigned in order, the phase will increment after 4 consecutive addresses are assigned, whereas the frame will be incremented after 16 addresses are assigned.

2.6.3 CAPCODE Alpha Character Definition

The alpha character in the FLEX CAPCODE indicates the type of decoding device to which the address is assigned. Table 2–12 defines the alpha character codes. The types include single-phase, any-phase, or all-phase. It also indicates if the address is the first, second, third, or fourth address in the subscriber unit (when addresses are assigned in order following standard rules), and specifies the rules for determining in which phase and frame the address is active.

Table 2–12. Alpha Character Codes

Standard Rules	No Rules (Nonstandard Form)
A – Single-phase, Subtract 0	U – Single-phase, Phase 0
B – Single-phase, Subtract 1	V – Single-phase, Phase 1
C – Single-phase, Subtract 2	W – Single-phase, Phase 2
D – Single-phase, Subtract 3	X – Single-phase, Phase 3
E – Any-phase, Subtract 0	Y – Any-phase
F – Any-phase, Subtract 1	
G – Any-phase, Subtract 2	
H – Any-phase, Subtract 3	
I – All-phase, Subtract 0	Z – All-phase
J – All-phase, Subtract 1	
K – All-phase, Subtract 2	
L – All-phase, Subtract 3	

The character A represents a single-phase subscriber unit using the standard rules for embedding phase and frame. The character B is similar to A except 1 is subtracted from the CAPCODE before the standard rule is applied. Likewise, the characters C and D indicate that 2 or 3 is to be subtracted before the rule is applied. Using these CAPCODE characters ensures that sequentially numbered CAPCODEs are assigned to a common phase and frame. These procedures modify the standard rules and are intended to simplify the order entry process for multiple address subscriber units. When addresses are assigned in order, the subtraction of 1, 2, or 3 ensures that the calculation for each additional address in a decoding device is referenced to the first address. Thus, all A, B, C, and D addresses are assigned to the same frame and phase.

Characters E through H and I through L represent any-phase and all-phase subscriber units where the subtract rule is modified to ensure that all addresses of a multiple address subscriber unit are in the same frame.

For the cases where no rule is defined, the letters U through X indicate single-phase subscriber units assigned to phases 0 through 3 (phases A through D) with the frame and battery cycle explicitly displayed. Y and Z indicate nonstandard addresses for any-phase and all-phase subscriber units.

If the subscriber unit contains only a single individual address and you are content with the recommended 30-second battery cycle, then the letter A, E, or I is added as a prefix to the 7-, 9- or 10-digit address where:

A = Single-phase unit
E = Any-phase unit
I = All-phase unit

If the unit is a two-address unit where both addresses are individual addresses, then A,E, or I would preface the address field of the first address. The B, F, or J would preface the second address. The B, F, or J indicates that the address is a second address and it is to have the properties of the first address. This rule eliminates the need for an administrative operator or a salesperson to calculate a starting address, which would allow standard rules to always apply.

In other cases, especially when a group address is to be included, it is advisable to use the U through Z forms of the CAPCODE so that the frame can be explicitly chosen to provide best battery life, and the required *same phase* operation can be met in the case of the single-phase units.

2.6.4 CAPCODE to Binary Conversion

Short CAPCODE – To convert a short address CAPCODE, the number 32,768 is added to the 7-digit decimal CAPCODE address (or to any CAPCODE less than 2,031,615). The resultant number is then converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air.

Long CAPCODE 2,101,249 to 1,075,843,072 – Long address set 1–2 is in this range. To convert a long address CAPCODE, the number 2,068,481 is subtracted from the CAPCODE address. The resultant number is then divided by 32,768 with the remainder, incremented by 1, being the first word of the long address. This is the same as calculating the ((CAPCODE–2,068,481) modulo 32768) +1. This value is converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the first address word.

The second word of the long address is determined by first calculating the integer portion of the (CAPCODE–2,068,481) divided by 32,768. This value is then subtracted from 2,097,151 (equivalent to 1's complement of the value in binary), and converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 1,075,843,073 to 3,223,326,720 – Long address sets 1–3 and 1–4 are in this range. The first word of the long address is calculated following the same rules for the long address sets 1–2. The second long address word is determined by subtracting 2,068,481 from the CAPCODE. The resultant number is divided by 32,768 with the integer portion added to 1,933,312. This value is converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the second address word.

Long CAPCODE 3,223,326,721 to 4,297,068,542 – Long address set 2–3 is in this range.The first word is determined by subtracting 2,068,479 from the CAPCODE. The resultant number is divided by 32,768 and is retained (Modulo 32,768). This value is then added to 2,064,383 with the result converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the first address word.

The second word of the long address is determined by subtracting 2,068,479 from the CAPCODE and finding the integer portion after dividing by 32,768. This value is then added to 1,867,776 and converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code word transmitted over the air as the second address word.

2.6.5 Binary to CAPCODE Conversion

With the address code word values that are transmitted over the air, the CAPCODE can be calculated by performing the inverse of the process specified previously. For example, the short address code word is converted to decimal and the number 32,768 is subtracted to arrive at the 7-digit address portion of the CAPCODE. For the two-word long address set 1–2, the address word 1 is first converted from binary to decimal. The address word 2 is then complemented, (or subtracted from 2,097,151 decimal) and converted to a decimal. This value is multiplied by 32,768, added to 2,068,480 and then added to address word 1. The result is the address portion of the FLEX CAPCODE.

2.6.6 CAPCODE Assignments

Table 2–13 defines the address usage assignment. Addresses not listed in this table are not defined and not reserved for future use.

Table 2–13. CAPCODE Assignments

CAPCODE Address Value	Description
0,000,000,000	Illegal
0,000,000,001 to 0,001,933,312	Short Addresses
0,001,933,313 to 0,001,998,848	Illegal
0,001,998,849 to 0,002,009,087	Reserved for Future Use
0,002,009,088 to 0,002,025,471	Information Service Addresses
0,002,025,472 to 0,002,029,567	Network Addresses
0,002,029,568 to 0,002,029,583	Temporary Addresses
0,002,029,584 to 0,002,029,599	Operator Messaging Addresses
0,002,029,600 to 0,002,031,614	Reserved for Future Use
0,002,031,615 to 0,002,101,248	Illegal
0,002,101,249 to 0,102,101,250	Long Address Set 1–2 Uncoordinated
0,102,101,251 to 0,402,101,250	Long Address Set 1–2 by Country†
0,402,101,251 to 1,075,843,072	Long Address Set 1–2 Global‡
1,075,843,073 to 2,149,584,896	Long Address Set 1–3 Global‡
2,149,584,897 to 3,223,326,720	Long Address Set 1–4 Global‡
3,223,326,721 to 3,923,326,750	Long Address Set 2–3 by Country†
3,923,326,751 to 4,280,000,000	Long Address Set 2–3 Reserved
4,280,000,001 to 4,285,000,000	Long Address Set 2–3 Information Service§ Global‡
4,285,000,001 to 4,290,000,000	Long Address Set 2–3 Information Service§ by Country
4,290,000,001 to 4,291,000,000	Long Address Set 2–3 Information Service§ World-Wide Use¶
4,291,000,001 to 4,297,068,542	Reserved for Future Use

† By country: The addresses are coordinated within each country and with countries along borders.
‡ Global: Address is coordinated to be unique worldwide.
§ Information service: Rules governing the use of these addresses are not currently defined.
¶ Worldwide Use: 1000 addresses are assigned to each country for worldwide use.

Chapter 3

TLV5594VF FLEX Decoder

The TLV5594VF FLEX™ decoder simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receivers and any of several off-the-shelf host microcontroller/microprocessors. Its primary function is to process information received and demodulated from a FLEX radio paging channel, select messages addressed to the paging device and communicate the message information to the host. The host interprets the message information in an appropriate manner (numeric, alphanumeric, binary, etc). The FLEX decoder also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when message information for the paging device is not being received.

Topic **Page**

3.1 Features

- FLEX paging protocol signal processor
- 4 programmable user address words
- 1600-, 3200-, and 6400-bps decoding
- Single-phase decoding
- Standard serial peripheral interface (SPI) in slave mode
- Low-current STOP mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- Real-time clock over-the-air update support
- Compatibility with synthesized receivers
- Low battery indication (external detector)
- 32-pin thin quad flat pack (TQFP) package
- Pin-compatible with all other FLEX decoder signal processors

3.1.1 Support

FLEX system software from Motorola™ is a family of software components for building world-class products incorporating messaging capabilities. FLEXstack™ software is specifically designed to support the FLEX decoder. FLEXstack software runs on a product's host processor and takes care of communicating with the FLEX decoder and fully interpreting the code words that are passed to the host from the FLEX decoder.

The TLV5590, produced by Texas Instruments (TI), converts an audio signal from an off-the-shelf receiver to a two-bit digital output for processing by the FLEX decoder.

3.1.2 Functional Description

Figure 3–1 shows the FLEX decoder functional block diagram. The FLEX decoder connects to a receiver capable of converting a 4-level audio signal into a 2-bit digital signal. The FLEX decoder has eight receiver control lines used to warm up and shut down a receiver in stages. The FLEX decoder has dual bandwidth control signals for two post-detection filter bandwidths to receive the two symbol rates of the FLEX signal. The FLEX decoder can detect a low battery signal during the receiver control sequences. It interfaces to a host microcontroller unit (MCU) through a standard SPI. It has a 38.4-kHz clock output capable of driving other devices. It has a one-minute timer that offers low-power support for time of day function on the host.

Figure 3–1. Functional Block Diagram

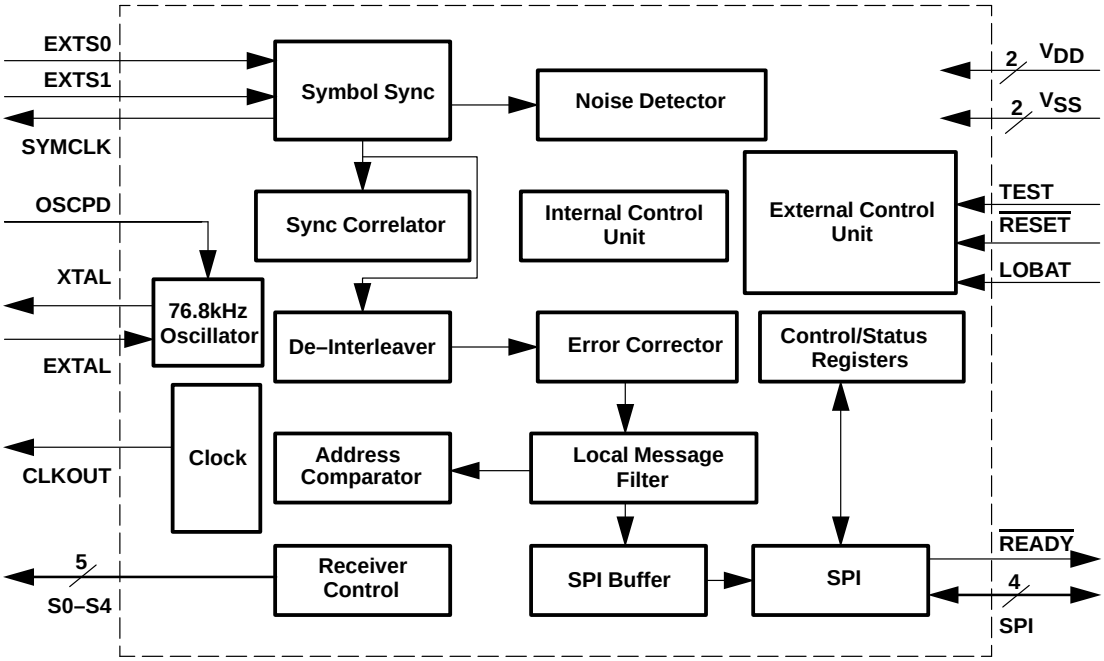
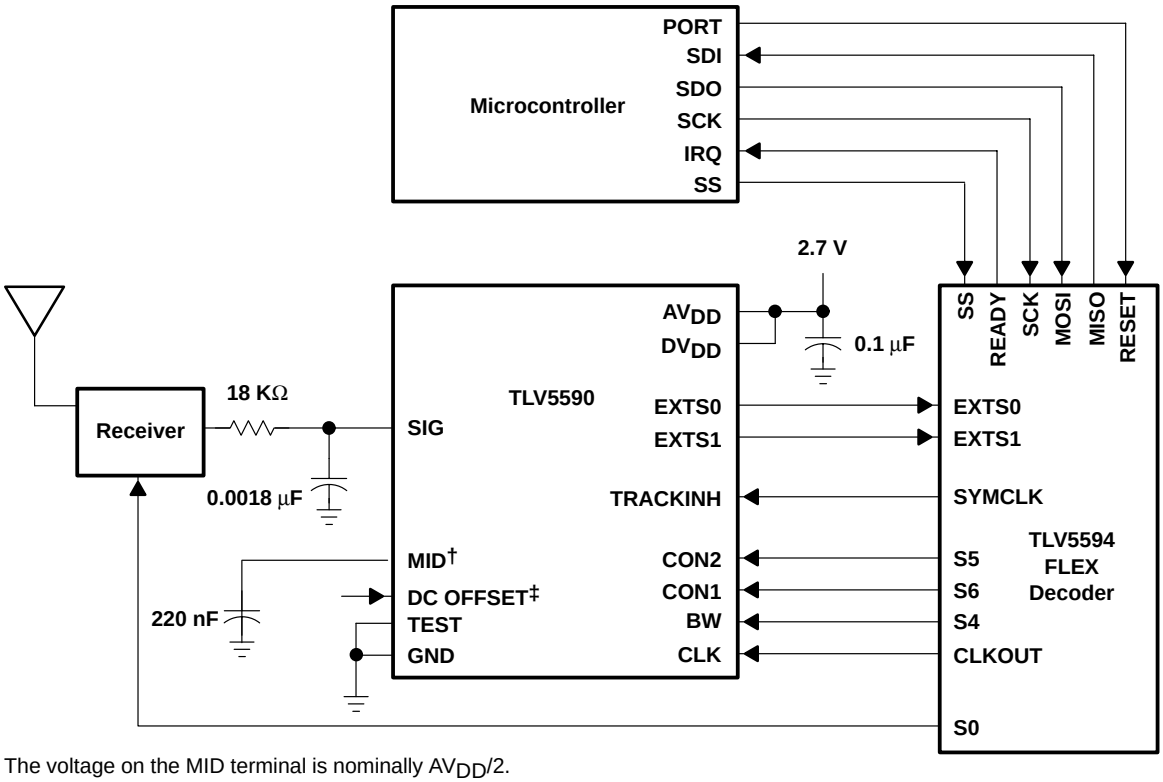


Figure 3–2 shows a system diagram of the FLEX decoder.

Figure 3–2. System Diagram



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

3.1.3 Powerdown

To ensure proper operation, the FLEX decoder must be in asynchronous mode when turned off.

The FLEXstack one-way API (application programming interface) has been modified to ensure that the FLEX decoder is in asynchronous mode when turned off. If you are using FLEXstack, be sure to download V1.2 or later, which is available as of 10/5/96.

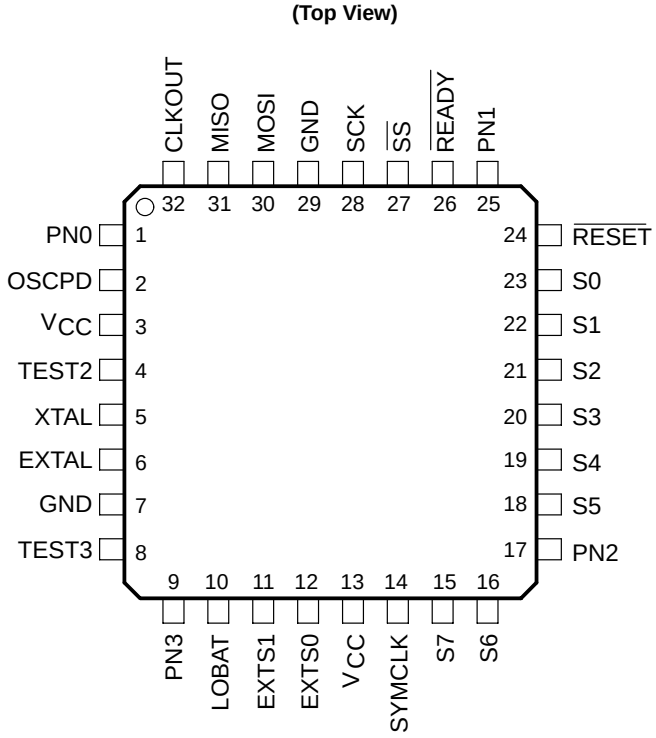
If you are not using FLEXstack, sending a Control Packet with the ON bit cleared does not guarantee the asynchornous mode. To ensure that you are in asynchronous mode, follow this sequence:

1) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.
2) Turn on the FLEX decoder by sending a Control Packet with the ON bit set.
3) Turn off the FLEX decoder by sending a Control Packet with the ON bit cleared.

Timing between these steps is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet. The minimum time between any of the steps should be 2 milliseconds. There is no maximum time between steps 1 and 2. The time between steps 2 and 3 should not exceed the programmed warm-up time or 95 millliseconds, whichever is smaller. The programmed warm-up time is the sum of the times programmed in the selected Receiver Warm-up Settings Packets.

Figure 3–3 shows terminal assignments for the FLEX decoder.

Figure 3–3. Terminal Assignments



3.1.4 Terminal Functions

Table 3–1 shows the terminal functions of the FLEX decoder.

Table 3–1. Terminal Functions

Terminal		I/O	Description
NAME	NO.		
CLKOUT	32	O	38.4-kHz clock output (derived from 76.8-kHz oscillator). May also be used to clock other functions of the pager circuitry.
EXTAL	6	I	76.8-kHz crystal oscillator input or external input
EXTS1	11	I	Most significant bit pair of the FLEX 4-level symbol currently being decoded
EXTS0	12	I	Least significant bit) pair of the FLEX 4-level symbol currently being decoded
LOBAT	10	I	Used to test a low battery voltage input signal
MISO	31	O	3-state data output for SPI communications
MOSI	30	I	Data input for SPI communications
OSCPD	2	I	Internal oscillator powerdown. Connected to VSS when using internal oscillator Connected to VDD when using an external source
$\overline{\text{READY}}$	26	O	Driven low when the TLV5594VF is ready for an SPI packet
$\overline{\text{RESET}}$	24	I	Active low reset to the TLV5594VF
S0	23	O	Five 3-state receiver control ports
S1	22	O	
S2	21	O	
S3	20	O	
S4	19	O	
SCK	28	I	Serial clock. Used to clock synchronous data for SPI communications.
$\overline{\text{SS}}$	27	I	Active low slave select. Used to select the TLV5594VF decoder SPI for data transfer.
SYMCLK	14	O	Recovery symbol clock
TEST	4	I	Manufacturing test mode terminals. During normal operation, the TEST terminals are connected to VSS.
VDD	3, 13	Power	Supply voltage
VSS	7, 29	Ground	Ground
XTAL	5	O	76.8-kHz clock output.

Note: Pin numbers shown are for 32-pin TQFP devices.

3.2 SPI Packets

All data communicated between the FLEX decoder and the host MCU is transmitted on the SPI in 32-bit packets. Each packet consists of an 8-bit ID followed by 24 bits of information. The FLEX decoder uses the SPI bus in full duplex mode. In other words, whenever a packet communication occurs, the data in both directions is valid packet data.

The SPI interface consists of a $\overline{\text{READY}}$ pin and four SPI pins ($\overline{\text{SS}}$, SCK, MOSI, and MISO).The $\overline{\text{SS}}$ is used as a chip select for the FLEX decoder. The SCK is a clock supplied by the host MCU. The data from the host is transmitted on the MOSI line. The data from the FLEX decoder is transmitted on the MISO line.

3.2.1 Packet Communication Initiated by the Host

When the host sends a packet to the FLEX decoder, it performs the following steps (see Figure 3–4):

1) Selects the FLEX decoder by driving the $\overline{\text{SS}}$ pin low.

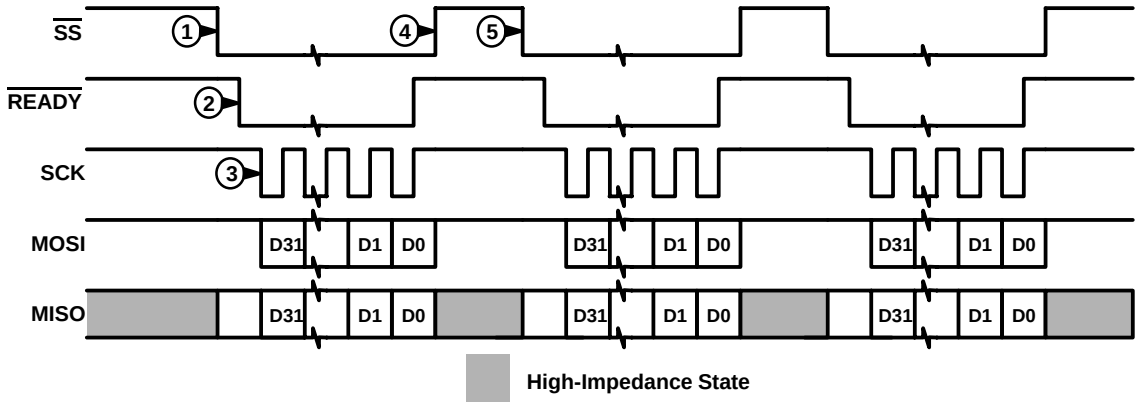
2) Waits for the FLEX decoder to drive the $\overline{\text{READY}}$ pin low.

3) Sends the 32-bit packet.

4) Deselects the FLEX decoder by driving the $\overline{\text{SS}}$ pin high.

5) Repeats steps 1 through 4 for each additional packet.

Figure 3–4. Typical Multiple Packet Communications Initiated by the Host



When the host sends a packet, it also receives a valid packet from the FLEX decoder. If the FLEX decoder is enabled (see subsection 3.3.1, *Checksum Packet*) and has no other packets waiting to be sent, the decoder will send a status packet.

The host must transition the $\overline{\text{SS}}$ pin from high to low to begin each 32-bit packet. The FLEX decoder must see a negative transition on the $\overline{\text{SS}}$ pin in order for the host to initiate each packet communication.

3.2.2 Packet Communication Initiated by the FLEX Decoder

When the FLEX decoder has a packet for the host to read, the following events occur (see Figure 3–5):

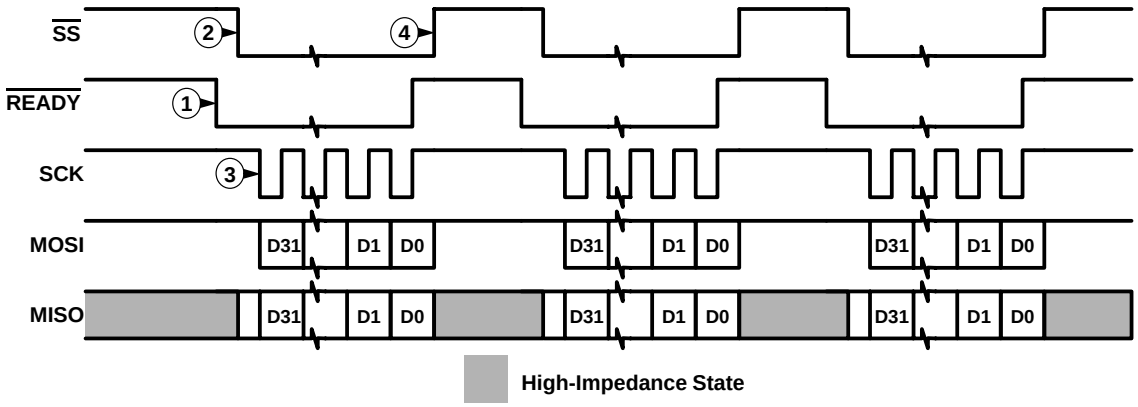
1) The FLEX decoder drives the $\overline{\text{READY}}$ pin low.

2) If the FLEX decoder is not already selected, the host selects the FLEX decoder by driving the $\overline{\text{SS}}$ pin low.

3) The host receives (and sends) a 32-bit packet.

4) The host deselects the FLEX decoder by driving the $\overline{\text{SS}}$ pin high (optional).

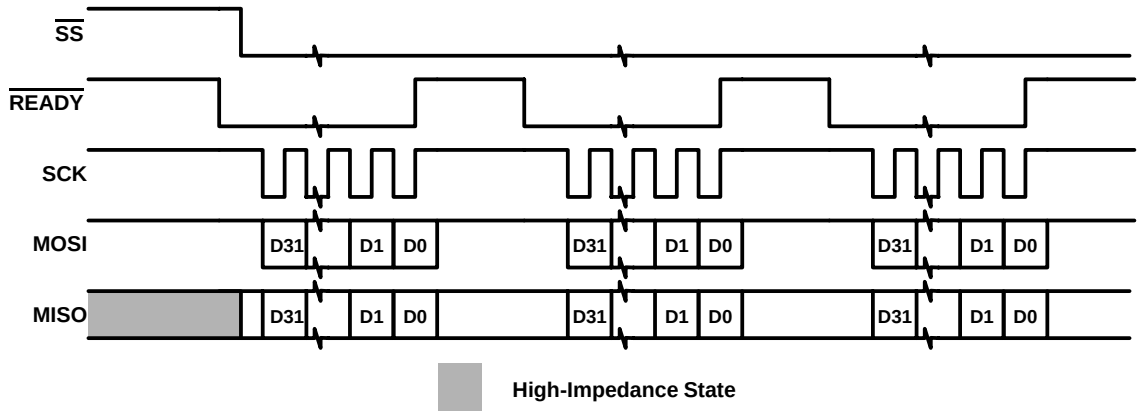
Figure 3–5. Typical Multiple Packet Communications Initiated by the FLEX Decoder



When the host reads a packet from the FLEX decoder, it must send a valid packet to the FLEX decoder. If the host has no data to send, TI suggests that the host send a checksum packet with all of the data bits set to 0 to avoid disabling the FLEX decoder (see subsection 3.3.1, *Checksum Packet*).

Figure 3–6 illustrates that it is not necessary to deselect the FLEX decoder between packets when the packets are initiated by the FLEX decoder.

Figure 3–6. Multiple Packet Communications Initiated by the FLEX Decoder With No Deselect



3.2.3 Host-To-Decoder Packet Map

The upper 8 bits of a packet comprise the packet ID. Table 3–2 describes the packet IDs for all of the packets that can be sent to the FLEX decoder from the host.

Table 3–2. Host-To-Decoder Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Checksum
01	Configuration
02	Control
03 – 0E	Reserved (host should never send)
0F	Receiver line control
10	Receiver control configuration (off setting)
11	Receiver control configuration (warm up 1 setting)
12	Receiver control configuration (warm up 2 setting)
13	Receiver control configuration (warm up 3 setting)
14 – 15	Reserved (host should never send)
16	Receiver control configuration (3200 sps sync setting)
17	Receiver control configuration (1600 sps sync setting)
18	Receiver control configuration (3200 sps data setting)
19	Receiver control configuration (1600 sps data setting)
1A – 1B	Reserved (host should never send)
1C – 1F	Special (ignored by FLEX decoder)
20	Frame assignment (frames 112 through 127)
21	Frame assignment (frames 96 through 111)
22	Frame assignment (frames 80 through 95)
23	Frame assignment (frames 64 through 79)
24	Frame assignment (frames 48 through 63)
25	Frame assignment (frames 32 through 47)
26	Frame assignment (frames 16 through 31)
27	Frame assignment (frames 0 through 15)
28 – 77	Reserved (host should never send)
78	User address enable
79 – 7F	Reserved (host should never send)
80	User address assignment (user address 0)
81	User address assignment (user address 1)
82	User address assignment (user address 2)
83	User address assignment (user address 3)
84 – FF	Reserved (host should never send)

3.2.4 Decoder-To-Host Packet Map

Table 3–3 describes the packet IDs for all of the packets that can be sent to the host from the FLEX decoder.

Table 3–3. Decoder-To-Host Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Block Information Word
01	Address
02– 57	Vector or Message (ID is word number in frame)
58 – 7E	Reserved
7F	Status
80 – FE	Reserved
FF	Part ID

3.3 Host-To-Decoder Packet Descriptions

The following sections describe the packets of information sent from the host to the FLEX decoder. In all cases the packets should be sent most significant bit (MSB) first (bit 7 of byte 3 = bit 31 of the packet = MSB).

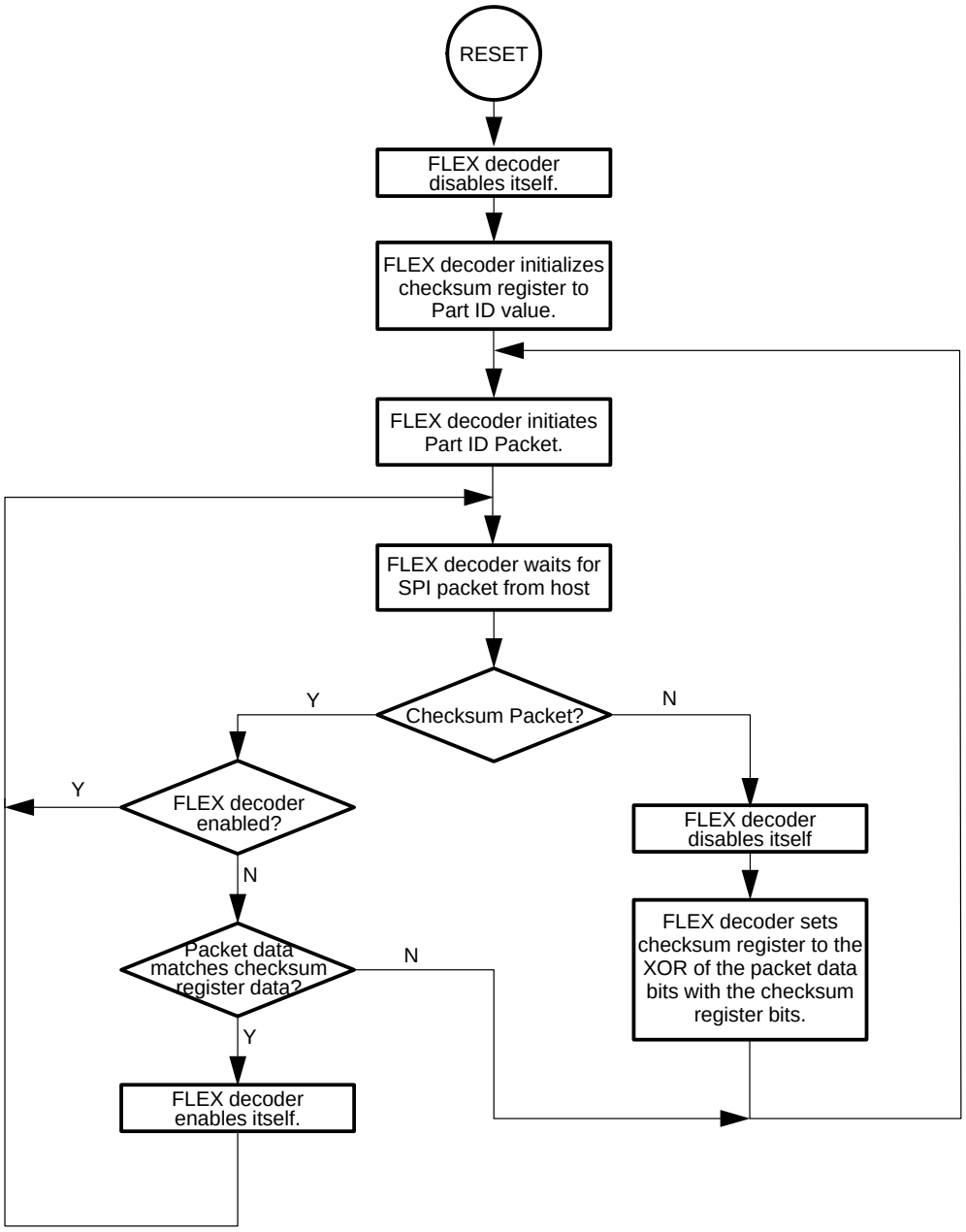
3.3.1 Checksum Packet

The Checksum Packet ensures proper communication between the host and the FLEX decoder. The FLEX decoder exclusive-ORs the 24 data bits of every packet it receives (except the Checksum Packet and the special packet IDs, 1C through 1F hexadecimal) with an internal checksum register. Upon reset and whenever the host writes a packet to the FLEX decoder, the FLEX decoder is disabled from sending any information to the host processor until the host processor sends a Checksum Packet with the proper checksum value (CV) to the FLEX decoder. When the FLEX decoder is disabled in this way, it prompts the host to read the Part ID Packet. Note that all other operation continues normally when the FLEX decoder is disabled. The FLEX decoder is only disabled in the sense that the data from the FLEX decoder cannot be read; all other operations continue to function.

When the FLEX decoder is reset, it is disabled and the internal checksum register is initialized to the 24-bit part ID defined in the Part ID Packet (see subsection 3.4.6, *Part ID Packet*). Every time a packet (other than the Checksum Packet and the special packets 1C through 1F) is sent to the decoder, the value sent in the 24 information bits is exclusive-ORed with the internal checksum register, the result is stored back to the checksum register, and the FLEX decoder is disabled. If a Checksum Packet is sent and the CV bits match the bits in the checksum register, the FLEX decoder is enabled. If a Checksum Packet is sent when the FLEX decoder is already enabled, the packet is ignored by the FLEX decoder and a null packet with the ID and data bits set to 0 is suggested. If a packet other than the Checksum Packet is sent when the FLEX decoder is enabled, the decoder is disabled until a Checksum Packet is sent with the correct CV bits.

Figure 3–7 shows the FLEX decoder checksum flow chart.

Figure 3–7. FLEX Decoder Checksum Flow Chart



When the host reads a packet out of the FLEX decoder but has no data to send, the Checksum Packet (see Table 3–4) should be sent so the FLEX decoder is not disabled. The data in the Checksum Packet could be a null packet, 32-bit stream of all zeros, because a Checksum Packet does not disable the FLEX decoder. When the host reconfigures the FLEX decoder, the FLEX decoder is disabled from sending any packets other than the Part ID Packet until the FLEX decoder is enabled with a Checksum Packet having the proper data. The ID of the Checksum Packet is 0.

Table 3–4. Checksum Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
Byte 1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
Byte 0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

CV: Checksum Value.

3.3.2 Configuration Packet

The Configuration Packet (see Table 3–5) defines a number of different configuration options for the FLEX decoder. The FLEX decoder ignores this packet when decoding is enabled (i.e., the ON bit in the Control Packet is set). The ID of the Configuration Packet is 1.

Table 3–5. Configuration Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	0	0	0	0	0	0	OFD_1	OFD_0
Byte 1	0	0	0	0	0	0	SP_1	SP_0
Byte 0	SME	MOT	COD	MTE	LBP	0	0	0

OFD: Oscillator Frequency Difference (Table 3–6). These bits describe the maximum difference in the frequency of the 76.8-kHz oscillator crystal with respect to the frequency of the transmitter. These limits should be the worst-case difference in frequency due to all conditions including but not limited to aging, temperature, and manufacturing tolerance. Using a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios. Note that this value is not the absolute error of the oscillator frequency provided to the FLEX decoder. The absolute error of the clock used by the FLEX transmitter must be taken into account. (e.g., if the transmitter tolerance is +/–25 ppm and the 76.8-KHz oscillator tolerance is +/–140 ppm, the oscillator frequency difference is +/– 165 ppm and OFD should be set to 0.)(value after reset = 0)

Table 3–6. Oscillator Frequency Difference

OFD_1	OFD_0	Frequency Difference
0	0	+/– 300 ppm
0	1	+/– 150 ppm
1	0	+/– 75 ppm
1	1	+/– 0 ppm

SP: Signal Polarity (Table 3–7). These bits set the polarity of EXTS1 and EXTS0 input signals. (value after reset = 0) The polarity of the EXTS0 and EXTS1 bits are determined by the receiver design.

Table 3–7. Signal Polarity

SP_1	SP_0	Signal Polarity EXTS1	EXTS0		FSK Modulation @ SP = 0,0	EXTS1	EXTS0
0	0	Normal	Normal		+ 4800 Hz	1	0
0	1	Normal	Inverted		+1600 Hz	1	1
1	0	Inverted	Normal		– 1600 Hz	0	1
1	1	Inverted	Inverted		– 4800 Hz	0	0

SME: Synchronous Mode Enable. When this bit is set, a Status Packet is automatically sent whenever the SMU (synchronous mode update) bit in the Status Packet is set. The host can use the SM (synchronous mode) bit in the Status Packet as an in-range/out-of-range indication. (value after reset = 0)

MOT: Maximum Off Time. When this bit is clear, the FLEX decoder assumes that there can be a maximum of 4 minutes between transmitted frames on the paging system. When this bit is set, the FLEX decoder assumes that there can be a maximum of 1 minute between transmitted frames on the paging system. This setting is determined by the service provider. (value after reset = 0)

COD: Clock Output Disable. When this bit is clear, a 38.4-kHz signal is output on the CLKOUT pin. When this bit is set, the CLKOUT pin is driven low. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4-kHz period. Also note that when the clock output is enabled, the CLKOUT pin always outputs the 38.4-kHz signal even when the FLEX decoder is in reset (as long as the FLEX decoder oscillator is recognizing clocks). (value after reset = 0)

MTE: Minute Timer Enable. When this bit is set, a Status Packet is sent at one-minute intervals with the minute time-out (MT) bit in the Status Packet set. When this bit is clear, the internal one-minute timer stops counting. The internal one-minute timer is reset when this bit is changed from 0 to 1 or when the minute timer clear (MTC) bit in the Control Packet is set. (value after reset = 0)

LBP: Low Battery Polarity. This bit defines the polarity of the FLEX decoder LOBAT pin. The low battery (LB) bit in the Status Packet is initialized to the inverse value of this bit when the FLEX decoder is turned on (by setting the ON bit in the Control Packet). When the FLEX decoder is turned on, the first low battery update in the Status Packet is sent to the host when a low battery condition is detected on the LOBAT pin. Setting this bit means that a high on the LOBAT pin indicates a low-voltage condition. (value after reset = 0)

3.3.3 Control Packet

The Control Packet defines a number of different control bits for the FLEX decoder (see Table 3–8). The ID of the Control Packet is 2.

Table 3–8. Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	1	0
Byte 2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
Byte 1	0	SPM	PS_1	PS_0	0	0	0	0
Byte 0	0	SBI	0	MTC	0	0	0	ON

FF: Force Frame 0–7. These bits enable and disable the forcing of the FLEX decoder to look in frames 0 through 7. When an FF bit is set, the FLEX decoder decodes the corresponding frame. Unlike the AF bits in the Frame Assignment Packets, the system collapse of a FLEX system does not affect frames assigned using the FF bits (e.g. whereas, setting AF_0 to 1 when the system collapse is 5 causes the decoder to decode frames 0, 32, 64, and 96, setting FF_0 to 1 when the system collapse is 5 only causes the decoder to decode frame 0.). This may be useful for acquiring transmitted time information. (value after reset = 0)

SPM: Single-Phase Mode. When this bit is set, the FLEX decoder decodes only one phase of the transmitted data. When this bit is clear, the FLEX decoder decodes all of the phases it receives. A change to this bit while the FLEX decoder is on does not take effect until the next block 0 of a frame. (value after reset = 0)

PS: Phase Select. When the SPM bit is set, these bits define what phase the FLEX decoder should decode, as shown in Table 3–9. This value is determined by the service provider. A change to these bits while the FLEX decoder is on does not take effect until the next block 0 of a frame. (value after reset = 0)

Table 3–9. Phase Select

PS Value		Phase Decoded (based on FLEX Data Rate)		
PS_1	PS_0	1600bps	3200bps	6400bps
0	0	a	a	a
0	1	a	a	b
1	0	a	c	c
1	1	a	c	d

SBI: Send Block Information words 2 – 4. When this bit is set, any errors or time-related block information words 2–4 are sent to the host. (value after reset = 0)

MTC: Minute Timer Clear. Setting this bit causes the one-minute timer to restart from 0.

ON: Turn On Decoder. Set this bit if the FLEX decoder should be decoding FLEX signals. Clear if signal processing should be off (very-low power mode). (value after reset = 0)

See subsection 3.1.3, *Powerdown*, for more information on the powerdown cycle.

3.3.4 Receiver Line Control Packet

The Receiver Line Control Packet (see Table 3–10) gives the host control over the settings on the receiver control lines (S0–S7) in all modes except reset. In reset, the receiver control lines are in high-impedance settings. The ID for the Receiver Line Control Packet is 15 (decimal).

Table 3–10. Receiver Line Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	1	1	1	1
Byte 2	0	0	0	0	0	0	0	0
Byte 1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
Byte 0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

FRS: Force Receiver Setting. Setting this bit to 1 causes the corresponding CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line (S0–S7). Clearing a bit gives control of the corresponding receiver control lines (S0–S7) back to the FLEX decoder. (value after reset = 0)

CLS: Control Line Setting. If the corresponding FRS bit was set in this packet, these bits define what setting should be applied to the corresponding receiver control lines. (value after reset = 0)

3.3.5 Receiver Control Configuration Packets

Receiver Control Configuration Packets allow the host to configure (1) what setting is applied to the receiver control lines S0–S7, (2) how long to apply the setting, and (3) when to read the value of the LOBAT input pin. For a more detailed description of how the FLEX decoder uses these settings, see Section 3.6, *Receiver Control.* The FLEX decoder defines 12 different receiver control settings. The FLEX decoder ignores these packets when decoding is enabled (i.e., the ON bit in the Control Packet is set). The IDs for these packets range from 16 to 27 (decimal).

3.3.6 Receiver Off Setting Packet

Table 3–11 shows Receiver Off Setting Packet bit assignments.

Table 3–11. Receiver Off Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	0	0	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0–S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the length of time the FLEX decoder keeps the receiver off before applying the first warm-up state's receiver control value to the receiver control lines. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 159.375 ms (ST = FF in hexadecimal). (value after reset = 625 μs)

3.3.7 Receiver Warm Up Setting Packets

Table 3–12 shows Receiver Warm Up Setting Packet bit assignments.

Table 3–12. Receiver Warm Up Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	s_3	s_2	s_1	s_0
Byte 2	SE	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

s: Setting number. This bit is the receiver control setting for which this packet's values are to be applied. Table 3–13 shows the names of each of the values for **s** that apply to this packet.

Table 3–13. Receiver Control Setting

s_3	s_2	s_1	s_0	Setting Name
0	0	0	1	Warm Up 1
0	0	1	0	Warm Up 2
0	0	1	1	Warm Up 3
0	1	0	0	Warm Up 4
0	1	0	1	Warm Up 5

SE: Step Enable. The receiver setting is enabled when this bit is set. If a step in the warm-up sequence is disabled, all steps following the disabled step are ignored. (value after reset = 0)

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0–S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the amount of time the FLEX decoder waits before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 79.375 ms (ST = 7F in hexadecimal). (value after reset = 625 μs)

3.3.8 3200 sps Sync Setting Packets

Table 3–14 shows the 3200 symbols per second (sps) Sync Setting Packet bit assignments.

Table 3–14. 3200 sps Sync Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	1	1	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0–S7) for this receiver state. (value after reset = 0)

ST: Step Time. This bit is the amount of time the FLEX decoder waits before expecting good signals on the EXTS1 and EXTS0 signals after warming up. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01) to 79.375 ms (ST=7F in hexadecimal). (value after reset = 625 μs)

3.3.9 Receiver On Setting Packets

Table 3–15 shows the Receiver On Setting Packet bit assignments.

Table 3–15. Receiver On Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	S_3	S_2	S_1	S_0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
Byte 0	0	0	0	0	0	0	0	0

s: Setting number. This bit is the receiver control setting for which this packet's values are to be applied. Table 3–16 shows the names of each of the values for **s** that apply to this packet.

Table 3–16. Receiver On Setting Names

s_3	s_2	s_1	s_0	Setting Name
0	1	1	1	1600 sps Sync
1	0	0	0	3200 sps Data
1	0	0	1	1600 sps Data

LBC: Low Battery Check. If this bit is set, the FLEX decoder checks the status of the LOBAT port just before leaving this receiver state. (value after reset = 0)

CLS: Control Line Setting. This bit is the value to be output on the receiver control lines (S0–S7) for this receiver state. (value after reset = 0)

3.3.10 Frame Assignment Packets

The FLEX protocol defines that each address of a FLEX pager is assigned a home frame and a pager collapse. This information is determined by the service provider. The FLEX decoder must be configured so that a frame that is assigned by one or more of the addresses' home frames and pager collapses has its corresponding configuration bit set. For example, if the FLEX decoder has one enabled address and it is assigned to frame 3 with a battery cycle of 4 (see Section 2.6, *FLEX CAPCODE,* for a definition of battery cycle) the AF bits for frames 3, 19, 35, 51, 67, 83, 99, and 115 should be set and the AF bits for all other frames should be cleared. There are 8 Frame Assignment Packets (see Table 3–17). The IDs for these packets range from 32 to 39 (decimal).

Table 3–17. Frame Assignment Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	1	0	0	f_2	f_1	f_0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
Byte 0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

f: Frame range. This bit value determines which 16 frames correspond to the 16 AF bits in the packet, as shown in Table 3–18. At least one of these bits must be set when the FLEX decoder is turned on by setting the ON bit in the control packet. (value after reset = 0)

Table 3–18. Frame Range Packet Bit Assignments

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	Frame 127	Frame 112
0	0	1	Frame 111	Frame 96
0	1	0	Frame 95	Frame 80
0	1	1	Frame 79	Frame 64
1	0	0	Frame 63	Frame 48
1	0	1	Frame 47	Frame 32
1	1	0	Frame 31	Frame 16
1	1	1	Frame 15	Frame 0

AF: Assigned Frame. If this bit is set, the FLEX decoder considers the corresponding frame to be assigned via an address's home frame and pager collapse. (value after reset = 0)

3.3.11 User Address Enable Packet

The User Address Enable Packet (see Table 3–19) is used to enable and disable the 16 user address words. Although the host is allowed to change the user address words while the FLEX decoder is decoding FLEX signals, the host must disable a user address word before changing it. The ID of the User Address Enable Packet is 120 (decimal).

Table 3–19. User Address Enable Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_9	UAE_8
Byte 0	UAE_7	UAE_6	UAE_5	UAE_4	UAE_3	UAE_2	UAE_1	UAE_0

UAE: User Address Enable. When this bit is set, the corresponding user address word is enabled. When it is cleared, the corresponding user address word is disabled. UAE_0 corresponds to the user address word configured using a packet ID of 128, and UAE_{15} corresponds to the user address word configured using a packet ID of 143. In some instances, if an invalid FLEX messaging address is programmed, it is not detected even when the address is enabled. (value after reset = 0)

3.3.12 User Address Assignment Packets

The FLEX decoder has 16 user address words. Each word can be programmed to be a short address or part of a long address. The addresses are configured using the Address Assignment Packets (see Table 3–20). Each user address can be configured as long or short and tone-only or regular. Although the host is allowed to send these packets while the FLEX decoder is on, the host must disable the user address word by clearing the

corresponding UAE bit in the User Address Enable Packet before changing any of the bits in the corresponding User Address Assignment Packet. This method allows for easy reprogramming of user addresses without disrupting normal operation. The IDs for these packets range from 128 to 143 (decimal).

Table 3–20. User Address Assignment Packet Bit Assignments

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Byte 3	1	0	0	0	a_3	a_2	a_1	a_0
Byte 2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
Byte 1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
Byte 0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

a: User Address word number. This bit specifies which address word is being configured. A zero in this field corresponds to address index zero (AI = 0) in the Address Packet received from the FLEX decoder when an address is detected (see subsection 3.4.2, *Address Packet*).

LA: Long Address. When this bit is set, the address is considered a long address. Both words of a long address must have this bit set. The first word of a long address must have an even user address word number and the second word must be in the address index immediately following the first word. Long addresses of the 2–3 and 2–4 set (see Section 2.6*, FLEX CAPCODE*) must be programmed to higher user address word numbers than long addresses of the 1–2, 1–3, and 1–4 set.

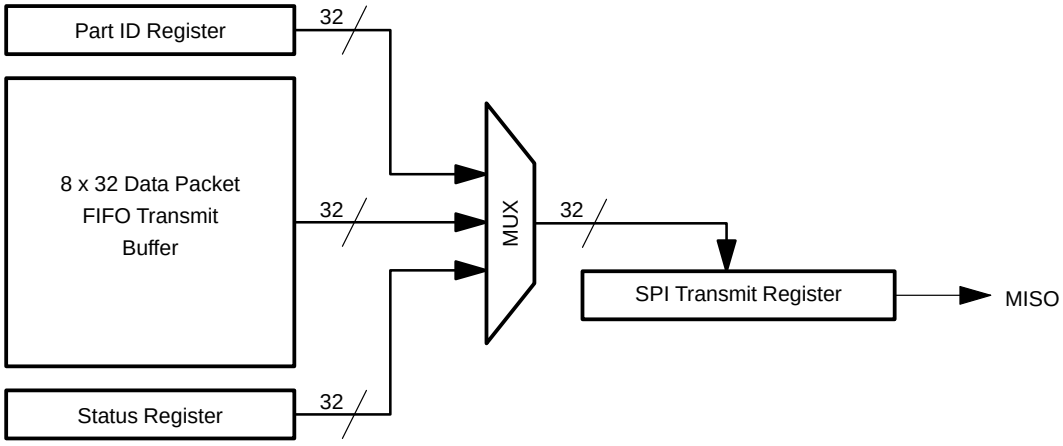
TOA: Tone-Only Address. When this bit is set, the FLEX decoder considers this address a tone-only address and does not decode a vector word when the address is received. If the TOA bit of a long address word is set, the TOA bit of the other word of the long address must also be set.

A: Address word. This bit is the 21-bit value of the address word. Valid FLEX messaging addresses must be used. In some instances, if an invalid FLEX messaging address is programmed, it is not detected even when the address is enabled.

3.4 Decoder-To-Host Packet Descriptions

The following sections describe the packets of information that are sent from the FLEX decoder to the host. In all cases the packets are sent MSB first (bit 7 of byte 3 = bit 31 of the packet = MSB). The FLEX decoder determines what data should be sent to the host. See Figure 3–8 for the FLEX decoder SPI Transmit Functional Block Diagram. If the FLEX decoder is disabled through the checksum feature (see subsection 3.3.1, *Checksum Packet*), the Part ID Packet is sent. Data packets relating to data received over the air are buffered in the 32-packet transmit buffer. The data packets include Block Information Word Packets, Address Packets, Vector Packets, and Message Packets. If the FLEX decoder is enabled and there is data in the transmit buffer, a packet from the transmit buffer is sent. If the FLEX decoder is enabled and no Data Packet or Part ID Packet is pending, the FLEX decoder sends the Status Packet (which is not buffered). If a buffer overflow occurs, the FLEX decoder automatically stops decoding and clears the buffer information.

Figure 3–8. FLEX Decoder SPI Transmit Functional Block Diagram



3.4.1 Block Information Word Packet

The Block Information Word Packet is the first field following the synchronization codes of the FLEX protocol. (see Chapter 2, *FLEX Signal Structure*). This field contains information about the frame such as number of addresses and messages, as well as information about current time. The first block information word of each phase is used internally by the FLEX decoder and is never transmitted to the host.

All time and date block information words 2–4 (f = 001, 010, or 101) can be optionally sent to the host by setting the SBI bit in the control packet (see subsection 3.3.3, *Control Packet*). Table 3–21 shows the Block Information Word Packet bit assignments. When the SBI bit is set and a block information word is received with an uncorrectable number of bit errors, the FLEX decoder sends the block information word to the host with the e bit set regardless of the value of the **f** field in the block information word. The FLEX decoder does not support decoding of the vector and message words associated with the

Data/System Message block info word (f = 101). The ID of a Block Information Word Packet is 0 (decimal).

Table 3–21. Block Information Word Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	e	x	x	x	x	f_2	f_1	f_0
Byte 1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
Byte 0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

e: Set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

x: Unused bits. The value of these bits is not guaranteed.

f: Word format type. The value of these bits modifies the meaning of the **s** bits in this packet as described in Table 3–22. If the e bit is not set, this field is one of 001, 010, or 101.

s: These are the information bits of the block information word. The definition of these bits depend on the f bits in this packet. Table 3–22 describes the block information words that the FLEX decoder decodes. See Section 2.5, *FLEX Local Time and Date,* for detailed information about these block information words.

Table 3–22. Block Information Word Definitions

$f_2f_1f_0$	s_{13} s_{12} s_{11} s_{10} s_9 s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	Description
001	m_3 m_2 m_1 m_0 d_4 d_3 d_2 d_1 d_0 Y_4 Y_3 Y_2 Y_1 Y_0	Month, Day, Year
010	S_2 S_1 S_0 M_5 M_4 M_3 M_2 M_1 M_0 H_4 H_3 H_2 H_1 H_0	Second, Minute, Hour
101	z_9 z_8 z_7 z_6 z_5 z_4 z_3 z_2 z_1 z_0 A_3 A_2 A_1 A_0	System Message

3.4.2 Address Packet

The Address Packet field follows the Block Information Word Packet field in the FLEX protocol. (see Chapter 2, *FLEX Signal Structure*). It contains all of the addresses in the frame. See Table 3–23 for the Address Packet bit assignments.

If fewer than three bit errors are detected in a received address word and the received address word matches an enabled address assigned to the FLEX decoder, an Address Packet is sent to the host processor. The Address Packet contains assorted data about the address and its associated vector and message. The ID of an Address Packet is 1 (decimal).

Table 3–23. Address Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	PA	x	x	LA	x	x	x	x
Byte 1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
Byte 0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

PA: Priority Address. This bit is set if the address was received as a priority address.

LA: Long Address type. This bit is set if the address was programmed in the FLEX decoder as a long address.

AI: Address Index (valid values are 0 through 15 and 128 through 143). The index identifies which of the addresses was detected. Values 0 through 15 correspond to the 16 programmable address words. Values 128 through 143 correspond to the 16 temporary addresses. For long addresses, the address detect packet is only sent once and the index refers to the second word of the address.

TOA: Tone Only Address. Set if the address was programmed in the FLEX decoder as a tone-only address. No vector word is sent for tone-only addresses.

WN: Word Number of vector (2–87). Describes the location in the frame of the vector word for the detected address. This value is invalid for this packet if the TOA bit is set.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3 Vector Packet

The Vector Packet field follows the Address Packet field. See Chapter 2, *FLEX Signal Structure*, for more details. Each Vector Packet must be matched to its corresponding Address Packet. The ID of the vector packet is the word number where the vector word was received in the frame. This value corresponds to the WN bits sent in the associated Address Packet. For long addresses, the first message word is transmitted in the word location that immediately follows the associated vector (see Section 3.7, *Message Building*). The word number (identified by b_6 to b_0) in the Vector Packet indicates the message start of the second message word if the message is longer than one word.

There are several types of vectors—three types of Numeric Vectors, a Short Message/Tone Only Vector, and a Short Instruction Vector. Each vector is described in the following subsections.

The Numeric Vector Packets have associated Message Word Packets in the message field. The host must use the n and b bits of the vector word to calculate what message word locations are associated with the vector. The message word locations must match.

For any Address Packet sent to the host (except tone-only addresses), a corresponding Vector Packet is always sent. If more than two bit errors are detected (via BCH calculations, parity calculations, check character calculations, or value validation) in the vector word, the e bit is set and the message words are not sent.

3.4.3.1 Numeric Vector Packet

Table 3–24 shows the Numeric Vector Packet bit assignments.

Table 3–24. Numeric Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	x	x	x	x	V_2	V_1	V_0
Byte 1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
Byte 0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

V: Vector type identifier.

Table 3–25 shows the Numeric Vector definitions.

Table 3–25. Numeric Vector Definitions

$V_2V_1V_0$	Name	Description
011	Standard Numeric Format	No special formatting of characters is specified
100	Special Format Numeric Vector	Formatting of the received characters is predetermined by special rules in the host. See Section 2.2, *FLEX Message Word Definitions.*
111	Numbered Numeric Vector	The received information has been numbered by the service provider to indicate that all messages have been properly received

WN: Word Number of vector (2–87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

K: Beginning check bits of the message.

n: Number of message words in the message including the second vector word for long addresses (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is in the word location that immediately follows the associated vector.

b: Word number of message start in the message field (3–87 decimal). For long addresses, the word number indicates the location of the second message word.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3.2 Short Message/Tone Only Vector

Table 3–26 shows the Short Message/Tone Only Vector Packet bit assignments.

Table 3–26. Short Message/Tone Only Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	x	x	x	x	V_2	V_1	V_0
Byte 1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
Byte 0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

V: 010 for a Short Message/Tone Only Vector.

WN: Word Number of vector (2–87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than 2 bit errors are detected in the word or, if after error correction, the check character calculation fails.

d: Data bits whose definition depend on the value of t in this packet, as shown in Table 3–27. If this vector is received on a long address and the e bit in this packet is not set, the decoder sends a Message Packet from the word location immediately following the Vector Packet. Except for the short message on a non-network address (t = 0), all message bits in the Message Packet are unused and should be ignored.

Table 3–27. Short Message/Tone Only Vector Definitions

t_1t_0	d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
00	c_3 c_2 c_1 c_0 b_3 b_2 b_1 b_0 a_3 a_2 a_1 a_0	First 3 numeric characters (see Note 1)
01	s_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0 S_2 S_1 S_0	8 sources (S) and 9 unused bits (s)
10	s_1 s_0 R_0 N_5 N_4 N_3 N_2 N_1 N_0 S_2 S_1 S_0	8 sources (S), message number (N), message retrieval flag (R—see Note 2), and 2 unused bits (s)
11		spare message type

Notes: 1) For long addresses, an extra five characters are sent in the Message Packet immediately following the Vector Packet.

2) For a description of the R and N bits, see the description of the same bits for numeric messages in subsection 2.2.1, *Numeric Data Message*.

t: Message type. These bits define the meaning of the d bits in this packet.

x: Unused bits. The value of these bits is not guaranteed.

3.4.3.3 Short Instruction Vector

The Short Instruction Vector is used for assigning temporary addresses that may be associated with a group call. Table 3–28 shows the Short Instruction Vector Packet bit assignments.

Table 3–28. Short Instruction Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
Byte 2	e	x	x	x	x	V_2	V_1	V_0
Byte 1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
Byte 0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

V: 001 for a Short Instruction Vector.

WN: Word Number of vector (2–87 decimal). Describes the location of the vector word in the frame.

e: This bit is set if more than two bit errors are detected in the word or, if after error correction, the check character calculation fails.

d: Data bits whose definition depend on the i bits in this packet, as shown in Table 3–29. If this vector is received on a long address and the **e** bit in this packet is not set, the decoder sends a Message Packet immediately following the Vector Packet. All message bits in the message packet are unused and should be ignored.

Table 3–29. Short Instruction Vector Definitions

$i_2i_1i_0$	d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	Description
000	a_3 a_2 a_1 a_0 f_6 f_5 f_4 f_3 f_2 f_1 f_0	Temporary address assignment (see Note)
001		Reserved
010		Reserved
011		Reserved
100		Reserved
101		Reserved
110		Reserved
111		Reserved for test

Note: While the FLEX decoder does not support this mode of the short instruction vector, it will be sent to the host if it is received.

i: Instruction type. These bits define the meaning of the **d** bits in this packet.

x: Unused bits. The value of these bits is not guaranteed.

3.4.4 Message Packet

The Message Packet field follows the Vector Packet field in the FLEX protocol. It contains the message data, checksum information, and may contain fragment numbers and message numbers. See Section 2.2, *FLEX Message Word Definitions*.

If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in Message Packets. See Table 3–30 for the Message Packet bit assignments.

The ID of the Message Packet is the word number where the message word was received in the frame.

Table 3–30. Message Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN6	WN5	WN4	WN3	WN2	WN1	WN0
Byte 2	e	x	x	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
Byte 1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
Byte 0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

WN: Word Number of message word (3–87 decimal). Describes the location of the message word in the frame.

e: This bit is set if more than 2 bit errors are detected in the word.

i: These are the information bits of the message word. The definitions of these bits depend on the vector type and which word of the message is being received. See Section 2.2, *FLEX Message Word Definitions,* for a detailed description of these bits.

3.4.5 Status Packet

The Status Packet contains various types of information that the host may require. The Status Packet is sent to the host whenever the FLEX decoder is polled and has no other data to send. The FLEX decoder can also prompt the host to read the Status Packet due to events for which the FLEX decoder was configured to send it (see subsection 3.3.2, *Configuration Packet*, and subsection 3.3.3, *Control Packet*, for a detailed description of the bits). Table 3–31 shows the Status Packet bit assignments. The FLEX decoder prompts the host to read a Status Packet if any of the following conditions are true.

- SMU bit in the Status Packet and the SME bit in the Configuration Packet are set.
- MT bit in the Status Packet and the MTE bit in the Configuration Packet are set.
- LBU bit in the Status Packet is set.
- BOE bit in the Status Packet is set.

The ID of the Status Packet is 127 (decimal).

Table 3–31. Status Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	1	1	1
Byte 2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
Byte 1	SM	LB	x	x	c_3	c_2	c_1	c_0
Byte 0	SMU	LBU	x	MT	x	x	x	BOE

FIV: Frame Info Valid. This bit is set when a valid frame info word has been received since becoming synchronous to the system and the f, c, and **n** fields contain valid values. If this bit is clear, no valid frame info words have been received since the FLEX decoder became synchronous to the system. This value changes from 0 to 1 at the end of block 0 of the frame in which the 1st frame info word is properly received. It is cleared when the FLEX decoder goes into asynchronous mode. This bit is initialized to 0 when the FLEX decoder is reset and when the FLEX decoder is turned off by clearing the ON bit in the Control Packet.

f: Current frame number. This bit value is updated every frame regardless of whether the FLEX decoder needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: Synchronous Mode. This bit is set when the FLEX decoder is synchronous to the system. The FLEX decoder sets this bit when the first synchronization words are received. It clears this bit when synchronization to the FLEX decoder signal is lost. This bit is initialized to 0 when the FLEX decoder is reset and when it is turned off by clearing the ON bit in the Control Packet.

LB: Low Battery. This bit is set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the Receiver Control Packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the Configuration Packet when the FLEX decoder is turned on by setting the ON bit in the Control Packet.

c: Current system cycle number. This value is updated every frame regardless of whether the FLEX decoder needs to decode the frame.This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SMU: Synchronous Mode Update. This bit is set if the SM bit has been updated in this packet. When the FLEX decoder is turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search window after the FLEX decoder is turned on expires (SM stays 0). The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial A search window expires. After the initial synchronous mode update, the SMU bit is set whenever the FLEX decoder transitions from/to synchronous mode. It is cleared when read. Changes in the SM bit due to turning off the FLEX decoder do not cause the SMU bit to be set. This bit is initialized to 0 when the FLEX decoder is reset.

LBU: Low Battery Update. This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. It is cleared when read. The host controls when the LOBAT pin is read via the Receiver Control Packets. Changes in the LB bit due to turning on the FLEX decoder do not cause the LBU bit to be set. This bit is initialized to 0 when the FLEX decoder is reset.

MT: Minute Time-Out. This bit is set if one minute has elapsed. It is cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

BOE: Buffer Overflow Error. This bit is set when information has been lost due to slow host response time. When the SPI transmit buffer on the FLEX decoder overflows, the FLEX decoder clears the transmit buffer, turns off decoding by clearing the ON bit in the Control Packet, and sets this bit. Cleared when read. This bit is initialized to 0 when the FLEX decoder is reset.

x: Unused bits. The value of these bits is not guaranteed.

3.4.6 Part ID Packet

The Part ID Packet is sent by the FLEX decoder whenever the FLEX decoder is disabled due to the checksum feature (see subsection 3.3.1, *Checksum Packet*). Because the FLEX decoder is disabled after reset, this is the first packet that will be received by the host after reset. Table 3–32 shows the Part ID Packet bit assignments. The ID of the Part ID Packet is 255 (decimal)**.**

Table 3–32. Part ID Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	1	1	1	1	1	1	1	1
Byte 2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
Byte 1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
Byte 0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

MDL: Model. This identifies the FLEX decoder model. Current value is 0.

CID: Compatibility ID. This value describes what other parts with the same model number are compatible with this part. Current value is 1. Any future versions of FLEX decoder that have MDL set to 0 and CID_0 set to 1 will be 100% compatible to this version.

REV: Revision. This identifies the revision and manufacturer of the FLEX decoder. Currently defined values are shown in Table 3–33.

Table 3–33. FLEX Decoder Revisions

Rev	Description
0	Motorola Semiconductor Products Sector Production Parts
1	Texas Instruments Production Parts

3.5 Electrical Characteristics

Table 3–34 shows the absolute maximum ratings over operating temperature ranges for the TLV5594 FLEX decoder.

Table 3–34. Absolute Maximum Ratings Over Operating Temperature Ranges (Unless Otherwise Noted)†

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, failsafe	–0.5 V to 6.5 V
Output voltage range, standard	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±20 mA
Virtual junction temperature, T_J	150°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes: 1) Applies to input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail-safe pins.

2) Applies to output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe pins.

Table 3–35 shows the recommended operating conditions for the TLV5594 FLEX decoder.

Table 3–35. Recommended Operating Conditions

		Min	Nom	Max	Unit
V_{CC}	Supply voltage	1.8	3.3	3.6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage†	0		V_{CC}	V
V_{IH}	High-level input voltage	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage			$0.2V_{CC}$	V
t_t	Input transition (rise and fall) time	0		25	ns
T_A	Operating ambient temperature range	–40	25	90	°C
T_J	Virtual junction temperature‡	–40	25	125	°C

† Applies to output buffers

‡ These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. Customer is responsible for verifying junction temperature.

Table 3–36 shows the electrical characteristics over recommended operating conditions for the TLV5594 FLEX decoder.

Table 3–36. Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = Rated	V_{CC} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = Rated		0.5	V
V_{IT+}	Positive-going threshold voltage†	CMOS compatible		0.7 V_{CC}	V
$V_{IT–}$	Negative-going threshold voltage†	CMOS compatible	0.2 V_{CC}		V
V_{hys}	Hysteresis# ($V_{IT+} – V_{IT–}$)	CMOS compatible	0.1 V_{CC}	0.3 V_{CC}	V
I_{OZ}	3-state-output Hi-Z current	V_I = V_{CC} or GND‡		±10	µA
I_{IL}	Low-level input current	V_I = GND§		–1	µA
I_{IH}	High-level input current	V_I = V_{CC}¶		1	µA

† Applies to input and bidirectional buffers with hysteresis
‡ 3-state or open-drain output must be in the high-impedance mode.
§ Specifications only apply with pullup terminator turned off.
¶ Specifications only apply with pulldown terminator turned off.

3.6 Receiver Control

The FLEX decoder has 5 programmable receiver control lines (S0–S4). The host controls the receiver warm-up and shut-down timing and the various settings on the control lines through configuration registers on the FLEX decoder. The configuration registers for most settings allow the host to configure (1) what setting is applied to the control lines, (2) how long to apply the setting, and (3) if the low battery (LOBAT) input pin is polled before changing from the setting. With this programmability, the FLEX decoder should be able to interface with many off-the-shelf receiver ICs. For details on the configuration of the receiver control settings, see Section 3.3.5, *Receiver Control Configuration Packets*.

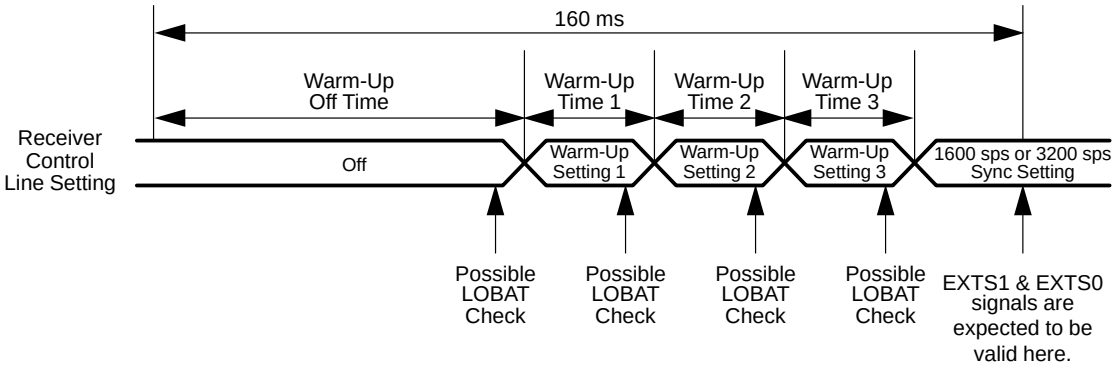
3.6.1 Receiver Settings at Reset

The receiver control ports are three-state outputs that are set to the high-impedance state when the FLEX decoder is reset and until the corresponding FRS bit in the receiver line control packet is set, or until the FLEX decoder is turned on by setting the ON bit in the Control Packet. This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the FLEX decoder. When the FLEX decoder is turned on, the receiver control ports are driven to the settings configured by the Receiver Control Configuration Packet until the FLEX decoder is reset again.

3.6.2 Normal Receiver Warm-Up Sequence

The FLEX decoder allows for up to four steps associated with warming up the receiver. When the FLEX decoder turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS0 and EXTS1 input pins. The first step of the warm-up sequence involves leaving the receiver control lines in the Off state for the amount of time programmed for Warm-Up Off Time. At the end of the Warm-Up Off Time, the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found. At the end of the last used warm-up setting, the 1600 symbols per second (sps) Sync Setting or the 3200 sps Sync Setting is applied to the receiver control lines, depending on the current state of the FLEX decoder. The sum total of all of the used warm-up times and the Warm-Up Off Time must not exceed 160 ms. If it exceeds 160 ms, the FLEX decoder executes the receiver shut-down sequence at the end of the 160 ms warm-up period. Figure 3–9 shows the receiver warm-up sequence while decoding when all warm-up settings are enabled.

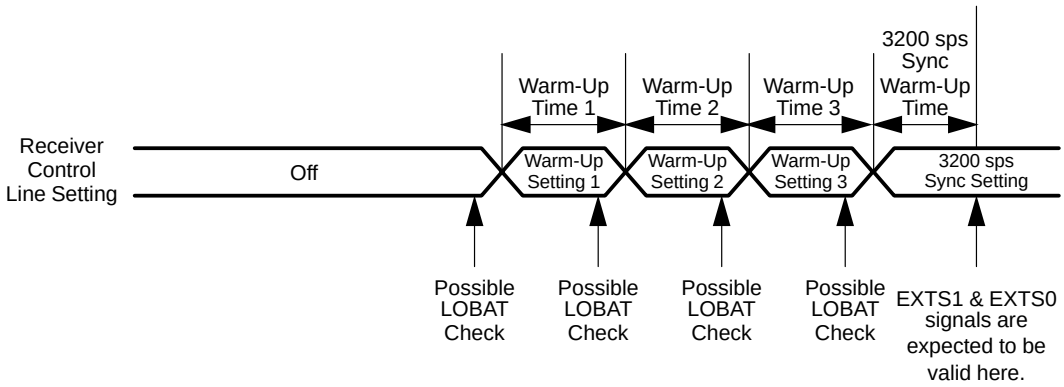
Figure 3–9. Receiver Warm-Up Sequence While Decoding



3.6.3 First Receiver Warm-Up Sequence

When the FLEX decoder is turned on by setting the ON bit in the Control Packet, the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found. When a disabled warm-up setting is found, the 3200 sps Sync Setting is applied to the receiver control lines and the decoder does not expect a valid signal until after the 3200 sps Sync Warm-Up Time has expired. Figure 3–10 shows the receiver warm-up sequence when the FLEX decoder is first turned on and when all warm-up settings are enabled.

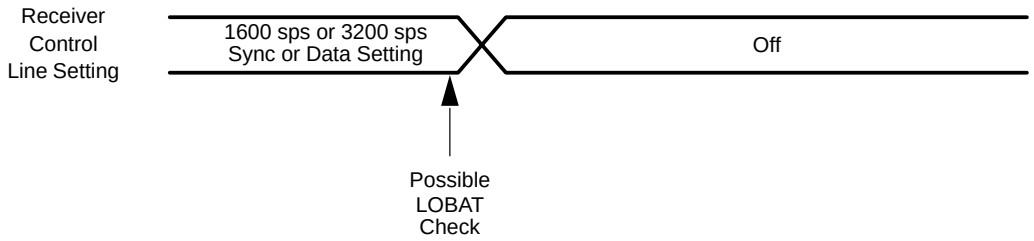
Figure 3–10. Receiver Warm-Up Sequence When Decoding Turned On



3.6.4 Receiver Shut-Down Sequence

Upon shutting down the receiver, the FLEX decoder transitions directly from the current *On* setting to the *Off* setting. Figure 3–11 shows the receiver turn-off sequence when all shut-down settings are enabled.

Figure 3–11. Receiver Shut-Down Sequence



3.6.5 Miscellaneous Receiver States

In addition to the warm-up and shut-down states, the FLEX decoder has four other receiver states. When these settings are applied to the receiver control lines, the FLEX decoder decodes the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the data that the FLEX decoder decodes. Because of this, there is no time setting associated with these settings. The four settings are as follows:

- **1600 sps Sync Setting**:

  This setting is applied when the FLEX decoder is searching for a 1600 sps signal.

- **3200 sps Sync Setting**:

  This setting is applied when the FLEX decoder is searching for a 3200 sps signal.

- **1600 sps Data Setting**:

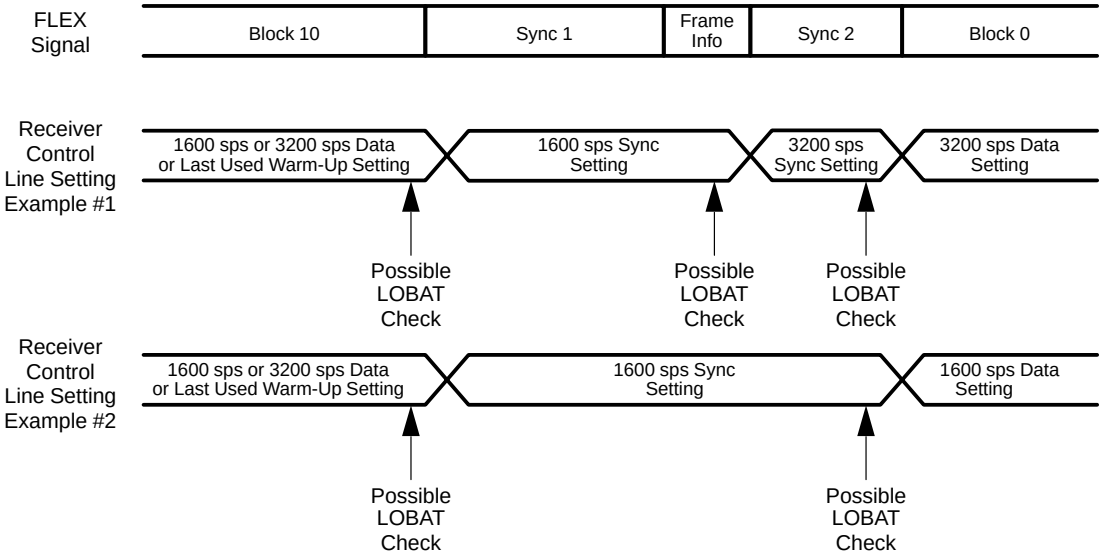
  This setting is applied after the FLEX decoder has found the C or $\overline{C}$ sync word in a 1600 sps frame.

- **3200 sps Data Setting**:

  This setting is applied after the FLEX decoder has found the C or $\overline{C}$ sync word in a 3200 sps frame.

Figure 3–12 shows some examples of how these settings are used in the FLEX decoder.

Figure 3–12. Examples of Receiver Control Transitions



3.6.6 Low Battery Detection

The FLEX decoder can be configured to poll the LOBAT input pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the FLEX decoder changes the receiver control lines from that setting to another setting. The FLEX decoder sends a Status Packet whenever the value on two consecutive reads of the LOBAT pin yields different results.

3.7 Message Building

A simple message consists of an Address Packet followed by a Vector Packet indicating the word numbers of associated Message Packets. Table 3–37 and Table 3–38 show a more complex example of receiving three Messages and two Block Information Word Packets in the first two blocks of a 2-phase 3200 bps, FLEX frame. Note that the messages shown may be portions of fragmented or group messages. Note further that in the case of a 6400-bps FLEX signal, there would be four phases: A, B, C and D, and in the case of a 1600-bps signal, there would be only a single phase A.

Table 3–37 shows the block number, word number (WN), and word content of both phases A and C. Note that the contents of words not meant to be received by the host are left blank. Each phase begins with a block information word (WN 0); this is not sent to the host. The first message is in phase A and has an address (WN 3), vector (WN 7), and three message words (WN 9–11). The second message is also in phase A and has an address (WN 4), a vector (WN 8), and four message words (WN 12–15). The third message is in phase C and has a 2-word long address (WN 5–6) followed by a vector (WN 10) and three message words. Because the third message is sent on a long address, the first message word (WN 11) begins immediately after the vector. The vector indicates the location of the second and third message words (WN 14–15).

Table 3–37. FLEX Signal

Block	Word Number	Phase A	Phase C
0	0	BIW1	BIW1
	1		BIW
	3	ADDRESS 1	BIW
	4	ADDRESS 2	
	5		LONG ADDRESS 3 WORD 1
	6		LONG ADDRESS 3 WORD 2
	7	VECTOR 1	
1	8	VECTOR 2	
	9	MESSAGE 1,1	
	10	MESSAGE 1,2	VECTOR 3
	11	MESSAGE 1,3	MESSAGE 3,1
	12	MESSAGE 2,1	
	13	MESSAGE 2,2	
	14	MESSAGE 2,3	MESSAGE 3,2
	15	MESSAGE 2,4	MESSAGE 3,3

The numeric FLEX decoder is only capable of receiving messages and information words from a single phase of a frame. While the example in Table 3–37 shows messages being transmitted in both phases of the frame, the paging infrastructure, when properly configured, only sends messages to a Numeric FLEX decoder device on the assigned phase. If messages are incorrectly sent in other phases, the Numeric FLEX decoder only receives messages sent in the phase it was configured to decode.

Table 3–38 shows the sequence of packets received by the host. The FLEX decoder processes the FLEX signal one block at a time in the assigned phase. Thus, the address and vector information in block 0 phase A is packetized and sent to the host in packets 1–3. Packets 4–11 correspond to information in block 1.

Table 3–38. FLEX Decoder Packet Sequence

Packet	Packet Type	Phase	Word Number	Comment
1st	ADDRESS	A	N.A. (7)	Address 1 has a vector located at WN 7
2nd	ADDRESS	A	N.A. (8)	Address 2 has a vector located at WN 8
3rd	VECTOR	A	7	Vector for Address 1: Message Words located at WN = 9 to 11, phase A
4th	VECTOR	A	8	Vector for Address 2: Message Words located at WN = 12 to 15, phase A
5th	MESSAGE	A	9	Message information for Address 1
6th	MESSAGE	A	10	Message information for Address 1
7th	MESSAGE	A	11	Message information for Address 1
8th	MESSAGE	A	12	Message information for Address 2
9th	MESSAGE	A	13	Message information for Address 2
10th	MESSAGE	A	14	Message information for Address 2
11th	MESSAGE	A	15	Message information for Address 2

The first message is built by relating packets 1, 3, and 5–7. The second message is built by relating packets 2, 5 and 8–11.

Appendix A

TLV5590 Data Sheet

This chapter contains a complete data sheet for the TLV5590 converter.

- **Supports FLEX™ Protocol Messaging Systems With The TLV559X FLEX Decoder**
- **3-Pole Butterworth Low-Pass Selectable Dual-Bandwidth Audio Filter**
  - **BW 1 = 1 kHz ±5% (– 3 dB)**
  - **BW 2 = 2 kHz ±5% (– 3 dB)**
- **Both Peak and Valley Detectors Available**
- **2-Bit Analog-to-Digital Converter**
- **Operating Temperature Range . . . –25°C to 85°C**
- **Four Modes of Operation:**
  - **Fast Track**
  - **Slow Track**
  - **Hold**
  - **Standby**
- **2.7-V to 3.3-V Single Power Supply Operation**

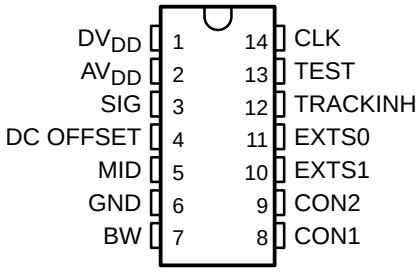
applications

- **FLEX Protocol Numeric and Alphanumeric Messaging Systems**
- **One-Way or Two-Way**

description

The Texas Instruments (TI™) TLV5590 analog-to-digital converter (ADC) is a system level solution to interface a 4-level baseband audio signal to a digital decoder. The TLV5590 is a direct interface to the TLV559X FLEX decoder. Designed primarily for messaging applications, the TLV5590 incorporates signal conditioning, both peak and valley detection along with analog-to-digital conversion. A selectable third-order Butterworth filter with cutoff frequencies of 1 kHz and 2 kHz is included. The peak and valley detectors are implemented with a unique design that does not require external capacitors. Two 8-bit digital-to-analog converters (DACs) are used in a feedback loop to automatically adjust to the peak and valley levels. The DAC outputs are used to set V_{ref+} and V_{ref-} for the 2-bit ADC. Modes of operation include fast track, slow track, hold, and standby. The standby mode maximizes battery life. The TLV5590 operates on a single power supply down to 2.7 V.

D PACKAGE
(TOP VIEW)



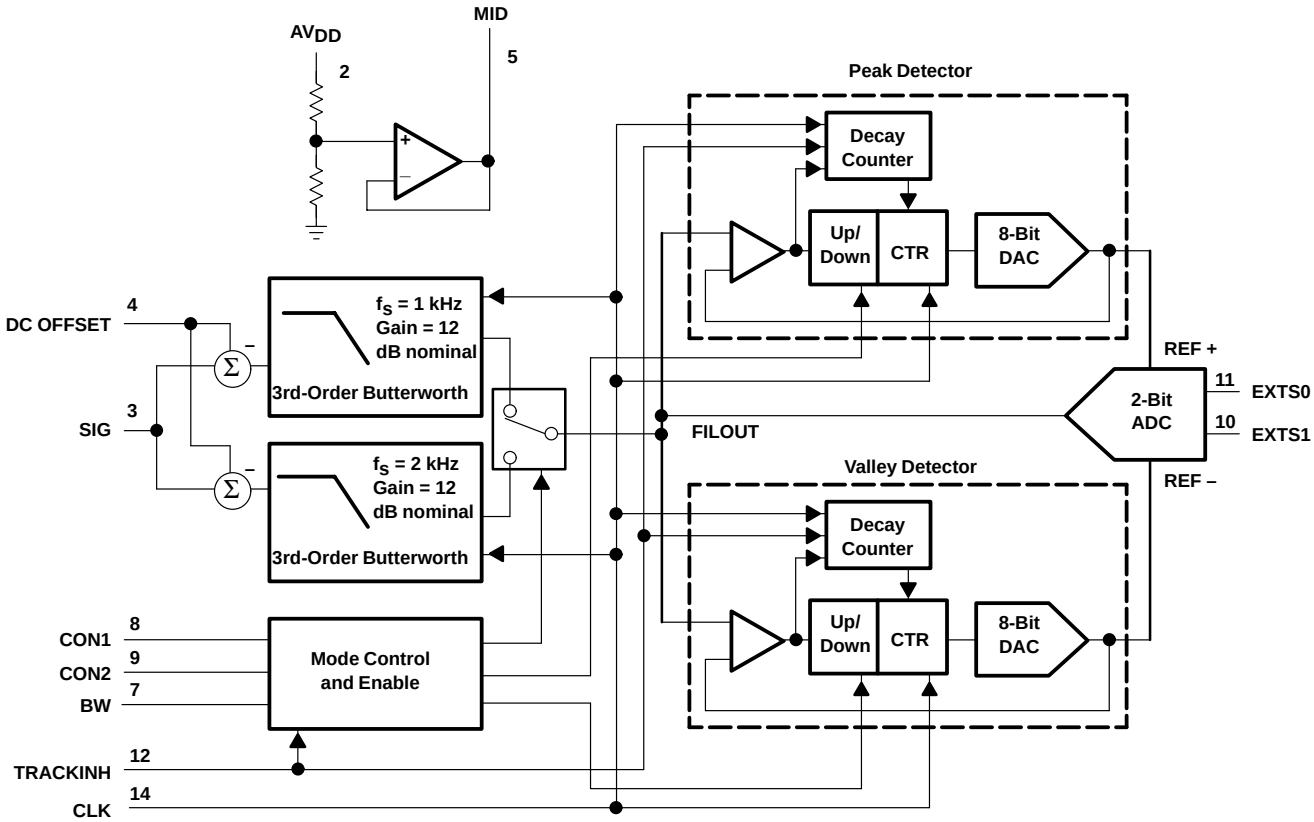
AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (D)
–25°C to 85°C	TLV5590ED

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FLEX is a trademark of Motorola Inc.
TI is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	2	I	Analog supply voltage
BW	7	I	Digital bandwidth select. A high level on BW selects the 2-kHz filter cutoff and a low level selects the 1-kHz filter cutoff.
CON1	8	I	Digital control 1 input. In conjunction with CON2, CON1 selects fast track, slow track, hold, or standby mode.
CON2	9	I	Digital control 2 input. In conjunction with CON1, CON2 selects fast track, slow track, hold, or standby mode.
CLK	14	I	Digital clock input. CLK input is a 50% duty cycle transistor-transistor logic (TTL)-level clock input with nominal frequency of 38.4 kHz. The CLK input is edge sensitive in all non-test modes. For all test modes, the CLK input is level sensitive.
DC OFFSET	4	I	Analog dc offset correction input. The dc component of the audio signal should be applied to DC OFFSET.
DV_{DD}	1	I	Digital supply voltage
EXTS0	11	O	Digital output 0 of the ADC. Data bit 0 is the least significant bit (LSB).
EXTS1	10	O	Digital output 1 of the ADC. Data bit 1 is the most significant bit (MSB).
GND	6		Return terminal for the IC current
MID	5	O	Analog midpoint output. MID is a buffered output of $AV_{DD}/2$.
SIG	3	I	Analog audio signal input. An appropriate resistance capacitance (RC) low-pass filter (antialiasing filter) should be connected to SIG.
TEST	13	I	Digital test input enable. TEST should be connected to ground in normal operation.
TRACKINH	12	I	Digital track inhibit logic input. A high level on TRACKINH disables the peak and valley detector counters; a low level enables the peak and valley detector counters. The counters continue to decay at the decay rate while TRACKINH is a low level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD}, DV_{DD} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I . . . . . –0.3 V to AV_{DD} + 0.3 V
Output voltage range, EXTS0, EXTS1 . . . . . –0.3 V to DV_{DD} + 0.3 V
Offset input voltage, V_{IO} . . . . . –0.3 V to AV_{DD} + 0.3 V
Peak input current (any input) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}		2.7		3.3	V
Power supply ripple				0.002	V_{pp}
Input clock frequency, $f_{(CLK)}$			38.4		kHz
Input clock duty cycle		45	50	55	%
Voltage offset applied at DC OFFSET, $V_{I(DC\ OFFSET)}$ (see Notes 1 and 2)		0.25		V_{DD}–0.25	V
Analog input voltage, $V_{I(pp)}$ (See Notes 1 and 2)	V_{DD} = 3.1 V	0.25		V_{DD} – 0.25	V_{pp}
High-level control input voltage, V_{IH}	V_{DD} = 2.7 V to 3.3 V			0.2 DV_{DD}	V
Low-level control input voltage, V_{IL}	V_{DD} = 2.7 V to 3.3 V	0.8 DV_{DD}			V
Operating free-air temperature, T_A		–25		85	°C

NOTES: 1. $V_{I(OFFSET)} = V_Q - V_{I(DC\ OFFSET)}$, where V_Q is the dc quiescent voltage of the signal applied to the SIG terminal.

2. $$V_{I(PEAK)} = \frac{\left(\frac{V_{DD}}{2} - 0.25\ V\right)}{4.217} - V_{I(OFFSET)} - 80\ mV$$

The pass-band filter gain represents the maximum specified voltage gain in volts/volt of the filter. The maximum gain for the filter is 4.217 V/V (12.5 dB). The input voltage range from this equation defines the maximum allowable input signal at the SIG terminal with a given voltage, $V_{I(DC\ OFFSET)}$, applied at the DC OFFSET terminal and a quiescent dc input voltage, V_Q, of the signal applied at the SIG terminal. When the input voltage is within this range, the peak and valley DACs do not overrange. The 80 mV value is the tolerance on the voltage output at the MID terminal.

electrical characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 2.7$ V to 3.3 V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

power

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{DD}	Operating supply current	Fast track, slow track, or hold mode		250	µA
$I_{DD(standby)}$	Standby supply current	$V_{I(DC\ OFFSET)} = 0.8$ V, $V_{I(SIG)} = 0.8$ V For all digital inputs, $0 < V_I < 0.5$ V or $V_I > DV_{DD} - 0.5$ V.		1	µA

digital

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -100$ µA	$DV_{DD} - 0.5$			V
V_{OL}	Low-level output voltage	$I_{OL} = 100$ µA			0.5	V
I_{IH}	High-level input current	$V_I = DV_{DD}$		0.1	1	µA
I_{IL}	Low-level input current	$V_I = 0$		–0.1	–1	µA
C_i	Input capacitance, digital input			10		pF

analog

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Voltage accuracy at MID	$V_{DD} = 3$ V, $C_{L(MID)} = 220$ nF	1.42	1.5	1.58	V
Z_i	Input impedance at SIG (see Note 3)	$f_{(IN)} = 800$ Hz		1		MΩ
$Z_{i(offset)}$	Input impedance at DC OFFSET (see Note 3)		1	3		MΩ
$I_{I(SIG)}$	Average input current into SIG	$GND < V_I < AV_{DD}$		50	200	nA
C_i	Input capacitance, analog input at SIG			10		pF

NOTE 3: The input is capacitive and, therefore, is dynamic. Impedance specifications are based on $f_{(CLK)} = 38.4$ kHz.

operating characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 3$ V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

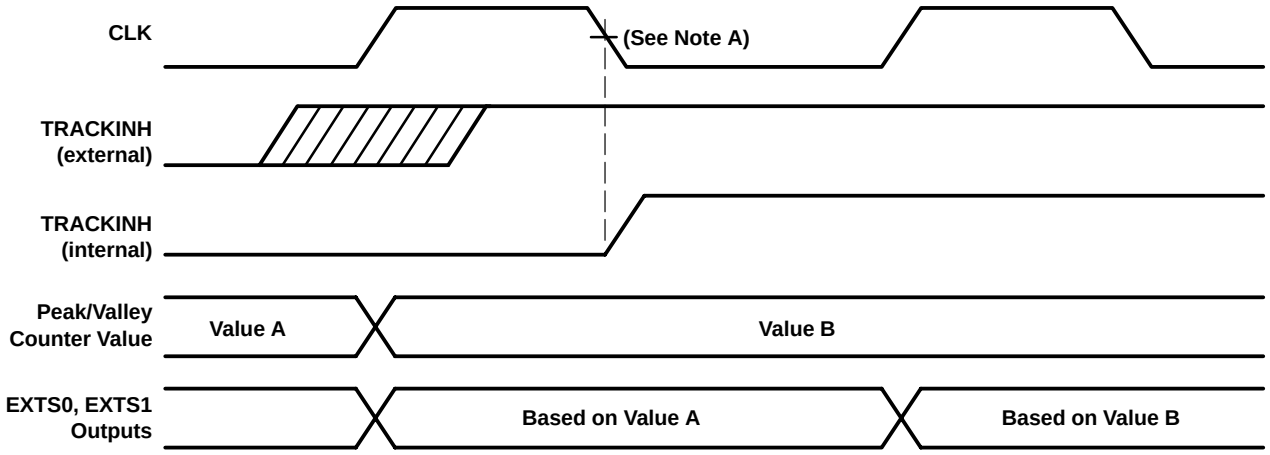
peak-and-valley DACs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Step size, LSB			$V_{DD}/255$		V
E_{FS}	Full-scale error				±1	LSB
E_{ZS}	Zero-code error				±3	LSB
	Voltage output drift	Hold mode		0		mV/ms
E_D	Differential linearity error				±1	LSB

low-pass filter

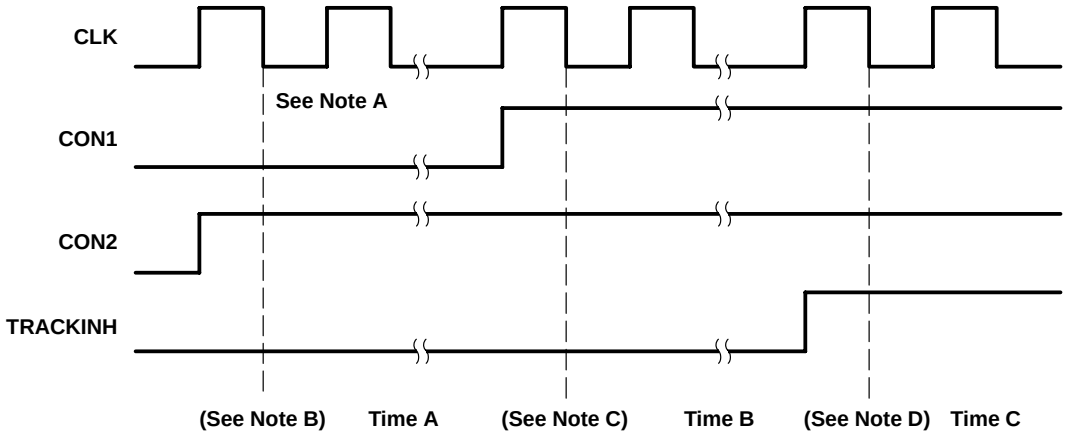
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Pass-band filter gain		$V_{I(DC\ OFFSET)} = 0.8$ V, $V_I = \pm 125$ mV	11.5	12	12.5	dB
	Filter attenuation	1-kHz filter	$V_I = \pm 500$ mV $f_{I(SIG)} = 1$ kHz	2	3	4	dB
		2-kHz filter	$V_I = \pm 500$ mV $f_{I(SIG)} = 2$ kHz	2	3	4	
t_s	Stabilization time		Off mode to hold mode (see Table 1)			5	ms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Internally the device recognizes input conditions on the falling edge of the clock only.

Figure 1. Timing Diagram



NOTES: A. Internally the device recognizes input conditions on the falling edge of the clock only.
B. On the next falling edge of the clock with the input conditions shown, the TLV5590 tracks signal in fast track mode (peak DAC counter counts down by 8 and up by 4) in time A.
C. On the next falling edge of the clock with the input conditions shown, the TLV5590 tracks signal in slow track mode (peak DAC counter counts up by 2 and down by 1 every 40 clock cycles) in time B.
D. On the next falling edge of the clock with the input conditions shown, the TLV5590 holds previous peak and valley levels in time C. For the 2-bit ADC, when TRACKINH = 1, EXTS0 and EXTS1 outputs respond in real time to the condition of SIG and DC OFFSET as long as the CLK signal is present.

Figure 2. Track and Lock Timing

TYPICAL CHARACTERISTICS

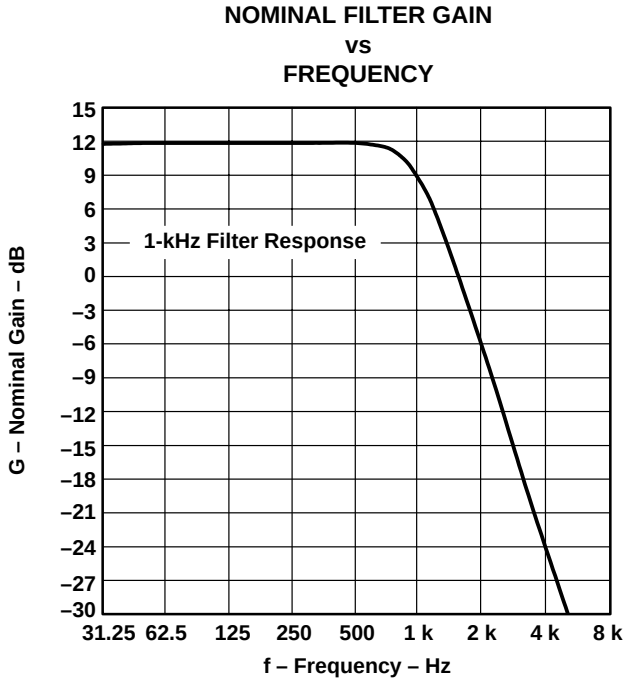


Figure 3

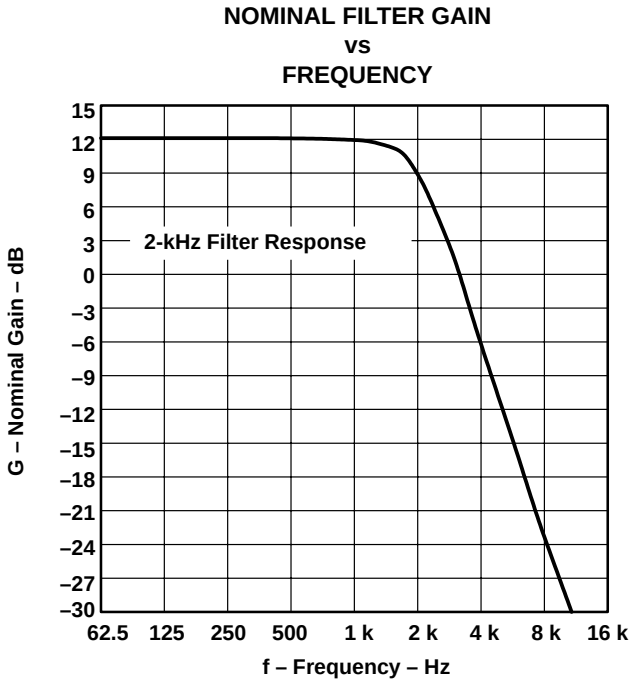


Figure 4

PRINCIPLES OF OPERATION

analog input operation

As shown in the functional block diagram, the signal input is dc-coupled using a single input terminal, SIG. The nominal dc content of the signal input should be supplied on an additional terminal, DC OFFSET. This allows the device to increase the signal to acceptable levels for threshold detection without saturating against the supplies. The signal processed by the device is effectively the voltage difference between the SIG and DC OFFSET terminals.

There is no antialiasing filter incorporated in the device. TI recommends that an external RC filter be added and set at the appropriate cutoff (see Figure 5).

The maximum peak analog signal voltage that can be applied to the SIG input terminal is given by:

$$V_{I(PEAK)} = \frac{\left(\frac{V_{DD}}{2} - 0.25\right)}{4.217} - V_{I(OFFSET)} - 80\ mV$$

where:

$V_{DD}/2$ = the nominal output voltage at the MID terminal

$V_{I(DC\ OFFSET)}$ = the voltage applied to the DC OFFSET terminal

and

$$V_{I(OFFSET)} = V_Q - V_{I(DC\ OFFSET)}$$

where:

V_Q = the dc quiescent voltage of the input signal

The value of 80 mV is the tolerance of the output voltage for the MID terminal at the output of the internal filter amplifier.

The peak-to-peak input voltage swing is double the result shown in the equation.

The main signal path consists of a third-order switched-capacitor Butterworth filter, with a switchable bandwidth between 1 kHz and 2 kHz to remove the noise from the input signal. The peak and valley amplitudes of the filter output signal are detected and subsequently used to convert the 4-level audio into 2-level digital signals using three switched capacitor comparators.

digital operation

The peak and valley detection is performed by a mixed mode solution using an 8-bit DAC and an up/down counter that has nonsymmetrical up and down count rates. Various modes are included to force the peak and valley circuits to slow track, fast track, or hold. An off mode is included that forces the device into a low-power condition. The decay rate of the peak and valley circuits is controlled by independent counters.

The device is clocked with a 38.4-kHz square wave supplied externally. The attack and decay times of the peak and valley circuits and the filter cutoff frequencies are directly related to this clock frequency. The decay timer is gated by the track inhibit input, TRACKINH, which is reset to 1 after an attack occurs and reset to 40 after a decay enable. The TRACKINH also prevents attack enable inputs from affecting the peak and valley counters.

PRINCIPLES OF OPERATION

digital control

Five digital inputs and the CLK input control the TLV5590. The five signals are BW, CON1, CON2, TRACKINH and TEST. All digital control inputs are latched internally on the falling edge of the CLK input. The BW input selects the cutoff frequency of the input signal third-order Butterworth switched-capacitor filter. The CON1 and CON2 inputs determine when the TLV5590 is in tracking fast, tracking slow, hold, or low-power standby mode. In test mode the CLK input is level sensitive, and in all other modes the CLK input is edge sensitive.

Table 1 lists the functions for the five control inputs.

Table 1. Control Inputs Function Table

BW		SWITCHED-CAPACITOR FILTER (– 3 dB POINT)
Low		1-kHz filter cutoff
High		2-kHz filter cutoff
CON1	**CON2**	**MODE**
Low	Low	Low-power standby (off) mode
Low	High	Fast track mode
High	Low	Hold mode
High	High	Slow track mode
TRACKINH		**RESULT**
Low		Tracking enabled
High		Tracking disabled

track inhibit

The TRACKINH input enables the counters to the peak and valley detector DACs. When enabled, the counters adjust to create a DAC output that is the same as the filtered input signal peak and valley. The counters decay at the fast or slow decay rates while the TRACKINH input is held low. The TRACKINH line should be connected to SYMCLK terminal on the TLV559X decoder.

analog-to-digital conversion

The TLV5590 employs a 2-bit ADC to convert a 4-level analog signal to digital data. The digital output is presented on EXTS0 and EXTS1 with EXTS0 being the LSB. The peak and valley DACs provide the maximum and minimum voltages (V_{ref+} and $V_{ref–}$) to the ADC. The input to the 2-bit ADC is the output of the Butterworth low-pass filter, FILOUT, as shown in the block diagram. The ADC transfer function is shown in Table 2.

Table 2. Filter Output Voltage Selection (see Note 4)

EXTS1	EXTS0	FILTER OUTPUT VOLTAGE (FILOUT)
Low	Low	FILOUT < ((peak – valley) x 50/256) + valley
High	Low	((peak – valley) x 50/256) + valley < FILOUT < ((peak – valley) x 134/256) + valley
High	High	((peak – valley) x 134/256) + valley < FILOUT < ((peak – valley) x 217/256) + valley
Low	High	FILOUT > ((peak – valley) x 217/256) + valley

NOTE 4. The constants 50/256, 134/256, and 217/256 have a ± 5% tolerance.

PRINCIPLES OF OPERATION

The thresholds for the ADC comparators are set by capacitor ratios in switched-capacitor comparators. For a 2-bit ADC, three comparators are used with thresholds set as shown in Table 3.

Table 3. Comparators and Associated Threshold Values (see Notes 4 and 5)

COMPARATOR	VALUE	UNIT
Lower threshold	((peak – valley) x 50/256) + valley	V
Middle threshold	((peak – valley) x 134/256) + valley	V
Upper threshold	((peak – valley) x 217/256) + valley	V

NOTES: 4. The constants 50/256, 134/256, and 217/256 have a ± 5% tolerance.
5. The comparator thresholds are measured with the input voltage level of the SIG terminal at 125 mV ac centered on 800 mV dc, and the input voltage at the DC OFFSET terminal is 800 mV dc.

peak and valley timing

The peak and valley attack and delay times are controlled by two 8-bit up-down counters clocked by the CLK input. The rate that the counters are clocked depends on whether the counters are in attack or decay mode. The peak counter is in attack mode when the input signal amplitude is greater than the output voltage from the peak DAC, and it is in decay mode when the input signal amplitude is less that the peak DAC output voltage. The valley counter is in attack mode when the input signal amplitude is less than the output voltage from the valley DAC, and it is in decay mode when the input signal amplitude is greater than the valley DAC output voltage.

When TRACKINH is held high, the attack and decay enable inputs to the peak and valley counters are disabled. When TRACKINH is held low, the attack and decay enable inputs to the peak and valley counters are enabled. The effect of the TRACKINH signal is exactly the same as when the device is configured in hold mode.

slow track mode attack and decay times

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 2] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is incremented or decremented by 2 on every clock cycle when the input signal amplitude is greater than or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)}] / (256 \times 40) /$ (TRACKINH duty cycle). So the peak and valley counter is decremented or incremented once every 40 clock cycles when the input signal amplitude is less than or greater than the peak and valley DAC output voltage.

When the counters receive an attack enable at the same time as a decay enable, the attack enable takes precedence. The decay counter is reset to 1 after an attack and reset to 40 following a decay.

The attack and decay times for a V_{DD} supply variation of 2.7 V to 3.3 V and a fixed clock input of 38.4 kHz are given in Table 4.

Table 4. Slow Track Mode Attack and Decay Times

DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
Attack rate (ATTR)	TRACKINH = Low	810	990	mV/ms
Decay rate (DECR)	TRACKINH = Low	10.125	12.375	mV/ms

PRINCIPLES OF OPERATION

fast track mode attack and decay times

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 4] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is incremented or decremented by a count of 4 on every clock cycle when the input signal amplitude is greater than or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 8] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is decrement or increment by 8 on every clock cycle when the input signal amplitude is less than or greater than the peak and valley DAC output voltage.

When the device is in fast track mode, the decay counter is reset to 1.

The attack and decay times for a V_{DD} supply variation of 2.7 V to 3.3 V and a fixed clock input of 38.4 kHz are given in Table 5.

Table 5. Fast Track Mode Attack and Decay Times

DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
Attack rate (ATTR)	TRACKINH = Low	1620	1980	mV/ms
Decay rate (DECR)	TRACKINH = Low	3240	3960	mV/ms

hold mode

In hold mode the peak and valley counters are disabled from counting when either attack or decay enable signals are present. There is no change to the peak and valley DAC output voltages in this mode.

When the device is in hold mode, the decay counter is reset to 1.

off mode

In off mode, the peak and valley counters are disabled from counting, and the device is set to low-power standby mode. Both peak and valley voltages float to the V_{DD} voltage as the resistor string element within the DAC structure is isolated from the ground (GND) supply to conserve power. When the off state is released, the peak and valley voltages return to the previously set values.

When the device is in off mode, the decay counter is reset to 1.

test

The TEST input allows access to internal circuitry for production testing purposes and the messaging system debug. For normal operation, TEST should be tied to ground. For the debug and test mode, the TEST input should be held high. The various operating modes are described in the following sections.

PRINCIPLES OF OPERATION

test mode 0 – peak and valley DACs and logic testing

Test mode 0 can be used for production testing, and it allows complete testing of the peak and valley DAC counters, decay counters, and the peak and valley DACs. The peak and valley DAC voltage outputs are accessible on the EXTS1 and EXTS0 terminals, respectively, and the decay rate-counter outputs are accessible on the SIG terminal. The DAC counters are controlled by the various digital inputs. The BW input controls the counter reset, and the TRACKINH input controls the peak and valley DAC counters up and down control, and multiplexes the decay rate-counter outputs onto the SIG terminal. The DC OFFSET input selects the counters fast and slow modes of operation. The counters are enabled and are clocked on each rising edge of the CLK input. Table 6 contains a terminal function summary of this test mode.

Table 6. Test Mode 0 Selection

TEST = HIGH, CON1 = LOW, CON2 = LOW		
TEST INPUTS		
TERMINAL	**INPUT**	**RESULT / MODE**
BW	Low	Logic enabled
	High	Logic reset
TRACKINH	Low	Peak and valley counters count down. Valley decay counter output on SIG terminal.
	High	Peak and valley counters count up. Peak decay counter output on SIG terminal.
DC OFFSET	Low	Device taken from fast track mode to test mode 0: a) Peak counter counts in slow track mode b) Valley counter counts in fast track mode
		Device taken from slow track mode to test mode 0, and the peak and valley counters count in slow track mode.
	High	Device taken from fast mode to test mode 0: a) Peak counter counts in fast track mode b) Valley counter counts in slow track mode
		Device taken from slow track mode to test mode 0, and the peak and valley counters count in fast track mode.
TEST OUTPUTS		
TERMINAL	**CONDITIONS**	**RESULT / MODE**
EXTS1		Peak DAC voltage
EXTS0		Valley DAC voltage
SIG†	TRACKINH = Low	Valley decay counter output
	TRACKINH = High	Peak decay counter output

† This function is valid when transitioning from slow track mode to the test mode 0. In fast track mode, the DC OFFSET terminal function is inverted for the valley counter only.

PRINCIPLES OF OPERATION

test mode 1 – switched-capacitor filter test

Test mode 1 places the output of the switched-capacitor low-pass filter directly on EXTS1. Note that the filter output is not capable of driving an external load and, therefore, must be buffered externally at the EXTS1 terminal of the TLV5590. The BW input selects the filter cutoff frequency. The peak and valley DAC counters, the decay counters, and the 2-bit ADC are all disabled during this test mode. Table 7 contains a terminal function summary of this test mode.

Table 7. Test Mode 1 Selection

TEST = HIGH, CON1 = LOW, CON2 = HIGH		
TEST INPUT		
TERMINAL	**INPUT**	**RESULT/MODE**
BW	Low	1-kHz cutoff frequency (–3 dB)
	High	2-kHz cutoff frequency (–3 dB)
TEST OUTPUT		
TERMINAL	**OUTPUT SIGNAL**	
EXTS1	Switched-capacitor filter output (unbuffered)†	

† The filter output must be buffered externally for testing.

test mode 2 – peak and valley DAC output test

Test mode 2 allows direct access to the peak and valley comparators and can be used for the messaging system debug. The peak and valley comparator outputs are accessible on the EXTS0 and EXTS1 terminals, respectively. The peak and valley counters are held at a constant value using the hold mode. Table 8 contains a terminal function summary of this test mode.

Table 8. Test Mode 2 Selection

TEST = HIGH, CON1 = HIGH, CON2 = LOW	
TEST OUTPUTS	
TERMINAL	**OUTPUT SIGNAL**
EXTS1	Peak DAC voltage
EXTS2	Valley DAC voltage

PRINCIPLES OF OPERATION

test mode 3 – comparator threshold test

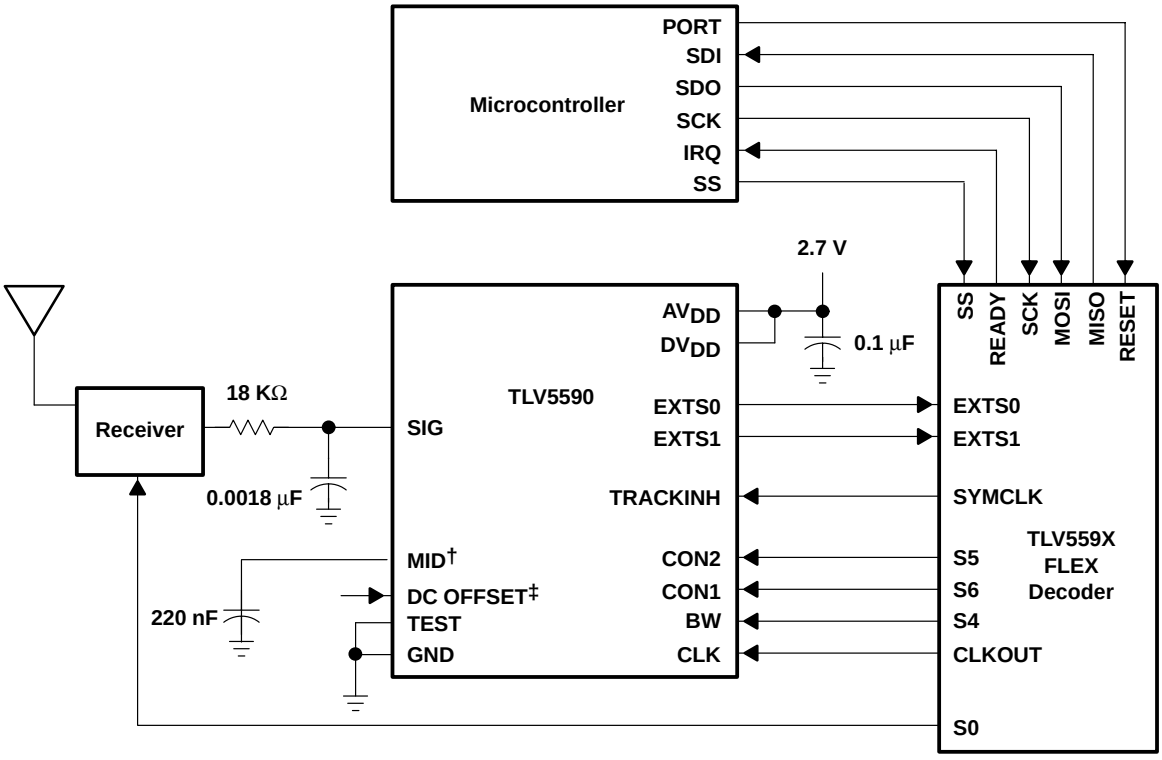
Test mode 3 allows a dc input voltage to be applied to force the peak and valley DAC voltages to settle independently at their nominal output voltages, including any effects of the filter dc offsets, gain errors, etc. The input signal can then be set at the comparator switching thresholds and the correct outputs should be decoded. The normal outputs of the ADC are present on EXTS0 and EXTS1. The BW and TRACKINH inputs override the peak and valley DAC counter disables. The switched-capacitor filter is forced into a 1-kHz cutoff mode. Table 9 contains a terminal function summary of this test mode.

Table 9. Test Mode 3 Selection

TEST = HIGH, CON1 = HIGH, CON2 = HIGH		
TEST INPUTS		
TERMINAL	INPUT	RESULT
BW	Low	Peak DAC counter normal operation
	High	Peak DAC counter disabled
TRACKINH	Low	Valley DAC counter normal operation
	High	Valley DAC counter disabled

APPLICATION INFORMATION

The TLV5590 converter is optimized for messaging applications. The TLV5590 optimizes the filtering and conversion resolution to meet the specific requirements of FLEX messaging devices. The combination of the TLV5590 converter and TLV559X decoder reduces overall system cost by allowing a low-cost microcontroller to be used in the messaging system. Figure 5 shows the basic connections between system elements.



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

Figure 5. TLV5590 Application Schematic

At least one bit of warm-up time in fast track mode followed by five bits of warm-up time in slow track mode is necessary before valid data can be present. Hold mode is used during a data transfer, and fast track mode is used for warm-up. Slow track mode is used for tracking during the synchronization portion of the data.

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Appendix B

Timing Diagrams

This appendix presents SPI interface timing, start-up timing, and reset timing for the TLV5594VF FLEX decoder.

Topic **Page**

B.1 SPI Timing

Figure B–1 and Table B–1 describe the timing specifications of the SPI interface.

Figure B–1. SPI Interface Timing Specifications

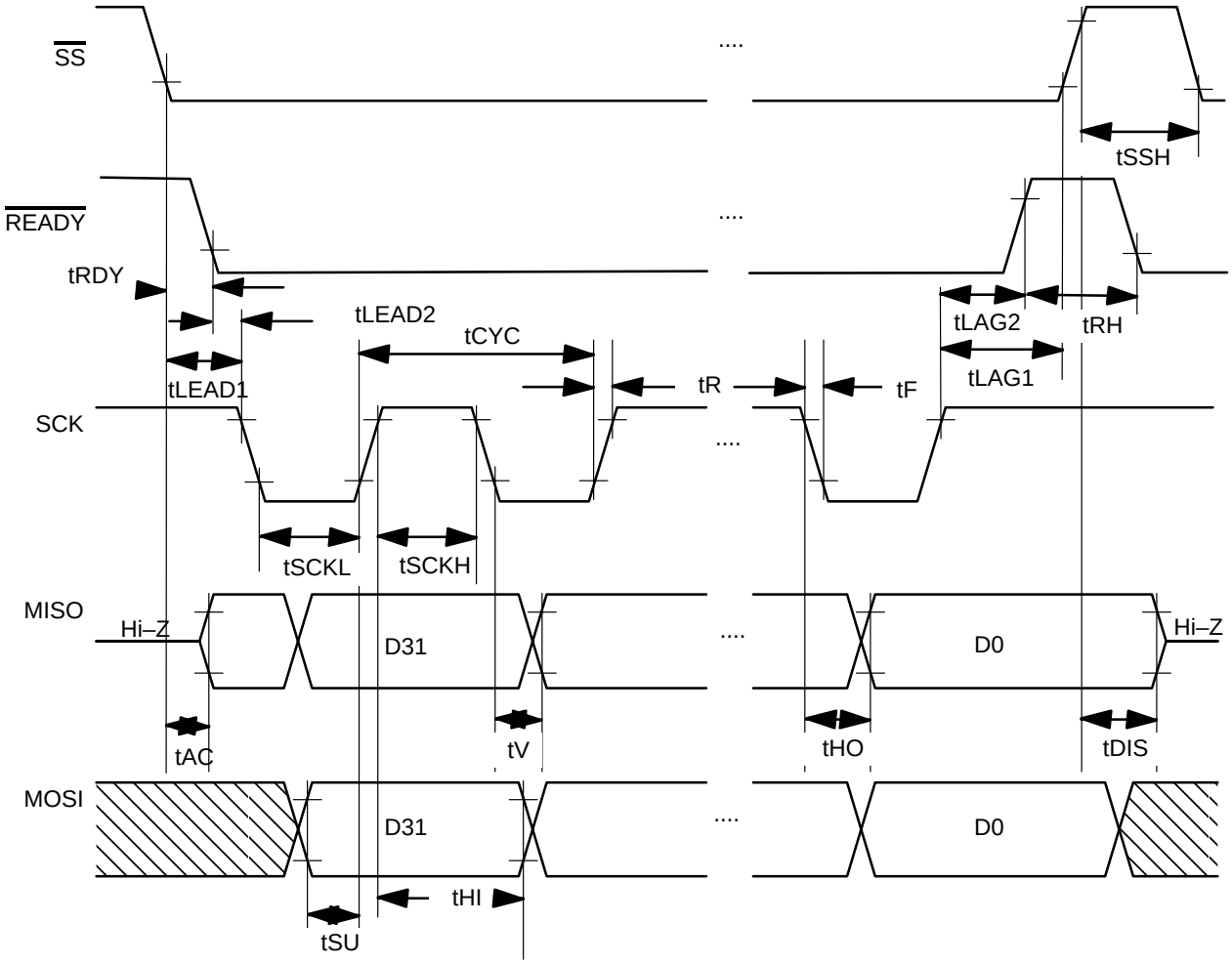


Table B–1.SPI Timing

Characteristic	Conditions	Symbol	Min†	Max†	Unit
Operating Frequency		f_{OP}	dc	1	MHz
Cycle Time		t_{CYC}	1000		ns
Select Lead Time		t_{LEAD1}	200		ns
Deselect Lag Time		t_{LAG1}	200		ns
Select-to-Ready Time	Previous packet did not program an address word ‡ CL=50 pf	t_{RDY}		80	µs
Select-to-Ready Time	Previous packet programmed an address word ‡ CL=50 pf	t_{RDY}		420	µs
Ready High Time		t_{RH}	50		µs
Ready Lead Time		t_{LEAD2}	200		ns
Not Ready Lag Time	CL=50 pf	t_{LAG2}		200	ns
MOSI Data Setup Time		t_{SU}	200		ns
MOSI Data Hold Time		t_{HI}	200		ns
MISO Access Time	CL=50 pf	t_{AC}	0	200	ns
MISO Disable Time		t_{DIS}		300	ns
MISO Data Valid Time	CL=50 pf	t_V		200	ns
MISO Data Hold Time		t_{HO}	0		ns
$\overline{SS}$ High Time		t_{SSH}	200		ns
SCK High Time		t_{SCKH}	300		ns
SCK Low Time		t_{SCKL}	300		ns
SCK Rise Time	20% to 70% V_{DD}	t_R		1	µs
SCK Fall Time	20% to 70% V_{DD}	t_F		1	µs

† The specifications given in this document indicate the minimum performance level of all FLEX decoders regardless of manufacturer. Individual manufacturers may have better performance than indicated.

‡ When the host reprograms an address word with a Host-to-FLEX decoder packet ID > 127 (decimal), there may be an added delay before the FLEX decoder is ready for another packet.

B.2 Startup Timing

Figure B–2 and Table B–2 describe the timing specifications of the FLEX decoder when power is applied.

Figure B–2. Startup Timing

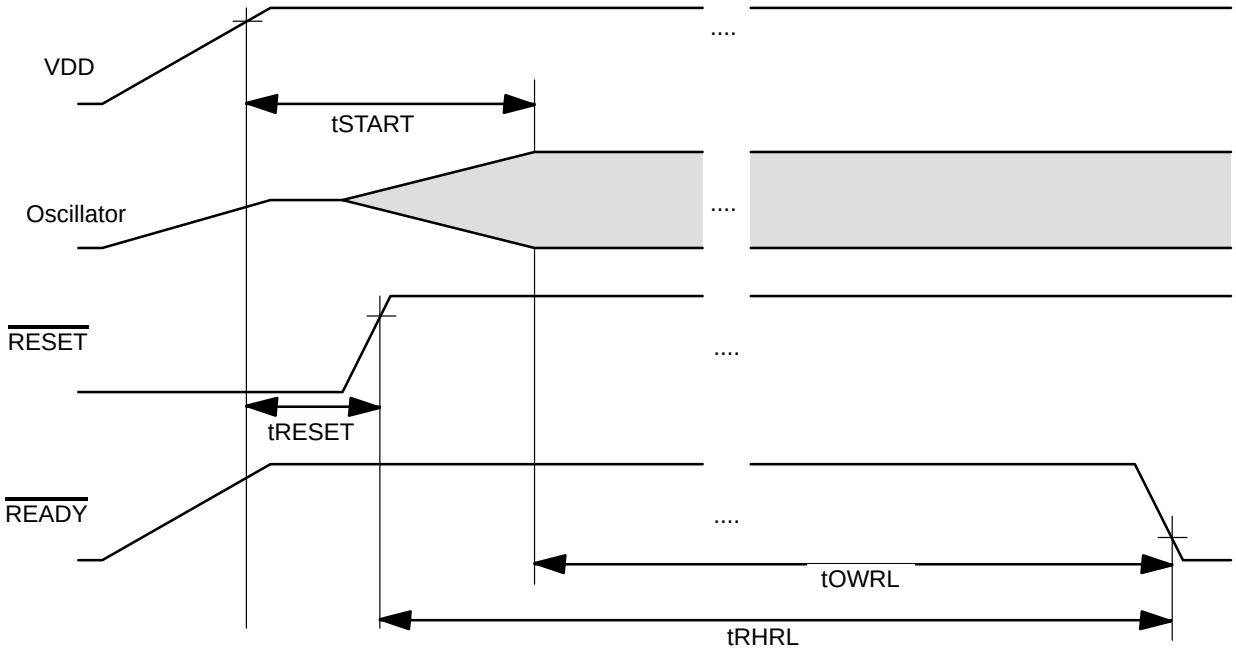


Table B–2. Startup Timing (V_{DD} = 1.8 V to 3.3 V, T_A = 0° C to 70° C)

Characteristic	Conditions	Symbol	Min†	Max†	Unit
Oscillator Startup Time		t_{START}		5	sec
$\overline{\text{RESET}}$ Hold Time		t_{RESET}	200		ns
$\overline{\text{RESET}}$ High to $\overline{\text{READY}}$ Low		t_{RHRL}	76 800	76 800	T‡
Oscillator Warmed Up to $\overline{\text{READY}}$ Low	CL=50 pf	t_{OWRL}	–	1	sec

† The specifications given in this document indicate the minimum performance level of all manufacturers of the FLEX decoder. Individual manufacturers may have better performance than indicated.

‡ T is one period of the 76.8 kHz clock source. Note that from power-up, the oscillator start-up time can impact the availability and period of clock strobes. This can affect the actual $\overline{\text{RESET}}$ high to $\overline{\text{READY}}$ low timing.

B.3 Reset Timing

Figure B–3 and Table B–3 describe the timing specifications of the FLEX decoder when it is reset.

Figure B–3. Reset Timing

Table B–3. Reset Timing (V_{DD} = 1.8 V to 3.3 V, T_A = 0° C to 70° C)

Characteristic	Conditions	Symbol	Min†	Max†	Unit
$\overline{\text{RESET}}$ Pulse Width		t_{RL}	200	–	ns
$\overline{\text{RESET}}$ Low to $\overline{\text{READY}}$ High		t_{RLRH}	–	200	ns
$\overline{\text{RESET}}$ High to $\overline{\text{READY}}$ Low	Stable 76.8 kHz clock source	t_{RHRL}	–	1	sec

† The specifications given in this document indicate the minimum performance level of all manufacturers of the FLEX decoder. Individual manufacturers may have better performance than indicated.

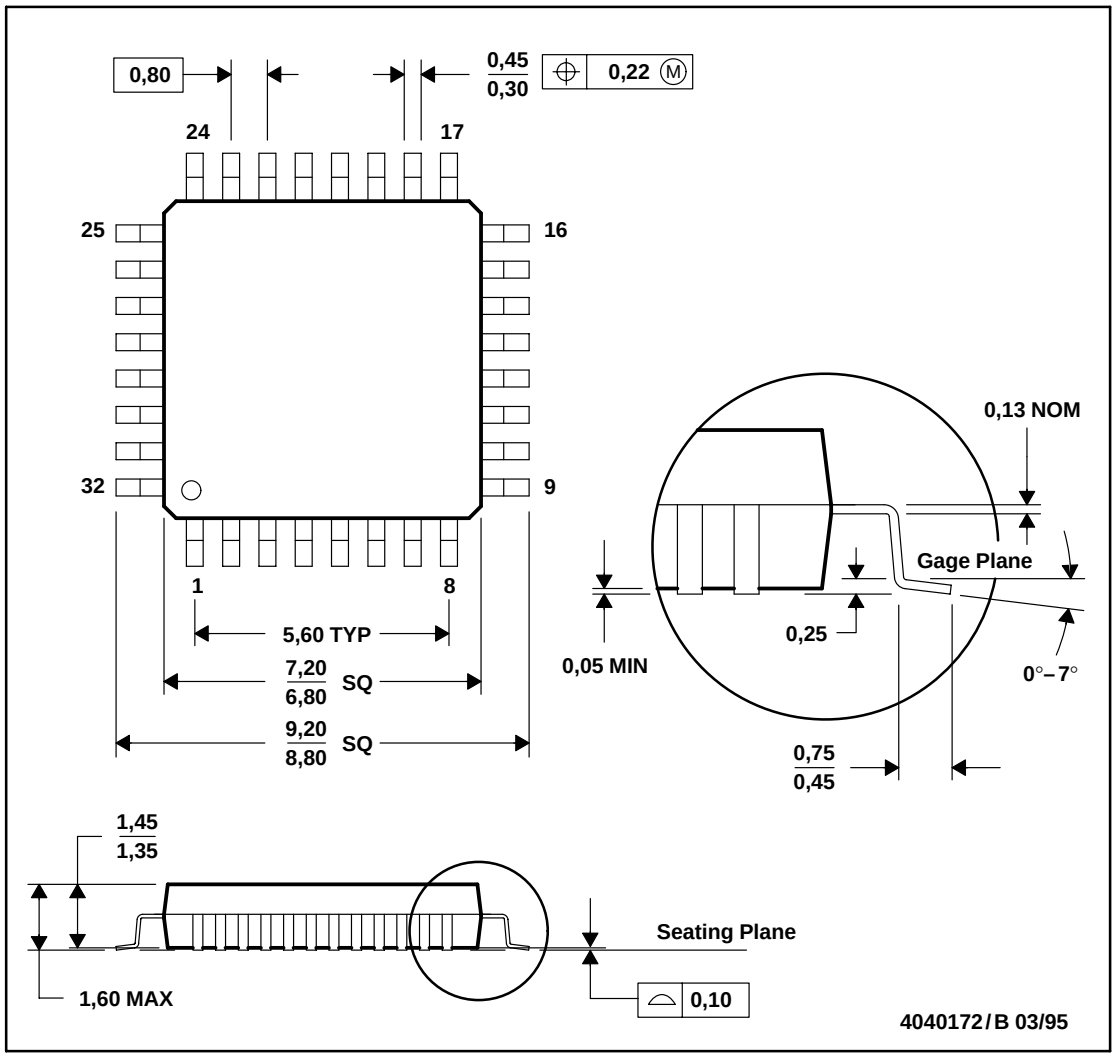
Appendix C

Mechanical Data

This appendix presents the mechanical data for the TLV5594VF FLEX decoder.

Plastic Quad Flatpack

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136