

*TMS320 DSP
DESIGNER'S NOTEBOOK*

Supporting External DMA Activity to Internal RAM for TMS320C5x Devices With the PZ Package

APPLICATION BRIEF: SPRA237

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Abstract

This document discusses how to use the DMA capability of TMS320C5x devices with the thin-quad-flat package.

The problem is that when moving to the small outline and footprint of the thin-quad-flat package (TQFP) for TMS320C5x devices, some functionality is removed to reduce pin count. This move from the 132-pin quad-flat package (PQ package) to the 100-pin TQFP (PZ package) removes two functional pins: interrupt acknowledge (IACK) and instruction acquisition (IAQ). Aside from its traditional function, the IAQ pin is also used to acknowledge the bus request (BR) signal for external DMA access to the single access RAM.



Design Problem

When moving to the small outline and footprint of the thin-quad-flat package (TQFP) for TMS320C5x devices, some functionality is removed to reduce pin count. This move from the 132-pin quad-flat package (PQ package) to the 100-pin TQFP (PZ package) removes two functional pins: interrupt acknowledge (IACK) and instruction acquisition (IAQ). Aside from its traditional function, the IAQ pin is also used to acknowledge the bus request (BR) signal for external DMA access to the single access RAM.

How do I use the DMA capability with the thin-quad-flat package?

Solution

All 'C5x devices with single-access RAM ('C50, 'C51, and 'C53) offer a unique feature allowing another processor to read and write to its internal memory. The TMS320C51 and TMS320C53 are offered in a 132-pin quad-flat package (PQ package) and a 100-pin TQFP (PZ package) for systems with size constraints. To use the DMA capability with the TQFP package, the following should be considered.

To initiate a read or write operation to the 'C5x single-access RAM, the Host or Master processor requests a hold state on the DSP's external bus. When acknowledged with HOLDA, the Host can then request access to the internal bus by lowering the bus request line (BR). Unlike the hold mode, which allows the existing operation to complete and allows the CPU operation to continue (if status bit HM = 0), a BR-requested DMA always freezes the operation currently being executed by the CPU. Because of this, the time required to grant the access to the internal single-access RAM is deterministic and does not vary. Access to the internal bus is always granted on the third cycle after the bus request signal is received. Therefore, the IAQ signal is not an essential signal for external DMA activity to the single-access RAM. The host is required to wait two 'C5x cycles after driving the bus request line low. The host can then safely assume that access to the internal bus has been granted and begin the DMA operation.

All other signals and timing conditions required for DMA access are the same as those listed in the TMS320C5x Users Guide.