# *Designing an Audioprocessor for Automobiles with the TMS320C50 DSP*

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TEXAS INSTRUMENTS

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## Abstract

This application report describes an audioprocessor designed to create an artificial sense of space that improves the listening quality of music in an automobile. This is achieved by constructing four different signals from two stereo channels. The signals are delayed in a time domain that will add echo normally missing in a car.

It is not the purpose of this project to restore the original sense of space but to create a new sense of space independent of the limitations of the actual room.

The equipment described in this report is designed mainly for research and development work using the Texas Instruments (TI™) TMS320C50 digital signal processor (DSP). This can be seen in its I/O functions and adapters designed to expand the system. However, it is also usable in practical applications.

The power supply is 12 V, from which 5 V is reserved for components. The equipment can be switched on by an external control signal from the control adapter of the amplifier in the car radio.

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# Introduction

The automobile offers an interesting environment to study digital audio signal processing. The acoustical environment of the car provides a good base for the qualified audio. The car designed with soft interior materials has weak reflections and short echoing time. This minimizes the impact of the listening room for audio processing.

It is possible to reach a broader bandwidth in the interior of the car than a normal living room. Since the interior of a car is considerably smaller and more enclosed, the acoustics amplify the lower frequencies of the sound about 12dB/octave after certain limits (such as 50 Hz).

Using the correct measurements and elements, it is possible to reconstruct a loudspeaker with a linear bass response until 10 Hz. Passengers in a car are usually sitting near the loudspeakers. The placement and distance of the listeners coupled with low reflections make it possible to get flat frequency response even in high frequencies.

The short echoing time mentioned above also causes negative features. Music not recorded in natural space normally doesn't contain a versatile image of space so the music may sound monotonic and colorless. Using digital signal processing to add missing echoes and create a sense of stereo feeling can change the situation. This is more successful in the car compared to other environments because the listeners are not moving. In other environments, echoes, reflections, and the movement of listeners can easily spoil the sense of artificial space made for sound.

## Technical Description

The digital audio processing and user interface control equipment was designed using the Texas Instruments TMS320C50 digital signal processor. For I/O functions there is crystal high quality AD/DA module with two 16-bit A/D-converters, one12-bit A/D-converter and four 16-bit DIA converters. There is also two 8-bit read/write ports for keyboard, display, and other possible interfaces. The signal-to-noise ratio is perhaps not suitable for the most demanding HIFI quality, but in car use it is enough, due to the heavy background noise.

There is 128 Kbytes static 20ns memory for slice buffers and changing data. The memory is battery protected and connected to a power supply even if the equipment is switched off. The memory contains the control data of the equipment. For program memory, 32 Kbytes EPROM is decoded in the global memory space of the processor.

It is possible to connect the equipment to a normal PC or other equipment by a UART-serial port. In the developing phase of the software it is possible to change the program without opening the equipment and updating the EPROM.

## Function

Discovering the various effects on sound is easy but evaluating these effects is difficult prior to listening for an extended period of time. That's why the first software version functions were easy to use and control but generated big differences in the space image of sound.

Normal stereo recordings have two different channels that differ slightly from each other. In a natural recording, the differences come from time and volume of musical instruments between different channels. In an artificially mixed recording, the difference is mainly in volume.

The equipment calculates the sum of signals in the different channels, that is, mono-sound, and then the difference of the signals that form the stereo image. Both signals are calculated as separate echoes. This can be controlled in the delay, input amplitude, and feedback amplitude. In the feedback loop, a low pass filter is used so high frequency sounds will not echo too much and sound metallic.

Echoed signals form each channel signal as required. Each channel can select repetition delay, mono and difference-signal ratio of mixing.

As the ear notices the delayed reflection of the sound, it makes sense of space. The sense will improve if the sound comes from different directions. The size of the space depends on the amount of the delay. The massiveness of the space depends on the difference in volume of the original signal and the echo. The ear determines the quality and content of the sound, based on the sound signal first. Therefore, the sound signal can be synchronized by the aid of echo so that the first sound you hear comes from the best source.

The sound that is sensed first should come from the front and back with enough sound delay that it makes sense of space. The ratio of mono and difference-signal and different types of echoing effects contribute to the largeness of the sound.

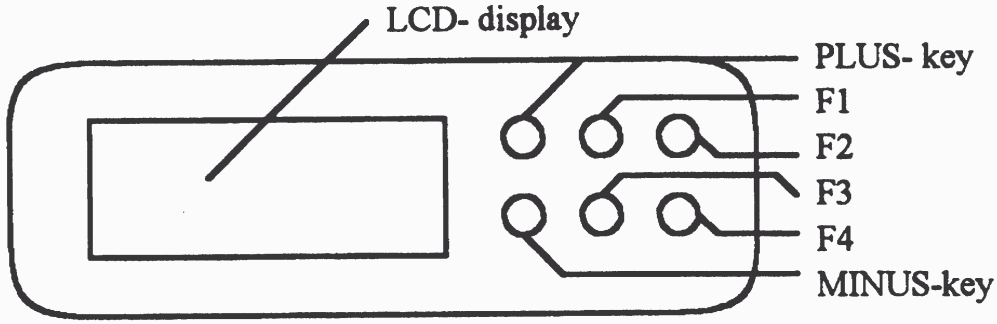
If we look at the mono signal delay in different loudspeakers, the sound seems to come from an indefinable place in the space generated by the delays. A successful stereo recording gets the sources of the sound to locate in different directions and places in the space. By the ratio of mono and difference signals it can be more clearly determined in the place of the sound source. The location of the sound source can be more clearly determined by the ratio of the mono and difference signals.

The sign of the difference signal determines which of the original channels the repetition is like. As the volume of the difference signal becomes equal to the mono signal, the situation is the same as the original channels.

# Interface

The interface of the equipment consists of a 6-key keyboard with press keys and a 16 x 2-character display module. Four gray keys are function keys and the others are (+/-) keys in red and black. The functions are shown in Figure 1.

*Figure 1. Location of the Display and Keys in Front Panel*




# Main Menus

## Setting Menu

The display shows abbreviations representing the first four settings of space. Each setting is selected by a respective key. The valid control parameters can be put into the selected memory location by pressing the function key for at least two seconds. After that, the menu changes to a storing menu.

## General Control Menu

The controls of the general control menu are main volume, input volume and adjustments of echo.

Each function is selected by respective function key. For example, select the Channel Menu by pressing the minus key (–). Select the Setting Menu by pressing the plus key (+).

## Channel Menu

The channel menu contains controls for each separate channel. Each of the four channels has a function key. Oress the (+) key to select the General Control Menu.

# Sub Menus

## Setting Menu -> Restoring Menu

In the Restoring menu, the alphabet is displayed along with special keys. Up to seven characters per name are allowed for control settings. By pressing the (+) key or (-) key, the next or the previous four-character group displays. Select a character from the group by pressing the respective function key. The group of four keys are space, backspace, plus (+), and minus (-). Pressing the (+) key restores the settings in the memory location. Pressing the (-) key will undo the restoring operation.

## General Control Menu -> Setting Echo Controls

In the Echo Menu you can adjust the mono, delays of channel difference, echo and feedback ratio. Each control is selected by its own key.

## Channel Menu -> Channel Control

The Channel Control menu consists of three parameters: volume of channel, delay, and deepness of stereo.

# Controls

When adjusting parameters, the name of the control is visible in the top row of the display. The bottom row displays the present value and the new value. The value will change 0 - 100% of the expected delays, which are 0 m - 100 m. The value is incremented or decremented by (+/-) key by one step. The top key accepts the adjustment and the bottom key will save the present value. The parameters change during the adjustment and the influence can be heard immediately. The value is increased or decreased in increments of 10 by pressing the (+/-) key.

## Hardware

The hardware of the equipment consists of the following ten main units:

- Processor unit
- Converter unit
- Analog unit
- I/O-interface
- Memory interface
- UART-serial interface
- Power supply
- Serial interface between the processor and converter
- LCD display
- Keyboard

Each unit is explained as follows.

## Processor Unit

The processor unit consists of the Texas Instruments TMS320C50 DSP and its peripheral components.

Unused interrupt and reset lines are connected to a voltage source by resistors. External test points make it possible to add the source of interrupt afterward.

The clock signal is made by an external crystal oscillator. A Schmitt-trigger inverter resets the processor when power is switched on. The inverter keeps the reset signal low long enough for the power lines to stabilize. The same circuit makes it possible to reset the processor via serial port.

## Converter Unit

The converter unit contains a Crystal CS4225 AD/DA converter module that resets the circuit and external components for the internal converter crystal oscillator. The reset circuit of the converter consists of a Schmitt-trigger inverter, capacitor, and resistor. The components of the oscillator are a crystal and load capacitor for the crystal.

## Analog Unit

The analog unit has analog input and output components for the converter and filters for internal reference voltages of the converter. The converter has tree input lines that can be selected by the software. All inputs are connected making it possible to use several audio sources.

The equipment is not provided with line buffers. In practice, close-connection active filter units acted as line buffers. If the equipment is connected to a normal amplifier, a separate line buffer card is recommended.

## I/O Interface

The I/O interface has an I/O decoder circuit, two 8-bit output ports, and two 8-bit input ports. Two extra chipselect lines in the I/O decoder unit are also in use. That use is explained in the serial unit between the processor and converter units. The I/O decoder circuit consists of one 74AC138 decoder.

Write ports are 74HC374 D-FFs and read ports are 74HC73 D latches. To enable, the decoder requires signals IS and STRB to be low. This means that an I/O cycle occurs and the external parallel access is active. In the read ports, the chip select line is connected direct to the OE. The LE of the circuit is firmly activated. In the write ports the chip select line is connected to the clock line of the flip-flops. The outputs of the flip-flops are enabled at all times.

## Memory Interface

The memory interface consists of a memory decoder and memory. The decoder is one 74AC138 circuit. To enable the decoder, the DS signal must be low and the processor must be switched on. It is connected to address bus address line A15, so the decoder divides the 64 Kbytes memory space by two and the BR signal differentiates the local and global data memory areas. One of the address lines is not used and is connected to signal ground.

There are four RAM circuits 32k x 8 bits with an access time of 20 ns. They form a two 32kWord x 16 bit memory area. In the global memory area there is one 32k x 8-bit EPROM connected to eight lower bits of data bus. The EPROM stores the program code and static settings. Boot load operation is accomplished from this circuit.

Signals OC and WR of the SRAM circuit are connected directly to the processor so that WR is assigned to memory circuit WR and RD to memory circuit OC.

The chip select lines of the memory are connected to the respective signals of the memory decoder. EPROM is connected in the same manner. Memory interface has its own battery-protected supply voltage that does not switch off with the equipment.

The decoder and EPROM circuits are also connected to the same voltage so there cannot be input voltages to a powerless circuit. Additionally, it does not make any difference because the currents are small compared to the capacity of a car accumulator, and the battery-protected periods are not long. There are two 1.5 V batteries.

## UART-Serial Interface

The control and read of the serial interface is made by software with control bits. While the serial interface is in use, communication with converter module must be stopped. The transmission of the serial interface is controlled separately by the XF output and is read by the BIO-input bit.

The serial buffer consists of two transistors, some resistors, and one capacitor. The negative voltage is made from a transmit signal sent from the opposite side.

## Power Supply

The power supply consists of two 5 V regulators. One produces the digital supply voltage and the other produces the analog supply voltage. The digital power supply voltage is divided in two parts: voltage for memory components and voltage for other digital components.

There is power at the digital regulator while power is connected to the equipment. The voltage for memory interface is fed from the regulator via a diode. If the power to the equipment is not switched on, the voltage for memory interface is fed from the protection battery.

The real power can be switched on from the control voltage input. It is connected via a Zener diode to an NPN transistor that controls two PNP switching transistors. These transistors switch voltage on the main voltage line of the digital part and analog voltage to the regulator. A coil with a ferrite core separates the digital and analog grounds from each other.

The electrolytic capacitors in power supplies have low impedance and noise-filtering capacitors that have a power coefficient. For the high frequency filtering there are ceramic (NPO) capacitors that have low power coefficient. Each digital component has a 100nF noise-filtering capacitor.

Equipment ground is isolated from the power supply ground by two diodes in parallel conducting in different directions. This is a simple way to form a *floating ground* that doesn't make earth loops into signal wires between different equipment. The ground of the equipment can float freely about +/- 0.6 V from the ground of the power supply. The amount of noise isolation is based on independence from the power supply voltage. It has been found that the circuit attenuates high disturbances from the charger in the equipment installed into cars.

## Processor and Converter Serial Interface

Both processor serial ports communicate with the converter. Another port is reserved for transmission of audio data in both directions and another for transmission of control words, setting data, and reading of state bits of the converter.

Used as a control port, the serial port of the processor is configured for an 8 bit transmission with an external clock and internal frame-synchronizing pulses. Transmission is made in burst mode, transmitting a series of succeeding bytes.

The control port of the converter is synchronous and the transmission takes place on the rising edge of the clock signal. The CS signal of the port must settle low before the first rising edge of the data clock to indicate the beginning of the transmission. CS must stay low at least during the time of the transmission. The data is transmitted via CDIN and CDOUT lines. CDIN is connected to TDX of the processor and CDOUT to TDR of the processor.

The clock signal is made from CLKOUT1 signal of the processor by division. The division rate may be selected by jumpers 64 (312.5 kHz) or 256 (78.1 kHz). The clock signal is fed straight to input TCLKX of the serial port and is inverted to CCLK input of the converter.

The CS signal is made by a D flip-flop with asynchronous RESET and SET. SET input of the D flip-flop is connected to one of the unused chip select lines of the I/O decoder. The write operation to that address location sets the D flip-flop.

The TFSX frame-synchronizing pulse of the processor serial ports is fed inverted to the clock input of the D flip-flop. The D input and RESET input of the D flip-flop are connected to the high state. So the falling edge of the frame-synchronizing pulse causes the D flip-flop to set. The inverted output (/Q) of the flip-flop is connected to the CS input of converter. CS is thus activated automatically as the first byte of the command is leaving and can be deactivated by software after the last byte has left.

The information left by the data is acknowledged by the receiving interrupt as TCLKX, TCLKR, TFSX, and TFSR are connected together. So the transmitting and receiving clocks of the transmitting port are the same and the transmitting frame-synchronizing pulse synchronizes and starts the receiving. That also enables the reading of data from the converter.

The reading operation happens by first confirming a partly write operation. This is done by writing the circuit address and then the address of the register that will be read. After that, CS must be set to the high state during a one-clock cycle.

Next, the address of the circuit is written as a read-bit set. Reading data is transmitted only after the address has moved along the CDOUT line. If we keep the receiving frame enabled, we can register the amount of bytes transmitted.

After the last byte it is done writing to the I/O port that deactivates the CS-signal. For a successful reading operation, the data transmission between the processor and converter must be stopped (that is why we get a fast enough interrupt time for CS-deactivating) or we must use a slower clocking frequency to control the circuit.

Another serial port is used for the transmission of audio data. The port is in 16 bit mode, external clocking, and external frame synchronizing. The transmission is made in continuous mode and a synchronizing pulse is made to start the transmission. The DR signal in the serial port of the processor is connected to SDOUT1 of the converter and to SDIN1 of the DX converter. SCLK of the converter is connected to the CLKX and CLKR inputs of the processor.

The converter is configured to produce a transmission clock. The data of the different channels go in succession so that every bit is in use. SDOUT1 deliver the data of the converters so that it goes in order of channel1, then channel2, and last, the data of the 12-bit converter. This is so that it runs two times in succession in 16-bit format, 4 lower bits zero.

The transmission is synchronized by the LRCK signal. This frequency is a sampling frequency of converters that is changed to 1 every time a transmission of channel1 starts. The write is synchronized by the same clock-signal so that the data of the DA converter1 is transmitted first.

The generation of the regular frame-synchronizing pulse for the serial port of the processor is complicated. This is why it is reasonable to use continuous mode without frame-synchronizing. The D flip-flop with an asynchronous set and reset generates a synchronization pulse of a starting point. The set input of the flip-flop is connected to the last free I/O writing address. Writing to that address can be used to set the flip-flop.

The D input of the flip-flop is connected to low state and reset to high state. LRSCK of the converter is connected to the clock input of the flip-flop. The output of the flip-flop is connected to FSR and FSX frame-synchronizing of the processor. So after setting the flip-flop, the next rising edge of LRCK causes the falling edge of the frame-synchronizing signals to start the transmission.

If the converter is working while the synchronization flip-flop is set, there is a minor possibility that the data transmission will not start because the synchronization pulse is too short. So it will happen if the setting happens just before the rising edge of LRCK. This can be avoided if LRCK of the converter is set by the software to input before setting the synchronizing flip-flop.

In that case LRCK is in three-state and the pull-up resistor determines that the state is high. After the synchronization flip-flop is set, the transmission can begin by setting the LRCK signal of converter as an output.

To keep the channels in order, the LRCK signal is connected to the interrupt line 4 as inverted. So we get an external interrupt in the beginning of every new frame of transmission. This makes it possible, for example, that the user interface software for the temporary processor time reservations (which means that all operations needed by samples will not have time to calculate during one sampling time) does not mix up the order of the AD-channels so it produces one sample to repeat the same as the previous one and that is almost outside of the hearing capacity.

## LCD Display

The LCD display is a model LMO93XMLN made by Hitachi with a 16 x 2-character module equipped by a background LED light. The display is connected to output ports so that the 8 bit data bus of the module reserves one port and ENABLE and RS (instruction/data) reserves two bits from another port. ENABLE must normally be kept in the low state. It may be only written to the display.

Data bits are written to a data port and RS-bit settings to another port. Next, the ENABLE bit is brought to the high state and back to the low state so that the data will move into the module. The software handles the write timing.

The module can also be connected via one 8 bit port. To write one character requires two writing cycles, but another output port is now totally free for another use.

## Keyboard

The keyboard has six closing keys. Every key is connected to its own bit in the input port. Every bit is connected to the pull-up resistor. Pressing a key produces a pull-down of a bit. The software eliminates switching oscillation.

## Software Function

In the beginning, the software sets up the processor, converter, buffers, and variables and starts the transmission. It includes a listing of the program in pseudo language and assembly language. The details of the program are explained in this document.

The reading and writing of the converter is in a signed 16 bit format. The receiving, transmitting, and processing of the data are performed in the interrupt subprograms. In the main program, the user interface is running in time left. The processing of the signal is made in the interrupt program activated by the external interrupt. It is connected to the data-synchronizing clock of the converter (see transmission of audio data) and is always activated at the beginning of every new conversion cycle. The software double buffers data acquisition and write so that transmission works faultlessly even if the procession time of the different channels is different.

To minimize the time consumed by interrupt programs, both data read and data write happen in the frame of receiving. For that reason it should be written to the DXR register immediately after the start of the transmission so that transmission is not stopped. Write operation happens one channel lagging, which means that in the interrupt of the first channel it will be given the data of the second channel and so on. The data of the first channel is then one sample late, which has no meaning in practice.

It is possible for software to compensate for the error if desired because the receiving programs of different channels are slightly different and the determination of runtime operations is quite slow. There are four different interrupt programs. The address of the next in turn is changed during the run to the address of the interrupt vector. That takes only two clock cycles that are fast compared to comparison operation.

The interrupt-program-processing signal first sets up the next receiving interrupt then saves the registers that will change. The reason is that internal interrupts must be enabled for successful data transmission. Afterward, they are taken care of by double buffered data transmission. Only after that it is possible to enable new interrupts.

In the first operation it calculates the mono signal, channel difference, and the echoes of both signals. The results are added to a main circular buffer. Next, the calculated signals of each channel are stored as temporary variables. After calculating, the programmable timer that the user interface will use for synchronizing its own functions is updated. The last original contents are returned from the interrupt program with the changed registers. After that the control is moved to the main program, it will work as a user interface.

The user interface is a loop containing code to read the keyboard, write to the LCD and converter module, and call the active menu routine. Each function is enabled by a certain time. The most common functions, such as writing to the display buffer, adjustment of parameters, giving commands for converter, etc., are separate subprograms. The user interface calculates the lowest level parameters for effects from adjustment parameters. It also restores the parameters into memory.

Each parameter has its own subroutine that does everything needed for adjusting. These subroutines are called by addresses in the adjust menu. The user interface only needs about 1% of the processor time to work fast enough. If necessary, so that the write operation of commands to the converter doesn't disturb the sound, there must be free processor time of about 10%.

## Calculation of Mono Signal and Channel-Difference Signal

The mono signal is made by calculating the sum of the channels and multiplying the result by the input volume. The channel-difference signal is made by multiplying the difference of the channels by input volume.

## Echo Effects

Echo effects take a value from the circular buffer pointed to by the echo's delay pointer, multiplies it by feedback volume and then to the input of an IIR Butterworth low-pass filter. The input signal is summed to the feedback signal and restored to the first value of the circular buffer.

## Calculation of Channel Signals

A value for the mono signal and the channel-difference signal is taken from a location in the circular buffer, pointed to by the repetition pointer of a channel. Both are multiplied by their own volume value and then summed and restored into the output buffer of the channel.

## Processing Parameters of Echoes

| | |
|---|---|
| **VOL** | Input volume |
| **MECHOP** | Address of the mono signal echo in the circular buffer |
| **DECHOP** | Address of the channel-difference signal echo in the circular buffer |
| **MECHOFB** | Volume of feedback of mono signal |
| **DECHOFB** | Volume of feedback of channel-difference signal |

## Processing Parameters of Channel

| | |
|---|---|
| **MVOL** | Volume of mono signal in calculating channel signal |
| **DVOL** | Volume of difference signal in calculating channel signal |
| **KAN** | Address of the location to repeat in the circular buffer |
| **OUT** | Restoring location of channel signal |

## General Adjustment Parameters of the User Interface

| | |
|---|---|
| **VOLUME** | Main volume (0... 100%). Changes attenuation in output of converter. |
| **MECHO** | Delay of mono signal's echo as response distance (0. .1 00m). Determines the difference between maximum value and repeat value in the circular buffer |
| **DECHO** | Delay of difference signal's echo as response distance (0... 100m). Determines the difference between maximum value and repeat value in the circular buffer |
| **MECHOR** | Feedback percentage of mono signal's echo (0...100%). Determines volume of echo's main signal and feedback |
| **DECHOR** | Feedback percentage of difference signal's echo (0...100%). Determines volume of echo's main signal and feedback. |

## Processing Parameters of Channels in the User Interface

**CHVOL** General volume of channel. Changes attenuation in output of converter per channel. Final result is also determined by main volume.

**SDEPTH** Depth of stereo sense (-100...100). Determines volume ratios of mono signal and difference signal used in calculating channel signal.

**DELAY** Repetition delay of channel as response distance (0...100m). Determines the difference between maximum value and repeat value of channel signal in circular buffer.

In every case the different volumes are 16 bit numbers and the result is scaled so that it stays at maximum volume at the same level. For example, echo effects are sensitive to overflow with high feedback. Eliminating the overflow theoretically causes the level of quantization to go too low. It is most reasonable to leave the adjustment of volume ratios in the control phase.

## Summary

This audioprocessor design was based on the Texas Instruments TMS320C50 DSP. The audio interface was accomplished by the Crystal CS4225 audio converter module. The user interface hardware consisted of a Hitachi LM093XMLN LCD and six press-keys.

The user interface software and signal processing software was designed and implemented. The design of the circuit was based on databooks of the processor and the audio module. The interface circuits were designed with regular digital and analog components. The circuit was drawn and the prototype was designed for the PCB by PADS-software.

The pseudo C-code of the user interface software was developed and simulated using a PC. Signal processing effects were also developed and tested using the PC. Preprocessed audio data was played using two 16 bit soundcards.

The hardware was built but not tested in practice because of delays in making the PCB.

## Equipment

| | |
|---|---|
| **Processor** | Texas Instruments TM5320C50 DSP |
| **Memory** | (4) 32k x 8 bit, 20ns SRAM with battery protection<br>(1) 32k x 8 bit EPROM |
| **Audio Converters** | Crystal CS4225 AD/DA converter module<br>(2) 16-bit A/D-converters, 50kHz, S/N-ratio> 82dB<br>(1) 12-bit A/D-converter<br>(4) 16-bit D/A-converters, 50kHz, S/N-ratio> 100dB |
| **Interfaces** | 3 x 2 channels multiplexed audio inputs<br>(4) audio outputs<br>(2) 8-bit input-ports<br>(2) 8-bit output-ports<br>UART-serial port<br>(2) free interrupt-lines |
| **Display** | Hitachi LM093XMLN LCD-display module with background light, 16 x 2 characters |
| **Keyboard** | 6-key keyboard and control module |

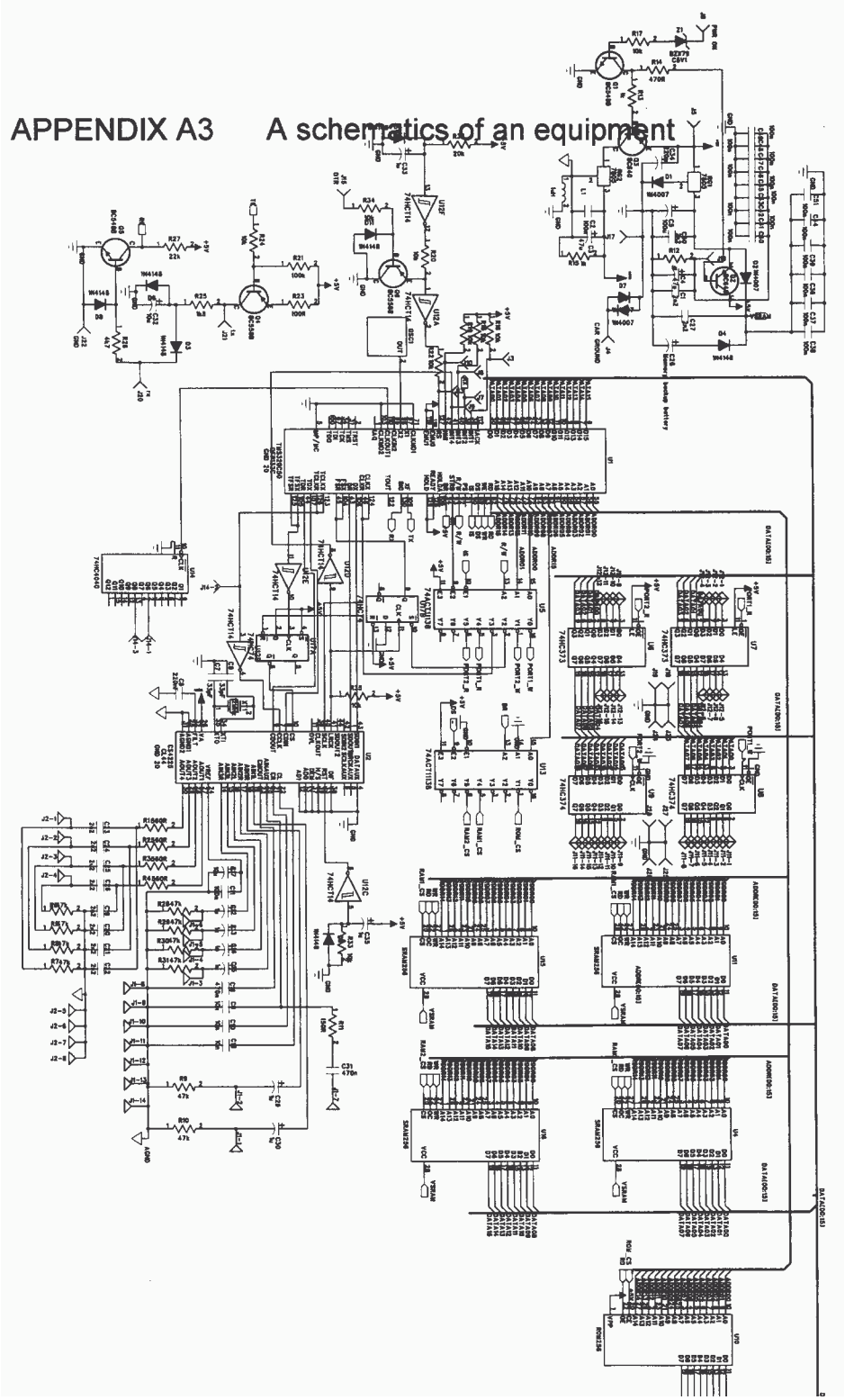
# Appendix A. Bill of Materials

| Qty | Part | Description | |
|---|---|---|---|
| **ICs** | | | |
| 1 | U1 | TMS320C50 DSP | |
| 1 | U2 | CS4225 | |
| 4 | U4 U11 U15-16 | 20 ns SRAM 256kX8 | |
| 1 | U10 | EPROM 32kX8 | |
| 2 | U5 U13 | 74ACT11138 | |
| 2 | U6-7 | 74HC373 | |
| 2 | U8-9 | 74HC374 | |
| 1 | U17 | 74HC74 | |
| 1 | U14 | 74HC4040 | |
| 1 | U12 | 74HCT14 | |
| 2 | RG1-2 | 7805 | |
| 1 | OSC1 | 40 MHz Crystal oscillator | |
| **Crystals** | | | |
| 1 | XT1 | XTAL1,12MHz | |
| **Transistors** | | | |
| 2 | Q1 Q5 | BC548B Transistor | |
| 2 | Q2-3 | BC640 | |
| 2 | Q4 Q6 | BC558B Transistor | |
| **Diodes** | | | |
| 4 | D1-2 D6-7 | 1N4007 | |
| 7 | D3-5 D8-11 | 1N4148 | |
| 1 | Z1 | Zener diode 5V1 | |
| **Capacitors** | | | |
| 2 | C7-8 | CAP,33pF | |
| 3 | C1 C27 C50 | CAP, 2n2 | |
| 4 | C21-22 C19-20 | CAP, 2n2 | SMD NPO |
| 3 | C9-10C18 | CAP, 10n | SMD NPO |
| 17 | C2C11 C36-49 C51 | CAP, 100n | |
| 1 | C6 | CAP, 220nF | |
| 2 | C16C31 | CAP, 470 | |
| 8 | C12-15 C33 C35 | CAPE 1µ | |
| 4 | C23-26 | CAP,2µ2 | |

| Qty | Part | Description | |
|---|---|---|---|
| **Capacitors (continued)** | | | |
| 2 | C17 C32 | CAPE 10μ/16V | LOW IMPEDANCE |
| 2 | C3-4 | CAPE 47μ/16V | LOW IMPEDANCE |
| 1 | C5 | CAPE 100μ/16V | LOW IMPEDANCE |
| 1 | C34 | CAPE 220μ/16V | LOW IMPEDANCE |
| **Batteries** | | | |
| 1 | C28 | Memory backup battery | |
| **Connectors** | | | |
| 1 | J14 | GENERIC 3 PIN SIP HEADER | |
| 1 | J2 | HEADER8 | |
| 1 | J1 | HEADER14 | |
| 2 | J11-12 | HEADER16 | |
| **Inductors** | | | |
| 1 | L1 | IND 1uH | |
| **Resistors** | | | |
| 1 | R23 | RES, 100R | |
| 1 | R11 | RES, 150R | |
| 1 | R14 | RES, 470R | |
| 4 | R1-4 | RES, 560R | |
| 3 | R12-13 R15 | RES, 1k | |
| 1 | R25 | RES, 1k8 | |
| 1 | R26 | RES, 4k7 | |
| 10 | R16-20 R22 R24 R33-35 | RES,10k | |
| 1 | R32 | RES, 20k | |
| 1 | R27 | RES, 22k | |
| 10 | R5-10 R28-31 | RES, 47k | |
| 1 | R21 | RES, 100k | |

# Appendix B. Equipment Schematic

*Figure 2. Equipment Schematic*



# Appendix C. PCB Components Wiring and Layout

*Figure 3. PCB Components Wiring and Layout (1 of 3)*

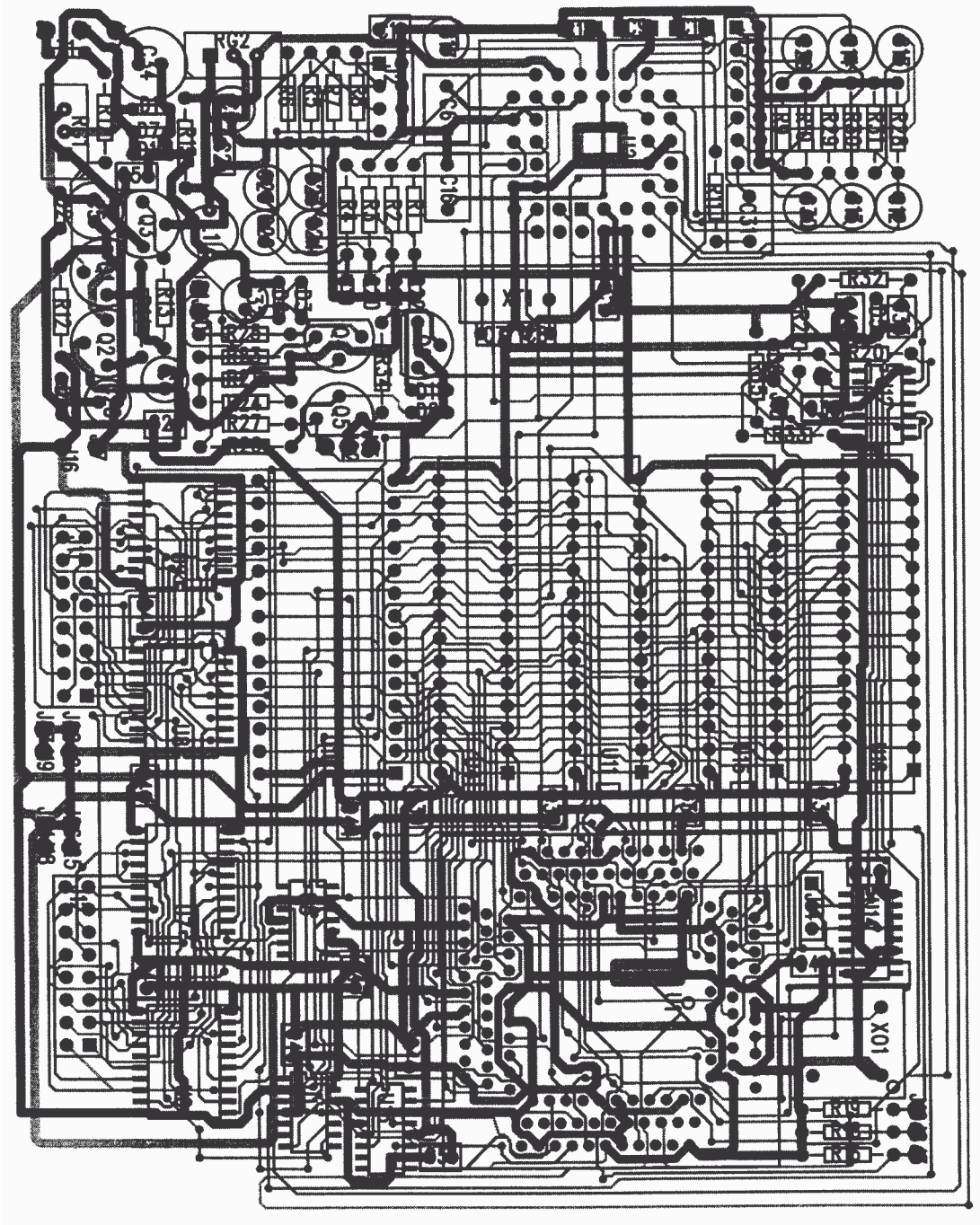


*Figure 4. PCB Components Wiring and Layout (2 of 3)*

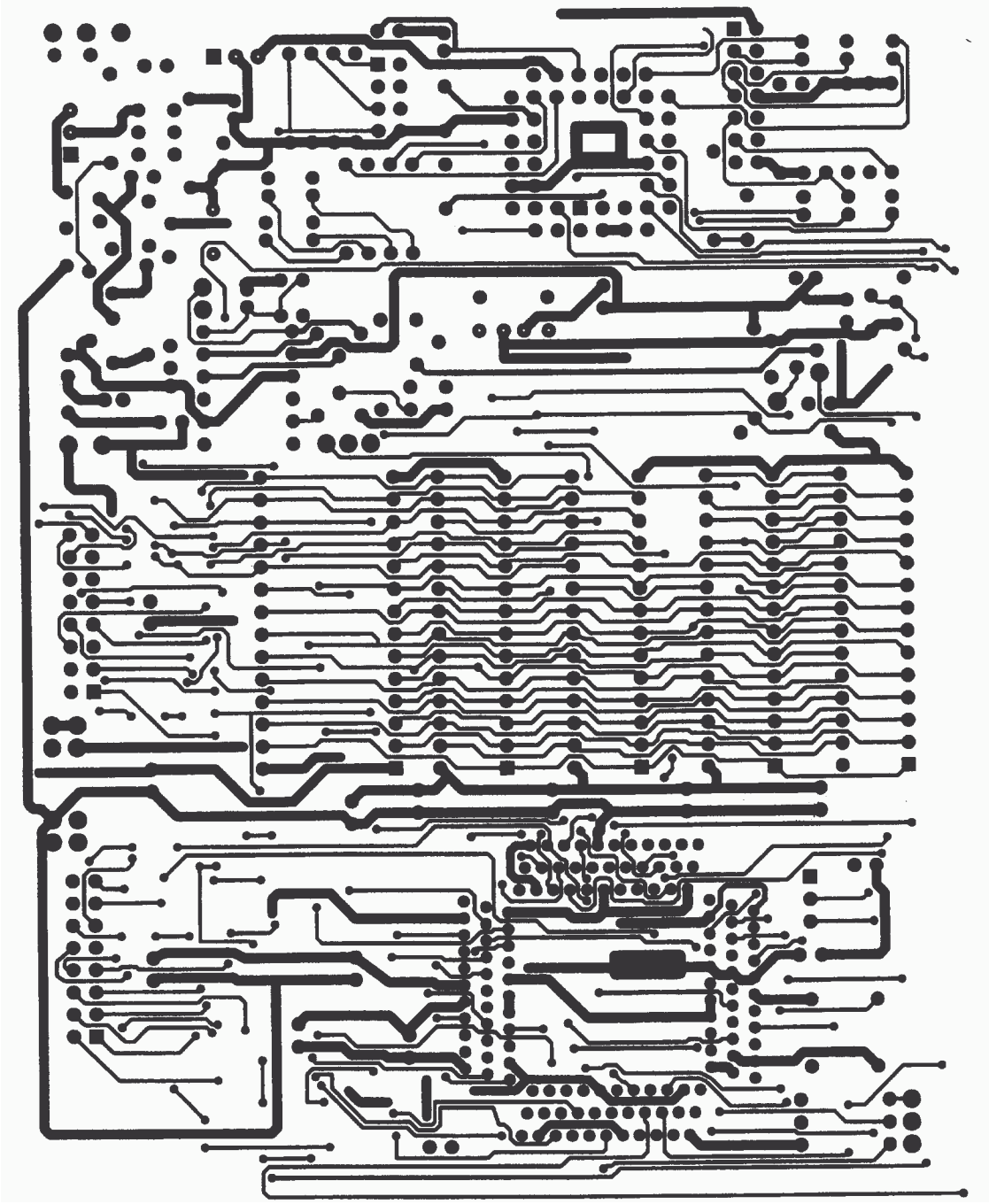


*Figure 5. PCB Components Wiring and Layout (3 of 3)*