Application Report
SPRA533

TMS320C6000 EMIF to External SBSRAM Interface

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Abstract

Interfacing external synchronous burst SRAM (SBSRAM) to the Texas Instruments (TI™) TMS320C6000 series of digital signal processors (DSPs) is simple compared to previous generations of TI DSPs thanks to the advanced external memory interface (EMIF). The EMIF provides a glueless interface to a variety of external memory devices.

This document describes:

- EMIF control registers and SBSRAM signals
- Interface schematic of x32/36 and x18 SBSRAM devices
- SBSRAM functionality and performance considerations
- Timing analysis of the interface between various ‘C6000 DSPs and Micron SBSRAM

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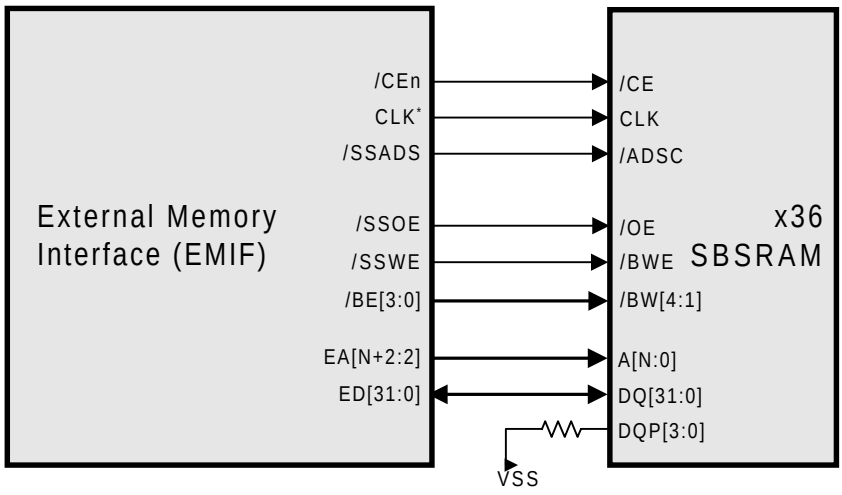
Interface of EMIF With SBSRAM

As shown in Figure 1, the EMIF interfaces directly to 32-bit-wide industry standard SBSRAMs. SBSRAMs are available in both flow through and pipeline; however, the ‘C6000 DSPs interface only to standard write pipeline SBSRAM (either single- or double-cycle deselect), which has the capability to operate at higher frequencies with sustained throughput.

The SBSRAM interface allows a high-speed memory interface without some of the limitations of SDRAM. Most notably, because SBSRAMs are SRAM devices, consecutive reads or consecutive writes to all addresses within the SBSRAM can occur on any cycle. The SBSRAM interface typically runs at half the CPU clock rate. On certain ‘C6000 devices, this interface may run at either the CPU clock speed or half of this rate, based on the setting of the SSCRT bit in the EMIF global control register. Other ‘C6000 devices allow the synchronous memory interfaces to run off an external clock that has no relation to the operating frequency of the DSP.

Figure 1 shows the connections used to interface to a 36-bit-wide SBSRAM. For this interface, the four parity bits of the SBSRAM should be tied to ground through a resistor because the ‘C6000 data bus is only 32 bits wide and cannot take advantage of the parity bits. This interface is almost identical to the interface to a 32-bit-wide SBSRAM, except that a 32-bit-wide SBSRAM has No Connects instead of parity bits.

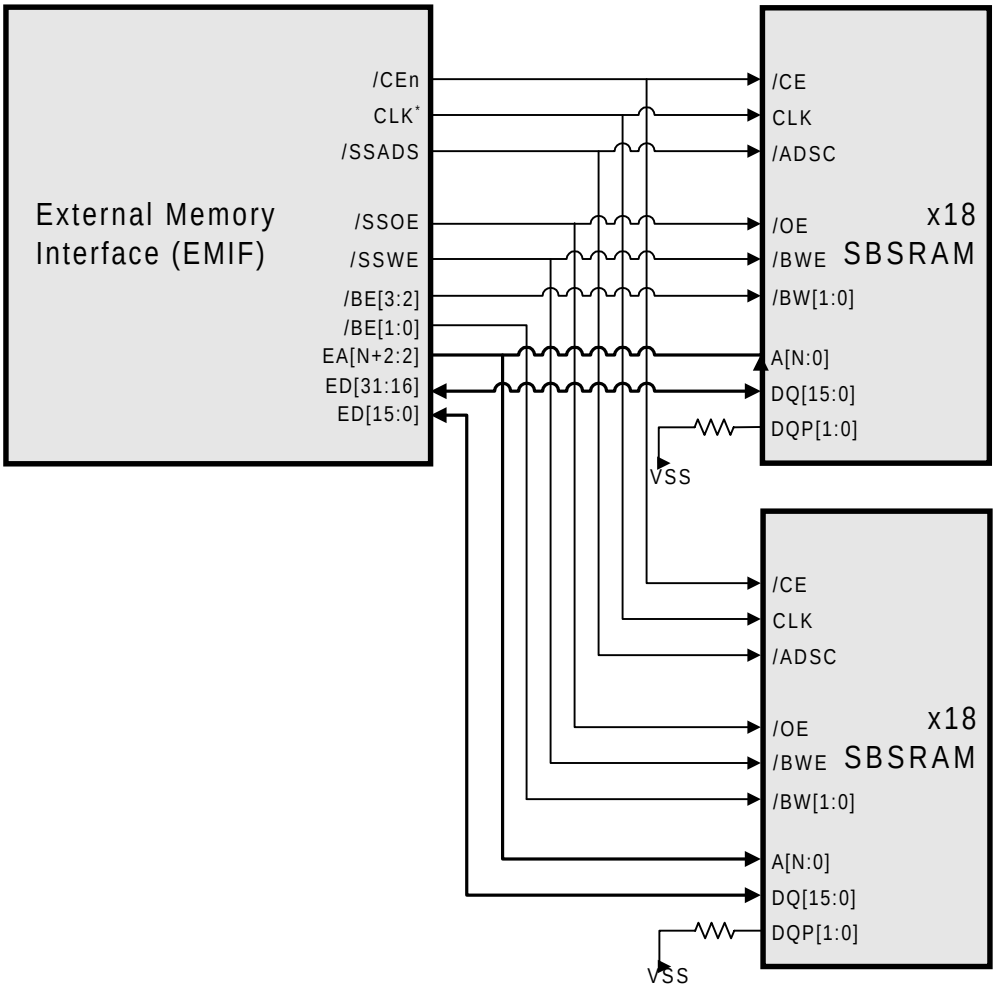
Figure 1. EMIF—One x36 SBSRAM Interface



* CLK = SSCLK for 'C6201/'C6701; CLK = CLKOUT2 for 'C6202; CLK = ECLKOUT for 'C6211/C6711

Figure 2 shows the connections used to interface to two 18-bit-wide SBSRAMs. For this example, two SBSRAMs are used in parallel to interface to the 32-bit-wide data bus of the ‘C6000 DSPs. The advantage of this interface is that with a given density SBSRAM, the addressable memory space is effectively doubled by using two devices in parallel. The parity bits of the SBSRAMs are tied to ground through a pull-down resister.

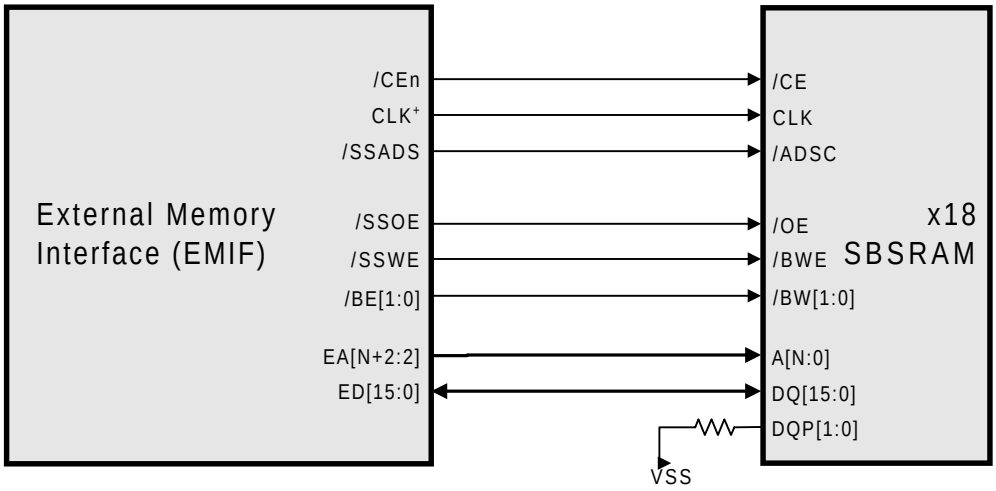
Figure 2. EMIF—Two x18 SBSRAM Interface



* CLK = SSCLK for 'C6201/'C6701; CLK = CLKOUT2 for 'C6202; CLK = ECLKOUT for 'C6211/C6711

Figure 3 shows an interface to a single x18 SBSRAM. This interface may be attractive for low-cost applications where device count and board space are critical. This interface is only supported on the ‘C6211 and ‘C6711 devices.

Figure 3. EMIF—One x18 SBSRAM Interface



+ CLK = ECLKOUT for 'C6211/C6711

Overview of EMIF

’C6201/’C6701 SBSRAM Interface

- Can operate at either 1/2x the CPU clock speed or 1x the CPU clock speed
- SSCLK is used as the SBSRAM clock.
- Has dedicated SBSRAM control signals. Any combination of synchronous memory types is allowed.
- Only supports 32-bit-wide SBSRAM interface

’C6202 SBSRAM Interface

- Can operate at 1/2x the CPU clock speed
- CLKOUT2 is used as the SBSRAM clock.
- SBSRAM control signals are MUXed with SDRAM control signals. Only one type of synchronous memory is allowed in the system.
- Only supports 32-bit-wide SBSRAM interface

’C6211/’C6711 SBSRAM Interface

- Clock speed is independent of internal CPU speed and can run at a maximum of 100 MHz. An external clock can be tied to ECLKIN for maximum flexibility or CLKOUT2 can be routed back to ECLKIN for simplicity, resulting in a memory clock speed of 1/2x the CPU clock speed.

- ECLKOUT must be used as the synchronous memory clock and is a mirror image of ECLKIN.
- SBSRAM control signals are MUXed with SDRAM and Async control signals. Any combination of synchronous memory types is allowed.
- 8-bit-wide and 16-bit-wide interfaces are allowed. The data bus byte lanes used depend on the endianness of the system.

EMIF Signal Descriptions

Figure 4 shows a block diagram of the EMIF, the interface between external memory and the other internal units of the ‘C6000. On the ‘C6201, ‘C6701, and ‘C6202, the interface with the processor is provided via the DMA (direct memory access) controller, program memory controller, and data memory controller. For the ‘C6211 and ‘C6711, the interface with the processor is provided via the enhanced DMA.

Figure 4 through Figure 6 show the block diagrams of the ‘C6201/’C6701, ‘C6202, and ‘C6211/’C6711 respectively. Note that the clocks and the control signals are slightly different for each of the three different style EMIFs. The signals listed in Table 1 describe the SBSRAM interface and the shared interface signals.

Figure 4. ’C6201/’C6701 EMIF SBSRAM Interface Block Diagram

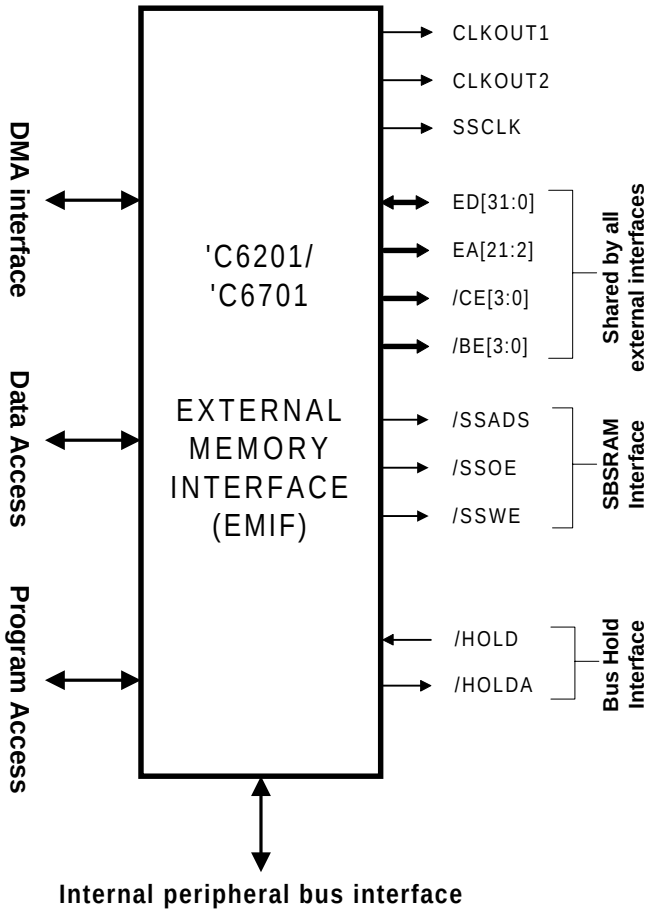


Figure 5. 'C6202 EMIF SBSRAM Interface Block Diagram

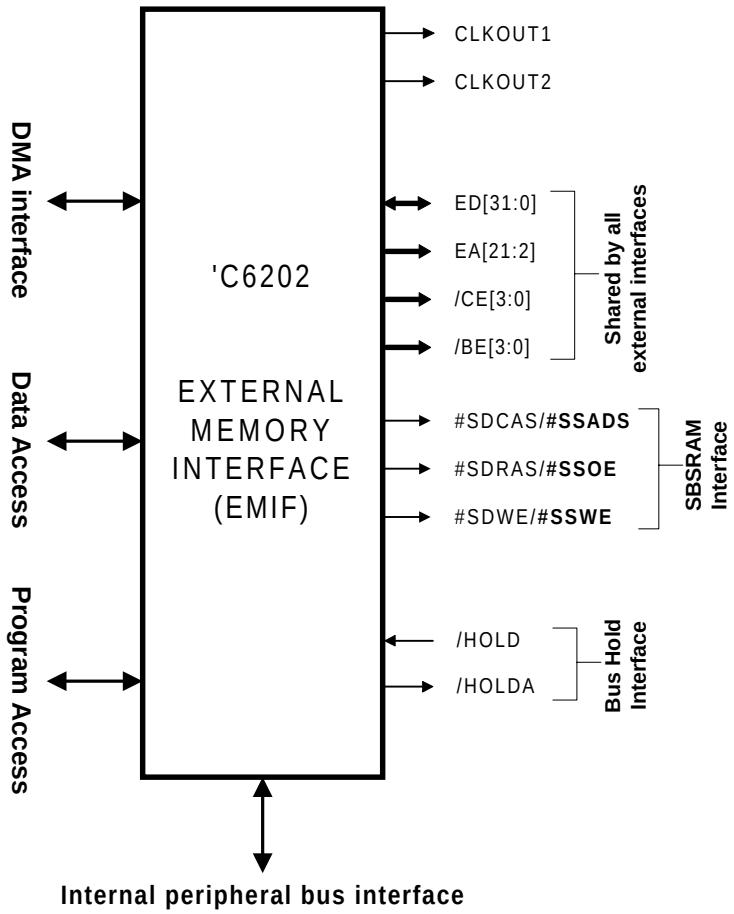


Figure 6. ’C6211/’C6711 EMIF SBSRAM Interface Block Diagram

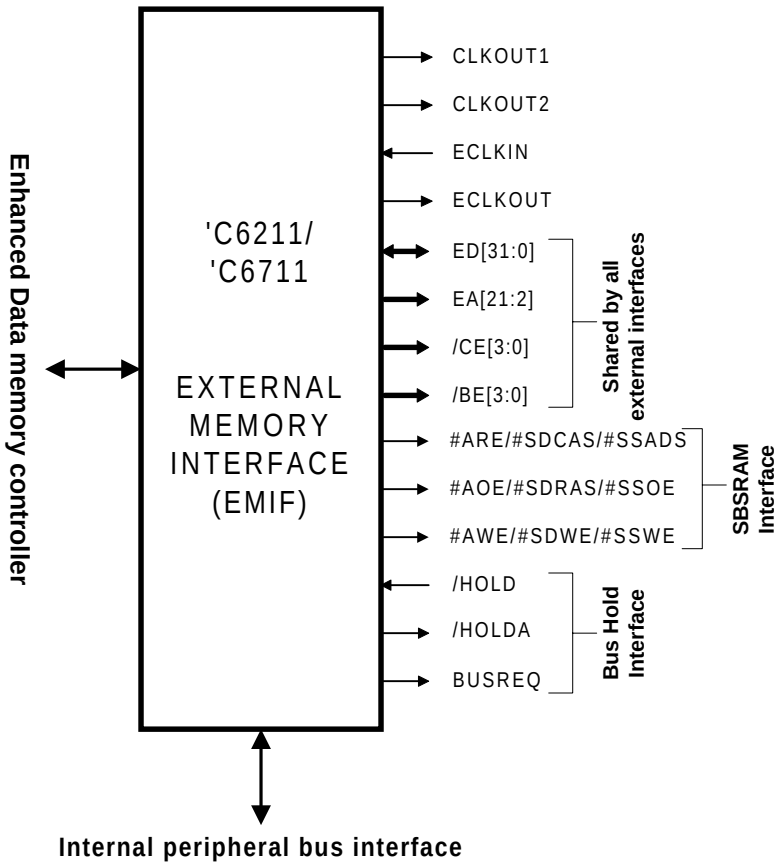


Table 1. EMIF SBSRAM Pins

SBSRAM Signal	'C6201/ 'C6701 Interface	'C6202 Signal Interface	'C6211/ 'C6711 Interface	SBSRAM Function
/CE	/CEx	/CEx	/CEx	Chip Enable. /CE must be active (low) for a command to be clocked into the SBSRAM.
CLK	SSCLK	CLKOUT2	ECLKOUT	SBSRAM Clock. Runs at either 1x or 1/2x the CPU rate.
/ADSC	/SSADS	#SDCAS/ **#SSADS**	#ARE/ #SDCAS/ **#SSADS**	Synchronous Address Strobe: Causes a new external address to be registered. If /CE is active, a READ or WRITE is performed.
/OE	/SSOE	#SDRAS/ **#SSOE**	#AOE/ #SDRAS/ **#SSOE**	Output Enable. Enables the data I/O drivers.
/BWE	/SSWE	#SSWE/ **#SSWE**	#AWE/ #SSWE/ **#SSWE**	Write Enable. Permits write operations.
/BW[4:1]	/BE[3:0]	/BE[3:0]	/BE[3:0]	Byte Write Enables. Allow individual bytes to be written when /BWE is active. A Byte Write Enable is LOW for a WRITE and DON'T CARE for a READ cycle. /BW1 controls Byte 1, /BW2 controls Byte 2, /BW3 controls Byte 3, and /BW4 controls Byte 4.
A[N:0]	EA[N+2:2]	EA[N+2:2]	EA[N+2:2]	Address Inputs. Registered on rising edge of SSCLK..
DQ[32:1]	ED[31:0]	ED[31:0]	ED[31:0]	Data I/O. Byte 1 is DQ[8:1], Byte 2 is DQ[16:9], Byte 3 is DQ[24:17], and Byte 4 is DQ[32:25].
/ADV	**3.3 V**	**3.3 V**	**GND**	'C6201/'C6701/'C6202:/ADV is tied to 3.3 V to disable the burst mode of the SBSRAM because bursting is accomplished by issuing back-to-back reads or writes. 'C6211/'C6711: /ADV is tied to GND to enable the burst mode of the SBSRAM.
/CE2	GND	GND	GND	Enable /CE2 at all times.
MODE	GND	GND	GND	Select linear burst.
ZZ	GND	GND	GND	Disable snooze mode.
VSS	GND	GND	GND	Ground
VCC	3.3 V	3.3 V	3.3 V	3.3 V supply
CE2	3.3 V	3.3 V	3.3 V	Enable CE2 at all times.
/ADSP	3.3 V	3.3 V	3.3 V	Disable /ADSP at all times.
/GW	3.3 V	3.3 V	3.3 V	Disable global write at all times.
Parity Data	1 kΩ to GND	1 kΩ to GND	1 kΩ to GND	Terminate Parity data because it is not used on 'C6000 interfaces.

Note: Bold text represents a departure from the style of interface used for the '6201.

Clocking the ’C6211/’C6711 EMIF

The EMIF of the ‘C6211/’C6711 requires an external clock to be provided via the ECLKIN input. For simplicity, CLKOUT2 can be routed into the ECLKIN pin to avoid the extra hardware required to create a clock externally. This method has the restriction of only allowing a memory interface at 1/2x the CPU clock speed (or 75 MHz for a 150-MHz device).

If an external clock is provided, the EMIF can operate up to 100 MHz. The ‘C6211 and ’C6711 data sheets specify that the rise/fall time of the externally provided clock must be no longer than 3 ns. This can prove difficult with most off-the-shelf oscillators. Our recommended approach is to use the ICS501 PLL Multiplier chip, which can produce a wide range of frequency outputs with standard crystals.

Clock-to-Output Relationship on ’C6000 Devices

To optimize the synchronous memory interfaces of the various ‘C6000 devices, the output signals are triggered off of different internal clocks of the ‘C6000 DSP. Figure 7 through Figure 10 show the clock relationship used for the various ‘C6000 DSPs. Because the ‘C6211/’C6711 SBSRAM interface is timed in reference to an externally provided clock, the ‘C6211 and ‘C6711 data sheets provide tdmax and tdmin but not Tosu and Toh parameters. The fact that the Tosu and Toh parameters use a factor of P in the equations allows the user to be unconcerned about the output edge being used internal to the ‘C6000. In this way, the Tosu parameter can be compared directly against the Tisu parameter of the memory at a given operating speed. (For more details, see the *Timing Constraints* section.)

The tdmax and tdmin parameters reference the actual clock edge of the ‘C6000 from which data is driven out. The Tosu and Toh terms are the notation used in ‘C6000 data sheets except those for the ‘C6211 and ‘C6711. The Tosu term shows the setup time to the rising edge of the clock. The Toh term shows the hold time from the rising edge of the memory clock. P refers to the CPU clock period.

Notice that the data sheet notation directly implies the clocking relationship of the device. For example, the data sheet for the full speed ‘C6201B SBSRAM interface states that Tosu = 0.5P – 1.3. Referring to the diagram in Figure 7, it can be seen that tdmax is relative to the falling edge of SDCLK, providing a setup time of 0.5P – tdmax. All other ‘C6000 data sheets can be analyzed in the same way.

Figure 7. Full Speed Interface—’C6201 rev2.1 vs. ’C6201B/’C6701

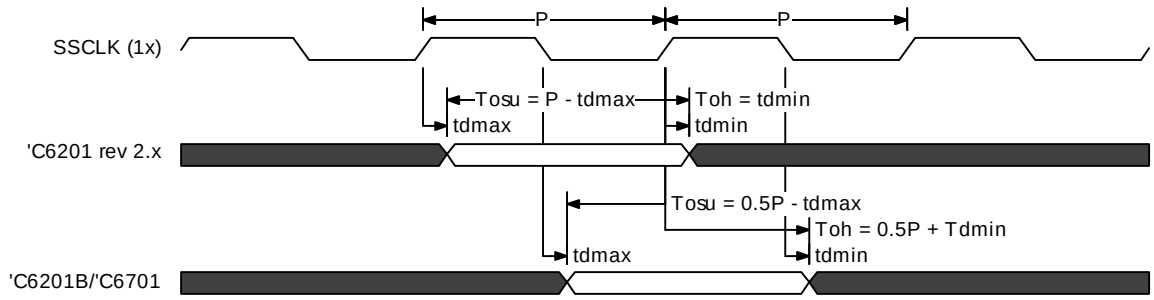


Figure 8. Half Speed Interface—'C6201 rev 2.1 vs. 'C6201B/'C6701

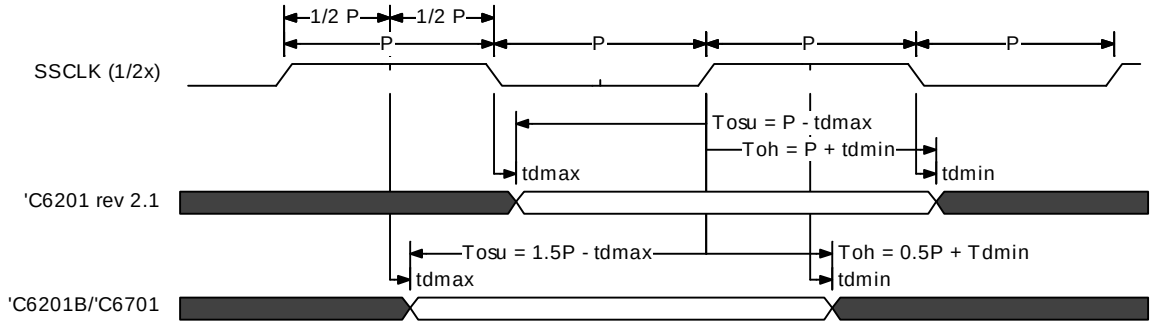


Figure 9. Half Speed Interface—'C6202

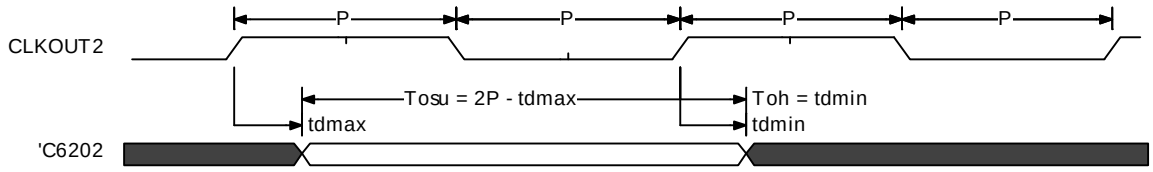
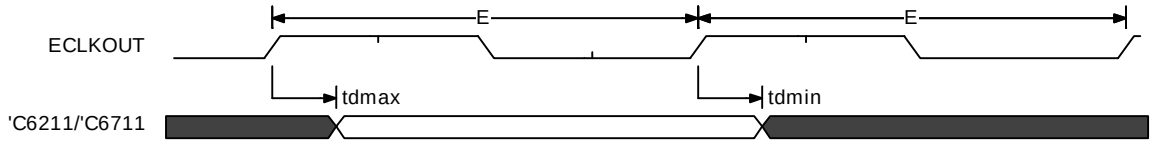


Figure 10 shows the clock relationship used for the 'C6211/'C6711 SBSRAM interface. Because this interface is timed in reference to an externally provided clock, the 'C6211 and 'C6711 data sheets provide Tdmax and Tdmin but not Tosu and Toh parameters.

Figure 10. External Clock Interface—'C6211/'C6711

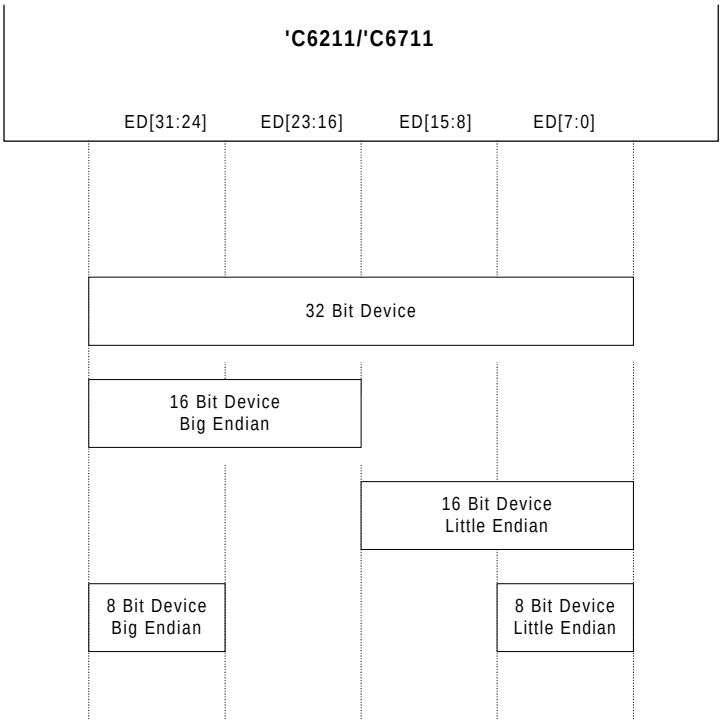


Byte Lane Alignment on the 'C6211/'C6711 EMIF

The 'C6711 EMIF offers the capability to interface to 32-bit, 16-bit, and 8-bit SBSRAM. Depending on the endianness of the system, a different byte lane is used for the SBSRAM interface. The alignment required is shown in Figure 11.

Note that BE3 always corresponds to ED[31:24], BE2 always corresponds to ED[23:16], BE1 always corresponds to ED[15:8], and BE0 always corresponds to ED[7:0], regardless of endianness.

Figure 11. Byte Lane Alignment vs. Endianness on the 'C6211/'C6711



EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory-mapped registers within the EMIF. A write to any EMIF register should not be done while EMIF accesses are in progress. The memory-mapped registers are shown in Table 2.

Table 2. EMIF Memory-Mapped Registers for SBSRAM

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	Reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control

EMIF Global Control Register

Figure 12 shows the EMIF global control register, which configures parameters common to all of the CE spaces. Table 3 only lists those parameters that are relevant for use with SBSRAM.[1]

[1] For a description of all of the parameters of the EMIF global control register, see the *TMS320C6000 Peripherals Reference Guide*.

Figure 12. EMIF Global Control Register Diagram

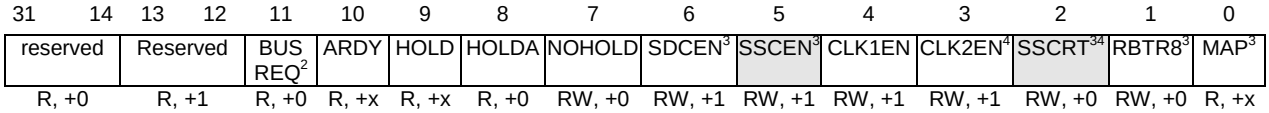


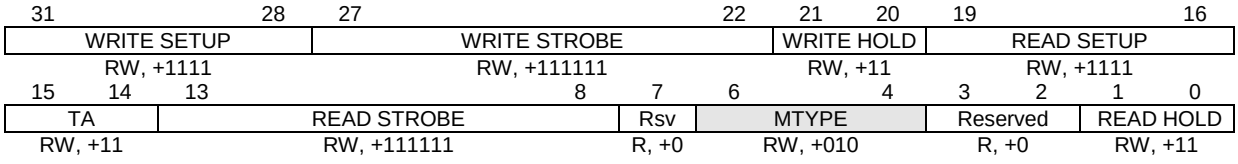
Table 3. EMIF Global Control Register Bit Field Description for SBSRAM

Field	Description
SSCEN	SBSRAM clock enable (for 'C6201, 'C6701, and 'C6202) 'C6201/'C6701: SSCEN=0, SSCLK held high SSCEN=1, SSCLK enabled to clock 'C6201/'C6701: SSCEN=0, CLKOUT2 held high if MemType = SBSRAM SSCEN=0, CLKOUT2 enabled to clock if MemType = SBSRAM
SSCRT	SBSRAM clock rate select ('C6201/'C6701 only) SSCRT=0, SSCLK ½x CPU clock rate SSCRT=1, SSCLK 1x CPU clock rate

CE Space Control Registers

Figure 13 and Figure 14 show the four CE space control registers, which correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or Asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. The only field of interest for SBSRAM is the MTYPE field. Modification of a CE space control register should not be done until that CE space is inactive.

Figure 13. 'C6201/'C6202/'C6701 EMIF CE Space Control Register Diagram



[2] Field exists only in TMS320C6211/ TMS320C6711.
[3] Fields do not exist in TMS320C6211/ TMS320C6711.
[4] Fields do not exist in TMS320C6202.

Figure 14. ’C6211/’C6711 EMIF CE Space Control Register Diagram

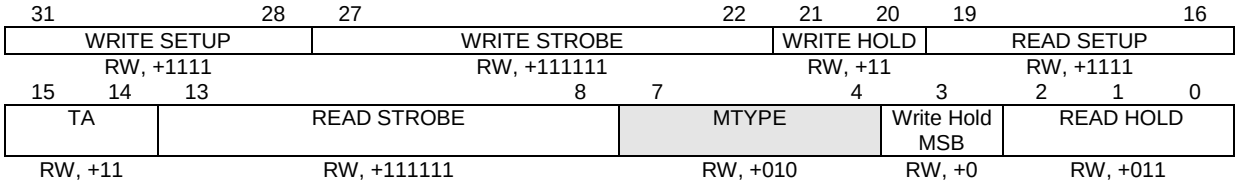


Table 4. EMIF CE Space Control Register Bit Field Description for SBSRAM

Field	Description
MType	Memory Type
	All devices:
	MTYPE = 100b: 32-bit-wide SBSRAM
	‘C6211/’C6711 only:
	MTYPE = 1010b: 8-bit-wide SBSRAM
	MTYPE = 1011b: 16-bit-wide SBSRAM
SSCRT	SBSRAM clock rate select
	‘C6201/’C6701 only:
	SSCRT=0, SSCLK ½x CPU clock rate
	SSCRT=1, SSCLK 1x CPU clock rate

SBSRAM Operations

The style of SBSRAM operations depends on whether or not bursting is done by default. On the ‘C6201, ‘C6701, and ‘C6202, the burst mode of the SBSRAM is not used (/ADV is disabled by tying it high). Instead, bursting is accomplished by issuing a new command on every clock cycle.

On the ‘C6211 and ‘C6711, the burst mode of the SBSRAM is used. When a command is issued, a sequential burst of four words is performed to/from the SBSRAM (/ADV is enabled by tying low).

Non-Burst-Mode Accesses by ’C6201, ’C6701, and ’C6202

For the ‘C6201, ‘C6202, and ‘C6701 interface to SBSRAM, the burst mode of the SBSRAM must be disabled. There is no associated performance degradation because bursts can still be done. Bursts are accomplished by issuing commands on consecutive cycles and can achieve a peak throughput equal to the clock speed of the interface.

Figure 15 shows a four-word write to SBSRAM. Every access strobes a new address into the SBSRAM.

Figure 15. SBSRAM Write—Half Speed

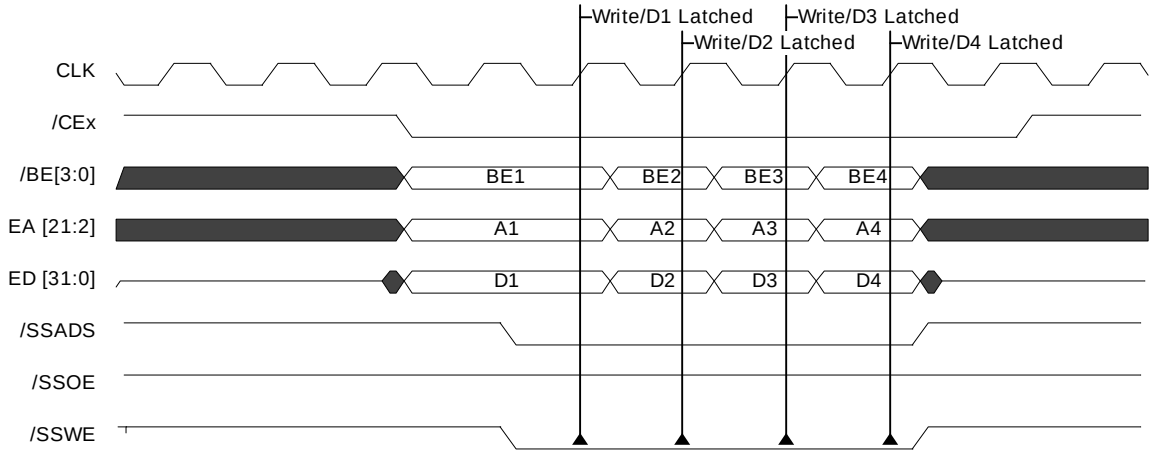
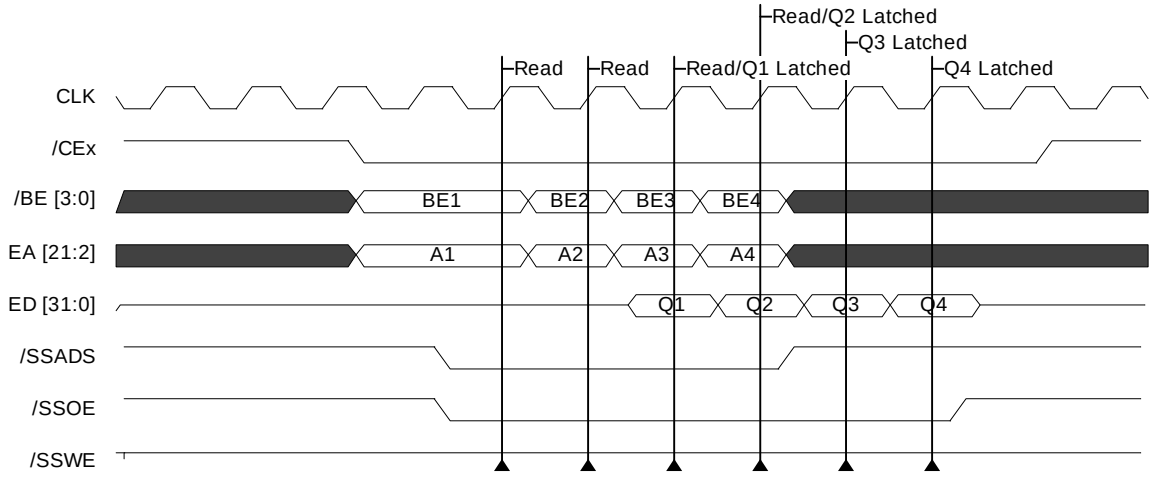


Figure 16 shows a four-word read of an SBSRAM. Every access strobes a new address into the SBSRAM, indicated by the /SSADS strobe low. The first access requires an initial read latency of 2 cycles; thereafter, all accesses have single cycle throughput.

Figure 16. SBSRAM Read—Half Speed



Burst-Mode Accesses by ’C6211 and ’C6711

The ‘C6211 and ‘C6711 take advantage of the internal burst counter of SBSRAMs when performing accesses (/ADV is always active, tied low). Although a performance advantage is not realized because bursts can take place by issuing consecutive commands, this interface does offer the advantage of issuing fewer commands to the SBSRAM. This results in slightly lower power consumption compared to the other ‘C6000 devices.

The internal burst counter of SBSRAM is a four-word counter, which can be programmed to increment linearly or in an interleaved fashion. Table 5 shows the addressing of the SBSRAM in linear mode, which must be used for the 'C6211/'C6711 interface. As Table 5 shows, the 2-bit counter automatically rolls over to 00 from 11. For example, if address 0111b were issued to the SBSRAM in burst mode, the subsequent access would be to 0100b, if the SBSRAM were allowed to continue the burst. Accesses done by the 'C6211/'C6711 prevent this by issuing a new command to the SBSRAM before the burst counter rolls over. So, if an access to 0111b is begun, on the subsequent cycle the 'C6211/'C6711 will issue address 1000b to continue the linear burst.

Random or decrementing accesses can still be performed by the 'C6211 and 'C6711. This is done in the same manner as the 'C6201 style interface. That is, if random accesses are performed, a new command will be issued on every cycle to interrupt the burst mode of the SBSRAM.

Table 5. SBSRAM Burst Counter

	Case 1	**Case 2**	**Case 3**	**Case 4**
SBSRAM Address	A[1:0]	A[1:0]	A[1:0]	A[1:0]
EMIF Address	EA[3:2]	EA[3:2]	EA[3:2]	EA[3:2]
First address	00	01	10	11
	01	10	11	00
	10	11	00	01
Fourth Address	11	00	01	10

Figure 17 shows a six-word write burst that begins at address 0100b. Since the two LSBs (least-significant bits) are 00, the 'C6211/'C6711 allows the internal burst counter to increment up to 0111b. On the fifth cycle, a new command is issued to address 1000b to continue the burst.

Figure 17. SBSRAM Write Burst by the 'C6211/'C6711

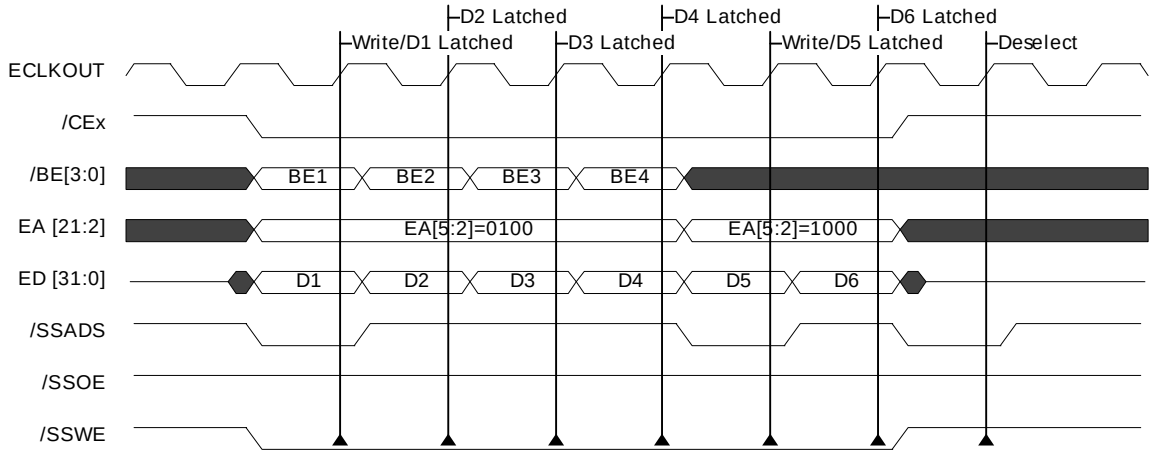
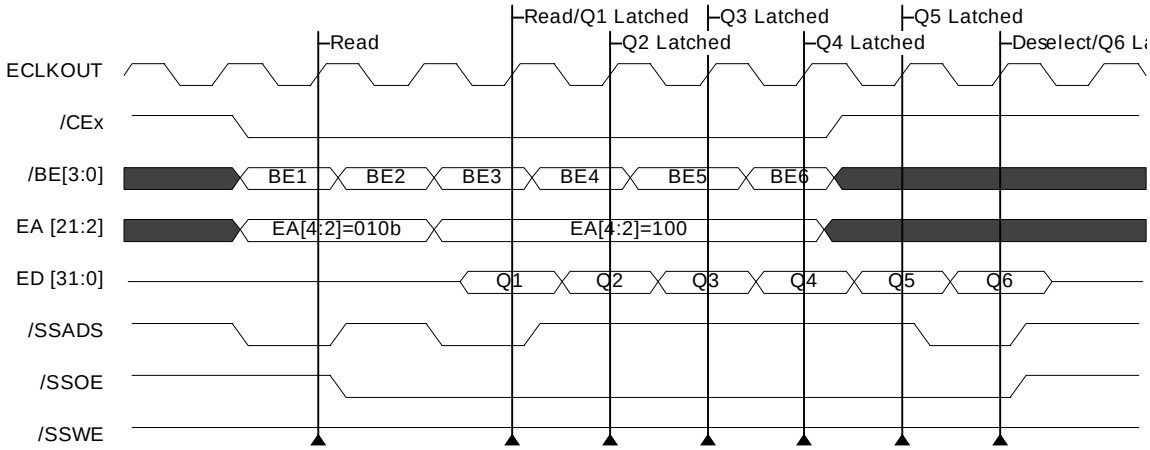


Figure 18 shows a six-word read burst that begins at address 010b. Because the two LSBs are 10b, the 'C6211/'C6711 allows the internal burst counter to increment up to 011b. On the third cycle, a new command is issued to address 100b to continue the linear burst.

Figure 18. SBSRAM Read Burst by the 'C6211/'C6711



Optimizing SBSRAM Accesses

SBSRAMs are latent by their architecture, meaning that read data follows address and control information. Consequently, the EMIF inserts cycles between read and write commands to ensure that no conflict exists on the ED[31:0] bus. The EMIF keeps this turnaround penalty to a minimum. The initial 3-cycle penalty is present when changing directions on the bus.

In general, the rule is that the first access of a burst sequence will incur at least a 3-cycle startup penalty. Therefore, to maximize throughput, attempt to minimize direction changes on the data bus when accessing SBSRAM.

Timing Constraints

This section discusses the timing constraints used to determine if an SBSRAM can operate with the 'C6000 at a given clock frequency.

For the following constraint calculations, a time t_{margin} is calculated representing the margin in the system after taking into account the worst-case numbers from the memory and the 'C6000 data sheets.

After calculating the time t_{margin}, it is a system-level issue to determine if the proper amount of margin has been met. The required timing margin is extremely system dependent, depending primarily on trace length and loading, but other factors can come into play. Therefore, this parameter should be determined for the particular system in question.

In general, the timing margin required is not the same for the different parameters of the read/write cycles. For output signals, the required timing margin is minimal because the output clock and output control/data signals both propagate from the 'C6000 DSP to the SBSRAM. Therefore, the timing margin must account for the possible skew between the two signals (clock versus control/data) caused by loading effects or differences in route length.

For example, signals on a board manufactured with 0.5-ounce copper traces in FR4 exhibit a propagation delay time of ~0.17 ns per inch. If the skew between clock and output signals is ±3 inches, the required board margin is ~0.5 ns for both output setup and hold. This does not consider settling time effects or other loading issues that should be considered when determining the amount of margin required.

The timing margin required for reads is more complicated. The issue with reads is that the memory is outputting data relative to a clock that has undergone a propagation delay when traveling from the 'C6000 DSP to the SBSRAM. The memory outputs the data a time t_{acc} from this delayed clock. The output data from the memory undergoes a delay itself before arriving at the 'C6000 DSP. Therefore, the timing margin for read setup must account for these two propagation delays. The read hold time is improved because of this and the margin required can be considered negligible.

Using the same board characteristics previously used, this implies that if both the clock and data paths are approximately 3 inches long, the round trip propagation delay for clock to SBSRAM and for data back to the 'C6000 is approximately 1 ns (6 inches $\times$ 170 ps/inch). Therefore, the margin required for reads in this example is at least 1 ns on the input setup time and <0 ns on the input hold time. This does not consider settling time effects or other loading issues that should be considered when determining the amount of margin required.

These numbers are guidelines. The actual margin required for any system might be different.

In the following discussion, *m* is used to denote the memory specifications. No additional designators are used to denote the 'C6000 DSP timing specifications.

TMS320C6000 Outputs (ED, EA, CE, BE, SSADS, SSOE, SSWE)

'C6201/'C6701/'C6202 Output Comparison

For simplicity, the 'C6201, 'C6701, and 'C6202 data sheets specify the outputs as a setup time (tosu) to the next rising edge and a hold time (toh) from the previous rising edge. Thus, the comparison between 'C6000 specifications and memory specifications is extremely straightforward. This also allows the user to be unconcerned with which clock edge triggers output data.

The following equations, derived from Figure 19, should be used to calculate the timing margin between the 'C6000 and the desired SBSRAM.

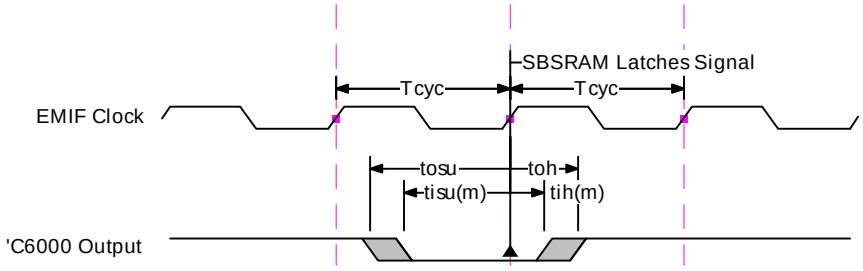
- Setup time: Output setup time (t_{osu}) from inactive to active must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the margin available is:

  $t_{margin} = t_{osu} - t_{isu(m)}$

- Hold time: Output hold time (t_{oh}) from active to inactive must be greater than the hold time required by the input ($t_{ih(m)}$). The margin is then:

  $t_{margin} = t_{oh} - t_{ih(m)}$

Figure 19. Outputs From 'C6000 (Write Data [ED], Control, and Address Signals)



'C6211/'C6711 Output Comparison

The 'C6211 and 'C6711 data sheets specify the outputs as a minimum delay and a maximum delay from the rising edge of ECLKOUT. When comparing these parameters against the specification for a particular SBSRAM, the maximum delay (t_{dmax}) is used to verify that the input setup time ($t_{is(m)}$) of the memory is met. The minimum delay (t_{dmin}) is used to verify that the input hold time ($t_{ih(m)}$) of the memory is met.

The following equations, derived from Figure 20, should be used to calculate the timing margin between the 'C6211/'C6711 and the desired SBSRAM.

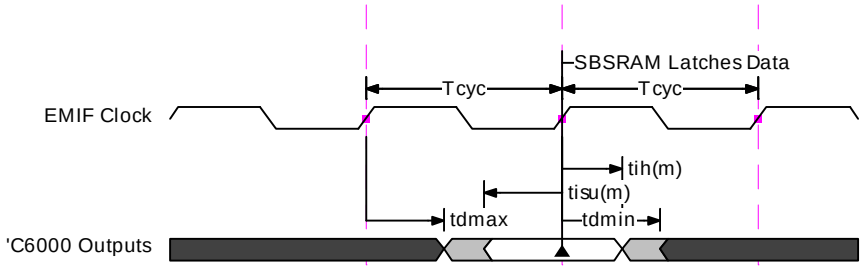
- Setup time: The maximum delay (t_{dmax}) from clock to output signal valid must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the margin available is:

  $t_{margin} = t_{cyc} – (t_{dmax} + t_{isu(m)})$

- Hold time: The minimum delay (t_{dmin}) from clock to output signal invalid must be greater than the hold time required by the input ($t_{ih(m)}$). The margin is then:

  $t_{margin} = t_{oh} – t_{ih(m)}$

Figure 20. Outputs From 'C6000 (Write Data [ED], Control, and Address Signals)



’C6000 Inputs (Output Data From the SBSRAM, Read ED)

Figure 21 shows the output data from the SBSRAM as it occurs during a read cycle. The situation is similar to the outputs from the ‘C6000 except that the SBSRAM must provide an ample setup and input hold to the ‘C6000.

The constraints can be expressed as follows:

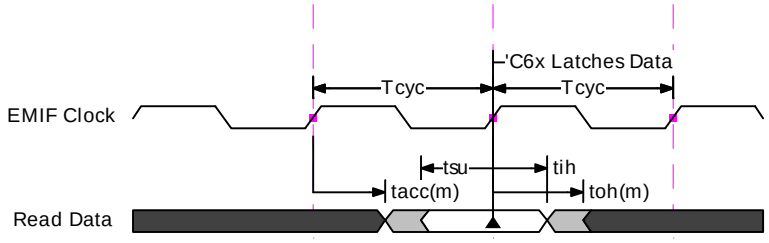
- Setup times: The access time ($t_{acc(m)}$) of the SBSRAM must provide a large enough input setup time (t_{su}) for the input to the ‘C6000.

  $t_{margin} = t_{cyc} – (t_{acc(m)} + t_{su})$

- Hold times: the output hold time ($t_{oh(m)}$) for data output from the SBSRAM, must provide a hold time greater than the hold time required by the input (t_{ih}) of the ‘C6000.

  $t_{margin} = t_{oh(m)} – t_{ih}$

Figure 21. Input to ‘C6000 (Read Data)



Timing Comparisons for Three SBSRAMs

This section summarizes the comparisons listed above for three different SBSRAMs with three different ‘C6000 devices. Although not every ‘C6000 device is shown in the following examples, the approach is the same for all of the current ‘C6000 devices.

For the following examples, notice that more margin is achieved with a faster memory. For example, if a 100-MHz interface is desired, a 133-MHz SBSRAM will provide more margin than a 100-MHz SBSRAM. Although the ‘C6000 DSPs are designed to operate with SBSRAMs at the rated speeds, sometimes the extra margin may be worth the extra cost of faster memories. Several vendors have SBSRAM devices available at 100 MHz or faster. The newest data sheets and should be compared to the ‘C6000 data sheet to guarantee operation with the desired margins.

’C6201B vs. Micron’s MT58L128L32P-7.5 at 100 MHz

The MT58L128L32P device is a 128K x 32 device, which results in an addressable space of 512 KB.

This example uses the ‘C6201B-200 running at its maximum clock speed of 200 MHz (P = 5). For this example, we assume that SSCLK is set to operate at 1/2x the CPU speed, resulting in Tcyc = 10 ns.

The timing parameters of the MT58L128L32P-7.5 and the ‘C6201B-200 can be summarized as follows:

‘C6201B-200 @ P = 5 ns		MT58L128L32P-7.5		Tmargin
Outputs	Tosu = 1.5P – 3 = 4.5 ns	Inputs	Tisu (m) = 1.5 ns	Tosu – Tisu (m) = 3 ns ✔
	Toh = 0.5P – 1.5 = 1 ns		Tih (m) = 0.5 ns	Toh – Tih (m) = 0.5 ns ✔
Inputs	Tisu = 2.5	Outputs	Tacc (m) = 4.2 ns	Tcyc – Tacc (m) – tisu = 3.3 ns ✔
	Tih = 1.5		Toh (m) = 1.5 ns	Toh – Tih (m) = 0 ns ✔

’C6202 vs. Micron’s MT58L512L18D-7.5 at 125 MHz

The MT58L512L18D is a 512K x 18 device. For the ‘C6202 interface, two of these devices are used in parallel, resulting in an addressable space of 2 MB.

This example uses the ‘C6202-250 running at its maximum clock speed of 250 MHz (P = 4 ns). Because the ‘C6202 EMIF uses CLKOUT2 (which is 1/2x the CPU speed) for synchronous memory interfaces, Tcyc = 8 ns.

The timing parameters of the MT58L512L18D-7.5 and the ‘C6202-250 can be summarized as follows:

‘C6202-250 @ P = 4 ns		MT58L512L18P-7.5		Tmargin
Outputs	Tosu = 2P – 3.8 = 4.2 ns	Inputs	Tisu (m) = 1.5 ns	Tosu – Tisu (m) = 2.7 ns ✔
	Toh = 1 ns		Tih (m) = 0.5 ns	Toh – Tih (m) = 0.5 ns ✔
Inputs	Tisu = 2	Outputs	Tacc (m) = 4.0 ns	Tcyc – Tacc (m) – tisu = 2 ns ✔
	Tih = 1.5		Toh (m) = 1.5 ns	Toh – Tih (m) = 0 ns ✔

’C6711 vs. Micron’s MT58LC64K32D9-10 at 100 MHz

The MT58LC64K32D9 is a 64K x 32 device, which results in an addressable space of 256 KB.

This example uses the ‘C6711-150 running at its maximum clock speed of 150 MHz (P = 6.67 ns). Because the CPU speed is independent of the EMIF clock speed, we use an externally provided clock of 100 MHz for the synchronous memory interface, resulting in Tcyc = 10 ns.

The timing parameters of the MT58LC64K32D9-10 and the ‘C6711-150 can be summarized as follows:

‘C6711-150		MT58LC64K32D9-10		Tmargin
Outputs	Tdmax = 6.0 ns	Inputs	Tisu (m) = 2.2 ns	Tcyc – Tdmax – Tisu (m) = 1.8 ns ✔
	Tdmin = 1.5 ns		Tih (m) = 0.5 ns	Toh – Tih (m) = 1.0 ns ✔
Inputs	Tisu = 1.5	Outputs	Tacc (m) = 5.0 ns	Tcyc – Tacc (m) – tisu = 3.5 ns ✔
	Tih = 1.0		Toh (m) = 1.5 ns	Toh – Tih (m) = 0.5 ns ✔

Complete Example Using ’C6201B

This section walks through the register configuration for interfacing the ‘C6201B with SBSRAM at half speed. Because no SBSRAM parameters directly tie the EMIF settings to a specific SBSRAM, this software example is generic to any SBSRAM device.

If a single 32- or 36-bit-wide SBSRAM is used, the block diagram for the interface schematic is identical to that shown in Figure 1. If two 18-bit-wide devices are used in parallel, the schematic is identical to Figure 2.

Assumptions

- CLKOUT1 frequency of 200 MHz
- 100-MHz SBSRAM clock frequency (SSCLK = ½ x CLKOUT1 frequency)
- SBSRAM to be located at CE2 (logical address 0x02000000)
- CLKOUT1 is not used in the system.
- SDCLK, CLKOUT2 is used in the systems.

Register Configuration

Table 6. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, SSCEN, CLK1EN, CLK2EN, SSCRT
EMIF CE2 Space Control	MTYPE

EMIF Global Control Registers

Because the SBSRAM is driven by SSCLK, we must set the following:

Figure 22. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	1	0	1	0	0	1

SDCEN = 1	indicates that SDCLK is enabled to clock, assuming it is in use by the system
SSCEN = 1	Indicates that SSCLK is enabled because it drives the SBSRAM interface
CLK1EN = 0	Indicates that CLKOUT1 is disabled, assuming it is NOT in use by the system
CLK2EN = 1	Indicates that CLKOUT2 is enabled, assuming it is in use by the system
SSCRT = 0	Specifies a **half-rate** SBSRAM Interface

Thus, a valid setting for the EMIF global control register is 0x00003369.

For additional information on the remainder of the fields, see the TI *TMS320C6000 Peripherals Reference Guide*.

EMIF CE2 Space Control Register

Figure 23. EMIF CE2 Space Control Register Diagram

31–28	27–22	21–20	19–16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15–14	13–8	7	6–4	3–2	1–0
Rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	100	00	11

MTYPE = 100 indicates that 32-bit-wide SBSRAM is located in the CE2 address space. The other fields are irrelevant because they refer to asynchronous memory and SBSRAM is configured for this space.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF43.

Code Segment

The following code segment sets up the EMIF as described above using the TMS320C6000 Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Enable CLKOUT2,SDCLK, and SSCLK*/
/*                    - Disable CLKOUT1 */
/*                      - Set for ½x SBSRAM interface */
RESET_BIT(&g_ctrl, SSCRT);
SET_BIT(&g_ctrl, CLK2EN);
RESET_BIT(&g_ctrl, CLK1EN);
SET_BIT(&g_ctrl, SSCEN);
SET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SBSRAM  */
LOAD_FIELD(&ce2_ctrl  ,MTYPE_32SBSRAM, MTYPE , MTYPE_SZ       );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

References

TMS320C6201/6201B Digital Signal Processors Data Sheet, Literature Number SPRS051, Texas Instruments.

TMS320C6202 Fixed-Point Digital Signal Processor Data Sheet, Literature Number SPRS072, Texas Instruments.

TMS320C6211 Fixed-Point Digital Signal Processor Data Sheet, Literature Number SPRS073, Texas Instruments.

TMS320C6701 Floating-Point Digital Signal Processor Data Sheet, Literature Number SPRS067, Texas Instruments.

TMS320C6711 Floating-Point Digital Signal Processor Data Sheet, Literature Number SPRS088, Texas Instruments.

TMS320C6000 Peripherals Reference Guide, Literature number SPRU190, Texas Instruments.

TMS320C6000 Peripheral Support Library Programmers Reference, Literature number SPRU273, Texas Instruments.

MT58L128L32P Data Sheet, Micron Technology, Inc.

MT58L512L18D Data Sheet, Micron Technology, Inc.

MT58LC64K32D9 Data Sheet, Micron Technology, Inc.

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    - TI Number -800-800-1450
  - Korea 080-551-2804
  - Malaysia 1-800-800-011
    - TI Number -800-800-1450
  - New Zealand 000-911
    - TI Number -800-800-1450
  - Philippines 105-11
    - TI Number -800-800-1450
  - Singapore 800-0111-111
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