Application Report
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TMS320TCI100 Power Sequencing Requirements

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ABSTRACT

This application report describes the power sequencing requirements for all TCI100 devices with respect to the dependencies associated with reset, clock, and signal pins during power up. It also explains what to avoid and potential issues associated with power-up sequencing with respect to the external memory interface (EMIF) peripheral.

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1 Overview

This document describes:

- Why CLKIN and ECLKIN should be active when core power is ramping
- Why $\overline{\text{RESET}}$ should be low during power sequencing
- Behaviors associated with power sequencing I/O before core, and core before I/O
- Details on overall power ramp and device operation
- Details on how $\overline{\text{RESET}}$ is registered within device logic and EMIF

1.1 Scope

The *TMS320TCI100 Fixed-Point Digital Signal Processor Data Manual* (SPRS218) states that there are no requirements for specific power sequencing between core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time (>200 ms second) if the other supply is below the proper operating voltage. This document provides additional recommendations for power sequencing to ensure the device and EMIF peripheral come up in a known state and reset properly. This document also provides specific requirements for clocks during power supply sequencing.

2 Requirements for RESET During Power Sequencing

When power ramping, RESET is required to be in low state, (i.e, active). The RESET signal is not connected internally to the clock phased-locked loop (PLL) circuit, however, the PLL does have edge detect circuitry that can detect a high to low transition of RESET. The PLL may need up to 250 µs to stabilize the following device power up, device reset or after the PLL configuration has been changed. During the time the PLL is initializing, RESET must be asserted to ensure proper device operation. Holding RESET low during the time the device is ramping core power, CV_{DD} keeps the CPU from latching the PLL edges while the PLL is initializing. If RESET is high (not asserted) during the time the PLL is initializing, this could cause the TCI100 device to come up in an undefined state resulting in unknown and unspecified behavior.

Requirement When Reset is Controlled by External Logic CPLD or FPGA

If RESET is controlled by an inactive device during the time the TCI100 device is power ramping, a pulldown resistor should be added to the RESET signal to ensure the RESET is low until the signal is driven high.

Requirement When Using TI's Reset Supervisor

When using TI's ultra-low supply-current-voltage supervisory circuits TPS32xxXxx, the output RSTVDD is an open drain transistor that needs to be connected to a positive voltage to work correctly.

In this case, a pull-up resistor is required for correct operation. Since CLKIN is connected to the same 3.3 I/O voltage as the voltage supply (this is true 99.9%), the RSTVDD signal begins to drive active low as soon as the I/O voltage crosses 0.4 V. The RESET is active low well before CLKIN can activate when I/O reaches 3.3 V to drive PLL.

3 Clock Requirements During TCI100 Power Ramp

When CV_{DD} and DV_{DD} have powered up, CLKIN and ECLKIN (if external clock is used for EMIFA or EMIFB) are active. This ensures that the PLL starts to initialize and RESET starts to register throughout device logic and the peripherals.

The bootmode can select three different options for EMIF clock:

- CPU/4
- CPU/6
- External clock

Once the clock is selected, the EMIF will reset.

Note: If the external clock is selected, it must be active for the EMIF to reset.

3.1 Clock Output Enabling During EMIF Reset

On TCI100, the reset controller controls the output buffer of A/BECLKOUTx, ensuring that A/BECLKOUTx is in a high-impedance state during device reset. Glitches can occur on the A/BECLKOUTx output buffer during EMIF reset. Therefore, take care to ensure that glitches on A/BECLKOUTx do not cause issues for external devices connected to the EMIF during EMIF reset .

If the EMIF has synchronous dynamic random access memory (SDRAM) in any CEx space, it is suggested that your connect the SDRAM clock enable to RESET. This ensures A/BECLKOUTx is gated off anytime the device is in reset and coming out of reset, therefore, avoiding any issues caused by glitches on A/BECLKOUTx before SDRAM is properly initialized.

Figure 1 describes the activity on AECLKOUT1 while the EMIF is resetting. Time interval 2E is described in the data sheet as delay time (RESET low to ECLKOUT high impedance min 2E). During this time the AECLKOUT can be in an undefined state and thus glitch.

PCLK = internal PLL clock

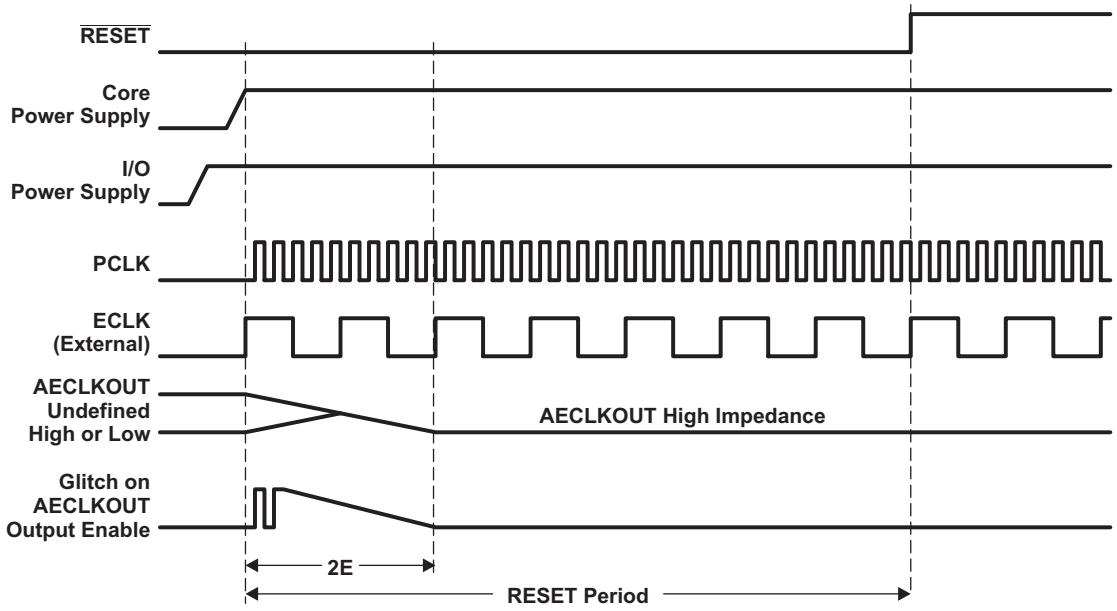

Figure 1. TCI100 EMIF RESET

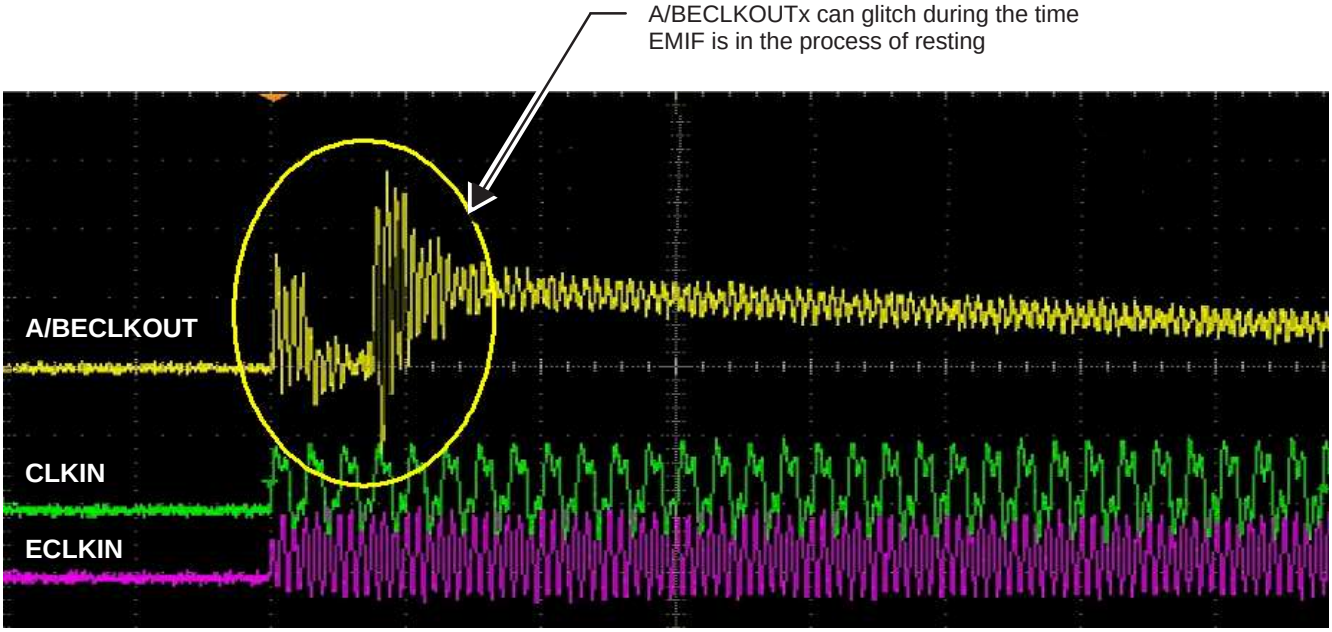

Figure 2. TCI100 EMIF Reset

4 Behaviors Associated With Power Sequencing

4.1 Power Sequencing I/O Before Core With Respect to EMIF I/O Buffers - (Not Recommended)

When power sequencing the device I/O before the core, the I/O buffers come up in an undefined state and have the potential to toggle until the core logic reaches 1.2 V. If the EMIF (`control\address\data\CLKOUT`) signals toggle during power ramping, while SDRAM is un-initialized, the SDRAM initialization specification is violated causing the SDRAM to come up in an undefined state. It is recommended to connect the SDRAM clock enable signal to the $\overline{\text{RESET}}$ signal. This gates off any activity on the EMIF I/O buffers from the SDRAM while I/O is active and the core is inactive, avoiding the possibility of violating the SDRAM initialization specification. Figure 3 shows the activity on the EMIF I/O buffers with respect to the power sequence I/O before core.

Sequencing the I/O before core in some applications may present an additional high current/peak in rush conditions and should be avoided, especially in multiprocessor application designs. For these reasons, it is strongly recommended to use a core before I/O sequence condition.

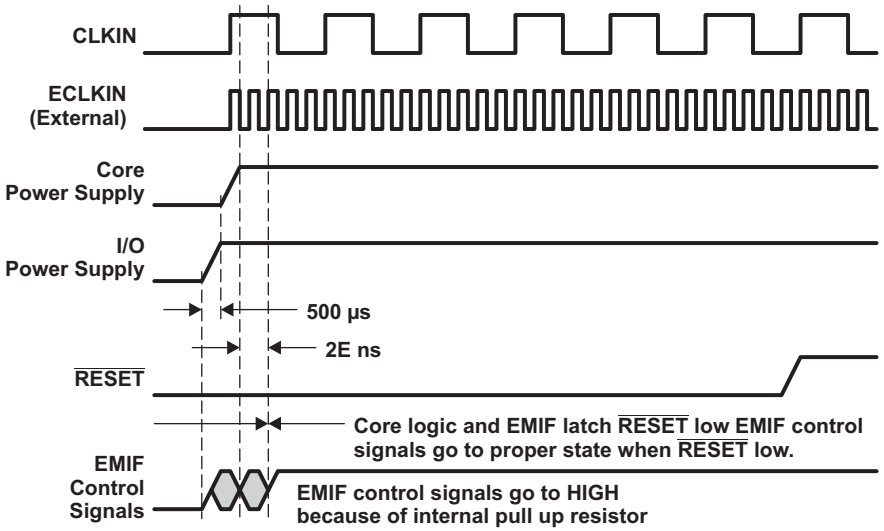

Figure 3. Before Core Power Sequence (*Not Recommended for New Designs*)

4.2 Power Sequencing Core Before I/O With Respect to EMIF I/O Buffers - (Recommended)

When power sequencing the device core before I/O, the I/O buffers are in an undefined state while the I/O is ramping from 0 V to 3.3 V and the EMIF is resetting. Once the I/O voltage reaches a valid voltage level and the EMIF registers reset, the EMIF buffers go to reset state. Since the toggling of I/O buffers only occurs while the I/O voltage is at an invalid level and SDRAM is ramping, the SDRAM initialization specification is never violated. It is also unlikely the glitch on AECLKOUT1 will cause any issues for the SDRAM while EMIF is resetting . Figure 4 shows the activity on the EMIF I/O buffers with respect to power sequence core before I/O, RESET, CLKIN, and ECLKIN.

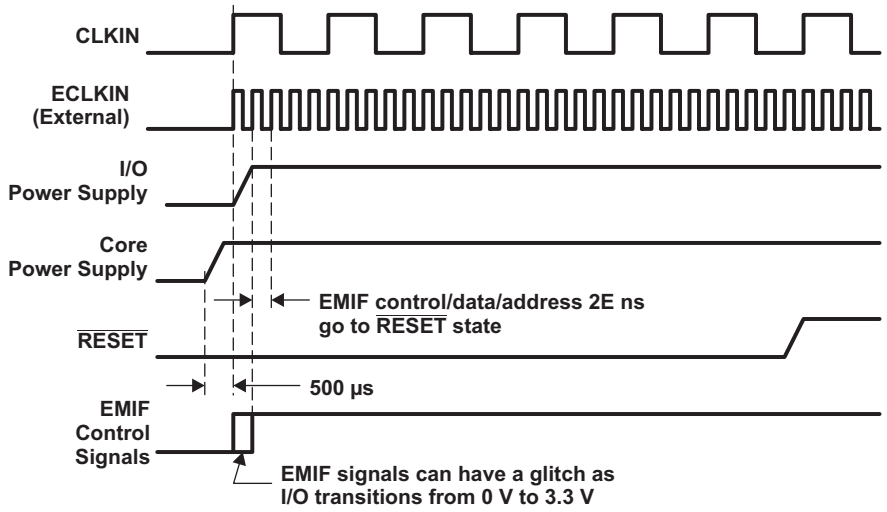

Figure 4. Core Before I/O Power Sequence

5 Details on How RESET Registers Within Core Logic

DSP core logic is synchronized to CLKIN, therefore, the device will not function without CLKIN active. To ensure RESET is registered by core logic, the core must be active (CV_{DD} = 1.2 V), RESET low, CLKIN active and the PLL has to be initialized. Once the PLL has been initialized, the following occurs:

- The device starts to clock internally
- RESET is registered throughout the device
- The bootmode is sampled and ECLKIN is selected
- If ECLKIN is selected for EMIF input clock and ECLKIN is active, RESET is registered within the EMIF logic

Note: If ECLKIN is selected and ECLKIN is not active the EMIF does not register RESET active.

- If I/O is active, RESET is latched by EMIF I/O input buffers

Note: During the time I/O is inactive or transmitting from 0 V to 3.3 V, the EMIF I/O buffers are in an undefined state

- EMIF control/address/data/CLKOUT goes to the active RESET state as defined in the device-specific data sheet.

If CLKIN is not active when core reaches CV_{DD} = 1.2V, the following will not happen:

- PLL initialization
- Device reset
- Bootmode register
- EMIF reset

6 Conclusion

To ensure the device comes out of reset properly and in a good state, you should follow the *recommended* information in this application report when power cycling the device. If the recommendation for power sequencing $\overline{\text{RESET}}$ and requirements for clocks are not followed, the device may come out of reset in an undefined state.

Proper power sequencing *within* the DSP is as important as *between* each DSP (multiprocessor application designs). During power sequencing, especially within multiprocessor designs, each end-use application should be individually evaluated for conditions that may cause excessive peak in rush currents.

It is strongly recommended that core come before I/O sequencing on all application designs to minimize this impact.

7 Reference Documents

1. *TMS320TCI100 Fixed-Point Digital Signal Processor Data Manual* (SPRS218)
2. *TMS320C6000 DSP Peripherals Overview Reference Guide* (SPRU190)

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