# AM62x (AMC) Escape Routing for PCB Design



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Introduction www.ti.com

#### 1 Introduction

The AM62x (AMC) is an extension of the low-power, low-cost Sitara Industrial/Auto grade family of processors. The AM62x (AMC) is based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options for a variety of embedded applications. The AM62x (AMC) is available in a 17.2-mm × 17.2-mm FBGA package with a 0.8-mm ball pitch. The package BGA design is built leveraging TI Flip Chip BGA Technology (FC-BGA) technology. This document is intended to provide a reference for escape routing on the AM62x (AMC) device. Care must be taken to route signals with special requirements such as DDR and high speed interfaces. Refer to the High-Speed Interface Layout Guidelines and DDR Routing Guidelines for more details. Details on Power Delivery Network are provided in AM62x PDN Application note and any routing and layout requirements specified in those documents supersede the generic requirements provided here.



# 2 Width/Spacing Proposal for Escapes

The AM62x (AMC) solution has been designed to support the following. AM62x (AMC) package supports similar feature set as several other competition solutions with approximately 15% smaller package area and ~10% wider line width. This solution reduces PCB foot print and utilizes lower cost PCB rules, enabling compact and low-cost systems.

Table 2-1. Width/Spacing Proposal for Escapes

PCB Feature	PCB Routing Requirements
Minimum via diameter	8 mils
Via hole size	8 mils
Minimum trace width/spacing required in the BGA breakout	3.2 mils / 3.7 mils
Number of layers used for escape	4 Layer
BGA land pad size	16 mils
Package Size	17.2 mm × 17.2 mm
PCB layers (signal routing, total) recommended	4, 8

Stackup Vision Www.ti.com

## 3 Stackup

PCB stack-up is one of the first and important considerations in realizing a successful PCB. The AM62x (AMC) device supports a BGA array or 21 × 21 with a 0.8-mm pitch and a body size of 17.2 mm. Due to the number of rows of signal balls around the periphery, TI recommends two signal routing layers. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, TI recommends allocating two layers for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as DDR, CSI, and USB require ground planes for impedance matching. Additionally, to meet the higher DDR interface speeds, ground layers both above and below the DDR signals are recommended. The escapes and routing on the AM62x (AMC) board design was achieved with 8 layers, as shown in Table 3-1.

Table 3-1. Example PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads, Ground and signal escapes
Layer 2	Ground
Layer 3	Signal Routing
Layer 4	Ground/Power
Layer 5	Power/Ground
Layer 6	Signal Routing
Layer 7	Ground
Layer 8	Bottom

An example 8-layer board stack-up for AM62x (AMC) is described above. This board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM62x (AMC) board is implemented without HDI (High Density Interconnect) and does not use micro vias, which are both intended to save board cost. All vias on the AM62x (AMC) board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis are performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

www.ti.com Via Sharing

## 4 Via Sharing

The FC-BGA pattern implemented on the AM62x (AMC) design offers several opportunities for via sharing. Vias are shared across BGA pins. Figure 4-1 and Figure 4-2 show the via sharing opportunities for VDD\_CORE and VSS power supplies respectively. Further opportunities for other power domains are illustrated in Figure 4-3. Via sharing across BGA pins provides for easier escape routing and also robust electrical connection by connecting multiple pins.

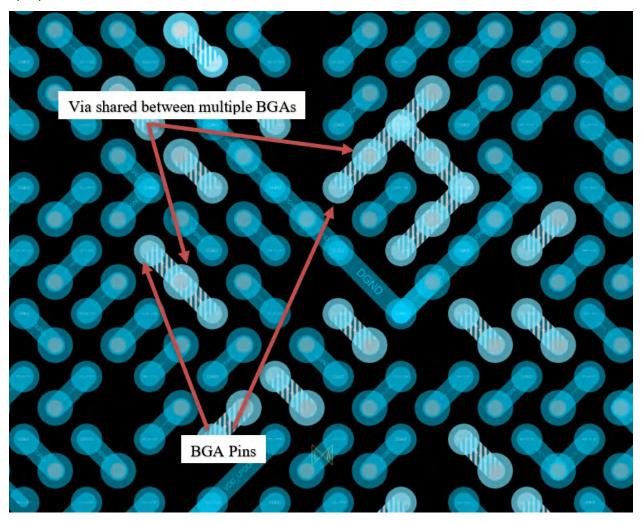


Figure 4-1. Via Sharing for VDD\_CORE Domain

Via Sharing w

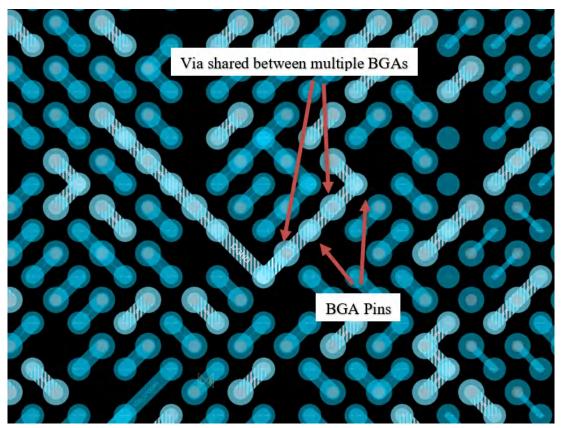


Figure 4-2. Via Sharing for VSS

www.ti.com Via Sharing

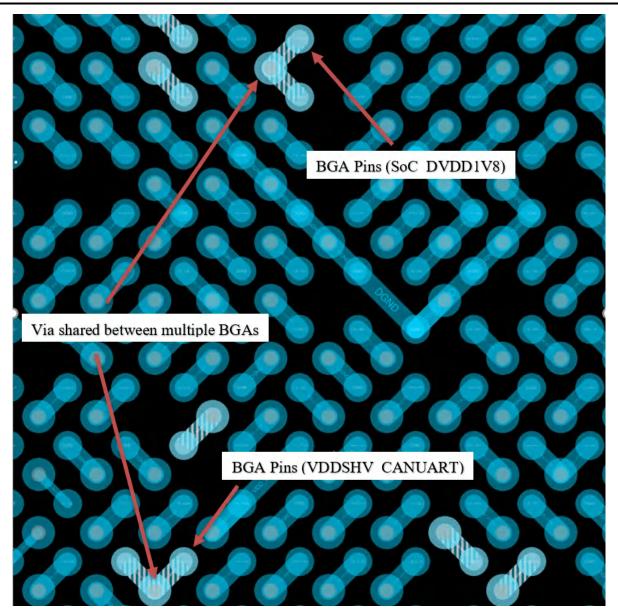


Figure 4-3. Via Sharing for Other Power Domains



## **5 Floorplan Component Placement**

Careful analysis is required to analyze the locations of the interfaces used on the device and the associated components and connectors. Optimum trace routing will have routes as short as possible with a minimum cross-over. The AM62x (AMC) offers interface selection flexibility through pin-mux choices. Pin-muxing enables a same interface function made available on multiple pins and is selectable through a pin mux option. Favorable pin-mux options that ease PCB routing and component placement can be fully utilized to further optimize the PCB design. Figure 5-1 shows the default arrangement of the signal balls as well as the power and ground balls. Priority is given to component placements without pin-mux options such as DDR, CSI, USB, OLDI/LVDS, and so forth.



Figure 5-1. AM62 (AMC) Floorplan



# **6 Critical Interfaces Impact Placement**

Placement of the AM62 device and some of the components or connectors is also dictated by some of the highest performance interfaces such as DDR, USB, and so forth. Additionally, due to the PCB losses at multigigabit rates, there are routing distance limits that may also limit component placement.

Routing Priority Superiority S

## 7 Routing Priority

As indicated earlier, critical interfaces affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interface with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established.

Table 7-1 lists a recommended priority order for interfaces contained on the AM62x (AMC) family of devices. Individual design requirements may drive a need for adjustment of the priorities but this serves as a good baseline and has been used for the board example illustrated in this document.

**Table 7-1. Routing Priority** 

Interface	Routing Priority
CSI	10 (Highest Priority)
DDR4/LPDDR4	9
OLDI	9
OSC	8
USB2, OSPI	8
Power distribution	7
RGMII	6
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog	3
GPMC	2
GPIO	1
UART / CANUART	1
I2C / Temp Diode	1 (Lowest Priority)

The multi-gigabit Camera Serial Interfaces (CSI) are the most critical due to their data rate and loss concerns. CSI is at the top of the priority list because it is sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the CSI connector and the AM62x (AMC) device. CSI signals are found on the outer layers of the BGA footprint allowing some of the CSI traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. Power distribution is often left to last, which can result in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.** 

www.ti.com SerDes Interfaces

#### 8 SerDes Interfaces

The package BGA ball map is also arranged to support routing the highest priority interfaces first. Therefore, the SerDes CSI interfaces are located close to the outer rings. The lanes located on the outermost row of BGAs can be escaped on the top layer. The lanes located on inner BGA rows require vias to escape as a differential pair on the bottom or on an interior layer. The BGA map facilitates this for inner rows. See Figure 8-1 for an example of the SerDes signals on the AM62x AMC board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing Serdes signals, refer to High-Speed Interface Layout Guidelines.

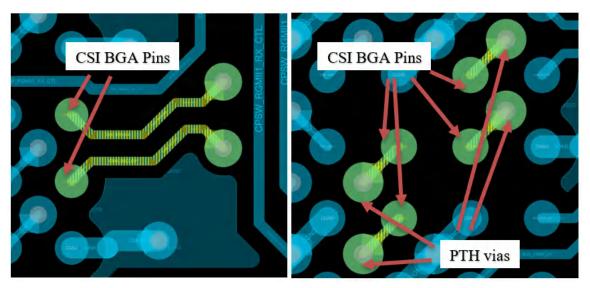


Figure 8-1. Serdes CSI Escapes for TOP layer (Left) and Inner layer (Right)

DDR Interfaces www.ti.com

### 9 DDR Interfaces

The AM62x (AMC) supports connection to either a DDR4 or LPDDR4 device. The DDR signals must be routed next. Refer to the DDR Routing Guidelines document for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR interface on the AM62x (AMC) Board. Routing for both DDR4 and LPDDR4 use a similar escape, with LPDDR4 requiring a lesser number of signals.

The DDR SDRAM memory devices are normally arranged so that the data group balls are closest to the AM62x (AMC) device. The Package BGA ball map has been planned to place the DDR address and command signals between data byte lane 1 and data byte lane0.

Figure 9-1 and Figure 9-2 illustrate how to escape the DDR byte lanes 0 and 1, respectively. The use of Plated Through Hole (PTH) vias make the routing of these signals between the SoC and SDRAM possible on any layer.

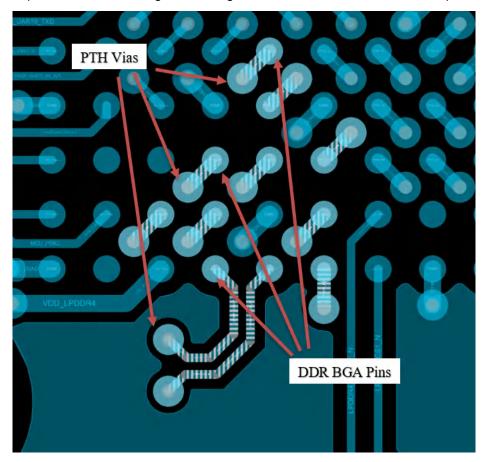


Figure 9-1. DDR Byte Lane0 Escape

www.ti.com DDR Interfaces

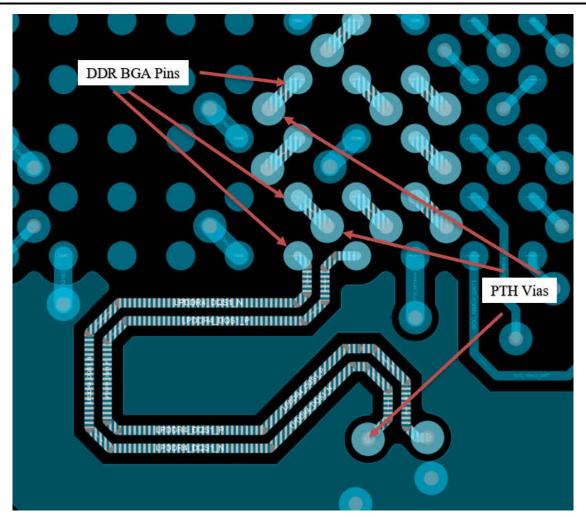


Figure 9-2. DDR Byte Lane1 Escape

The address, command, and clock signals are routed directly to the memory device.

The top and inner layers are used to escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually and must include the stub to the memory pad and all via lengths. Refer to the DDR Routing Guidelines document for detailed recommendations for DDR routing.

DDR Interfaces

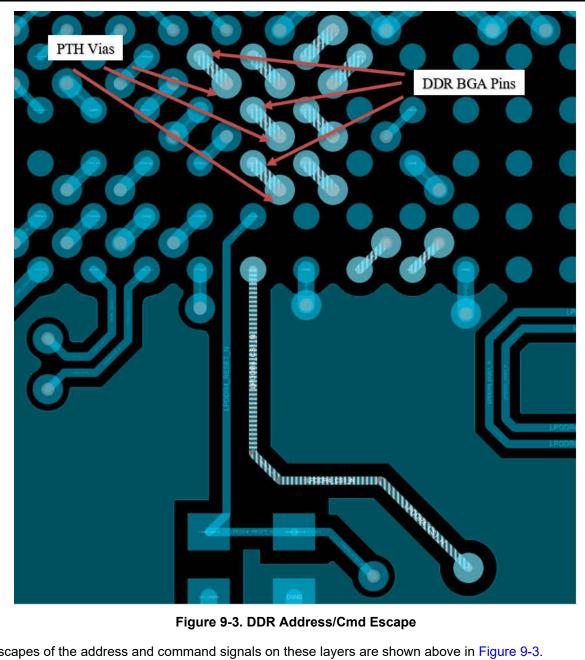


Figure 9-3. DDR Address/Cmd Escape

The escapes of the address and command signals on these layers are shown above in Figure 9-3.

Address signals were routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. It is required to have the same number of vias for each of the address and command signals. The use of Plated Through Hole (PTH) vias allows the flexibility of routing the address/cmd signals on any layer.

www.ti.com Power Decoupling

## 10 Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed next after the SerDes and DDR interfaces. TI recommends completing all SerDes and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SerDes and DDR routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation thus these may also need to be completed at this time.

Special care is needed for the 1-uF output capacitors connected to the CAP\_VDDS\* BGA pins on the AM62x (AMC) device. These capacitors should be placed as close to the pin as possible and a low inductance path should be present between the CAP\_VDDS BGA pin and the supply pad on the capacitor. The layout used on the CAP\_VDDS1, CAP\_VDDS3, and CAP\_VDDS6 nets on the AM62x (AMC) board is shown below in Figure 10-1. The sharing of the GND pad of the capacitors is with other capacitors in the vicinity, which allows saving routing resources. Also, keep the PTH vias for the capacitor power and GND pad connections as close to each other as possible to minimize the loop inductance.

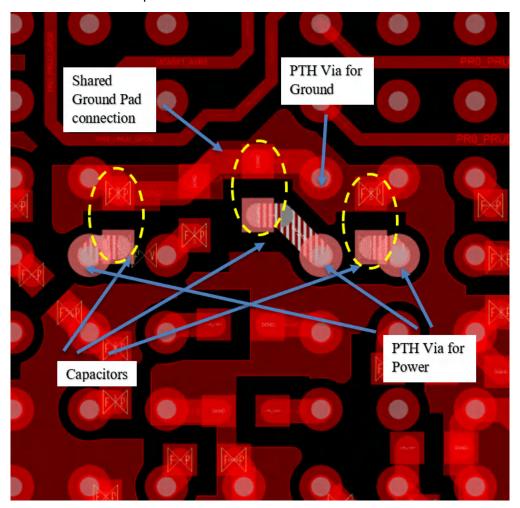


Figure 10-1. AM62 SK EVM Output Capacitor Placement for CAP\_VDDS0

This placement can be improved if the capacitors are placed directly under the SoC. The decoupling capacitors for the VDD\_CORE and VDDS\_DDR supplies should also receive the same priority as those on the CAP\_VDDS\* pins and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62x (AMC) device.



# 11 Route Lowest Priority Interfaces Last

When the length matching and simulations for high speed interfaces and DDR have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, the layout can continue with the medium and then the lower priority interfaces.

www.ti.com Summary

# 12 Summary

A picture with AM62x (AMC) with all signals and power escaped is shown in Figure 12-1.

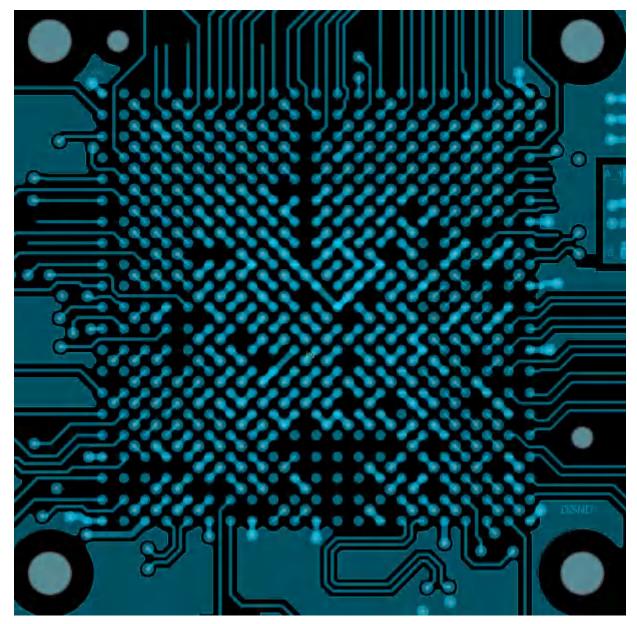


Figure 12-1. AM62x with Complete Signal and Power Escapes

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