User's Guide

AM62P, AM62P-Q1 Processor Family Schematic, Design Guidelines and Review Checklist

ABSTRACT

The user's guide for AM62Px (AM62P, AM62P-Q1) processor family includes custom board, schematic design guidelines, processor peripherals circuit implementation recommendations, and schematic review checklist for custom board designers using processor from any of the processor families. The user's guide includes information related to processor power, external clocks, GPIO configurations, processor peripherals supported and interfacing the processor peripherals to attached (external) devices. Schematic review checklist (included at the end of each section), provides a comprehensive list of review points for the peripheral described in the specific section. The recommendation for custom board designers is to review the custom board schematic design implementation using the provided review checklist (points) and verify the recommendations or guidelines in the checklist have been implemented (followed).

Additionally, links (including product page on TI.com) have been provided for processor product pages, processor related collaterals, FAQs related to processor and processor peripherals published on E2E, and commonly referenced documents during custom board design. The recommendation for the custom board designers is to refer to the added links during custom board design to minimize design errors, optimize the design efforts, possibly reduce board build iterations and optimize the project timeline.

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1 Introduction

1.1 User's Guide Usage Guidelines

The user's guide AM62Px (AM62P, AM62P-Q1) processor family specific, *Schematic Design Guidelines and Schematic Review Checklist* includes schematic design guidelines that can be used by custom board designers during the custom board schematic design phase. Schematic review checklist is included at the end of each section and can be used by custom board designers to review the custom board schematic once the design is complete and before start of the layout.

1.1.1 Custom Board Schematics Design Guidelines - References Used in the User's Guide

The user's guide includes schematic design guidelines and schematic review checklist that can be used by custom board designers during custom board schematics design for the selected processor and the peripherals implemented (on-board or carrier (or add-on)) including memory (DDR, flash), power, communication interfaces, IOs and other circuit sections.

In the user's guide, reference to *Processor* implies the selected AM62Px processor OPN and references to the *Attached devices* implies the external (on-board or carrier (or add-on)) peripherals that are interfaced to the processor (based on the target end equipment being designed and the application use case).

1.1.2 Processor Family-Specific User's Guide

The user's guide covers AM62P, AM62P-Q1 processor (GPNs). Each of the processor GPN can have multiple orderable part numbers. The user's guide includes schematic design guidelines and schematic review checklist that can be used during custom board design. Processor family-specific user's guide provides processor focused guidelines and checklist and helps custom board designers when designing the board for a specific processor family. The user's guide is simpler and is easy to use for the chosen processor and processor family (AM62Px in this case).

1.1.3 Schematic Design Guidelines

The user's guide provides schematic design guidelines that can be used during custom board schematic design phase to implement the circuit connections between the processor and peripherals supported by the selected processor. Links to relevant FAQs have been added (as part of the guideline in each section) in addition to the design guidelines. FAQs (links added) provide additional information on a specific peripheral or interface topic including description and details on the implementation/use case and learning from customer interactions.

The recommendation is for custom board designers to follow the schematic design guidelines to minimize design errors that can affect board functionality, performance and to optimize the custom board design/build/test efforts.

1.1.4 Schematic Review Checklist

Schematic review checklist that can be used by custom board designers to review the custom board schematic covering specific peripherals have been added at the end of each section, sub section of the user's guide.
The general recommendations, processor power and processor peripherals sections, sub sections described in the user's guide includes the checklist at the end. The schematic review checklist is categorized as *General*, *Schematic Review*, and *Additional*. Custom board designers can use the schematic review checklist to perform self-review of the custom board schematic design. Self-review minimizes possible schematics errors that can result in functional or performance related concerns and also reduced the reviewers efforts during formal reviews (internal or external). Schematic reviews minimizes the efforts required during custom board bring-up or performance testing resulting in increased board design quality and adherence to the planned timeline.

For information on available checklists and format, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

1.1.4.1 Common Checklist for Use With All Schematic Design Guidelines and Schematics Review Sections

1. Reviewed above section, including FAQ links and relevant application notes on TI.com.
2. Reviewed pin attributes and signal description sections in the processor-specific data sheet.
3. Reviewed timing and switching characteristics section, and any additional information available in the processor-specific data sheet.

1.1.4.1.1 Custom Board Schematic Design Implementation Checklist Sub-Sections Description

The schematic implementation review checklist includes 3 sub-sections:

General:

The general section lists (summarizes) the circuit implementations in bullets that are required (expected) to support the functionality for the peripheral section described above the checklist section (design guidelines section). The section also include care abouts to be considered when the section is interfaced or connected to another section to implement the required peripheral or module functionality (does not require circuit implementation). The recommendation is to review and close the list of implementation checks provided before continuing with the schematic review.

Schematic Review:

The schematic review section lists (summarizes) the circuit implementations in bullets that are required (expected) to be added by the custom board designers for the circuit section to support the functionality including the values, connections and other implementations to be followed for implementing the peripheral or module. The recommendation is to compare for the custom board schematic design implementation with the schematic checklist to make sure the implementation follows the design guidelines before the start of the layout.

Additional:

The additional section lists (details) the implementation and use case description in bullets that can be used by custom board designers along with the schematic review section to understand the circuit implementation rationale (need to implement) before considering optimizing the circuit design.

1.1.5 FAQ Reference for User's Guide Usage During Schematic Self-review

The below FAQ includes guidelines for custom board designers to perform a self-review using the available processor-specific collaterals:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Custom Board Schematics Self Review

1.2 AM62Px [AMH] Processor Family List of Processors

The user's guide applies to all the processors listed below. All relevant documents for the selected processor are available on the product pages on TI.com. The recommendation is to follow the product page link listed below to view the relevant product page.

See the *Ordering and Quality* section for information on the OPNs on the following product pages:

- AM62P
- AM62P-Q1

1.3 Updates to Schematics Design Guidelines and Schematics Review Checklist

As part of efforts for continuous improvement of the collaterals, there can be changes or addition of sections to the *Schematics Design Guidelines and Schematics Review Checklist* user's guide with respect to the current revision published on TI.com (based on customer feedback, learnings, addition/enhancement of sections, errors or improvements) that are updated during the next document revision.

The below FAQ lists the changes customer board designers are required to follow during custom board schematic design (before the release of the revised user's guide on TI.com):

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design - Updates to Hardware Design Considerations and Schematic Design Guidelines collaterals

The recommendation is to review the FAQ for possible updates frequently during all phases of the custom board design.

2 Related Collaterals

2.1 Links to Commonly Referenced Collaterals During Custom Board Schematic Design

A number of documents relevant to the selected processor (family) are available on the processor-specific product page on TI.com. The recommendation for custom board designers is to read the relevant collateral (listed in the below FAQs) before starting the custom board design.

The following FAQ summarizes some of the key collaterals that can be referred, when starting the custom board design:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – Collaterals to Get started

2.2 Hardware Design Considerations for Custom Board Design User's Guide

During the custom board design phase, the recommendation is to read, review and follow the applicable recommendations in the processor-specific *Hardware Design Considerations for Custom Board Design* user's guide linked below:

Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family

3 Processor-Specific Information

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

3.1 Selection of Processor OPN (Orderable Part Number)

Selection of the processor OPN (based on the required features) is a critical and important phase during custom board design. To get an overview of the processor family (AM62P, AM62P-Q1) architecture and for selecting the required processor OPN (processor used on the custom board) based on the required functionalities and features, package (AMH) and speed grade, see the *Functional Block Diagram*, *Device Comparison*, *Device Naming Convention*, *Device Speed Grades* and *Packaging Information* sections of the processor-specific data sheet.

The recommendation is to update the schematics with the selected processor OPN.

For information on the supported (available) packages for AM62Px processor family, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A / AM62D-Q1 / AM62P / AM62L Custom board hardware design - Available Device Packages

3.2 Processor-specific Data Sheet Use Case and Version Referenced for User's Guide Edits

Processor-specific data sheet includes:

1. Pin attributes (ball number, pin to muxed function mapping).
2. Signal descriptions.
3. Pin connectivity requirements.
4. Electrical characteristics, timing and switching characteristics, and timing diagrams for the applicable processor peripherals.
5. Recommended operating conditions for the processor supply rails.
6. Sequencing for the processor supply rails (Power-up and Power-down).
7. Maximum operating conditions and Recommended operating condition.
8. Detailed Description of the processor internal structure.
9. Applications, Implementation, and Layout.
10. Device and Documentation Support including Device Nomenclature (Device Naming Convention), Tools and Software.
11. Revision History.
12. Mechanical, Packaging, and Orderable Information.

Processor-specific data sheet with revision number referenced (during user's guide edits):

SPRSP89B – DECEMBER 2023 – REVISED AUGUST 2025 (AM62Px Sitara Processors data sheet (Rev. B))

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Current Data sheet revision, updates, revision backup and usage notes

3.3 Peripheral Instance Naming Convention - Data Sheet and TRM

For naming of peripherals and available number of peripheral instances, the processor-specific TRM tends to be *generic* and the processor-specific data sheet is *specific* (includes the number of supported instances). The recommendation is to always refer to the processor-specific data sheet for the supported peripherals and peripheral instances.

A suffix number is assigned to the peripheral name, in the processor-specific data sheet signal naming, even when there is a single peripheral instance. The suffix starts with *0*.

For the common platform Ethernet switch 3-port gigabit (CPSW3G0) port names, port 0 is the internal (communications port programming interface (CPPI) host) port of the switch.

3.4 Processor Peripherals and IO Connection When Not Used

During the custom board design, some of the processor peripherals are not be used (unused). Processor peripherals (including peripherals that have a dedicated function) have specific connectivity requirements when not used. Refer to the *Pin Connectivity Requirements* section of processor-specific data sheet for connecting the peripherals when not used. The connectivity requirements section includes recommendations for connecting the supply rails and the interface signals.

Processor GPIOs (muxed with peripherals, SDIO or LVCMOS buffer type) that support configuration of alternate functions (muxed), can be left unconnected when not used (in case there are no connectivity requirements specified). The pad configurations for the peripherals and IOs can be the reset state.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries

3.5 Ordering and Quality Information for AM62Px Processor Family

For information related to ordering and quality for the selected processor, see the links below:

AM62P-Ordering and quality

AM62P-Q1-Ordering and quality

3.6 Checklist for Selection of Required Processor GPN (Generic Part Number) and OPN (Ordering Part Number)

General

During the custom board schematic design process, review and verify the following collaterals and information:

1. Availability of commonly used memory interfaces, high-speed communication, on-board synchronous and asynchronous communication interfaces, camera and display interfaces.
2. On-board debug and diagnostics support (JTAG, UART, OBSCLK[1:0] and CLKOUT0).
3. Number of supply rails required, recommended operating conditions for supply rails, power-up and power-down sequence for core, memory interface, analog and IO supplies.
4. Electrical characteristics and timing information for the selected peripheral.
5. Availability of application notes, peripherals interface circuit implementation recommendations or examples, and layout guidelines.
6. Silicon errata related to processor functioning, boot modes (supported and care abouts, workarounds for the configured boot mode) and the peripherals of interest.
7. Availability of SK for evaluation and design files for reference and/or reuse.

4 Processor Power Architecture

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

For an overview of TI power management portfolio, see the TI *Power management* page.

WEBENCH® circuit designer tool provides a visual interface that can be used to create customized power architecture.

4.1 Generating Processor-Specific and Peripherals (Attached Device) Supply Rails

The required supply rails for the selected processor and attached devices can be generated using integrated (using PMIC, discrete DC/DCs, discrete LDOs) or discrete (using DC/DCs, discrete LDOs) power architecture.

PMIC (integrated power architecture) are designed for a specific processor or processor family. Use of PMIC simplifies power architecture (power supply rails) design. The PMIC generates the commonly required (used) processor and the attached device supplies. The PMIC internally manages power-up sequencing, power-down sequencing, supply slew rate control, optional residual voltage (voltage decay) detection and meets the processor-specific power (PDN) requirements. Additional discrete DC/DCs and discrete LDOs can used to generate the other on-board supplies (based on the use case) required based on the use case.

Use of discrete power architecture provides flexibility in selection of power devices and power architecture design. The design efforts can increase since the custom board designers are responsible for selection of discrete DC/DCs and LDOs that sources the required load current, DC/DCs and LDOs that can be adjusted or configured to generate the required supply voltages, DC/DCs and LDOs that can support the required load current transient, controls, supply slew rate and supports configuring the required supply sequencing.

Processor power supply rails have slew rate requirements specified. The recommendation is to follow the *Power Supply Slew Rate Requirement* section of processor-specific data sheet for the supply rails (generated or switched).

The family of power converters (DC/DCs and LDOs) products and related collaterals that can be used for implementing the on-board supplies using PMIC or discrete power architecture are summarized in the below sections:

4.1.1 AM62P, AM62P-Q1 Processor Family Power Architecture

4.1.1.1 Power Management IC (PMIC) Based Power Architecture

The recommended PMICs for integrated power architecture includes TPS65224-Q1. Space, performance, and BOM (bill of materials) optimized power architecture can be designed using PMICs to power the processor and the attached devices.

The PMIC generates commonly used (required) supply rails for the AM62P, AM62P-Q1 processors and attached devices. PMIC OPNs (NVM configurations) are added based on the use case. nRSTOUT0 output of the PMIC goes high after the supplies ramp + the recommended MCU_PORz reset input delay time.

Note

For automotive functional safety use cases, the recommendation is to connect MCU_I2C0 interface of the processor to PMIC (TPS65224 / TPS65222) I2C1 interface.

For PMIC based power architecture implementation (without functional safety), refer to the *Starter Kit SK-AM62P-LP* schematic.

For more information, see the *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs* application brief.

See the following FAQs:

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 Design Recommendations / Custom board hardware design – common queries for PMIC TPS65224-Q1

[FAQ] TMUX1308-Q1: EN and Control inputs termination - AM62P, AM62A use case

For information related to residual voltage and detection, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage, Detection and supply decay

4.1.1.1.1 PMIC Based Power Architecture Checklist for TPS65224x

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. PMIC selection (OPN) and configuration of the output voltages
3. PMIC checklist for addition of required input and output capacitors including values, feedback connection, and pin connection
4. Voltage rating of the selected capacitors considering derating
5. Configuration of the recommended PMIC control and IO signals
6. Connection of the required control signals for processor IO supply sequencing and slew rate control
7. Processor I2C instance used to interface to PMIC
8. Provision to configure processor core voltage
9. Processor to PMIC and PMIC to processor IO interface connections
10. Connection of analog inputs to TPS65224 PMIC ADC inputs
11. Naming of the supply rails (indicate configured output voltage level)
12. Net name matches (same name) for processor and attached devices IO supplies
13. Connection of interrupt, EN/PB/VSESNSE, sleep signals and connection of the required pulls for the PMIC IOs

Schematic Review

Follow the below list for the custom schematic design:

1. Configuration of the PMIC output to match the processor and attached devices IO supply operating voltages as per the custom board requirements
2. The custom board PMIC implementation with the SK schematic implementation for capacitors quantity, size and values, IOs connection
3. Connection of the PMIC buck output feedback (tie the feedback after the output bulk capacitors or remote feedback)
4. Core voltage configuration using GPIO3 (GPIO3 High -- BUCK1,2 : 0.85V, GPIO3 Low/Floating -- BUCK1,2 : 0.75V), Connection and sequencing of VDD_CORE and VDDR_CORE
5. Provision to configure processor core voltage (using GPIO3 for TPS65224)
6. PMIC nRSTOUT0 slew (pullup value) when connected directly to processor MCU_PORz input (recommend using a discrete push-pull output type buffer)
7. Connection of the required control signals for processor IO supply sequencing (load switch EN for processor and attached device IO supply voltage and provision for load switch output voltage slew rate control using external capacitor)
8. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline)
9. Matching of the PMIC output voltage level with the supply requirements for the processor and attached devices (based on the OPN)
10. Processor I2C instance used to interface to PMIC (Follow SK or review the required I2C instance based on the use case)
11. Configuration of discrete DC/DC outputs and LDOs used along with the PMIC to generate additional supply rails
12. External implementation of SD card supply switching and power switch reset logic to support UHS-I SD card
13. Connection of analog inputs and analog input range for GPIO4 or GPIO5 (used as ADC)
14. External LDO implementation for generating VPP supply (eFuse programming), LDO output enable (EN) control, addition of bulk and decoupling capacitors considering load current transient and provision for isolation resistor for testing the VPP supply output enable timing

Additional

1. In case custom board design power architecture is based on TI PMIC, the recommendation is to obtain a detailed review of the implementation done with the PMIC team (business unit or product line).

2. A 0Ω resistor or jumper is recommended at the output of the PMIC and discrete DC/DC, LDO for isolation or current measurement for the initial board build. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection for connecting TPs to 0Ω resistor or jumper.
3. The recommendation is to connect the feedback for the PMIC buck output after the bulk capacitor. The recommendation is to connect the feedback to make sure the removal of the 0Ω resistor does not affect the PMIC operation (connect on the PMIC side of the resistor). PMIC supports connecting remote feedback near to the load.
4. The recommendation is to show the PMIC input bulk capacitors for buck (DC/DC) inputs and VSYS separately and near to each of the pin for ease of placement and routing.
5. To support PMIC remote voltage sensing, the recommendation is to connect the feedback pins FB_Bx of the device to the respective sense pins on the processor. Alternatively, connect the FB_Bx pin to a representative load capacitor. With differential feedback, also connect the negative feedback pin to the negative terminal of the same load capacitor.
6. The recommendation is to review and follow the FAQs related to residual voltage.
7. In case a non-TI PMIC is used, the recommendation for custom board designers is to review and follow the relevant processor collaterals including the processor-specific data sheet and *Maximum Current Ratings* application note. The recommendation is to review the *Recommended Operating Conditions*, *Supply Slew Rate Requirements*, *MCU_PORz Timing Requirements*, *Power-Up Sequencing and Power-Down Sequencing* sections of the processor-specific data sheet and confirm the selected PMIC based power architecture supports the above requirements and residual voltage (RV) check.

4.1.1.1.2 Additional References

For information, see the following section in the processor-specific data sheet.

- Device Connection and Layout Fundamentals
- Power Supply
- Power Supply Designs

4.1.1.2 Discrete Power Devices (DC/DC, LDO) Based Power Architecture

To generate the processor and the attached devices supply rails a Discrete power architecture can be considered.

The power architecture can be based on discrete DC-DC converters and LDOs.

For information related to available or recommended discrete power architecture, see the processor-specific (*AM62P*, *AM62P-Q1*) product page on TI.com.

Processor-specific product page provides the updated information on the available power architecture.

When a custom (TI or Non-TI) discrete power architecture is implemented, take note of the supplies sizing (current rating), supplies sequencing, supplies slew rate control and MCU_PORz input L->H delay (hold time) (for oscillator start-up and stabilization) requirements after all the supplies ramp. The recommendation is to verify the above listed requirements as per the processor-specific data sheet are followed.

During supply rail power-down (power off), the recommendation is for the MCU_PORz input to reach a valid logic low level before the supplies begin to ramp down. The discrete power architecture is recommended to be designed to be able to turn off all supply rails and monitor the power rails decay to less than 300mV before initiating a new power-up sequence anytime any of the supply rail drops below the minimum value defined in *Recommended Operating Conditions*.

MCU_PORz input is recommended (required) to be held low (active) during power-up until all the processor supplies ramp and are valid (stable) plus minimum delay of 9.5ms (mentioned as 9500000ns in processor-specific data sheet) for internal oscillator to start-up and stabilize (when using external crystal plus internal oscillator, see the processor-specific data sheet) or MCU_PORz input is held low (active) until all the processor supplies ramp and are valid and external oscillator clock output is stable (when using external LVCMOS digital clock source (oscillator)) plus minimum delay of 1.2µs (mentioned as 1200ns in processor-specific data sheet) (see the processor-specific data sheet).

The recommendation is to consider the *Maximum Current Ratings* application note for supply sizing.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Discrete power Architecture

4.1.1.2.1 Discrete DC/DCs

The recommendation is to consider discrete DC/DC such as the TPS62826 or LM61460-Q1 or similar switching power devices.

For an overview of the available discrete DC/DC (Buck) switching devices, see the *AC/DC & DC/DC converters (integrated FET)* page.

Additionally, refer the following document and video library:

Quick Reference Guide To TI Buck Switching DC/DC Application Note

Power Supply Design training resources - Video library

4.1.1.2.2 Discrete LDOs

The recommendation is to consider discrete LDO devices such as TPS74518, TLV7103318, TLV75518 or similar LDOs.

For an overview of the available discrete LDOs, see the TI *Linear and low-dropout (LDO) regulators* page.

Additionally, refer below application notes:

Low Dropout Regulators Quick Reference Guide

Linear Regulator Design Guide For LDOs

A Topical Index of TI LDO Application Notes

4.1.1.2.3 Discrete Power Devices (DC/DC, LDO) Based Power Architecture Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. The configured output voltage level and the current sizing (rating) for the supply rails.
3. Output voltage feedback connection and feedback resistor divider tolerance.
4. Selected discrete DC/DC supports active discharge.
5. Discrete DC/DC output slew rate meets the processor requirements.
6. Sequencing of the supply rails as per the processor requirements.
7. MCU_PORz input (DC/DC PG output) slew rate.
8. Voltage rating of the selected capacitors considering derating.
9. Implementation of SD card interface IO supply supporting UHS-I SD card.
10. Implementation of VPP (eFuse programming) supply.
11. Naming of the supply rails.
12. Matching of the Discrete DC/DC or Discrete LDO voltage levels.
13. Net name matches (same name) for processor and attached devices IO supplies.

Schematic Review

Follow the list below for the custom schematic design:

1. The resistor divider value including tolerance connected to the feedback to generate the required output supply voltage matches with the calculated value for discrete DC/DC or LDO.
2. DC/DC or LDO outputs current sizing.
3. Discrete DC/DC or LDO PG outputs have the required pullup and connects to other DC/DC or LDO EN for supply sequencing.
4. DC/DC or LDO outputs slew rate matches the processor slew rate requirements.

5. MCU_PORz input (DC/DC PG output) slew rate (connect through discrete push-pull output type buffer) and L to H delay (MCU_PORz input low hold time for clock start-up and stabilization) implementation after all the processor supplies ramp.
6. MCU_PORz input low hold time after supplies ramp, in case the DC/DC PG output connects directly to the processor MCU_PORz input.
7. Implementation of VPP (eFuse programming) supply including capacitors to support load current transients and output enable (EN).
8. Implementation of LDO for SD card interface IO supply for supporting UHS-I SD card.
9. Naming of the supply rails (indicate configured output voltage).
10. Matching of the Discrete DC/DC or Discrete LDO voltage levels with the supply requirements for the processor and attached devices.
11. Voltage rating of the selected capacitors considering derating (> twice the worst-case applied voltage is a commonly used guideline).
12. Discrete power device selection including output supply voltage rails (operating voltage/amplitude) and current rating, active discharge, provision to enable, slew rate control, residual voltage detection (Allow to power-up only when the supply voltages are < 300mV after power-down).

Additional

1. In case custom board design power architecture is based on TI power, the recommendation is to obtain a detailed review of the implementation with the relevant business unit or product line.
2. A 0Ω resistor or jumper is recommended at the output of the discrete DC/DC, LDO for isolation or current measurement for the initial board build. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection for connecting TPs to 0Ω resistor or jumper.
3. The recommendation is to add a zener at the output of discrete DC/DC or discrete LDO when adjustable output type discrete DC/DC or discrete LDO are used.

4.2 Processor Power Rails Supply Control, Sequencing and Supply Overload Protection

4.2.1 Load Switch (Processor Supply Rail Power Switching)

Load switches are used to switch and sequence the processor and attached devices supply rails. Load switches are used to control (turn on and off) power to a specific peripheral or sub-system referenced to (powered by) the same input supply rail, instead of using multiple discrete DC/DCs or LDOs to generate the supply. In some applications, there is a recommended power-up and power-down sequence that is recommended to be followed. Load switches simplifies the implementation of power sequencing to meet the power-up and power-down sequence timing requirements. The load switch enable can controlled by the PMIC or discrete DC/DC PG output to meet the processor power sequencing requirements.

Consider load switches such as TPS22965, TPS22918, TPS22902, and TPS22946.

For an overview of the available load switch families, see the TI *load switches* page.

4.2.1.1 Load Switch (Processor Supply Rail Power Switching) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Load switch current rating.
3. Connection and sequencing of the load switch enable.
4. Output voltage slew rate control configuration.
5. Voltage rating of the selected capacitors considering derating.

Schematic review

Follow the below list for the custom schematic design:

1. Input and output capacitor values, ratio as per the data sheet and capacitor voltage rating.
2. Output voltage slew rate is configured (capacitor value selection) as per the processor IO supply slew rate requirements.

4.2.2 eFuse IC (Power Switching and Protection)

On the custom board design, an eFuse can be used at the supply input for protection. eFuse power switching and protection ICs are integrated power path protection devices that are used to limit circuit current and voltages to a safe level during fault conditions. eFuses offer a number of benefits to the design and include protection features that are often difficult to implement with discrete components. For an overview of the available eFuse families, see the TI *eFuses and hot swap controllers* page.

5 General Recommendations

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

The below sections include general recommendations that are recommended to be followed before the start of the custom design. The section also includes general recommendations while using the SK collaterals as reference (including schematics) and during design of custom board schematics.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on processor core, VDD_CORE, VDDR_CORE, VPP and other core supplies

5.1 Processor Performance Evaluation Module (SK - Starter Kit)

Processor (hardware) performance evaluation modules and platforms (SKs) are not reference designs. The modules and platforms do not represent proper or complete board or end equipment function implementation. In some cases, the SKs are partially or completely designed and released for fabrication before the processor design is complete. The time line is such that the hardware platform is available when the first silicon is available. New (additional) processor requirements come up during processor bring-up and bench validation. All the new requirements are not accounted for in the SK (hardware evaluation platform). Therefore, TI expects custom board designers to carefully review and follow all requirements defined in the processor-specific data sheet, silicon errata, hardware design considerations user's guide, schematic design guidelines and TRM when designing custom boards.

Processor (hardware) performance evaluation platforms are not designed to be comprehensive of any custom board or end equipment specific requirements, such as EMI or EMC (Electro Magnetic Interference, Electro Magnetic Compatibility tests including radiated susceptibility, radiated emissions, ESD), noise susceptibility, thermal management, and so forth.

For design update notes that custom board designers can refer along with the SK schematics, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

5.1.1 Evaluation Module (Starter Kit) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.

2. SK being referenced (followed) matches with the selected processor family and OPN.
3. Processor package on the referenced SK board matches with the processor selected for custom board design.
4. The SK schematic revision referenced includes D-Notes, R-Notes, and CAD Notes.

5.2 Processor-Specific SK Versus Data Sheet

During the design phase of custom board design, in case any discrepancy is seen between the processor-specific SK and processor-specific data sheet during processor evaluation or custom board design, the recommendation is to follow the processor-specific data sheet. Despite the best efforts by the SK designer, the SK schematic can have errors that still function but are not completely aligned with the processor-specific data sheet specifications.

5.2.1 Notes About Component Selection

Note

Component values, package size and voltage rating in the SK schematics are being provided as starting point for the custom board designer and are not always optimized. The recommendation for custom board designer is to validate if the values, size and voltage rating are appropriate for the specific custom board implementation and make the required updates.

The recommendation is to review the SK BOM with respect to the custom board design requirements and optimize the components based on the processor-specific data sheet recommendations, application requirements, custom board design methodology being followed and available (company specific or generic) design or component selection guidelines.

The recommendation is to perform design calculations for the circuit implementation, perform board level tests and measurements, conduct internal design reviews before finalizing the components (value, package, voltage ratings and power ratings).

5.2.1.1 Series Resistor

Provision for a series resistor (0Ω) on the processor IOs interfaces is recommended based on the use case. The values for the series resistor used in the SK schematics can be used as a starting point for custom board designs. The recommendation for custom board designers is to verify the values on the custom board and adjust accordingly (step function that occurs on the pin is not near the mid-supply). Simulation as required is recommended to finalize the values.

5.2.1.2 Parallel Pull Resistor

Note

There is no firm rule or requirement for external pull unless the pull requirements are defined in an industry standard. Industry standard definition for pulls is the main reason we can make firm recommendations for external pulls on the eMMC and SD card signals. For the other peripherals, the recommendation is for customers to evaluate the function of the attached devices connected to every processor signal on the custom board and apply appropriate technical/engineering judgment to determine the need to have external pulls that prevent any input from floating when attached device input buffer is turned on. The recommendations provided in the design guide are generic and customer is expected to review the design requirements and the availability of pulls internal to the attached device before implementing. Be sure to not provide an external pull in contention with an internal pull. Example: An example is adding an external pull that is in contention with the internal pull (internal to the attached device), such that the contention creates a mid-supply potential on the signal (input).

The recommendation is to provide provision for parallel pulls to the processor IOs that has a trace connected and not being driven actively or for the IOs connected to the attached device inputs that can float (to prevent the attached device inputs from floating until the host software configures the IO). Parallel pull polarity and pull value depends on the specific peripheral connectivity recommendations, recommendations for improved processor performance and reliability, and relevant interface or interface standards requirements. The recommendations for pullups are provided.

Pull values used in processor-specific SK can be used as a starting point and custom board designer can select the appropriate pull values based on the recommendations for the processor and attached device, or specific board design requirements.10kΩ or 47kΩ (choice of pullup allowed to standardize the component selection and BOM) pull value is recommended for IOs or interfaces that do not have specific recommendations. The pull value can be chosen based on the board design to optimize the use of components or reduce current or improve noise performance.

When a trace is connected to the processor pins (IO pads) and the IOs are not being actively driven (floating), a parallel pull (47kΩ) is recommended. Processor IO buffers are (TX (Output) and RX (Input) are disabled during and after reset and internal pulls (pullup and pulldown)) turned off during reset and after reset. The IOs are in a high impedance state, effectively behaving as an antenna that can pick up noise. Without a parallel pull, the IOs are in high impedance state. High impedance makes noise to couple energy easily on the floating signal trace and develop a potential that can exceed the IO recommended operating conditions. The potential creates an electrical over-stress (EOS) on the IOs. Electrostatic discharge (ESD) protection circuits internal to the processor were designed to only protect the device from ESD during handling before being installed on a PCB.

5.2.1.3 Drive Strength Configuration

The AM62P, AM62P-Q1 processor family currently does not support configuring drive strength (any other available configuration) besides the nominal (default) value (Example: drive strength for SDIO or LVCMOS buffers). The nominal (40Ω for SDIO and 60Ω for LVCMOS) value is the only configuration at which processor-level STA (Static Timing Analysis) is closed. The AM62P, AM62P-Q1 processor family implements eMMC (dedicated) hard macro PHY and the nominal impedance is set to 50Ω for the MMC0 IOs. The IBIS model has been currently updated to contain only the drive strengths where the timing has been closed internally.

For information related to drive strength configuration support, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Drive Strength Configuration for SDIO and LVCMOS I/Os

5.2.1.4 Processor-specific Data Sheet Recommendations

Custom board designers are responsible for implementing the required or recommended circuits to make sure the custom board design follows the processor-specific data sheet pin connectivity requirements. Example: Requirements for I2C Open-Drain Electrical Characteristics - Input Slew Rate limit requirements when pulled to 3.3V supply.

In case processor-specific data sheet recommendations are not available, the recommendation is to follow the schematic design guidelines or to follow the SK schematic implementation as a starting point.

5.2.1.5 Processor IOs Protection - Provision for External ESD Protection Devices

An external ESD protection is recommended for the processor IOs that are connected directly to external inputs or connected to external connector. Internal ESD protection were not designed to handle the board level ESD requirements. For an overview of the ESD protection devices, see the TI *ESD protection* page.

5.2.1.6 Peripheral Clock Outputs Series Resistor

Series resistor (22Ω) on the clock outputs are recommended to be added near to the processor clock output (for MCSPI, MCASP) pins since the clock is also being used for retiming. The series resistor additionally supports possible reflection control (signal distortion).

For MMC0, MMC1, MMC2, OSPI0, GPMC0 interfaces, an unbonded pad is used (internal) for retiming (loopback). We do not use the same clock that is sent across the PCB to the attached device for our capture clock. We branch the output clock into two paths inside the device, where the clock is sent to two separate IO cells. One IO cell is connected to a package ball, which is used to source a clock to the attached device. The other IO cell is unbounded (not connected to any package ball). The clock used as the receive capture clock is sent out through the unbonded IO cell and looped back into the device before being used as the capture clock. We do this so the clock has the same delay that is inserted on the clock going out to the attached device and the same delay that is inserted on the data coming back in from the attached device. The unbonded IO cell pad never experiences the voltage step that is produced on the source end of a PCB signal trace. A low value series resistor (0Ω to start) is recommended (provisioned) to control possible signal reflections (signal integrity purpose).

5.2.1.7 Peripheral Clock Outputs Pulldown Resistor

A pulldown is recommended on peripherals clock outputs (eMMC, SDIO, SD card, OSPI0, MCSPI, MCASP, GPMC0) connected to the attached device near to the clock input of the attached device. Optionally capacitor (8 to10pF) can be provisioned and configured as no populate. The capacitor can be mounted in case issues related to board level signal integrity is observed. The recommendation is to connect the capacitor to the attached device clock input with shortest stub.

5.2.1.8 Component Selection Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Selection of resistors value, tolerance, size and wattage.
3. Some specific resistors have ±1% tolerance requirements (refer to the processor or attached device data sheet, SK schematics, or EVMs).
4. Standard tolerance resistors can be used for other use cases, Example: pullup, pulldown, LED current limit, attached device address configuration or series resistor.
5. The recommendation is to compare the pull values implementation on the custom board with the SK schematic.
6. Voltage rating of the capacitors used includes derating (for non-polarized capacitors, > x2 the worst case applied voltage is a commonly used guideline).
7. DC bias effect considered while choosing the voltage rating of capacitors (to be within the recommended value) for CAP_VDDSn.
8. Package selection (application and use case dependent, consider voltage and temperature range).
9. Selection of compatible attached devices (DDR and flash memory, EPHY (EPHy)).
10. Selection of required memory size (DDR) and providing provision for expanding the memory as required.
11. Reviewed the FAQs related to passive components value, tolerance and voltage rating.

As a starting point for information on key components used on the EVMs and SKs, component values and tolerances, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

5.2.2 Additional Information Regarding SK Design (Schematic, Board) and Reuse

5.2.2.1 Updated SK Schematic With Design, Review and CAD Notes Added

During custom board design, as part of the custom board design process, the custom board designers can (tend to) reuse the SK design (CAD files) and make the required edits. Alternatively, custom board designers can reuse the common circuit implementations (sections), including processor, memory, power and high-speed communication interfaces. Since the SK design is expected to have additional functions, custom board designers tend to optimize the SK schematic design as per the custom board requirements. While optimizing the SK schematics, errors can be introduced into the custom board design that can affect functionality, performance or reliability of the custom board. When optimizing the SK schematics, custom board designers can have queries related to the SK circuit implementation. Common design and optimization errors across multiple custom board designs were observed during the schematics review and during custom board debugs. Based on the customer queries, customer inputs, internal suggestions, and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) have been added near each section of the SK schematic for custom board designers to review and follow (implement the recommendations to minimize board design errors).

The available downloadable design documents are listed in the below product overview document:

5.2.2.1.1 AM62P, AM62P-Q1 Processor Family

SK-AM62P-LP Design Package Folder and Files List Product Overview

5.2.2.2 SK Design Files Reuse for Custom Board Design

Based on the design approach being followed during the custom board design and project timeline, the SK design files can be used as a starting point to make the required updates (changes as per the custom board requirements). The recommendation is to review the SK schematic design before implementation. The recommendation is to review the component selection for size, tolerance and voltage rating as per the custom board functional and performance requirements.

The following FAQ includes the PDF schematic and additional information related to starter kit SK-AM62P-LP:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design - Reusing TI SK (EVM) design files

5.2.2.2.1 SK Design Files Reuse for Custom Board Design - Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Latest version of the selected or required SK design files (collaterals) are being referenced.
3. D-Notes and R-Notes added close to the schematic sections have been reviewed and considered.
4. Resetting of circuit components mounting option configuration (DNI configuration is reset, all components are shown as populate) when saved as a different project or the schematic pages or circuit sections are rearranged.
5. Changes in circuit connections (connection missing) including off-page connections when the schematics design is translated to an alternate CAD tool.

5.2.3 SK Schematic Pages Sequencing (Based on Functions, Reuse) and SK Board Layout

For the SK schematics revisions that are currently being released or in works (to be released in the future), TI is arranging (sequencing) the schematics pages in a modular format for ease of reuse. The schematic pages flow starts with required pages including processor power supplies generation, processor supplies and peripheral connections, attached devices circuit implementation. Optional debug and monitoring sections are added after the required pages. The arrangement helps custom board designers to delete the schematic sections that are not used during the custom board design.

The SK board design implementation is a flat architecture with the processor and the attached devices integrated on the same board. Custom board designers can follow the SK implementation when designing flat architecture custom board. In case the customer board architecture is SOM (System on Module) and Carrier board, the board layout approach (signal routing requirements), recommendations can change. The recommendation is for customer to verify the below guidelines and also follow general SOM design and layout guidelines to address board level signal integrity concerns:

1. Signal connections (high speed, differential signals) between the SOM and the Carrier board (including polarity)
2. Selection of high speed connector (lower contact resistance and inductance) that does not affect the board functionality or performance when high speed signals transition between the boards
3. Provision for adequate number of ground pads between signals on the connectors are provided to shield the signals to optimize board performance (minimize issues related to signal integrity)
4. The recommended or required terminations for memory and other high speed or low speed peripherals have been provided

5. Fail-safe operation requirements between SOM and the Carrier board signals have been addressed
6. Completeness of the circuit implementation connected across SOM and Carrier board
7. IO level compatibility between the SOM and Carrier board signals
8. Any of the processor IOs or attached device IOs interfaced to the processor that can float has provision for parallel pull and the polarity has been verified
9. The required simulations have been performed before start of board build (SOM and Carrier)

For additional input on high-speed design including SOM based design, refer below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

5.3 Processor-Specific SDK

In case the custom board design is for a new platform or updates being made for a platform, the recommendation is to use the latest Version/ Revision of the software development tools on TI.com.

Refer below link to download the required SDK version:

PROCESSOR-SDK-AM62P

1. ***MCU-PLUS-SDK-AM62P:*** MCU+ SDK for AM62P – RTOS, No-RTOS
2. ***PROCESSOR-SDK-LINUX-AM62P:*** Processor SDK Linux for AM62P

Refer to *AM62P Software Build Sheet* (Build Sheet of supported features for AM62Px processor family).

In case an older Version/Revision is being used, the recommendation is to verify the compatibility using the release notes or reach out to TI (through E2E).

5.4 General Design Recommendations (to Know) Before Starting the Custom Board Design

5.4.1 Processor Documentation

During the custom board design phase, the recommendation is to refer/use the latest version of the collaterals/ documentation, examples include the processor-specific data sheet, silicon errata, TRM, and other commonly referenced board design collaterals. Review the processor-specific product page on TI.com at frequent interval and look for latest available document revision or addition of new documents.

Tips for documentation search: Search the documentation for words such as: *recommended*, *require*, *do not*, *note*, *pin connectivity*, and so forth. Important criteria for the processor typically contain one or more words.

Tips to get updated information: On a TI.com processor product page, there is a ***Notifications*** **button**. Registering at the button enables automatic notification of processor documentation changes.

The latest revision of the processor-specific data sheet or other collaterals are available on TI.com. The recommendation is to archive the older revision internally for future use.

5.4.2 Processor Pin Attributes (Pinout) Verification

Verify the following attributes for the processor pins used in the custom board design:

- Processor pin number labeling and naming (pin number associated with the processor symbol section) corresponds to the correct pin numbers listed in the *Pin Attributes* section of the processor-specific data sheet. The recommendation is to maintain the processor-specific data sheet names internal to the symbol and change the function (net) names as per the application use case.
- Supply voltages that are connected to the processor power pins follow the *Recommended Operating Conditions*.
- All processor pins (grouped into functions and having separate symbol block) including reserved pins are included in the schematics to minimize tool related and functional errors.
- A number of processor IOs TX (Output) and RX (Input) buffers are disabled and internal pulls (pullup and pulldown) are turned off during reset and after reset. External pulls (10kΩ or 47kΩ) are recommended to hold any attached device in a valid state until software initializes the IOs trace is connected and IOs are not being

actively driven. When a TP is connected to the processor IO, a parallel pull (47kΩ) is recommended. When adding pull is not feasible, the recommendation is to route the traces away from high frequency signals.

- For improved custom board performance, consider provisioning for external measurement of processor supply rails (voltage), current draw for the supply rails and on-board temperature measurement at hot spots.

For queries related to processor-specific data sheet pin attributes, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SOC data sheet Pin Attributes Excel format

5.4.3 Device Comparison, IOSET and Voltage Conflict

Availability of features listed in the comparison table are a function of shared IO pins, where IO signals associated with a number of the features are multiplexed to a limited number of pins. The recommendation is to use SysConfig-PinMux tool to assign signal functions to pins. The SysConfig-PinMux tool provides a better understanding of limitations associated with pin multiplexing.

Processor peripherals are timing closed using the IOs grouped as IOSETs. IOSETs are grouping of signals specific to an interface that are timing closed as a set. Any interface that has IOSETs is recommended to select all interface signals from the same IOSET. Some interface signals can be shared over multiple IOSETs. The valid combinations of pins for an IOSET supporting a specific peripheral are detailed in the SysConfig-PinMux tool.

Voltage Conflict:

Signals are grouped by functional IO domain, not by power domain. There is a possibility to encounter voltage conflict warnings with some peripheral IO configuration. The warning is to highlight difference between the preferred voltage and the configured voltage for IOs so custom board designer can take necessary action in case there is a real voltage conflict. The warning is most useful when grouping GPIO signals from different voltage domains since the current tool configuration only allows one preferred voltage per peripheral. Any peripheral that includes IOs (pins) with different voltages levels, a warning is shown. The warning is shown because the preferred voltage is a different level than the IO (pin) voltage (Example: Preferred voltage is 3.3V while the pin voltage is 1.8V). The warning can be suppressed as long as 1.8V is the intended voltage for selected IOs (pins). The indication of conflict is not a hardware issue or a tool bug, but a notification that the preferred voltage is different than IO (pin) voltage configured. The warning are there simply to highlight the conflict between preferred operating voltage and selected (configured) operating voltage. A long as you understand the reason for the conflict, the warnings can be suppressed.

For information on voltage conflict and IOSET, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to SysConfig-PinMux IOSET and Voltage Conflict

5.4.4 RSVD Reserved Pins (Signals)

Pins named RSVD are Reserved. The recommendation is to leave the RSVD pins unconnected (no test points (TPs)) as recommended in the processor-specific data sheet.

The recommendation is to leave the RSVD pins unconnected (do not connect any PCB trace or test point).

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Connection recommendations for RSVD pins

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

5.4.5 Note on PADCONFIG Registers

A number of the processor IOs (LVCMOS or SDIO buffer type) support multiplexing of multiple (different) functions on the same pin. The required IO function can be chosen from the supported multiple functions. The list of functions available for each IO (pad) is listed in the *SIGNAL NAME* column in the *Pin Attributes* table of the processor-specific data sheet.

The required function is configured using the MUXMODE field of the relevant (associated) pad configuration register. The PADCFG_CTRL0_CFG0_PADCONFIG0 to PADCFG_CTRL0_CFG0_PADCONFIG150 registers support (can be used) the signal multiplexing of the IOs in the processor MAIN domain and MCU_PADCFG_CTRL0_CFG0_PADCONFIG0 to MCU_PADCFG_CTRL0_CFG0_PADCONFIG33 registers support (can be used) the signal multiplexing of the IOs in the processor MCU domain.

The *Description in the Pad Configuration Register Bits* table in *Pad Configuration Register Functional Description* subsection of the *Pad Configuration Registers* section of the processor-specific TRM summarizes the *Bit Field* description, supported configurations and the *Reset Values* for the PADCONFIG registers. The recommendation is to review and follow the notes listed at the end of the table while configuring the PADCONFIG registers. The recommendation is to not (never) set the RXACTIVE bit without a valid logic input being sourced to the pin that is associated with the respective PADCONFIG register. A floating input can damage the processor IO or affect the reliability of the processor. ST_EN bit is set by default. The recommendation is to verify the ST_EN bit and set the bit to 1 in case the bit value has been reset to 0. The recommendation is to not modify the default value of the bit. A summary of all the PADCONFIG registers default configuration is listed in the *Pad Configuration PADCONFIG Registers* table in the *Pad Configuration PADCONFIG Registers* subsection of *Pad Configuration Registers* section of the processor-specific TRM.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on PADCONFIG bits and PADCONFIG registers default values summary

5.4.6 Processor IO (Signal) Isolation for Fail-Safe Operation

The recommendation is to power the processor IO supply for IO group and the attached device (or FPGA or MCU or Processor) IO supply to the same power source to make sure there are no violations related to fail-safe operation. In case the processor and the attached devices or an additional processor are connected to (powered by) different power sources, signal isolation is recommended since many of the processor IOs are not fail-safe. The recommendation is to connect the signals through a FET bus switch circuit designed to isolate the two devices anytime the IO power is not valid for the device connected as input. The FET bus switch and control logic are recommended to be powered from an always-on power supply and only enabled by an AND function of power good signals from multiple (different) power sources.

5.4.7 Pin Connectivity Requirements and Reference to Processor-Specific SK

The *Signal Description* and *Pin Connectivity Requirements* sections of processor-specific data sheet includes connection recommendations for peripherals, IOs and pins (functions) specific to processor family.

The processor-specific SK can be referenced when the processor-specific data sheet does not include specific connection requirements.

5.4.8 Custom Board High-Speed Interface Design Guidelines

For recommendations on USB2.0 and CSI-RX signals connection and routing, see the *High-Speed Interface Layout Guidelines*. The recommendation is to include appropriate constraints or notes related to the routing requirements to be followed during the custom board design.

For USB interface, adding common-mode is an option to improve the custom board USB interface noise immunity performance when the custom board is expected to operate in harsh industrial environments. Adding common-mode choke can reduce the signal amplitude and degrade USB interface performance (speed, data throughput, communication errors). The recommendation is to add provision to bypass the common-mode choke using 0Ω resistors. The recommendation is to add provision for external ESD protection for the USB interface and USB supply based on the application requirement.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

5.4.9 Recommendation for LVCMOS (GPIO) Output Current Source or Current Sink

The DC current outputs sourced by the processor IO configured as output needs to remain less than the maximum I_{OH} and I_{OL} values defined to achieve the V_{OL} maximum and V_{OH} minimum values defined in the *Electrical Characteristics* table. The output currents defined in the processor-specific data sheet shall not be used as limits for steady-state currents. The data sheet output current limits are only expected to be reached when charging or discharging signal capacitance to transition a signal from low to high or from high to low. Once the signal reaches a valid logic state, the steady-state current is expected to be much lower than the data sheet current limit values. The outputs can tolerate some level of steady-state current as required to over-drive typical pull resistors, but we do not expect large steady-state current like what is needed to drive an LED or similar load continuously. The recommendation is to use an external FET or transistor switch controlled by processor IO to drive LEDs or similar loads that can draw continuous current.

5.4.10 Connection of Slow Ramp Signal (Input) or Capacitor Load (Output) to Processor IOs

LVCMOS (SDIO) inputs have slew rate requirements specified (as part of the electrical specifications). Connecting slow ramp input (signal) directly to the LVCMOS (SDIO) inputs is not recommended. There can be long-term reliability issues (concerns) associate with the input buffer if the applied input (signal) spends more time in the voltage region between V_{IHSS} and V_{ILSS}. The transition time allowed (recommended) is <1000ns. The slew rate has frequency dependency. A maximum slew of 1000ns is recommended when the signals toggle rate is not high (non-frequency dependent limit). When IO is operating at 1.8V (as an example), the non-frequency dependent limit of 1.8E+6V/s becomes the larger value when the signal toggle rate is < 100kHz. The frequency dependent limit of 18fV/s (f = toggle frequency of the input signal in Hz) becomes the larger value when the signal toggle rates is >100kHz. When a slow ramp input is applied (when the input is at mid-supply), shoot-through current can flow from VDD through the partially turned on P-channel transistor and the partially turned on N-channel transistor to VSS. Accumulated exposure to slow ramp input results in IO performance, board performance or processor reliability concerns.

Connecting a large capacitor directly at the LVCMOS (SDIO) outputs is not recommended. LVCMOS (SDIO) output buffers are not designed to drive large capacitive loads. When LVCMOS (SDIO) type IOs are configured as output and a capacitor is connected at the output, the recommendation is to follow the processor-specific data sheet recommendations for the allowed capacitor value or add series resistor to limit the IO current draw. The recommendation is to perform simulations to finalize the capacitor value.

5.4.11 Processor and Processor Peripherals Design Related Queries During Custom Board Design

During the custom board design, there can be questions (queries) related to processor and processor peripherals. The recommendation is to start an E2E query for queries related to processor and processor peripherals, for the device experts to support. The recommendation is to include queries related to a specific section of the design or peripheral or specific topic in an E2E query to minimize assignment and response delay.

5.4.12 General Design Recommendations (to Know) Before Starting the Custom Board Design Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Latest version of the selected SK design is referenced.
3. Refer to the relevant collaterals on TI.com to minimize design errors (design efforts).
4. Processor schematics symbol used on custom board schematic follows the ball name, pin numbers and IOSET grouping recommendations for specific peripherals as per the processor-specific data sheet *Pin Attributes* section.
5. The required IO functions and required PADCONFIG configurations are considered.
6. Buffering of the processor IOs (outputs, based on the use case) - to drive higher load.
7. Fail-safe operation and output capacitor load requirements for processor IOs are considered.
8. The recommendation is to frequently check the product page on TI.com for the latest documents revision (for the documents of interest).
9. The recommendation is to use E2E (to seek clarification rather than making assumptions).

5.4.13 Attached Devices Recommendations

TI does not make attached devices recommendations for custom board design.

The recommendation is to refer the *DDR Electrical Characteristics* section of the processor-specific data sheet for selection of LPDDR4 memory.

The MMCSD host controller and PHY associated with the MMC0 are designed to be compliant with the standard, as described in the processor-specific data sheet (and TRM). The recommendation is to refer the *MMC0 - eMMC Interface* section of the processor-specific data sheet when selecting the eMMC.

During the custom board design, as a starting point for information on key devices (components) used on the EVMs and SKs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

6 Processor-Specific Recommendations for Power, Clock, Reset, Boot and Debug

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Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

6.1 Common (Processor Start-Up) Connections

6.1.1 Power Supply

When selecting or designing the processor power architecture, the recommendation is to consider the below listed guidelines:

- The current (power) requirement for each of the supply rail varies based on the interfaces used and the operating environment.
- The current draw of processor supply rails is estimated using the *Power Estimation Tool (PET)* for a specific use case.
- If the supply rail powers the other on-board attached (peripheral) devices, include the maximum current draw of the attached devices for sizing the supply rail.
- For power supply sizing the recommendation is to consider the maximum current for the processor supply rails. For information on the maximum current rating for different supply rails, the recommendation is to frequently check processor (AM62P / AM62P-Q1) product page.
- The recommendation is to verify the output current ratings of the selected power architecture (including PMIC, discrete DC/DCs and discrete LDOs) meet the maximum current ratings of the selected processor and attached devices. The recommendation is to add additional margins for design or manufacturing variances.
- The recommendation is to verify if the power supply sequence (power-up and power-down) and supplies slew rate follows the processor-specific data sheet. For the recommended power sequencing requirements, refer to the *Power Supply Sequencing* section of processor-specific data sheet.

For more information about processor *Recommended Operating Conditions (ROC)*, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition

Below are some guidelines to consider when selecting or designing the processor power architecture:

1. Supply rails are configured to the required operating voltage level and the supply outputs are within the processor ROC.
2. Power architecture follows the power-up and power-down sequence as specified in the processor-specific data sheet.
3. Power architecture meets the slew rate requirements specified for the supply rails in the processor-specific data sheet.
4. All the power supplies ramp-up and are stable before the MCU_PORz input is released (deasserted).
5. The delay between the processor power supplies ramp up and the MCU_PORz input high follows the processor-specific data sheet recommendations (9.5ms min).
6. The recommendation is to make sure the supplies are enabled only when the supply voltages ramp-down below 300mV (no residual voltage) during cold reset.
7. All the supply rails decay below 300mV (There is no time or decay voltage tolerance associated with the requirement) before any of the power rail is allowed to ramp up after a power cycle.
8. MCU_PORz input slew is minimum to avoid internal reset circuit glitch (the recommendation is to connect the MCU_PORz input through discrete push-pull output type buffer with minimum slew).

For information on residual voltage and detection, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Residual Voltage, Detection and supply decay

Note

Read the note at the start of *Pin Connectivity Requirements* section of the processor-specific data sheet for connecting the supply rails and processor signals named RSVD.

6.1.1.1 Core and Peripherals Supplies

For proper operation, the recommendation is to connect all power supply pins (balls) with the supply voltages recommended in the *Recommended Operating Conditions* section of the processor-specific data sheet. Power supply pins that have specific connectivity requirements are listed in the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Note

Powering MCU domain and MAIN domain independently is not a supported option. The processor family does not support (implement) separate MCU and MAIN power supply domains. All power supply pins (rails) are required to be powered and are recommended to follow the supply sequence as defined in the processor-specific data sheet. The concept of MCU and MAIN applies to internal functions and processor domains.

Note

Refer below section *Supply Connection for Partial IO (Low Power) Mode Configuration* of user's guide for VDD_CANUART supply connection.

Processor core supply VDD_CORE and peripheral core supplies VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 are recommended to be powered from the same power source and can be configured for 0.75V or 0.85V operation (specified nominal operating voltage as per the *Recommended Operating Conditions* (ROC)). When processor core and peripheral core supplies are operating at 0.75V, the recommendation is to ramp 0.75V supply before 0.85V supply.

Peripheral core supplies for MMC0, VDD_MMC0 (pin 1K3, renamed as VDDR_CORE from SR1.2) and VDDA_0P85_DLL_MMC0 (pin 1J1, named as VDDR_CORE from SR1.2) are specified to operate at 0.85V (in case MMC0 interface (eMMC) is used or not used).

The recommendation is to connect VDD_MMC0 and VDDA_0P85_DLL_MMC0 to the same power source as VDDR_CORE (from SR1.2). The supply changes have been made to enhance AM62Px eMMC interface speed performance.

There is update to the *Pin Connectivity Requirements* in the latest revision of the processor-specific data sheet for MMC0 interface. Recommend reviewing the *Pin Connectivity Requirements* for MMC0 (eMMC) interface and following the same for the MMC0 power and signals.

In case MMC0 (eMMC) interface is not used on the current custom board design, VDD_CORE is configured for 0.75V and each of the balls (VDD_MMC0 (1K3), VDDA_0P85_DLL_MMC0 (1J1)) are connected to the same power source as VDD_CORE, the recommendation is to provide provision to connect VDD_MMC0, VDDA_0P85_DLL_MMC0 (both pins renamed as VDDR_CORE) to 0.85V (VDDR_CORE) to make the design compatible to use processor silicon revision from SR1.2.

VDDR_CORE is specified to operate at 0.85V. When VDD_CORE is operating at 0.85V, the recommendation is to ramp VDD_CORE and VDDR_CORE together (powered from the same source).

The recommendation is to always connect VDDS_OSC0 and VDDA_MCU supplies.

The processor family supports multiple analog supply pins that provides power supply to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x = 0-4], VDDA_1P8_CSI_DSI and VDDA_1P8_OLDI0. Filtered (ferrite) power supplies are recommended.

Connection of VDDA_1P8_USB (filtered) and VDDA_3P3_USB to a 3.3V analog supply for supporting USB2.0 interface is recommended.

Note

The below updates VDD_MMC0, VDDA_0P85_DLL_MMC0 (both pins renamed as VDDR_CORE) have been made in the below data sheet:

SPRSP89B – DECEMBER 2023 – REVISED AUGUST 2025 (AM62Px Sitara Processors data sheet (Rev. B))

For more information, see the *Recommended Operating Conditions* and *Power Supply Sequencing* sections of the processor-specific data sheet.

For more information on eMMC memory interface HS400 support, see the following FAQ:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – Power supply connection and Board layout recommendations to support HS400

6.1.1.1.1 Power Supply Ramp (Slew Rate) Requirement and Dynamic Voltage Scaling

The recommendation for all processor power supplies is to allow for controlled supply ramp (follow supply slew requirements). For more information, see the *Power Supply Slew Rate Requirements* section of the processor-specific data sheet.

The processor (family) does not support dynamic voltage scaling (change) for processor core, peripherals core and peripheral analog supplies.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling for SOC core (VDD_CORE), Peripheral Core and Analog supplies

6.1.1.1.2 Additional Information

For information on processor power-sequencing requirements, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Processor power-sequencing requirements for power-up and power-down

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

For information on processor power supply rails filtering using ferrite, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

6.1.1.1.3 Processor Core and Peripheral Core Power Supply Checklist

General

1. Review Section 1.1.4.1 of the user's guide.
2. Connection of processor core VDD_CORE and peripheral core VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 supply rails.
3. VDD_MMC0 (pin 1K3, renamed as VDDR_CORE from SR1.2) and VDDA_0P85_DLL_MMC0 (pin 1J1, named as VDDR_CORE from SR1.2) supply rail.
4. ROC, slew rate and voltage sequence requirements for processor core and peripheral core supply rails.
5. Connection of VDD_CORE and VDDR_CORE when VDD_CORE supply is 0.75V or 0.85V.
6. Connection of VDD_MMC0 and VDDA_0P85_DLL_MMC0.
7. Peripheral core supply filters.
8. Connection of core supply when specific peripherals are not used.
9. Connection of peripherals core supply VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK (CSIRX0 and DSITX0) when peripheral is not used but the boundary scan function is required.

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to compare the implementation of the bulk and decoupling capacitors for the supply rails with SK schematic implementation or refer PDN application note.
2. The supply rail operating voltage connected to processor core supplies follows the ROC.
3. Recommended supply voltage 0.75V or 0.85V is applied to the processor core VDD_CORE and peripheral core VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 supply rails operating voltage.
4. VDD_MMC0 (pin 1K3, will be renamed as VDDR_CORE from SR1.2) and VDDA_0P85_DLL_MMC0 (pin 1J1, will be named as VDDR_CORE from SR1.2) supply rail operating voltage supported is a fixed 0.85V
5. Connection of VDD_MMC0 and VDDA_0P85_DLL_MMC0 to the same source that is sourcing the VDDR_CORE.
6. Processor core and peripheral core supply rails connected to the relevant supply pins follow the recommended voltage sequence. Refer *Power-Up Sequencing – Supply / Signal Assignments* section of the processor-specific data sheet for sequencing the core supplies when, partial IO low power mode is used and when partial IO low power mode is not used.
7. Slew rate of the supply rail follows the data sheet requirements.
8. The potential applied to VDDR_CORE never exceeds the potential applied to VDD_CORE +0.18V during power-up or power-down. The sequencing requires VDD_CORE to ramp up before VDDR_CORE and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V.
9. The recommendation is to power VDD_CORE and VDDR_CORE from the same source when the VDD_CORE is operating at 0.85V.
10. Ferrite filters are provided for peripheral core supplies (CSI_DSI, USB, CANUART) as per the SK schematic implementation.
11. Connection of core supplies VDDA_CORE_CSI_DSI VDDA_CORE_DSI_CLK (CSIRX0 and DSITX0), when specific peripherals are not used as per pin connectivity requirements.
12. Connection of core supplies VDDA_CORE_CSI_DSI VDDA_CORE_DSI_CLK (CSIRX0 and DSITX0), when peripheral is not used but the boundary scan function is required, as per pin connectivity requirements. Ferrites and bulk capacitors are optional for peripheral core supplies.

Additional

1. The recommendation is to add a 0Ω resistor or jumper for isolation or current measurement at the PMIC DC/DC or LDO output for the core supply. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection to connect the TPs. Choose the resistor package based on the supply rail current and the resistor current carrying capacity.
2. Dynamic voltage scaling (DVS) of core supplies is not supported (not recommended or allowed).
3. Changing the core voltage is not allowed after the device is released from reset. If the core supply is turned off, the recommendation is to ramp down all the power rails as per the power-down sequence and wait until all supply rails decay below 300mV before turning on power.
4. When USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are not used reduces power when low power is a critical requirement.

6.1.1.1.4 Peripheral Analog Power Supply Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Recommended supply voltages are connected to peripheral analog power supply rails VDDS_MMC0, VDDS_OSC0, VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_PLL3, VDDA_PLL4, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VDDA_TEMP2.
3. Connection of 3.3V USB analog supply VDDA_3P3_USB.

4. ROC, slew rate and voltage sequence requirements for peripheral analog supply rails.
5. Peripheral analog supply filters.
6. Connection of peripheral analog supply when specific peripherals is not used.
7. Connection of peripheral analog supply (for CSIRX0 and DSITX0), when specific peripherals is not used but boundary scan function is required.

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to compare the implementation of bulk and decoupling capacitor for the supply rails with SK schematic implementation.
2. The supply rail operating voltage connected to peripheral supplies follows the ROC.
3. Recommended supply voltages 1.8V is connected to the 1.8V peripheral analog power supply rails VDDS_MMC0, VDDS_OSC0, VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_PLL3, VDDA_PLL4, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VDDA_TEMP2.
4. The recommendation is to connect supply rail VDDA_3P3_USB to a 3.3V analog supply for supporting USB2.0 interface.
5. Processor analog supply rails connected to the relevant supply pins follow the recommended voltage sequence. Refer *Power-Up Sequencing – Supply / Signal Assignments* section of the processor-specific data sheet for sequencing the analog supplies.
6. Slew rate of the analog supply rails follows the data sheet requirements.
7. Filters (ferrite) are provided for peripheral analog supplies (CSI_DSI, PLL, USB (1.8V), MCU_OSC0), as per the SK schematic implementation.
8. Connection of peripheral analog supply when specific peripherals are not used as per pin connectivity requirements.
9. Connection of peripheral analog supply (VDDA_1P8_CSI_DSI for CSIRX0 and DSITX0), when specific peripherals is not used but boundary scan function is required as per pin connectivity requirements. Ferrites and bulk capacitors are optional.

Additional

1. The recommendation is to add a 0Ω resistor or jumper for isolation or current measurement at the PMIC DC/DC or LDO output for the analog supply. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection to connect the TPs. Choose the resistor package based on the supply rail current and the resistor current carrying capacity.
2. Dynamic voltage scaling (DVS) of analog supplies is not supported (not recommended or allowed).
3. When USB driver is not initialized and the USB calibration procedure does not happen, connecting the supplies and leaving all of the USB pins for USB0, USB1, or both is acceptable. Grounding the USB supplies per pin connectivity requirements when both USB interfaces are not used saves power.

6.1.1.2 IO Supply for IO Groups

The below FAQ includes recommendations on CAP_VDDSn capacitor value, and the effect of the capacitor assembly (mounted or shorted):

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to CAP_VDDSx CAP_VDDS

Note

Refer below section *Supply Connection for Partial IO (Low Power) Mode Configuration* of user's guide for VDDSHV_CANUART supply connection.

The processor family supports x8 (eight) dual-voltage IO supply for IO groups (VDDSHVx [x = 0-3, 5-6]), IO supply for IO group CANUART (VDDSHV_CANUART) and IO supply for IO group MCU (VDDSHV_MCU). Each IO supply for IO group is connected (referenced) to a fixed set of IOs. Each IO supply for IO group can be connected to fixed (VDDSHV5, VDDSHV6 supports dynamic supply switching) 3.3V or 1.8V supply independently. The IO supply for IO group defines a common operating voltage for the entire set (fixed set) of IOs.

Processor pads (pins) designated as CAP_VDDSn [n = 0-3, 5-6], CAP_VDDS_CANUART, and CAP_VDDS_MCU connects the external capacitor to the internal IO supply for IO group regulator when the IO supply for IO groups connect to 3.3V supply (optional when IO supply for IO groups supplies connect to 1.8V). A 1μF (connected between the pins and VSS, see the processor-specific data sheet) capacitor is recommended. See the processor-specific data sheet for the recommended capacitor voltage rating and allowed capacitance range. When IO supply for IO groups are connected to 3.3V, the steady state DC output VDDSHVx/2, is the voltage to be considered for choosing the capacitor voltage rating considering the DC bias effect.

To minimize PCB loop inductance, place the capacitors on the back side of the PCB in the array of the BGA. The choice of capacitor voltage rating influences capacitor package (size) selection.

The recommendation is to select capacitor with ESR < 1Ω, keep the trace loop inductance < 2.5nH.

6.1.1.2.1 Additional Information

A number of processor IOs are not fail-safe. For information on available fail-safe IOs, see the processor-specific data sheet. The recommendation is to connect the IO supply of attached devices to the same power source connected to the respective processor dual-voltage IO supply for IO group (VDDSHVx) to make sure the custom board design never applies potential to any of the processor IOs that is not powered. Applying external input to the IOs that are not fail-safe when IO supply for IO groups supply is not available can affect the processor functionality, performance and reliability.

For more information on power-sequencing requirements between the processor and attached devices including signal isolation for fail-safe operation, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe)

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

Note

The recommendation is to verify that a valid supply voltage for the VDDSHVx is present before applying input to the associated processor IOs or peripherals.

The recommendation is to connect the VDDSHVx supplies and associated CAP_VDDSn (when IO supply connected is 3.3V, optional for 1.8V) capacitor irrespective of the usage of the processor IOs or peripherals.

6.1.1.2.2 IO Supply for IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of IO supply for IO groups.
3. ROC, voltage sequence and slew rate requirements for processor IO supply for IO groups.
4. Connection of recommended external capacitor for IO groups pins. Selection of CAP_VDDSn capacitor voltage rating.

Schematic Review

Follow the list below for the custom schematic design:

1. The recommendation is to compare the implementation of bulk and decoupling capacitor for the supply rails with SK schematic implementation.

2. A valid fixed 1.8V/3.3V supply source is connected to (VDDSHV_CANUART, VDDSHV_MCU, VDDSHV0, VDDSHV1, VDDSHV2, VDDSHV3) all the IO supply for IO groups as per the ROC.
3. A valid supply 1.8V/3.3V (that can be dynamically switched) source is connected to VDDSHV5, VDDSHV6 as per the ROC.
4. All IO supply for IO groups VDDSHVx have a valid supply connected irrespective of the use of IOs referenced to the IO supply for IO group.
5. Supply rails connected to the IO supply for IO group VDDSHVx follow the ROC.
6. Slew rate requirements followed for processor IO supply for IO groups. Refer processor-specific data sheet.
7. Connection of the recommended capacitor to CAP_VDDSn pin and VSS. Each CAP_VDDSn pin requires a separate 1μF capacitor connected with respect to VSS (ground) (for internal LDO, across CAP_VDDSn pin and VSS).
8. CAP_VDDSn capacitor package (recommend using the smallest possible (0201 or package size closest to 0201) package to minimize loop inductance).
9. Voltage rating of the CAP_VDDSn capacitor selected for the capacitance value to be in the range 0.8μF to 1.5μF including aging, temperature and effect of DC bias. Use 10V or above.
10. Select CAP_VDDSn capacitor with < 1Ω ESR, keep the trace loop inductance < 2.5nH.
11. IO supply voltage sequence follow the power-up and power-down sequence as per processor-specific data sheet.

Additional

1. The recommendation is to add a 0Ω resistor or jumper for isolation or current measurement at the PMIC DC/DC or LDO output for the IO supply rails. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connection to connect the TPs. Choose the resistor package based on the supply rail current and the resistor current carrying capacity.
2. In use case where the VDDSHVx IO supply rails are sourced from the 3.3V supply, all IOs referenced to (powered by) the VDDSHVx are required to operate at 3.3V IO level. If a VDDSHVx power rail is sourced from a 1.8V supply, all IOs referenced to (powered by) the VDDSHVx are required to operate at 1.8V IO level.
3. Some interfaces span multiple VDDSHVx, for example MMC2 and GPMC0. When using any of the interface, all VDDSHVx domains supporting a specific interface (peripheral) needs to be powered from the same power source.
4. A number of processor IOs are not fail-safe. Applying input voltage to the IOs while the corresponding VDDSHVx supply is off is not recommended or allowed.
5. The recommendation is to verify all IO pins on each VDDSHVx (or VDDSHV_MCU) connects to a single voltage level.
6. Leaving VDDSHVx rails unconnected is not recommended. The recommendation is to connect IO supply for IO group pins to either 1.8V or 3.3V, depending on the use case.

6.1.1.3 Supply for VPP (eFuse ROM Programming)

VPP (eFuse ROM programming) supply used for programming the processor eFuse is recommended to be sourced (powered) from a separate LDO that support the required (refer processor-specific data sheet) load current, load current transient and active (quick) output discharge. The LDO is recommended to be enabled only during eFuse programming. VPP operating voltage is required to be within the ROC range during eFuse programming. An LDO powered from a higher input voltage (2.5V or 3.3V) is recommended to compensate for the voltage drop through the series pass transistor and maintain the correct operating voltage during high load current transients. Local bulk capacitors are recommended near the processor VPP pin to support the LDO transient response.

Powering VPP supply rail from a supply rail with a variation outside the ROC (±5%), or using a Load switch or FET based switch can be a concern due to high load current transients and the requirement for the VPP supply rail be within the processor supply ROC. Load switch or FET based switch topology does not account for the voltage drop going through the load switch. The load switch can be an option if the custom board designer uses power source with smaller variation (compared to ROC), such that the supply variation combined with the voltage drop through the load switch never exceeds the VPP recommended operating range. As an alternate approach, an external supply for programming the eFuse can be used. The supply requirements are similar to the on-board LDO and the recommendation is to time the external supply EN (enable) using one of the processor IO. When external VPP supply is used, the recommendation is to provision for the bulk and decoupling capacitor on the processor board near to VPP supply pin.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

6.1.1.3.1 Supply for VPP Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Implementation approach of VPP supply and isolation of supply.
3. Recommended operating conditions for OTP eFuse programming.
4. Control of VPP supply (LDO EN).
5. Recommended bulk and filter capacitors.
6. Connection recommendations for external supply.
7. External VPP supply timing control.
8. VPP supply sequence.
9. Connecting the VPP supply to a continuous 1.8V supply rail is not recommended or allowed or supported option.

Schematic Review

Follow the list below for the custom schematic design:

1. Recommended bulk and filter capacitors are provided (follow SK schematic implementation).
2. Processor supply rail connected to the VPP supply (for eFuse programming) follows the processor ROC.
3. Implementation of on-board supply or provision to connect external supply with the bulk and decoupling capacitors added on the processor board.
4. A fixed output LDO or PMIC output (maximum current of 400mA) is recommended (use of FET based switch or Load switch is not recommended or allowed).
5. Choose on-board LDO that with nominal voltage of 1.8V and supports a minimum current of 400mA, has good load current transient response, and quick output discharge (active discharge) capability. Follow the LDO specs used on the SK schematics.
6. When an adjustable LDO is used, the recommendation is to verify the output voltage configuration, output voltage accuracy, output voltage slew and use of output over voltage protection (zener).
7. Processor IO is used to control the EN of the LDO and the recommended pull is provided.
8. The recommendation is to verify if EN pull holds the LDO in off-state during and after power cycling.
9. When external supply is connected, the recommendation is to add bulk and decoupling capacitor provision on the processor board near to the processor VPP pin and provided a TP to connect the external supply.
10. External VPP supply (when used) follows the recommended power sequence and slew rate requirements as per the processor-specific data sheet.

Additional

1. The recommendation is to always provide provision on the processor board to connect VPP supply (on-board or external supply).
2. The recommendation is to connect LDO output to the processor VPP pin with a low loop inductance path to source the high load current transients, where the supply on the VPP pin never drops below the minimum operating voltage.
3. Series resistor or jumper is provided to isolate the processor VPP supply from the LDO output for testing the timing or LDO output. The resistor package is expected to be rated for current > 400mA.

4. When an adjustable output LDO is used, consider adding an external zener based over voltage protection at the LDO output and provide provision to isolate the LDO output connected VPP supply pin to test the LDO output.
5. Due to the load current transient requirement during eFuse programming, using load switch or FET based switch is not recommended. A load switch or FET based switch is likely to have higher voltage drop that is not compensated.
6. If the use case requires use of load switch or FET based switch, the recommendation is to characterize the board performance by measuring the voltage on the processor VPP pin during programming and verify that VPP supply never drops below the ROC minimum value. Several variables in the path of VPP supply can cause the supply to be out of the ROC and are required to be characterized before implementing. Check if the load switch or FET based switch violates the maximum VPP supply slew rate requirement defined in the processor-specific data sheet.
7. The recommendation is to leave the processor VPP supply pin floating (Hi-Z) or grounded during power-up sequences, power-down sequences, and normal device operation.

6.1.1.4 Supply Connection for Partial IO (Low Power) Mode Configuration

6.1.1.4.1 Partial IO Mode Functionality

Processor circuit sections related to partial IO functionality are disabled when power is applied to the processor (for the first time, cold reset). When partial IO circuits are disable, the MCU_PORz input signal propagates to the circuits implementing partial IO functionality. The MCU_PORz input signal is blocked from the circuits implementing partial IO functionality after the software enables the partial IO functionality (circuits) and configures the processor to monitor wakeup inputs. This is necessary since the MCU_PORz input signal is asserted by the PMIC when the signal begins the power down sequence associated with the other processor power rails.

6.1.1.4.2 Partial IO Low Power Mode When Used

The recommendation is to connect VDD_CANUART and VDDSHV_CANUART to an always-on power source to support partial IO low power mode.

VDD_CANUART can operate at 0.75V or 0.85V, there is no voltage dependency with the VDD_CORE during normal operation. The only voltage dependency is during power-up and power-down sequencing.

For partial IO low power mode implementation, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A / AM62D-Q1 / AM62P Custom board hardware design – Partial IO LPM support

6.1.1.4.3 Partial IO Low Power Mode When Not Used

The recommendation is to connect VDD_CANUART to the same power source as VDD_CORE and VDDSHV_CANUART to any valid IO supply source.

6.1.1.4.4 Processor-specific Data Sheet Reference for Power Sequence

The recommendation is to refer to the notes related to partial IO low power mode in the *Power-Up Sequencing*, *Power-Down Sequencing* and *Partial IO Low Power Mode Power Sequencing* sections of the processor-specific data sheet.

6.1.1.4.5 Partial IO (Low Power) Mode Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of VDD_CANUART and VDDSHV_CANUART supplies to implement partial IO low power mode functionality.
3. Connection of VDD_CANUART and VDDSHV_CANUART in case partial IO low power mode functionality is not implemented.
4. VDD_CANUART operating voltage requirement with respect to VDD_CORE.

5. ROC, slew rate and voltage sequence requirements for VDDSHV_CANUART and VDD_CANUART.

Schematic Review

Follow the below list for the custom schematic design:

1. VDDSHV_CANUART and VDD_CANUART supplies are available before the other processor supplies are available, when partial IO low power mode functionality is implemented.
2. The recommendation is to connect VDD_CANUART and VDDSHV_CANUART to an always-on power source when implementing partial IO low power mode.
3. Voltage rails (levels) connected to VDDSHV_CANUART and VDD_CANUART follow the ROC and slew rate requirements as per the processor-specific data sheet.
4. When VDD_CANUART is connected to an always-on power source, the recommendation is to never apply a potential to VDD_CORE which is greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down.
5. Partial IO low power mode requires VDD_CANUART to ramp up before and ramp down after VDD_CORE.
6. VDD_CANUART and VDD_CORE operating voltage does not have any dependency (can operate at different core voltages).
7. The recommendation is to connect VDDSHV_CANUART to a valid 1.8V or 3.3V IO supply source in case partial IO low power mode is not implemented.
8. VDDSHV_CANUART and VDD_CANUART follow the recommended power sequence when partial IO low power mode functionality is not used.
9. The recommendation is to connect VDD_CANUART to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 in case partial IO low power mode is not implemented.

Additional

1. The recommendation is to verify the IO level compatibility between the processor inputs and the inputs connected from the attached devices (wakeup source).
2. **Partial IO mode functionality:** Processor circuit sections related to partial IO functionality is disabled when power is applied to the processor (for the first time, cold reset). When partial IO circuits are disabled, the MCU_PORz input signal propagates to the circuits implementing partial IO functionality. The MCU_PORz input signal is blocked from the circuits implementing partial IO functionality after the software enables the partial IO functionality (circuits) and configures the processor to monitor wakeup inputs. This is necessary since the MCU_PORz input signal is asserted by the PMIC when the signal begins the power down sequence associated with the other processor power rails.

6.1.1.5 Additional Information

Placement of 0Ω resistor (shunt) or a jumper in line with the core supply and other supply rails are recommended for initial board builds. 0Ω resistor (shunt) or jumper can be used during board bring-up and debug to isolate the supply or for current measurement. The recommendation is to add TPs for measurement. The recommendation is to follow kelvin current sense connections for connecting the TP to the resistor or jumper.

Shunt resistor connected to INA (instrumentation amplifier) following kelvin sense connection are used to measure the supply rails current in SK.

The recommendation is to verify the effect of adding 0Ω resistor (shunt) provision on the custom board performance (voltage drop in cases shunt (resistor) value in milliohm (mΩ) is used for measurement).

6.1.2 Capacitors for Supply Rails

6.1.2.1 AM62P, AM62P-Q1 Processor Family

The recommendation is to verify that the required number of decoupling and bulk capacitors including value are provided for all power supply rails, including dual-voltage IO supply for IO group supply rails.

The recommendation is to place the decoupling capacitors close to the processor supply pins. Larger bulk capacitors can be placed further away.

The recommendation is to use Low-ESL capacitors and the recommendation is to connect the capacitors with the shortest possible traces to keep the loop inductance minimal. For more information, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

As a starting point the recommendation is to follow the SK schematic implementation, for bulk and decoupling capacitors. Performing simulation (PDN analysis) is recommended to optimize the use of capacitors. For filtered (ferrite) power supplies implementation, follow the processor-specific SK. Additionally, follow the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

The recommendation is to use feedthrough (3-terminal) capacitors (used on the starter kit SK-AM62P-LP) to optimize the number of capacitors used. Use of 3-terminal capacitors minimizes the loop inductance and can be used to optimize processor performance, mainly the DDR performance.

6.1.2.2 Additional Information

When any of the processor peripheral instances (CSI-2 (Camera Serial interface 2, CSIRX0) and DSI (DSITX0, Display Serial interface), DDR Subsystem (DDRSS0) and USB2.0 (USB0 and USB1)) are not used, the supplies (peripheral core, analog) associated with the peripherals have specific connectivity requirements. For more information, see the *Pin Connectivity Requirements* section of the processor-specific data sheet. Power supply filter (ferrite) and capacitors (bulk) are optional.

6.1.2.3 Capacitors for Supply Rails Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Use of bulk and high frequency capacitors.
3. Number of capacitors used, package and value.
4. Voltage rating of the capacitors used.

Schematic Review

Follow the below list for the custom schematic design:

1. All processor power rails use bulk and high frequency decoupling capacitors. The critical power domains that require the focused attentions are the low voltage, high current domains (VDD_CORE, VDDR_CORE).
2. As a starting point, the recommendation is to follow the validated SK, or PDN application note. When there is difference between the SK and PDN, the recommendation is to follow the PDN. When information is not available in the PDN, follow the SK implementation.
3. The recommendation is to use Low-ESL capacitors connected with short traces to minimize the PCB trace loop inductance.
4. The recommendation is to verify each of the power rail pins has a decoupling capacitor and each of the supply rail group has a bulk capacitor.
5. Voltage rating of the capacitors used (> twice the worst-case applied voltage is a commonly used guideline).

Additional

1. In case difference is observed between the SK and the PDN application note on the capacitor number recommendation and value, the recommendation is to consider the recommendations in the PDN application note
2. While optimizing the capacitors, the recommendation is to perform static and dynamic PDN analysis to verify that the Reff, Cap LL, and Impedance targets are met
3. In some situations, the SK uses 3-terminal capacitors, due to low inductance packaging. Make sure the 3-terminal capacitors connections are not implemented as an in-line or filter component

4. The recommendation is to show the connections of the capacitor near to the relevant pin for ease of placement and routing

6.1.3 Processor Clocks (Inputs / Outputs)

6.1.3.1 Clock Inputs

6.1.3.1.1 MCU_OSC0 (High Frequency) Clock (Internal Oscillator) or LVCMOS Digital Clock (External Oscillator)

MCU_OSC0 25MHz (mandatory) reference clock is required for the processor to operate. The clock is used internally to generate a number of clocks that are required for the processor to operate. The other clock inputs depends on specific end equipment or board functionality implemented. Clocking option supported includes external crystal + internal oscillator or external 1.8V LVCMOS square-wave digital clock source. Spread spectrum clocking (clock input) is not a supported clock option.

In case 25MHz external crystal connected to the internal high frequency oscillator (MCU_HFOSC0) is the clock source for the internal processor operation, the recommendation is to place the discrete load capacitors used to implement the oscillator circuit close to the MCU_OSC0_XI and MCU_OSC0_XO pins. When crystal based oscillator is implemented, the recommendation is to follow the *MCU_OSC0 Crystal Circuit Requirements* table of the processor-specific data sheet for choosing the load capacitors. The load capacitor capacitance value includes the PCB capacitance. The recommendation is to refer to *Clock Routing Guidelines, Oscillator Routing* section of the processor-specific data sheet for placement and routing of the crystal and load capacitors.

A 1.8V LVCMOS clock source can be used as processor clock source. When clock output from the external oscillator is connected to the XI input (through a series resistor), the recommendation is to ground XO as per the recommendations in the processor-specific data sheet. The inverter shown in the (figure *1.8V LVCMOS-Compatible Clock Input* in the processor-specific data sheet) was meant to represent an LVCMOS output, where the LVCMOS output can be the oscillator output buffer, or the LVCMOS output from some clock distribution device. There is no requirement to invert the clock source.

For more information on LVCMOS clock source including specifications, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

Internal AC coupling capacitors have been implemented on both XI and XO signal paths that connect to an internal comparator that creates a square wave. A DC steady-state condition on the XI pin relative to the XO pin allows the comparator to generate glitches on the internal clock tree of the device and cause the clock circuit to do unpredictable operations. Connecting a DC input to XI is not recommended or allowed.

For information on clock selection and clock specifications, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding Crystal selection and clock specifications

For information on crystal (MCU_OSC0) Start-up Time, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Queries regarding crystal (MCU_OSC0) Start-up Time

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

Note

25MHz is the only crystal frequency currently supported. See the processor-specific data sheet for information on the supported crystal frequency and recommended crystal parameters.

Refer *MCU_OSC0 LVCMOS Digital Clock Source*, *MCU_OSC0 LVCMOS Digital Clock Source Requirements* section of the processor-specific data sheet.

When an external clock (LVCMOS) oscillator is used as the clock source for the processor and the EPHY (EPHy, EPHYs), a single oscillator can be used or separate (individual) oscillators can be used. When a single oscillator is used, the clock output is recommended to be buffered before connecting to processor and EPHy.

Single output buffer (individual ICs) for processor and EPHy or dual or multiple output buffer (single IC) with a single input for processor and EPHy, can be used to connect the clock output from the oscillator to the processor and the EPHy.

For specific use case (requirement for some of the industrial applications using Time Sensitive Networking (TSN)), two or more output (based on number of EPHYs used) buffer with a single input is recommended for the processor and the EPHy.

6.1.3.1.2 WKUP_LFOSC0 (Low Frequency) Clock (Internal Oscillator) or LVCMOS Digital Clock (External Oscillator)

A low frequency (32.768kHz) WKUP_LFOSC0 is supported by the processor family. Based on the use case, a 32.768kHz external crystal + internal oscillator can be used as the clock source or an external 1.8V LVCMOS square-wave digital clock source can be used.

WKUP_LFOSC0 has limited use cases and can be optional. When WKUP_LFOSC0 is not used, the recommendation is to connect the WKUP_LFOSC0_XI to VSS and to leave the WKUP_LFOSC0_XO unconnected. For more information on connecting the unused WKUP_LFOSC0, see the *WKUP_LFOSC0 Not Used* section of the processor-specific data sheet.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : LFOSC usage in the processor

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

The recommendation is to place the discrete components used to implement the external crystal based oscillator close to the WKUP_LFOSC0_XI and WKUP_LFOSC0_XO pins. For the crystal, the load capacitance selected is recommended to be in the range specified in the *WKUP_LFOSC0 Crystal Electrical Characteristics* table of the processor-specific data sheet. There is no requirement to add the PCB capacitance to the load capacitance.

The figure labeled *WKUP_LFOSC0 Crystal Implementation* in the processor-specific data sheet shows the recommended crystal circuit. TI recommends that preproduction printed-circuit board (PCB) designs include the two optional resistors Rbias and Rd in case these are required for proper oscillator operation when combined with production crystal circuit components. In a number of use cases, DNI or delete Rbias and Rd is a 0Ω resistor. The resistors option can be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCB.

6.1.3.1.3 EXT_REFCLK1 (External Clock Input to MAIN Domain)

EXT_REFCLK1 input is routed to clock multiplexers as a selectable clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN, and CPTS (Time Stamping Module). The EXT_REFCLK1 is an option when an end equipment/ application requires a specific clock frequency to be fed to the timer modules. An example application is time synchronization. When EXT_REFCLK1 is used as a clock source, depending on the availability of external clock, a pulldown (10kΩ) is recommended near to the processor clock input pin.

6.1.3.1.4 Clock Input Checklist - MCU_OSC0

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Configuration of processor clock input source, crystal + internal oscillator or external oscillator.
3. Selection of crystal, crystal frequency and crystal load capacitor.

4. Selection of MCU_OSC0 external crystal load capacitor.
5. Connection recommendations when crystal + internal oscillator or external oscillator is used.
6. Connection of XO when external oscillator output is connected to XI.

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of 25MHz MCU_OSC0 clock is mandatory.
2. Selection of External crystal or External clock oscillator as per the data sheet requirements.
3. Verify the crystal, crystal frequency and crystal load capacitor selected follows processor-specific data sheet recommendations.
4. 25MHz is the clock input frequency currently supported. Refer processor-specific data sheet for supported clock input frequencies.
5. Direct connection of crystal (without series or parallel resistor) and connection of the crystal load capacitance circuit (MCU_OSC0) as per processor-specific data sheet.
6. External crystal load capacitor is recommended to be 2x of the crystal load, including PCB capacitance (approximately 4pF).
7. The recommendation is to select crystal load value such that a standard value capacitor can be selected for the load capacitor.
8. The recommendation is to retain the HFOSC0 registers in the default state.
9. When external oscillator is used, the recommendation is to add decoupling capacitor and a bulk capacitor near to the oscillator supply pin and series resistor on the clock output pin.
10. The recommendation is to connect XO to VSS when external oscillator (LVCMOS clock) output is connected to XI.
11. Addition of series resistor (22Ω) on the clock output pin close to the oscillator.

Additional

1. Refer to the *Applications, Implementation, and Layout* section of the processor-specific data sheet for clock routing guidelines.
2. The recommendation is to connect the 25MHz (performance has been validated only with 25MHz frequency) crystal directly to the processor XI and XO pins, no series or parallel resistors are recommended. The internal oscillator implements Automatic Gain Control (AGC) for amplitude control.
3. Processor-specific data sheet shows that MCU_OSC0 does not start until the core voltage ramps because there are some cases where the oscillator does not start until VDD_CORE ramps. In most of the use cases, the oscillator starts when VDDS_OSC0 supply ramps (although the oscillator starting when VDDS_OSC0 ramps is not always the case). The oscillator start-up diagram in the processor-specific data sheet shows the maximum start-up time, which includes the case where the delay is based on VDD_CORE being valid.
4. A DC steady-state condition is not allowed on MCU_OSC0_XI because MCU_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state.
5. The LVCMOS clock sourcing the MCU_OSC0_XI input is required to have monotonic transitions and shall be connected to MCU_OSC0_XI with a point-to-point connection, by a series resistor placed near the clock source. The series termination resistor value shall match the clock source output impedance to the transmission line impedance. For example, a 20Ω is used when clock source has 30Ω output impedance and the PCB signal trace has 50Ω characteristic impedance. This allows the reflection that returns from the far end of the unterminated transmission line to be completely absorbed such that this does not introduce any non-monotonic events.
6. The recommendation is to minimize the PCB trace length connecting the external clock source to MCU_OSC0_XI. This reduces capacitive loading and minimizes probability of external noise sources coupling to the clock signal. Reduced capacitive loading improves rise/fall times of the clock signal which reduces the probability of jitter being introduced (to the clock source or the custom board).
7. The recommendation is to verify the crystal selection with the crystal supplies or manufacturer.

6.1.3.1.5 Clock Input Checklist - WKUP_LFOSC0

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Selection of WKUP_LFOSC0 clock source - external crystal + internal oscillator or external oscillator.
3. Selection of WKUP_LFOSC0 external crystal frequency.
4. Selection of crystal load capacitor.
5. Connection of series and parallel resistors to the crystal base oscillator circuit.
6. Selection of external oscillator and connection of capacitor and series resistor.
7. Connection of XO when external oscillator output is connected to XI.
8. Connection of XI and XO when WKUP_LFOSC0 is not used.

Schematic Review

Follow the below for the custom schematic design:

1. WKUP_LFOSC0 clock input frequency supported is 32.768kHz.
2. Connections of the clock circuit (WKUP_LFOSC0), as per the processor-specific data sheet recommendations.
3. Selection of crystal load and load capacitance value (follow the processor-specific data sheet), with the load capacitance being x2 of the crystal load (PCB capacitance is not included).
4. When external oscillator is used, the recommendation is to add decoupling capacitor and a bulk capacitor near to the oscillator supply pin and series resistor on the clock output pin.
5. Connection of XO when external oscillator is used (XO is grounded).
6. Connection of the XI input when the WKUP_LFOSC0 is not used (XI is grounded).
7. Connection of series and parallel resistors for initial prototype (preproduction) and production boards (can be removed) as per processor-specific data sheet requirements.

Additional

1. Crystal load capacitance versus LFOSC0 registers. The only LFOSC0 register bits custom board designers change are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the *Load Capacitance Equation*.
2. Refer to the processor-specific data sheet for the recommended circuit configuration (passives) during preproduction PCB and the production PCB.
3. WKUP_LFOSC0 has limited use cases, the recommendation is to provide provision to ground the XI input when the clock option is not used.

6.1.3.2 Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for the attached devices (External peripherals - Example: EPHY).

WKUP_CLKOUT0 is driven low after reset for AM62P, AM62P-Q1 processors.

The recommendation is to connect the clock as point-to-point connection. When CLKOUT0 and WKUP_CLKOUT0 are used to source more than x1 attached devices, buffering the CLKOUT0 and WKUP_CLKOUT0 is recommended.

The CLKOUT0 and WKUP_CLKOUT0 clock outputs performance is not defined in the processor-specific data sheet since there are a number of boards or end equipment specific dependencies that can impact the clock performance. The recommendation is to check the performance on the actual board (clock output meets board or end equipment specific requirements).

6.1.3.2.1 Clock Output Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Configuration of CLKOUT0 and WKUP_CLKOUT0 clock outputs.

Schematic Review

Follow the list below for the custom schematic design:

1. WKUP_CLKOUT0 is driven low after reset. Add a TP for testing.
2. When the WKUP_CLKOUT0 is used as an IO or as a 32.768kHz clock source, custom board designer is expected to consider the effect of the output being 25MHz being the output during the reset.
3. Series resistor 0Ω provision is provided to control possible signal reflection.
4. Connection of clock output to single or multiple loads. When connected to multiple loads (inputs), each of attached device inputs are recommended to be connected to a buffered output.
5. Pulls are provided near to the attached device clock input that can float (to prevent the attached device inputs from floating until host software configures the clock output).

Additional

1. EXT_REFCLK1 can be configured as CLKOUT0. The recommendation is to connect clock signal as point-to-point, without any branches. When connecting CLKOUT0 to multiple clock inputs, use a buffer (with one input and multiple outputs or individual buffers (based on the application use case)).
2. The CLKOUT0 and WKUP_CLKOUT0 clock outputs performance is not defined in the processor-specific data sheet since there are a number of boards or end equipment specific dependencies that can impact the clock performance.

6.1.4 Processor Reset

Processor reset module includes cold, warm reset inputs, and cold, warm reset status outputs.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design - Processor Reset inputs, Reset Status Outputs and Connection Recommendations

6.1.4.1 External Reset Inputs

The processor family supports x3 (three) external reset inputs (pins) including MCU and MAIN domain cold reset input (MCU_PORz), MCU and MAIN domain warm reset request input (MCU_RESETz) and MAIN domain warm reset request input (RESET_REQz).

MCU_PORz is the external MCU and MAIN domain cold reset input. The recommendation is to hold the MCU_PORz input low during the supply ramp and crystal/oscillator start-up and clock stabilization. Follow the recommended MCU_PORz input timing in the *Power-Up Sequencing* diagram of the processor-specific data sheet.

MCU_PORz input is 3.3V tolerant, fail-safe input type IO. Although 3.3V input can be applied, the input threshold follow the 1.8V IO level and is referenced to VDDS_OSC0.

When PMIC based power architecture is used, the recommendation is to connect the open-drain output type reset signal (nRSTOUT0) from PMIC to the processor through push-pull output type logic gate or discrete buffer (with fast rise time) as MCU_PORz input (rather than connecting a slow rising open-drain output that can glitch the internal reset circuit). In case nRSTOUT0 is directly used, the recommendation is to adjust the pullup to minimize the slew (<100ns).

The recommendation is to provide provision to connect a 22pF glitch filter at the MCU_PORz input. The recommendation is to always connect a valid input to MCU_PORz. Not connecting a valid input to MCU_PORz input is not an allowed use case. In case MCU_PORz input is not connected, the processor is not able to complete the reset sequence during power-up and can cause unpredictable or random behavior. When the processor internal circuit does not go through a valid reset, internal circuits can be in random (undefined) states.

The recommendation is to provide provision to connect a filter (glitch) capacitor at the MCU_PORz input. The capacitor value and mounting of the capacitor is use-case dependent. The recommendation is to choose the capacitor value such that the capacitor used does not cause the LVCMOS input to violate the slew rate requirements or cause reset to glitch internally.

External warm reset inputs MCU_RESETz and RESET_REQz can be used to perform external warm reset. An external push button or a reset circuit can be implemented to perform a warm reset of the processor. Some of the registers retain the state (for example, boot mode inputs capture register Devstat) during warm reset. Refer to the processor-specific TRM for information related to the resets and the functionality.

For connecting the warm reset inputs, follow the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Cold reset input (LVCMOS IO) has slew rate requirements specified. Connecting a slow ramp input to the MCU_PORz reset input is not allowed or recommended. Slow ramp input can cause internal reset circuit to glitch. The recommendation is to use a fast rise time discrete push-pull output type buffer output as MCU_PORz input.

Warm reset inputs (LVCMOS IOs) have input slew rate requirements specified. Connecting a capacitor (slow ramp) directly at the input is not recommended. A schmitt trigger-based debouncing logic (circuit) is recommended. For implementing the debouncing logic, follow the processor-specific SK schematic. When push-button is connected to control RESET_REQz or MCU_RESETz warm reset inputs, the recommendation is to add provision for external ESD protection.

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: MCU_PORz input slew rate

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design - Processor Reset inputs, Reset Status Outputs and Connection Recommendations

Usage note for MCU_RESETz reset input and MCU_RESETSTATz reset status output

MCU_RESETz input and MCU_RESETSTATz have specific use case recommendation. See the advisory *i2407-RESET. MCU_RESETSTATz is unreliable when MCU_RESETz is asserted low* of the processor-specific silicon errata.

6.1.4.2 Reset Status Outputs

The processor family supports x3 (three) reset status outputs (pins) including MAIN domain POR (cold reset) status (PORz_OUT) output, MCU domain warm reset status (MCU_RESETSTATz) output and MAIN domain warm reset status (RESETSTATz) output.

When reset status outputs PORz_OUT, MCU_RESETSTATz and RESETSTATz are used to drive attached device reset inputs (/reset), a pulldown (10kΩ) is recommended for the processor reset status outputs to assert the reset (hold the attached devices in reset) of the attached devices during power-up and processor reset.

Note

An external pulldown connected at the output of reset status output holds the attached devices reset input low, in use cases where none of the attached devices have internal pullups. In case where any of the attached device has an internal pullup enabled, the reset signal is pulled to a mid-supply. The recommendation is to verify specific use-case before connecting the reset status outputs.

MAIN domain warm reset status output RESETSTATz can be used to reset on-board memories or peripherals that support external reset input functionality (eMMC, OSPI, or EPHY) or SD card power switch EN. The PORz_OUT can be used to latch the hardware strap configurations during reset (Example: latching the Ethernet PHY strap configurations or the boot mode configurations).

In case the reset status outputs are not used, the recommendation is to connect the reset status outputs to a test point for testing or future enhancements. Optionally a pulldown (10kΩ) can be provided and can be populated when used.

Note

MCU_RESETz input and MCU_RESETSTATz have specific use case recommendation. See the advisory *i2407- RESET. MCU_RESETSTATz is unreliable when MCU_RESETz is asserted low* of the processor-specific silicon errata.

6.1.4.3 Additional Information

The BOOTMODE[15:00] inputs that are used to configure the processor boot mode is recommended to be held in a known state to select the appropriate boot mode configuration as defined in the processor-specific TRM, until the boot mode configuration is latched during the rising edge of the PORz_OUT.

6.1.4.4 Processor Reset Inputs Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. MCU_PORz input connection, L->H delay after supply ramps.
3. MCU_PORz input IO level and fail-safe capability.
4. MCU_PORz input state during processor supplies ramp.
5. Reset inputs follow the slew rate requirements (FS RESET, LVCMOS) as per the processor-specific data sheet.
6. Slew rate when open-drain output type reset signal (nRSTOUT0) from PMIC or discrete DC/DC or discrete LDO is connected to MCU_PORz input.
7. RESET_REQz input and MCU_RESETz input voltage level and connection.
8. Connection of warm reset inputs when not used.

Schematic Review

Follow the below list for the custom schematic design:

1. MCU_PORz input is held low during power supply ramp-up or ramp-down.
2. Cold reset input (MCU_PORz) deassertion hold time (9.5ms (9500000ns) minimum) after all supplies ramps is provided as per the processor-specific data sheet requirement.
3. Cold and warm reset inputs slew rate requirements have been considered and required buffers are added. Slow slew rate can glitch the reset internally.
4. Slew rate when open-drain output type reset signal (nRSTOUT0) from PMIC or discrete DC/DC or discrete LDO is connected directly to the reset input. Lesser slew is better (<100ns). The recommendation is to connect through fast rise time discrete push-pull output type buffer.
5. MCU_PORz (POR) input is 3.3V tolerant and fail-safe. The threshold follows the 1.8V IO level (VDDS_OSC0).
6. Provision for a glitch filter (capacitor) is provided at the MCU_PORz reset input (add 22pF (place holder) capacitor provision).
7. IO levels of MCU and MAIN domain warm reset input RESET_REQz follows the VDDSHV0 supply (1.8V or 3.3V) and MCU domain reset input MCU_RESETz follows the VDDSHV_MCU supply (1.8V or 3.3V).
8. Connection of push button warm reset inputs through debouncing circuit (Schmitt trigger buffer output).
9. The recommendation is to connect the warm reset inputs when not used as per pin connectivity requirements (a pullup is recommended).

Additional

1. MCU_PORz input has slew rate requirement specified. When connecting PMIC_POWERGOOD (open-drain output type signal) to MCU_PORz input is the only available option, adjust the pullup to optimize the rise time (~ 100ns).
2. The processor is required to restart (release reset) only after the voltages ramp down below 300mV during power-down (There is no time or tolerance associated with the ramp down requirement. Each power rail is recommended to decay below 300mV before any power rail is allowed to ramp up).
3. Not connecting a valid MCU_PORz input causes unpredictable and random behavior, since processor does not get a valid reset input and the internal circuits are in random states. Slow ramp reset input causes internal processor reset circuit to glitch.
4. LVCMOS inputs have slew rate requirements specified. A schmitt trigger based debouncing circuit is recommended for the slow ramp push button output signal connected to the processor warm reset inputs. Schmitt trigger based debouncing circuit is recommended when using a push button or an RC as reset input.
5. Provision for external ESD protection for manual (push button) reset input added near to the reset signal.
6. Fail-safe operation (MCU_RESETz input and RESET_REQz input) when connected to external reset inputs. Applying an external input signal to the processor reset inputs before the processor supply ramps can cause voltage feed and affects the board performance.
7. Reviewed MCU_RESETz input related silicon errata.
8. The recommendation is to follow the reset requirements including slew rate and MCU_PORz input hold time after supplies ramp when a non-TI power architecture is considered.

6.1.4.5 Processor Reset Status Outputs Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection (termination) of PORz_OUT, RESETSTATz and MCU_RESETSTATz status outputs.
3. Reviewed MCU_RESETSTATz related silicon errata.
4. IO level compatibility between the processor reset status output and attached device reset input.
5. Capacitor load connection at the output of reset status output.
6. Reset status output when not used.
7. External ESD protection for the reset status outputs when connected to carrier board or external connector.

Schematic Review

Follow the below list for the custom schematic design:

1. PORz_OUT is used as input to latch the processor boot mode configuration or attached device strap configuration during processor cold reset.
2. RESETSTATz, MCU_RESETSTATz is used to reset the attached devices when the processor undergoes any type of global reset (cold or warm).
3. PORz_OUT, MCU_RESETSTATz and RESETSTATz have pulldown added to hold the attached devices in reset during supply ramp and processor reset near to the processor pin.
4. Connection of capacitor directly on the reset output near to the reset input of the attached device (capacitor > 22pF). Perform simulation.
5. IO level compatibility between the processor reset status output and attached device reset input (can cause residual voltage affecting custom board performance).
6. Provision for TP provided when any of the reset status outputs are not used.
7. Processor reset output IO level and the attached device input IO levels are recommended to be matched to avoid voltage leakage.

6.1.5 Configuration of Boot Modes (for Processor)

The processor family supports x16 boot mode input pins that can configured by custom board designers to boot from the required (designed) memory interface or peripheral.

For supported boot mode configurations, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62Ax / AM62Px / AM62D-Q1 / AM62L - Supported bootmode configurations

Internal pulls (pullup or pulldown) are not enabled for the processor boot mode inputs during cold reset. The recommendation is to connect external pulls (10kΩ or 47kΩ) (pullup or pulldown) to configure the required boot mode. The recommendation is to not leave any of the boot mode inputs unconnected including reserved pins.

In use case where dip switches are used to configure the required boot modes, the recommendation is to use resistor divider value of 1kΩ (pullup) and 47kΩ (pulldown) for improved noise performance.

When the boot mode is configured using only resistors (without using dip switches), a standard resistor (same value can be used for pullup and pulldown) value can be used. As an example a 10kΩ or 47kΩ can be used since either pullup or pulldown is populated. The recommendation is to provide provision to connect pullup or pulldown to all boot mode pins including pins that are reserved or not used.

BOOTMODE14 and BOOTMODE15 pins are Reserved. Optionally, AM62P, AM62P-Q1 processor family can be configured for POST (Hardware Power-on-Self-Test) functionality when BOOTMODE15 = 1 and DS_DM_RESET_MASK = 0.

The recommendation is to add provision for pullup and pulldown for the boot mode inputs (pins) that have configuration capability for testing/debug (including provision for USB0 DFU, UART0 boot mode configuration), design flexibility, and future enhancement. The recommendation is to populate either pullup or pulldown for each boot mode pins. Connecting boot mode pins directly to ground or IO supply rail is not recommended or allowed since IOs have alternate function that can be configured after boot and can be unintentionally configured as output by the software.

Boot mode inputs (pins) are not fail-safe. The recommendation is to not apply any external inputs before the processor IO supply ramps. When connecting boot mode using pullups/pulldowns without the use of boot mode buffer the recommendation is to connect the IO supply that is connected to the IO supply for IO group referenced by the processor IOs. When using boot mode buffers the recommendation is to connect the IO supply that connects the processor IOs to the B-port supply pin of buffers (processor side). When external inputs from carrier board are connected to configure the boot mode inputs, the inputs are recommended to be driven after the processor supply ramps and are required to be stable before the MCU_PORz input is pulled high.

Based on the application requirement, a buffer that is driven only when reset status output (PORz_OUT or optionally RESETSTATz is low) can be used to drive the boot configuration inputs to the processor.

A series resistor (1kΩ) is recommended at the output of the buffer (to limit the output current in case the boot mode pins are configured as an output before the buffer OE is deasserted). For more information, see the processor-specific SK for implementation.

6.1.5.1 Processor Boot Mode Inputs Isolation Buffers Use Case and Optimization

In the SK, the boot mode inputs BOOTMODE[15:00] are configured using x2 buffers (for isolation). The buffers make sure that the SYSBOOT pulls (pullup and/or pulldown) (boot mode configuration resistors) control the IO level of the signals when the boot mode inputs are latched (during PORz_OUT rising edge). The boot mode configuration resistors are isolated from other connected peripherals (since boot mode input pins have alternate functions) so that the other connected peripherals do not conflict with the intended boot mode configuration (IO levels).

The buffers are enabled when PORz_OUT is low. Once PORz_OUT is deasserted (goes high), the buffer outputs are in Hi-Z state.

For optimizing the custom board design (including BOM), the boot mode buffers can be optimized or deleted (use case dependent, custom board designer to verify). The recommendation is to select the pull resistors value, so that the resistors do not affect the operation of the attach devices.

6.1.5.2 Boot Mode Configuration

For configuring the required processor boot mode, refer to the *ROM Code Boot Modes* table in the *Initialization* chapter of the processor-specific TRM.

6.1.5.2.1 Notes for USB Boot Mode

USB0 interface supports DFU (Device Firmware Upgrade) boot. When the USB0 is configured for DFU boot, permanent 3.3V supply (direct or using divider) is not recommended to be connected to the USB0_VBUS input. Connecting a permanent supply equivalent to the USB0_VBUS divider input is not allowed. Connecting supply without the *USB VBUS Detect Voltage Divider / Clamp Circuit* violates fail-safe operation.

A 5V supply from the host (switched) connected through the USB interface connector is recommended to be connected to USB0_VBUS input through resistor divider, as per the processor-specific data sheet recommendations. Zener diode can be removed and the two resistors (16.5kΩ and 3.48kΩ) can be combined into a single 20kΩ resistor for the *USB VBUS Detect Voltage Divider / Clamp Circuit* if the custom board design does not apply a VBUS potential > 5.5V, and on-board supply is connected.

6.1.5.3 Boot Mode Implementation Approaches

For implementing the boot mode, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation with isolation buffers used

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation without isolation buffers

6.1.5.4 Additional Information

When external inputs are connected to configure the boot mode inputs, the boot mode configuration inputs are recommended to be stable before the processor MCU_PORz (cold reset) is released (L->H).

When using Ethernet boot and Reduced Gigabit Media Independent Interface (RGMII) interface, the recommendation is to use an EPHY that supports RGMII_ID on the EPHY RDx data path and disables RGMII_ID on the TDx data path (processor implements fixed RGMII_ID on the TDx outputs). Processor ROM does not enable or disable RGMII_ID mode for the attached EPHY. RGMII_ID is set using pin strapping for the EPHY.

The recommendation is to select an EPHY, with capability to set the RGMII_ID through pin strap. Refer the processor-specific SK for implementation using TI EPHY.

6.1.5.5 Configuration of Boot Modes (for Processor) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of processor boot mode inputs.
3. Boot mode configuration (using dip switches and resistor divider or resistors).
4. Recommended boot mode inputs status during latching.
5. Boot mode inputs connection recommendation to alternate functions.
6. Fail-safe capability of boot mode inputs.

Schematic Review

Follow the below list for the custom schematic design:

1. Boot mode configuration inputs are connected to the processor using resistor, switch + resistor divider, and buffers as per the SK implementation.
2. The recommendation is to verify the boot mode input configuration setting follows the processor-specific TRM recommendations for PLL clock input, primary boot and secondary boot.
3. Boot mode inputs IO compatibility (1.8V or 3.3V referenced to (powered by) VDDSHV3).
4. The recommendation is to use 1kΩ and 47kΩ value resistors when dip switches are used to configure the boot.

5. When dip switches are not used a standard 10kΩ resistor can be used for pullup and pulldown to configure the boot mode. The recommendation is to populate either pullup or pulldown to configure the required boot mode. Resistor divider is optional when dip switches are not used.
6. All boot mode configuration input pins have external pulls or a circuit to drive the required boot mode input during processor cold reset (do not leave any of the boot mode configuration input pins unconnected).
7. External boot mode inputs applied are recommended to be stable before the processor cold reset input (MCU_PORz) is released (0->1).
8. Series resistor 1kΩ is used at the output of the buffer when boot mode is implemented with buffers or driven by external control signals.
9. The recommendation is to connect boot mode input signals to alternate functions through 0Ω for isolation or testing of the boot mode functionality.
10. Boot mode inputs are not fail-safe (no external boot mode input is recommended to be applied before the processor supplies ramp).

Additional

1. Processor BOOTMODE input pins do not have internal pullup or pulldown enabled during reset (when the boot mode input configuration is being latched).
2. For initial (early or first prototype) designs, the recommendation is to connect external PU/PD resistors for the boot mode inputs (pins). See processor-specific TRM for information on the boot modes supported.
3. Boot mode inputs are latched when PORz_OUT goes high. If the boot mode inputs are reconfigured for alternate function during operation, boot mode inputs are required to be released/set back to the required configuration to select the boot mode whenever the processor is reset (cold reset). Boot mode configuration is a concern if signal is driven from external peripheral.
4. Connecting the boot mode inputs directly to IO supply or VSS is not recommended. Shorting of multiple boot mode inputs together and connecting to a common resistor is not recommended. (Custom board designs can have firmware configuration issues, where the LVCMOS IOs that are intended to be inputs are unexpectedly configured as outputs, driving a logic high signal instead of remaining in high-impedance state).
5. The recommendation is to add external ESD protection for boot mode inputs, in case the boot mode switches are configured in an uncontrolled environment.
6. Boot mode inputs are not fail-safe. Applying external inputs before the processor IO supplies ramp is not recommended or allowed. Applying external input signal to the processor boot mode inputs before processor supply ramps can cause voltage feed and can affect the custom board functionality.
7. Boot mode input buffers are optional and are provided on the SK to support test automation.
8. When using buffers or logic gates to configure the boot mode inputs, the recommendation is to verify the device used supports OE (output enable capability).

6.2 Custom Board Debug Using JTAG and EMU

6.2.1 JTAG Interface and EMU Signals When Used

When JTAG interface is implemented, the recommendation is to use the TI recommended, defined and supported 20-pin connector (rather then the 10-pin ARM connector). The 10-pin JTAG connector does not include the TRSTn signal or the EMU0, EMU1 signals. The recommendation is to connect the JTAG (TDI, TCK, TMS and TRSTn) and EMU (EMU0 and EMU1) signals as per the *Pin Connectivity Requirements* section of the processor-specific data sheet. The recommendation is to place the pullups and pulldown (10kΩ) near to the processor JTAG interface pins.

The recommendation is to add external ESD protection for all JTAG interface and EMU0 and EMU1 signals close to the external interface connector. EMU0 and EMU1 signals support boot sequence and debug after cold reset (MCU_PORz input high). Pullup for TDO is optional and depends on the selected debugger. Optionally, the recommendation is to connect a series resistor (0Ω) on the TDO (close to processor) signal for matching JTAG tool buffer impedance.

For additional information, refer to the *On-Chip Debug* chapter of the processor-specific TRM.

For more information, see the below FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – JTAG

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – JTAG Pulldown/ Pullup

6.2.2 JTAG Interface and EMU Signals When Not Used

For connecting the JTAG interface signals and EMU signals when JTAG interface is not used, refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet.

During custom board design, the recommendation is to provision for a minimal JTAG interface signals including EMU0, EMU1 connected to test points or a header footprint to support debugging early prototype. JTAG interface related components can be a DNI in the production version of the board. The recommendation is to provide provision to populate recommended pulls as per the *Pin Connectivity Requirements* section, and provide provision for external ESD protection near to the JTAG connector or TPs.

6.2.3 Additional Information

Buffering of clock and JTAG interface signals are recommended whenever the JTAG interface connects to more than one attached device. Buffering of clock is recommended even for single device implementations. For implementation, see the processor-specific SK.

When trace interface is used, the recommendation is to connect TRC_DATAn signals to the emulation connector. All TRC_DATAn signals are pin-MUXed with other signals. The recommendation is to use either trace functionality or a GPMC interface. Short and skew matched connections (board trace) for TRC_DATAn signals are used for trace functionality. The trace signals are referenced to (powered by) VDDSHV3, and can be at a different supply voltage from the other JTAG signals. For additional recommendations on TRC/EMU design and layout, see the *Emulation and Trace Headers Technical Reference Manual*. A summary is available in the *XDS Target Connection Guide*.

When boundary scan is used, the recommendation is to connect EMU0 and EMU1 pins to the JTAG connector.

For implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual*.

6.2.4 Custom Board Debug Using JTAG and EMU Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of JTAG interface signals.
3. Connection of the required pulls.
4. JTAG interface signals IO compatibility.
5. Fail-safe operation of the JTAG interface signals.

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of JTAG interface signals and EMU0, EMU1 signals to the JTAG interface connector.
2. Connection of supply voltage to the JTAG connector including filter capacitor (the recommendation is to connect the voltage source that connects to VDDSHV_MCU).
3. Connection of the recommended pullup and pulldown as per the pin connectivity requirements near to the processor JTAG interface pins.
4. Pullup and pulldown values used (recommend value is 10kΩ).
5. JTAG interface signals IO compatibility (IO supply referenced to (powered by) VDDSHV_MCU).
6. Fail-safe operation of the JTAG interface signals. No JTAG inputs are available when the processor supplies are off.

Additional

1. The recommendation is to include (implement) at least a minimal JTAG signals on the custom board designs, connected to test points or header for debugging early prototypes. The minimum recommended JTAG signals are TCK, TMS, TDI, TDO, TRSTn and EMU0, EMU1. If required, the recommendation is to delete JTAG routes and component footprints (except the pulldown on TRSTn and the pullups on TMS and TCK) in the production version of the board.
2. When trace is implemented, the TRC_DATAn signals are recommended to be connected to the emulation connector. All TRC_DATAn signals are pin-muxed with other signals. If the trace connections are implemented, the recommendation is to not use other muxed functions. The recommendation is to use short and slew matched traces (routes) for TRC_DATAn signals. Trace signals are referenced to (powered by) a different power domain and can be operating at a different voltage compared to JTAG signals.
3. The recommendation is to add provision for external ESD protection. The external ESD protection can be populated when JTAG interface is used.
4. The recommendation is to verify fail-safe operation when using JTAG interface. Applying an external input signal to the processor JTAG inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.

7 Processor Peripherals Power, Interface and Connections

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

Note

There is no firm rule or requirement for external pull unless the pull requirements are defined in an industry standard. Industry standard definition for pulls is the main reason we can make firm recommendations for external pulls on the eMMC and SD card signals. For the other peripherals, the recommendation is for customers to evaluate the function of the attached devices connected to every processor signal on the custom board and apply the appropriate technical/engineering judgment to determine the need to have external pulls that prevent any input from floating when attached device inputs buffer is turned on. The recommendations provided in the design guide are generic and customer is expected to review the design requirements and the availability of pulls internal to the attached device before implementing. Be sure to not provide an external pull in contention with an internal pull. Example: An example is adding an external pull that is in contention with the internal pull (internal to the attached device), such that the contention creates a mid-supply potential on the signal (input).

7.1 Supported Processor Cores and MCU Cores

The recommendation is to refer to *Features* section of the processor-specific data sheet for the supported Processor Cores. The *Device Comparison* section of the processor-specific data sheet can be referenced for the selection of the Arm Cortex-A53 Microprocessor Subsystem cores.

The *Operating Performance Points OPP* section of the processor-specific data sheet can be reference for definition of the required device grade and device operating performance points.

Refer below FAQ for additional details:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on processor core, PLL, VDD_CORE, VDDR_CORE, VPP and other core supplies

7.2 Supply Connections for IO Supply for IO Groups

7.2.1 AM62P, AM62P-Q1 IO supply

Processor family supports IO supply for IO group VDDSHVx [x = 0-3, 5-6], VDDSHV_MCU and VDDSHV_CANUART. IO supply for IO groups support connecting dual-voltage (3.3V or 1.8V, fixed or dynamically switched) supply. Each dual-voltage IO supply for IO group provides power supply to a fixed set of IOs (or peripherals). Either 3.3V or 1.8V supply voltage can be connected to any of the dual-voltage IO supply for IO group.

The IO supply requirements depends on the IO buffer type (LVCMOS, SDIO or open-drain I2C) and the peripherals being connected.

The IO supply requirements depends on the IO buffer type (LVCMOS, SDIO or open-drain I2C).

VDDSHV5 and VDDSHV6 IO supply for IO group referenced to MMC1 and MMC2 signal groups have been designed to support power-up, power-down, or dynamic supply voltage change (switching) without dependency on other processor supply rails. The dynamic voltage switching capability allows UHS-I SD card support.

A valid supply is recommended to be connected to the IO supply for IO groups irrespective of the IO usage.

Based on the selected memory type (LPDDR4), the recommendation is to connect DDR PHY IO supply and DDR clock IO supply as per the ROC.

7.2.2 Supply Connections for IO Supply for IO Groups Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Standards referenced in the electrical characteristics including recommended operating conditions and any additional information available.
3. IO buffer type and the allowed supply configuration.
4. Connection of supply to all the IO supply for IO groups (VDDSHVx [x = 0-3, 5-6], VDDSHV_MCU, and VDDSHV_CANUART).
5. Sequencing of the processor IO supply.
6. Connection of processor DDRSS IO supply.
7. IOs pullup supply voltage reference.

Schematic Review

Follow the list below for the custom schematic design:

1. IO groups supported included LVCMOS, SDIO and I2C OD type IO buffers.
2. IO buffer type LVCMOS supports fixed (1.8V or 3.3V) or SDIO type dynamic voltage switching (1.8V or 3.3V).
3. Connection of valid supply (fixed, 1.8V or 3.3V) to IO supply for IO groups (VDDSHVx [x = 0-3], VDDSHV_MCU, VDDSHV_CANUART) and dynamically switched (1.8V or 3.3V) supply to IO supply for IO groups (VDDSHVx [x = 5-6]).
4. IO supply for IO groups referenced by the signals interfaced to the attached device and the attached device IO supply are connected to the same supply source.
5. Pullups are connected to the same supply rail or voltage level that is connected to the processor VDDSHVx and the attached device.
6. IO supply source used follows the ROC as per processor-specific data sheet.
7. Connection of the IO supply and supply sequencing follows the processor-specific data sheet.
8. Connection of processor DDRSS IO supply (PHY IO and Clock IO, VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source) based on the selected memory type (LPDDR4).

Additional

1. The recommendation is to follow the power sequencing requirements as per the processor-specific data sheet based on the IO supply for IO groups voltage level (3.3V or 1.8V) used.
2. Dynamic voltage switching is supported by specific IO supply for IO groups (VDDSHV5 and VDDSHV6).

3. Dynamic voltage switching for the IO supply for IO group referenced by (connected to) LVCMOS IO buffers is not recommended or allowed (VDDSHV0-3, VDDSHV_MCU, VDDSHV_CANUART).
4. Connecting 3.3V input supply (non sequenced, permanently ON, 3.3V supply connected to the PMIC input) directly to the IO supply for IO groups VDDSHVx is not recommended, since the IO supply is available for an undefined time in case the PMIC does not start-up and generate the other processor supply rails. The recommendation is to refer the updated power sequence diagrams in the processor-specific data sheet.

7.3 Memory Interface (DDRSS (DDR4/LPDDR4), MMCSD (eMMC/SD Card/SDIO), OSPI/QSPI and GPMC)

7.3.1 DDR Subsystem (DDRSS)

The processor family supports x1 instance of DDR sub system DDRSS0 and supports interfacing to 16-bit or 32-bit SDRAM.

The currently supported memory interface using DDR subsystem (DDRSS0) is LPDDR4 memory interface.

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDRSS : DDR4 / LPDDR4 MEMORY Interface

[FAQ] AM625: DDR4/ LPDDR4 performance difference

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.3.1.1 DDR4 SDRAM (Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.3.1.1.1 AM62P, AM62P-Q1 Processor Family

Currently Not Supported.

7.3.1.2 LPDDR4 SDRAM (Low-Power Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.3.1.2.1 AM62P, AM62P-Q1 Processor Family

For implementation guidelines and routing topology, see the *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*.

7.3.1.2.1.1 Memory Interface Configuration

The allowed memory configurations are x1 (single), 32-bit or x1 (single), 16-bit.

x1 (single), 8-bit memory configuration is not an allowed or valid configuration.

7.3.1.2.1.2 Routing Topology and Connection of Memory Terminations

When a 32-bit, single-rank, or dual-rank LPDDR4 is used, the recommendation is to follow balanced *T* topology for address, CKE, and CK signals routing.

When a 16-bit, single-rank LPDDR4 is used, follow the point-to-point topology. The recommendation is to connect the unused Data strobe pins (DDR0_DQS2-3 and DQS2-3_n) as per the *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines* recommendation.

The data interface signals connection topology is point-to-point for LPDDR4, and is categorized into different byte lanes.

VTT termination does not apply for LPDDR4 memory type. Terminations that are required for address and control signals are supported (handled) internally (on-die).

7.3.1.2.1.3 Resistors for DDRSS Control and Calibration

A pulldown (10kΩ) is recommended for DDR0_RESET0_n (LPDDR4_RESET_N) close to memory (LPDDR4) device. Adding a filter capacitor (47pF or similar) across the pulldown resistor is optional.

The recommendation is to connect the recommended (follow processor-specific data sheet or SK schematics) resistors for DDR0_CAL0 (IO Pad Calibration Resistor, close to processor cal pin), ODT_CA_A, ODT_CA_B (2.2kΩ used on SK, DDRSS On-Die Termination for Chip Select n, n=0-1, close to memory (LPDDR4) device) and ZQn (Memory Device Calibration reference resistor, n = 0-1, close to memory (LPDDR4) device).

7.3.1.2.1.4 Capacitors for the Power Supply Rails

The recommendation is to verify adequate bulk and decoupling capacitors have been provided for the processor DDRSS supply rails and memory (LPDDR4) device supply rails.

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.3.1.2.1.5 Data Bit or Byte Swapping

During custom board design, in case bit swapping is required, bit swaps within a data byte, and swapping across bytes is allowed with some restrictions. Address and control bit swapping is not supported.

For more information, see the *Channel, Byte, and Bit Swapping* section of *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*.

The recommendation is to update the schematics with the bit swapping changes including notes for future reference or reuse.

7.3.1.2.1.6 LPDDR4 Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Memory selected confirms to the relevant JEDEC (JESD209-4B) standard.
3. Memory configuration used.
4. The recommendation is to add layout notes on the schematic (the recommendation is to follow the *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*).
5. Supply rails connected to the processor DDRSS peripheral supply rail and the attached memory device IO.
6. Connection of address, clock, control and data signals.
7. Connection of DDRSS RESETn signal to LPDDR4_RESET_N memory reset input.
8. Connection of chip select CSn0, CSn1 to the attached memory device.
9. ODT pullup connection, DDR CAL0 and Memory ZQn resistor connections.
10. Swapping of Data Bits or Data Bytes.

Schematic Review

Follow the below list for the custom schematic design:

1. For LPDDR4 memory interface, x16 and x32 are the supported memory configurations. For connecting the DDRSS to 16-bit or 32-bit memory devices - refer *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*.
2. The recommendation is to compare the bulk and decoupling capacitors used and values with SK schematic implementation.
3. Supply rails connected to the processor DDRSS peripheral supply and the attached memory device IO follow the processor and attached memory device ROC.
4. Connection of address, clock, control and data signals. For LPDDR4 memory interface, x16 and x32 are the supported data bus width. For connecting the DDRSS to 16-bit or 32-bit memory devices - refer *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*.

5. Connection of DDRSS RESETn signal directly to LPDDR4_RESET_N memory reset input (to hold the signal low during power-on initialization). The recommendation is to add a pulldown (10kΩ) for DDRSS RESETn signal and place close to the memory device reset input pin.
6. Connection of chip select CSn0, CSn1 to the attached memory device. Follow *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines* based on selected memory.
7. Memory device ODT pulled up through a resistor (2.2kΩ or similar, the recommendation is to not connect DDRSS signals and follow the SK schematics).
8. DDR0_CAL0, DDRSS IO pad calibration resistor (240Ω, ±1%) connected across DDR0_CAL0 and VSS.
9. ZQ0, ZQ1, Memory device IO calibration resistor (240Ω, ±1%) connected across ZQ and VDD_LPDDR4.
10. Data Bit or Byte Swapping. Follow *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*.

7.3.2 Multi-Media Card/Secure Digital (MMCSD)

The processor family supports x3 (three) Multi-Media Card/Secure Digital (MMC/SD/SDIO) (8b + 4b + 4b).

7.3.2.1 MMC0 - eMMC (Embedded Multi-Media Card) Interface

7.3.2.1.1 AM62P, AM62P-Q1 Processor Family

The processor family supports x1 peripheral instances MMC0. MMC0 supports 8-bit eMMC (MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)) interface. eMMC interface implemented internal to the processor is a dedicated hard macro PHY. The MUX MODE, DSIS, and MUX MODE AFTER RESET columns in the *Pin Attributes (AMH Package)* table of the processor-specific data sheet is blank since the pins (interface) are implemented with a hard macro PHY (does not support pin multiplexing).

Review eMMC related silicon errata *AM62Px Sitara™ Processors Silicon Errata, Silicon Revision 1.0, 1.1*. The recommendation is to provide provision to connect VDDA_0P85_DLL_MMC0, VDD_MMC0 and VDDR_CORE to the same supply source to support future enhancements (and maintain compatibility between current silicon revision used and the next coming silicon revisions). Refer above section: *Core and Peripherals Supply*.

For more information on eMMC memory interface HS400 support, see the following FAQ:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – Power supply connection and Board layout recommendations to support HS400

Note

There are changes in the power supply pins ROC and naming to support HS400. Refer processor-specific data sheet for details.

For more information on eMMC memory interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

For more information, refer to the *MMC0 - eMMC Interface* section of the processor-specific data sheet.

7.3.2.1.1.1 MMC0 Interface Used

7.3.2.1.1.1.1 IO Power Supply

The MMC0 IO interface of the processor is referenced to (powered by) VDDS_MMC0 (1.8V) supply.

The recommendation is to connect VDDS_MMC0 and IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.2.1.1.1.2 eMMC Interface Signals Connection

The recommendation is to make the following connections:

- The recommendation is to add a series resistor (0Ω) for MMC0_CLK signal (close to processor clock output pin to control reflections)
- The recommendation is to connect a resistor between MMC0_CALPAD (close to processor CALPAD pin) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

Note

No external pulls are recommended to be added (required) for MMC0 eMMC PHY since the hard macro eMMC PHY implements the required pulls internally.

Pullups for DAT[7:0] and CMD are internally enabled by the eMMC hard macro PHY during and after reset. Pulldown is enabled for the DS and the clock output (CLK) is driven low after reset by the SS.

There are no PADCONFIG registers associated with the MMC0 pins. The internal pulls associated with the MMC0 pins are dynamically controlled by the MMC0 host (and PHY).

7.3.2.1.1.1.3 eMMC (Attached Device) Reset

The recommendation is to implement the attached device reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (without ANDing logic) to reset the attached device, the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO levels. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input can be slow and introduce too much delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.3.2.1.1.1.4 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for MMC0 supply rails and the attached device (core and IO supplies).

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.3.2.1.1.2 MMC0 Interface Not Used

MMC0 interface signals do not support alternate function. When MMC0 is not used, the interface signals and the MMC0 supplies have specific connectivity requirements.

For connecting the unused MMC0 interface signals and MMC0 supply rails, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

7.3.2.1.1.3 MMC0 (eMMC) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and implements a dedicated hard macro PHY for eMMC interface. MMC0 has specific connection requirements. Refer pin connectivity requirements for connecting the eMMC interface signals when eMMC interface is not used.
3. Connection of pulls for data and control signals.

4. Series resistor provision for MMC0_CLK and placement.
5. Processor IO supply for IO group (VDDS_MMC0) and the attached eMMC device IO supply power source.
6. Implementation of attached device reset logic to support boot mode configuration and when not used for boot.
7. Implementation of attached device reset logic to support boot mode configuration.
8. Implementation of attached device reset logic in case boot from the attached device is not required.
9. Reset signal IO level compatibility between processor and attached device.
10. Addition of required capacitors and value.
11. The recommendation is to connect VDDA_0P85_DLL_MMC0, VDD_MMC0 and VDDR_CORE to the same supply source to support future enhancements and maintain compatibility between silicon revisions. Refer above section: *Core and Peripherals Supply*.
12. Here is a quick checklist in case eMMC interface issues are observed:
    - Has the custom board been designed to be compliant to the PCB trace delay requirements defined in the MMC0 timing conditions table found in the processor-specific data sheet?
    - Which data transfer mode are being used when the issue is seen?
    - Has the interface been tested by reducing the operating speed and does that work?

Schematic Review

Follow the below list for the custom schematic design:

1. Required bulk and decoupling capacitors are provided for processor and attached device supply rails. The recommendation is to compare with the SK schematic (SK-AM62P-LP) implementation as a starting point.
2. VDDS_MMC0 MMC0 PHY IO supply (1.8V) and the attached eMMC device IO supply is powered from the same power source and follow the ROC.
3. Required pulls for data, CMD, and clock (state) are enabled (internally) by the eMMC hard macro PHY and controlled by the processor software (eMMC device pullups are disabled).
4. The recommendation is to provision for a series resistor (0Ω) on MMC0_CLK and placed close to the processor clock output pin. The series resistor has been provisioned to control possible signal reflections, which can cause false clock transitions.
5. In case eMMC boot mode configuration is required, 2-input ANDing logic can be used for implementing eMMC attached device reset. Processor GPIO is connected as one of the inputs to the AND gate with provision for pullup near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
6. Alternatively, warm reset status output RESETSTATz can be connected directly to reset the attached device. In case RESETSTATz is used, the recommendation is to match IO level between the processor reset status output and the attached device reset input. Verify IO level matching implementation (level shifter or resistor) follow the design recommendations.
7. In case eMMC memory is not used for boot, the attached eMMC device reset input can be controlled by using processor GPIO only. The recommendation is to pulldown the reset input of the eMMC memory device.

Additional

1. ANDing logic additionally performs IO level translation. The recommendation is to verify the reset input IO level compatibility while optimizing the reset ANDing logic. IO level mismatch can cause supply leakage and affect board performance.
2. The PHY implemented for the AM62Px MMC0 port supports only eMMC interface and implements internal pulls (does not require external pulls to hold the attached device in a known state until the interface is initialized). There are no PADCONFIG registers associated with the MMC0 pins. The internal pulls associated with the MMC0 pins are controlled by the MMC0 host (and PHY).
3. The MMC0_CLK pin is driven low after reset. An external pulldown is not required.
4. The MMC0_DAT[7:0] pins have internal pullups enabled during reset. The MMC0_CMD pin is driven high during reset. So, an external pullup is not required.
5. The MMC0_DS pin has the internal pulldown enabled during reset.

6. In summary, pull resistors for MMC0 (eMMC) signals are enabled internally during and after reset and there is no requirement to add external pulls.
7. The recommendation is to verify eMMC memory device reset eMMC_RSTn is enabled (eMMC non-volatile configuration space) for the external reset logic to be functional. The GPIO reset option is used to reset the attached eMMC device without resetting entire processor if there is a case where the peripheral becomes unresponsive. Only warm reset status output can be used to reset the attached eMMC device. Software forces a warm reset when the peripheral becomes unresponsive. However, using warm reset status output resets the entire processor, rather than trying to recover the specific peripheral without resetting the entire processor. When RESETSTATz is used to reset the attached device, the recommendation is to verify the IO level of RESETSTATz matches the attached device IO levels.
8. A level translator is recommended to match the reset IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input can be slow and introduce too much delay. If too low it causes the processor to source too much steady-state current during normal operation.
9. Adding a capacitor at the reset input of eMMC attached device is not recommended when RESETSTATz or processor IO is connected directly. A stand-alone reset connection using RC to reset the eMMC memory device is not recommended.

7.3.2.1.2 Additional Information on eMMC PHY

The recommendation is to refer to the notes in the *Signal Descriptions* section, *MMC, MAIN Domain* sub-section of the processor-specific data sheet.

Note

There are implementation difference in the eMMC Controller and eMMC PHY IPs used in different processor families. The recommendation is to follow the processor-specific recommendations for the eMMC interface including recommended terminations when migrating to a different processor family. The recommendation is to review the processor-specific data sheet, TRM, and following the connection recommendations for the processor and attached device.

Processor-specific SK implementation can be followed as a starting point reference.

7.3.2.1.3 MMC0 – SD (Secure Digital) Card Interface

The CD (Card Detect) and WP (Write Protect) pins are not available on MMC0 interface. MMC0 can be used to interfaces with fixed SDIO devices (on-board).

Interfacing SD card to MMC0 port is not recommended. The recommendation is to configure MMC1 port for SD card interface.

7.3.2.2 MMC1/MMC2 – SD (Secure Digital) Card Interface

The processor family supports x2 peripheral instances MMC1, MMC2 that can be configured for SD card interface. MMC1, MMC2 interface supports 4-bit SD card interface including support for UHS-I SD card. The recommendation is to use **MMC1 for SD card interface (based on the custom board design requirements)**. MMC1 is recommended for implementing SD card interface since MMC1 supports SD card boot mode, MMC1 IOs are connected to the IO supply for IO group that support SD card functionality. When MMC2 interface is used to implement SD card interface, the signals (SDCD and SDWP) are required to be multiplexed to the IOs connected to VDDSHV0.

For more information, refer to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

7.3.2.2.1 IO Power Supply

MMC1 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV5 supply rail (IO supply for IO group 5). VDDSHV5 is designed to support power-up, power-down, or dynamic voltage switching independently of other power rails, allowing the operating voltage to change from 3.3V to 1.8V as the transfer speed is increased.

VDDSHV5 supply is recommended to start with 3.3V and allow changing to 1.8V when software is expected (required) to change the IO supply voltage (to support UHS-I SD card).

The recommendation is to use separate supply sources (discrete LDO or PMIC) that can be switched independently for VDDSHV5 supply rail when configured for SD card interface.

MMC1 SD Card Detect (CD) and Write Protect (WP) signals are referenced to (powered by) VDDSHV0 supply rail (IO supply for IO group 0). The recommendation is to connect the pullups (10kΩ or 47kΩ) for MMC1_SDCD, MMC1_SDWP to the same supply rail connected to VDDSHV0 (fixed supply).

MMC2 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV6 supply rail (IO supply for IO group 6). VDDSHV6 is designed to support power-up, power-down, or dynamic voltage switching independently of other power rails, allowing the operating voltage to change from 3.3V to 1.8V as the transfer speed is increased.

VDDSHV6 supply is recommended to start with 3.3V and allow changing to 1.8V when software is expected (required) to change the IO supply voltage (to support UHS-I SD card).

The recommendation is to use separate supply sources (discrete LDO or PMIC) that can be switched independently for VDDSHV6 supply rail when configured for SD card interface.

MMC2 SD Card Detect (CD) and Write Protect (WP) signals are referenced to (powered by) VDDSHV6 (IO supply for IO group 6) supply rail or VDDSHV0 supply rail (IO supply for IO group 0). The selection of IOs referenced to (powered by) IO supply for IO group 0 or 6 is use case dependent. The recommendation is to add external pullups (10kΩ) for MMC2_SDCD and MMC2_SDWP (optional) signals can be connected to VDDSHV6 or VDDSHV0 supply rail (depending on the pins (IOs) selected) (close to attached device).

7.3.2.2.2 Signals Connection

The recommendation is to make the following connections when MMC1 and MMC2 signals are used to implement SD card interface:

7.3.2.2.2.1 MMC1 Signals Used for SD Card Interface (Recommended)

- The recommendation is to add a series resistor (0Ω) for MMC1_CLK (close to processor clock output pin to control possible signal reflections). A pulldown (10kΩ) is recommended for MMC1_CLK near to the attached device input to hold the clock in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) until the host configures the signal as clock.
- The recommendations is to add external pullups (47kΩ) for the SD card data signals (MMC1_DAT[3:0]) and CMD signal (MMC1_CMD) to prevent the attached device inputs from floating until the host software drives the interface signals. The recommendation is to connect the SD card interface signals pullup to dual-voltage IO supply for IO group (MMC1 = VDDSHV5) supply rail.
- The recommendation is to add external pullups (10kΩ or 47kΩ) for the MMC1_SDCD and MMC1_SDWP signals connected to the VDDSHV0 supply rail (close to attached device (SD card socket)).
- SD Card Detect (SDCD) input to the processor connects directly to ground when the SD card is inserted. A series resistor (100Ω) to limit the current in case the IO is programmed as output unexpectedly is recommended.

7.3.2.2.2.2 MMC2 Signals Used for SD Card Interface

- The recommendation is to add a series resistor (0Ω) for MMC2_CLK (close to processor clock output pin to control possible signal reflections). A pulldown (10kΩ) is recommended for MMC2_CLK near to the attached device input to hold the clock in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) until the host configures the signal as clock.
- The recommendations is to add external pullups (47kΩ) for the SD card data signals (MMC2_DAT[3:0]) and CMD signal (MMC2_CMD) to prevent the attached device inputs from floating until the host software drives the interface signals. The recommendation is to connect the SD card interface signals pullup to dual-voltage IO supply for IO group (MMC2 = VDDSHV6) supply rail.
- For supporting SD card interface, the recommendation is to connect MMC2_SDCD and MMC2_SDWP signals referenced (power) to VDDSHV0. The recommendation is to add external pullups (10kΩ or 47kΩ) for the MMC2_SDCD and MMC2_SDWP signals connected to the same supply rail that is connected to VDDSHV0 supply rail (close to attached device (SD card socket)).

- SD Card Detect (SDCD) input to the processor connects directly to ground when the SD card is inserted. A series resistor (100Ω) to limit the current in case the IO is programmed as output unexpectedly is recommended.

7.3.2.2.2.3 Additional Information

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design –SD card Interface

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1: Why is MMC1 powered by two different voltage supplies, VDDSHV0 and VDDSHV5 ?

[FAQ] AM62A7-Q1: how to connect the pin net VDDSHV4, VDDSHV5, and VDDSHV6 if SD card is not used

[FAQ] AM6442: AM6442 MMC1

FAQ] AM625: MMC interface

The FAQs are generic and can also be used for the AM62P, AM62P-Q1 processor family.

7.3.2.2.3 SD Card Power Supply Switch EN Reset Logic

The recommendation is to provide provision for a software-enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as the input to the power switch.

Use of power switch allows power cycling of the SD card supply (since resetting the power switch is the only way to reset the SD card) and resetting the SD card to the default state when UHS-I SD card is used.

The recommendation is to implement the SD card power switch enable and reset logic using a 3-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support SD card boot) near to the ANDing logic AND gate and provision for 0Ω to isolate the GPIO output for testing or debug. The other two inputs to the AND gate are the MAIN domain POR (cold reset) status output (PORz_OUT) and MAIN domain warm reset status output (RESETSTATz).

The external power switch sourcing the SD card power supply is recommended to default to ON (powered state) to support SD card boot.

For implementation, see the processor-specific SK.

7.3.2.2.4 External ESD Protection for the SD Card Interface Signals

External ESD protection is recommended for the SD card interface signals (data, clock, and control signals). Internal ESD protection is not designed to handle the board or end equipment level ESD requirements.

7.3.2.2.5 Capacitors for the IO Supply for IO Groups Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDSHV0, VDDSHV5 and VDDSHV6 supply rails and attached devices.

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

> **Note**
>
> The recommendation is to follow the processor-specific connection recommendations for data and control signals. The recommendation is to place the series resistor for the clock close to processor clock output pin to control possible signal reflections.

7.3.2.2.6 SD Card Interface (MMC1) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Verify the MMC port used for SD card interface. The recommendation is to use MMC1 for SD card interface.
3. Implementation of series resistor and pulldown for MMC1_CLK
4. MMC1 CMD and DAT[3:0] signals interface
5. IO supply for IO group supply connection
6. Pull values used for the data, command and clock signals
7. Implementation of MMC1 SDCD and SDWP signals connection
8. Circuit implementation to support UHS-I card
9. Supply rail connected to the SD card power switch input
10. Implementation of SD Card Power Supply Switch EN Reset logic
11. ESD protection provision for the SD interface signals

Schematic Review

1. Required bulk and decoupling capacitors are provided for the supply rails. The recommendation is to follow the processor-specific SK implementation for bulk and decoupling capacitors when recommendations are not available.
2. Supply rails connected to processor IO supply for IO groups VDDSHVx (VDDSHV5 and VDDSHV0) follow the ROC.
3. The MMC1 CLK, CMD, and DAT[3:0] signals interfaces are implemented using SDIO buffers referenced to (powered by) IO supply for IO group VDDSHV5 (SDIO buffer type IOs support dynamic voltage switching 3.3V or 1.8V to support UHS-I SD card).
4. 47kΩ pullup is recommended for data and command signals to meet the SD card specification (in case internal pullups are unexpectedly enabled the resulting pullup (47kΩ parallel to the internal pullup) value is still within the specified range).
5. Series resistor (0Ω) for MMC1_CLK is placed close to processor clock output pin to control possible signal reflections (which can cause false clock transitions). A pulldown (10KΩ) is placed near to the attached device clock input.
6. MMC1 SDCD and SDWP signals are implemented using LVCMOS buffers referenced to (powered by) IO supply for IO group VDDSHV0, which operate at fixed 1.8V or 3.3V.
7. The recommendation is to add a series resistor 100Ω on the SDCD pin since the processor IO connects directly to the ground when the SD card is inserted.
8. To support UHS-I SD card, the recommendation is to implement a discrete LDO or PMIC based supply with capability to switch the output between 3.3V and 1.8V and connect the switched output voltage to the IO supply for IO group, VDDSHV5 referenced to (powered by) the SD card interface IO signals.
9. To support UHS-I SD card, while the IO voltage for SD card interface can be 1.8V or 3.3V, the SD card VDD supply is a fixed 3.3V supply (3.3V_SYS, IO supply for IO group 3.3V supply).
10. The recommendation is to provide provision for a software-enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as the input to the power switch.
11. The recommendation is to implement the SD card power switch enable and reset logic using a 3-input ANDing logic. Processor GPIO is connected as one of the inputs to the AND gate with provision for pullup (to support SD card boot) near to the ANDing logic AND gate and provision for 0Ω to isolate the GPIO output for testing or debug. The other two inputs to the AND gate is the MAIN domain POR (cold reset) status output (PORz_OUT) and MAIN domain warm reset status output (RESETSTATz). The external power switch sourcing the SD card power supply is recommended to default to ON (powered state) to support SD card boot.

Additional

1. **The recommendation is to connect the SD card interface to MMC1 interface since MMC1 supports boot**. The logic level of the MMC1_SDCD and MMC1_SDWP inputs is expected to be fixed when the host switches the IO operating voltage to support UHS-I SD card. The MMC1_SDCD and MMC1_SDWP signals are connected to the internal SD card connector switches and pulled high through external resistors connected to the VDDSHV0.

2. Dynamic voltage switching is implemented since UHS-I SD card begins operating with 3.3V IO level and changes to 1.8V IO level when SD card transitions to one of the higher speed data transfer modes. An external pull is recommended for any of the processor or attached device IOs that can float (to prevent the attached device inputs from floating until driven by the host).
3. Use of power switch allows power cycling of the SD card supply (since resetting the power switch is the only way to reset the SD card) and resetting the SD card to the default state when UHS-I SD card is used. Power cycling (SD card power supply connection through power switch) the SD card is the only way to switch the SD card back to 3.3V IO mode, since SD card does not have a reset pin. LDO with dynamic supply switching capability to source the processor IO supply for IO group are required to support UHS-I SD card. The processor supply connected to IO supply for IO group is expected to power ON/OFF and switch the IO voltage along with the SD card supply. The circuits and the software driver that are controlling the supplies verifies that both devices are OFF/ON and are operating at the same IO voltage.
4. During processor boot, the ROM code checks the status of the card detect input (SDCD). The input is recommended to be low to indicate SD card is inserted (detected).
5. For implementing SD card interface using MMC2 interface signals, for the data, CMD, clock signals MMC1 connection can be followed. The IO supply for IO group referenced by the MMC2 signals is VDDSHV6. The MMC2_SDCD and MMC2_SDWP signals can also be referenced to VDDSHV6. Connecting an UHS-I SD card to MMC2 requires MMC2_SDCD and MMC2_SDWP to be connected to a fixed supply voltage. The signal functions are recommended to be implemented using alternate pin option (IOSET) that uses an LVCMOS IO type referenced to fixed voltage source VDDSHV0.

7.3.2.3 MMC1/MMC2 SDIO (Embedded) Interface

The processor family supports x2 peripheral instances MMC1, MMC2 that can be configured for SDIO interface. **The recommendations is to use MMC2 interface for on-board fixed voltage embedded SDIO devices use case such as Wi-Fi or Bluetooth transceivers since MMC2 interface has been tested for SDIO interface on the SK. MMC1 can be used for SDIO as required. Since the SDIO interface has not been tested on MMC1, customer is expected to check the availability of software support and perform the required performance tests on the custom board design.**

A fixed IO supply is used for embedded SDIO interface and simplifies the power architecture. The signals used includes data, command, clock and reset signals. Connecting SDCD and SDWP signals are optional and can be use case dependent.

There are no specific guidelines about implementation of pulls for embedded SDIO (providing or not providing pulls internal to the interfaced device). Custom board designer implementing an embedded SDIO device is responsible to determine the supported pulls on the SDIO device and apply appropriate external pulls on the custom board design. The processor IOs buffers (for a number of IOs) are off during reset and after reset and are not enabled until the board has booted and the software configures. To prevent floating inputs, the recommendation is to use external pulls on the signals connected to the inputs of attached devices that can float.

For more information, refer to the *MMC1/MMC2 - SD/SDIO Interface* section of the processor-specific data sheet.

Additionally, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – SDIO (embedded) interface

7.3.2.3.1 IO Power Supply

MMC1 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV5 supply rail (IO supply for IO group 5). MMC1 SD Card Detect (CD) and Write Protect (WP) signals (optional) are referenced to (powered by) VDDSHV0 supply rail (IO supply for IO group 0). The recommendation is to connect the pullups (10kΩ) for MMC1_SDCD, MMC1_SDWP for the SDIO interface to the same supply rail VDDSHV0.

MMC2 (CMD, CLK and Data) interface IOs are referenced to (powered by) VDDSHV6 supply rail (IO supply for IO group 6). MMC2 SD Card Detect (CD) and Write Protect (WP) signals (optional) are referenced to (powered by) VDDSHV6 (IO supply for IO group 6) supply rail or VDDSHV0 supply rail (IO supply for IO group 0). The pullups (10kΩ) for MMC2_SDCD, MMC2_SDWP for the SDIO interface can be connected to VDDSHV6 or VDDSHV0 supply rail.

7.3.2.3.2 Signals Connection

Note

The recommendation is to follow the below general recommendations in case there are no pulls recommended. The custom board designer is responsible to review the pulls supported by the attached device and make sure no reverse polarity pulls are externally added.

The recommendation is to make the following connections for MMC1 interface:

- The recommendation is to connect a series resistor (0Ω) for MMC1_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for MMC1_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to add external pullups (47kΩ) for the data lines (MMC1_DAT[3:0]) and CMD signal (MMC1_CMD) connected to the respective dual-voltage IO supply for IO group (MMC1 = VDDSHV5) supply rail (close to attached device).
- The recommendation is to add external pullups (10kΩ) for MMC1_SDCD and MMC1_SDWP (optional) signals connected to the VDDSHV0 supply rail (close to attached device).

The recommendation is to make the following connections for MMC2 interface:

- The recommendation is to connect a series resistor (0Ω) for MMC2_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for MMC2_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to add external pullups (47kΩ) for the data lines (MMC2_DAT[3:0]) and CMD signal (MMC2_CMD) connected to the respective dual-voltage IO supply for IO group (MMC2 = VDDSHV6) supply rail (close to attached device).
- The recommendation is to add external pullups (10kΩ) for MMC2_SDCD and MMC2_SDWP (optional) signals can be connected to VDDSHV6 or VDDSHV0 supply rail (depending on the pins (IOs) selected) (close to attached device).

7.3.2.3.3 SDIO (MMC2 Recommended, Embedded) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. There are no specific guidelines about implementation of pulls (CLK, DATA, CMD, SDCD, SDWP) for embedded SDIO (providing or not providing pulls internal to the interfaced device). Custom board designer implementing an embedded SDIO device is responsible to determine the supported pulls on the SDIO device and apply appropriate external pulls on the custom board design.
3. Implementation of series resistor and pulldown for MMC2_CLK
4. MMC2 CLK, CMD, and DAT[3:0] signals interfaces, IO supply for IO group supply connection
5. Implementation of MMC2 SDCD and SDWP signals connection
6. Implementation of attached device reset

Schematic Review

Follow the list below for the custom schematic design:

1. Required bulk and decoupling capacitors are provided for the supply rails. The recommendation is to follow the processor-specific SK implementation for bulk and decoupling capacitors when recommendations are not available.

2. The MMC2 CLK, CMD, and DAT[3:0] signals interfaces are implemented using SDIO buffers referenced to (powered by) IO supply for IO group VDDSHV6 (SDIO buffer type IOs support dynamic voltage switching 3.3V or 1.8V to support UHS-I SD card).
3. For embedded SDIO application, the recommendation is to power IO supply for IO group from the same fixed 1.8V or 3.3V power source that is used to power the IOs of the attached device (Example: Wi-Fi module).
4. MMC2 SDCD and SDWP signals are implemented using LVCMOS buffers referenced to (powered by) IO supply for IO group VDDSHV6 or VDDSHV0 (IOSET configuration), which operate at fixed 1.8V or 3.3V. For SDIO use case VDDSHV6 can be used since the IO supply is not switched. Use of SDCD and SDWP is use case dependent and there are no specific recommendations.
5. Series resistor (0Ω) for MMC2_CLK is placed close to processor clock output pin to control possible signal reflections (which can cause false clock transitions). A pulldown (10KΩ) is placed for MMC2_CLK near to the attached device clock input to hold the clock input in a low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state). The recommendation is to verify processor or attached device internal pulls are not configured when external pulls are used.
6. Pull values used for the data, command and clock signals. The recommendation is to follow the attached device recommendations or compare the implementation with the SK schematic implementation. When no recommendations are available for SDIO pulls, as good design practice, a 47kΩ pullup is recommended for the pullup value (to be within the SD card specification when internal pulls are enabled unexpectedly). With 47kΩ, the resulting pull resistance (47kΩ external pullup in parallel to the internal pulldown) value is still within the specified range. The recommendation is to verify processor or attached device internal pulls are not configured when external pulls are used.
7. Supply rails connected to processor IO supply for IO group VDDSHVx (VDDSHV6 when used for SDIO or VDDSHV0 when IO set is configured) and attached device IO supply follow the ROC.
8. Processor IO can be used to implement the attached device reset. A pulldown is recommended to hold the attached device in reset condition until the host initializes the SDIO interface.

Additional

1. Processor IO buffers are (TX (Output) and RX (Input) are disabled during and after reset and internal pulls (pullup and pulldown)) turned off during reset and after reset. An external pullup is recommended for any of the processor or attached device IOs that can float (to prevent the attached device inputs from floating until driven by the host). Pullups are recommended on all data and command signals.
2. The recommendation is to verify if the required external ESD protections have been provided for the interface signals in case the signals are connected over an add-on card.
3. When using MMC1 for embedded SDIO interface, software changes are required since the SK only implements the SDIO interface on MMC2. Custom board designers are responsible for testing the performance.
4. The processor IOs buffers (for MMCx signals) are off during reset and after reset and are not enabled until the board has booted and the software configures. To prevent floating inputs, the recommendation is to use external pulls on the signals connected to the inputs of attached devices that can float. To prevent floating inputs, use external pulls on any signals connected to the inputs of attached devices that can float.

7.3.2.4 Additional Information

The recommendation is to refer to the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the processor-specific data sheet.

7.3.3 Octal Serial Peripheral Interface (OSPI) or Quad Serial Peripheral Interface (QSPI)

Note

Refer the linked section for implementing series resistors and parallel pulls: *Processor-Specific SK Versus Data Sheet*.

The processor family supports x1 Octal Serial Peripheral Interface (OSPI0) instance that can be configured for OSPI0 or QSPI0 interface. OSPI0 is a Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. The OSPI0 instance supports OSPI/QSPI interface with DDR/SDR support. OSPI0 supports Serial NAND and Serial NOR flash memory devices. The OSPI0 peripheral has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI0 peripheral is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling the completion via interrupts or status registers.

For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM to be accessed using user programmable configuration registers.

For more information, see the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet.

For more information on OSPI or QSPI memory interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

[FAQ] OSPI FAQ for Sitara/Jacinto devices

7.3.3.1 IO Power Supply

The processor IOs used for the OSPI0 (OSPI or QSPI) interface are referenced to (powered by) VDDSHV1 supply rail (IO supply for IO group 1).

The recommendation is to connect VDDSHV1 and the IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.3.2 Signals Connection

The recommendation is to make the following connections:

- The recommendation is to connect a series resistor (0Ω) for OSPI0_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for OSPI0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
- The recommendation is to provide provision for a series resistor (0Ω) for OSPI0_LBCLKO (close to processor clock output pin to be able to connect or disconnect the LBCLKO).
- The recommendation is to add provision for external pullup (10kΩ) for CS signal close to attached device input.
- The recommendation is to add provision for external pullup (10kΩ) for INT# output near to the processor IO input configured as interrupt input.
- The recommendation is to provide provision for external pullups (10kΩ or 47kΩ) for the data lines (DAT0:7) connected to the attached device inputs (signals) to prevent the attached device inputs from floating until driven by the host. The recommendation is to connect the pullup resistors to the same power supply that is used to source the VDDSHV1 supply rail.

7.3.3.3 OSPI/QSPI Device Reset

The recommendation is to implement the attached device (OSPI/QSPI memory) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (without ANDing logic) to reset the attached device, the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the OSPI/QSPI reset input can be slow and introduce too much delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

The recommendation is to choose memory device that supports external reset input pin in addition to the data, clock, and chip select inputs.

7.3.3.4 Loopback Clock

Refer *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet. The section provides the PCB routing guidelines that is recommended to be followed when connecting OSPI, QSPI, or SPI memory devices.

The recommendation is to verify the loopback clock configuration. Different clock loopback configurations can be implemented using OSPI0_LBCLKO (OSPI0 Loopback Clock Output) and OSPI0_DQS (OSPI0 Data Strobe or Loopback Clock Input) signals. Refer the below diagrams in the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of processor-specific data sheet for information related to supported loopback configurations:

- OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback
- OSPI Connectivity Schematic for External Board Loopback
- OSPI Connectivity Schematic for DQS

External Board Level Loopback

Processor DQS (or Loopback Clock input) is used along with the DS data strobe output of the attached memory device

The recommendation is to connect the DS (in case DS (Read Data Strobe) pin is available on the attached device) pin of the attached device to the OSPI0_DQS pin of the processor. The recommendation is to leave the OSPI0_LBCLKO pin unconnected when not used.

The recommendation is to configure the external loopback in case DS pin is not available on the attached device (Example: QSPI).

The recommendation is to connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor (take note of the length matching requirements).

When External Loopback is not used, the recommendation is to leave the OSPI0_LBCLKO and OSPI0_DQS pins unconnected.

Note

D0 and D1 pins of the processor OSPI0 interface is recommended to be connected to D0 and D1 pins of the OSPI/QSPI memory device to support legacy x1 commands. Swapping of the data bits is not allowed.

7.3.3.5 Interface to Multiple (Attached) Devices

Connecting OSPI0 peripheral (memory interface) to multiple memory devices is currently not supported. The recommendation is to connect the OSPI0 interface (processor) to x1 memory device. When OSPI0 is interfaced to multiple memory devices, the interface creates a split data bus which can degrade signal integrity at higher speeds. For accessing memory device using OSPI0 at higher speeds, a point-to-point connection of the OSPI0 interface signals is recommended.

7.3.3.6 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDSHV1 supply rail and the attached device (CORE and IO supplies).

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.3.3.7 OSPI0 or QSPI0 Peripheral Interface Implementation Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Required memory interface configuration and recommended connections.
3. IO level compatibility between processor and attached device. Connection of attached device IO supply and the IO supply for IO group referenced to (powered by) the OSPI0 interface signals.
4. Provision for series resistor and pulldown for OSPI0_CLK.
5. Provision for pullups for data and control signals.
6. IO level compatibility between processor and attached device.
7. Implementation of reset logic and connection of attached device reset input.
8. Clock loop back configuration based on the memory device and interface selected (OSPI/QSPI).
9. Connection of DQS input from memory (QSPI) or LBCLKO from processor (QSPI).

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to compare the OSPI0 or QSPI0 memory interface with SK schematic implementation for provisioning of parallel pulls, series resistors, and the resistor values.
2. The recommendation is to compare implementation of attached device reset logic with the SK schematic implementation.
3. Series resistor (0Ω) provision for OSPI0_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for OSPI0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
4. Provision for pullups (10kΩ or 47kΩ) are provided for data and control signals that can float (to prevent the attached device inputs from floating until driven by the host). The recommendation is to verify the supply source connected to the pullups.
5. Connecting the OSPI0 interface to multiple attached devices (more than x1 attached device) is not recommended or allowed.
6. IO level compatibility between processor and attached device. The attached device IO supply and the IO supply for IO group VDDSHV1 referenced to (powered by) the OSPI0 interface signals are connected to the same supply source.
7. Supply rail connected to the IO supply for IO group VDDSHV1 referenced to (powered by) OSPI0 peripheral and attached device IO supply follows the ROC.
8. Implementation of external loopback (based on the use case).
9. Connection of DQS from OSPI memory device and pulldown added for DQS input near to processor.
10. Connection of OSPI0_LBCLKO for QSPI memory device through 0Ω.
11. Pulling up the reset input to a high state during reset or supply ramp (is not recommended).
12. Implementation of reset logic when used for boot using a 2-input (RESETSTATz and processor IO) ANDing logic or using MAIN domain warm reset status output RESETSTATz.
13. When OSPI0 interface is not used for boot, the reset logic can be implemented using a processor IO. A pulldown is recommended near to the reset input.

Additional

1. The recommendation is to verify that the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the processor-specific data sheet is followed.
2. In case OSPI/QSPI boot mode is implemented, the recommendation is to verify the silicon errata, selected memory meets the boot criteria described in the processor-specific TRM (or verify with TI, recommend using E2E).

7.3.4 General-Purpose Memory Controller (GPMC)

The processor family supports x1 General-Purpose Memory Controller (GPMC0) instance that can be interfaced to NAND flash using 8-bit or 16-bit NAND flash interface signals or NOR flash using supported parallel memory interface (Synchronous or Asynchronous) options listed in the processor-specific data sheet and *Device Comparison* table.

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

Refer to the *Memory Interfaces* chapter, *General-Purpose Memory Controller (GPMC)* section of the processor-specific TRM for supported, GPMC features, various access types and wide range of external devices GPMC interface can communicate with. For the supported signals refer *GPMC I/O Signals* section of the processor-specific TRM, *Signal Descriptions, GPMC MAIN Domain GPMC0 Signal Descriptions* section of the processor-specific data sheet.

7.3.4.1 IO Power Supply

The processor IOs used for GPMC interface are referenced to (powered by) VDDSHV3 supply rail (IO supply for IO group 3).

The recommendation is to connect VDDSHV3 and the IO supply rail of the attached device to the same supply source.

VDD (CORE voltage) of the attached device can be powered from (by) an independent (different power supply source) supply source.

7.3.4.2 GPMC Interface

The recommendation is to verify the memory interface configuration used and number of attached devices connected to the GPMC interface.

The recommendation is to connect the GPMC interface to x1 (single) device when configured in synchronous mode. Using multiple attached devices (CSn) requires splitting the GPMC clock (and other interface signals) on-board, which can cause signal integrity concerns affecting performance.

A detailed timing analysis is recommended when interfacing multiple devices in asynchronous mode. When interfacing multiple devices in asynchronous mode, the control signals are required to be routed to multiple devices. The split routing and loading (trace length and number of devices) custom board performance.

7.3.4.3 Signals Connection

The recommendation is to connect a series resistor (0Ω) for GPMC0_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for GPMC0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).

The recommendation is to provision for external pullups (10kΩ) on GPMC0_CSn0-3 (depending on the configuration) to prevent the attached device inputs from floating until driven by the host.

The recommendation is to provision for external pulls (10kΩ) for the GPMC address and data interface signals to prevent the attached device inputs from floating until driven by the host.

7.3.4.3.1 GPMC NAND

Active high ready and active low busy (R/B#) output from the NAND flash are open-drain output type signals and are connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). The recommendation is to add pullup (commonly used value 10kΩ) close to the attached device.

7.3.4.4 Memory (Attached Device) Reset

When using NAND flash or NOR flash using GPMC interface, availability of reset input depends on the selected memory device.

In case the reset pin is supported, the recommendation is to review the required reset configuration and connect the relevant external reset input signal to the memory reset input pin including implementing 2-input ANDing logic. Adding a pullup on the reset pin enables the memory during supply ramp and this is not recommended.

7.3.4.5 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDSHV3 supply rail and the attached device (CORE and IO supplies).

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.3.4.6 GPMC Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. GPMC interface configuration and recommended connections.
3. Connection of series resistor and pulldown for GPMC0 clock.
4. IO level compatibility between processor and attached device.
5. Connection of required pulls for IOs.
6. Supported address and data range.
7. Connection of open-drain output type signal active high ready and active low busy (R/B#) outputs from the NAND flash.
8. Boot mode inputs configured for alternate function (GPMC interface).
9. GPMC interface timing required versus calculated and effect of layout on the timing. Timing and IO load calculation performed when connecting to multiple devices in Async mode.

Schematic Review

Follow the below list for the custom schematic design:

1. GPMC interface configuration and recommended connections. Connection of GPMC memory NAND/ NOR, address and data signals - multiplexed or non-multiplexed, synchronous or asynchronous, data bit width as per the processor-specific TRM.
2. Supported address and data range (IOs pinned out for the processor as mentioned in the processor-specific data sheet).
3. IO level compatibility between processor and attached device. The attached device IO supply and IO supply for IO group VDDSHV3 referenced to (powered by) the GPMC interface signals are connected to the same supply source.
4. The recommended pulls (47kΩ) are provided for the interface signals that can float (to prevent the attached device inputs from floating until driven by the host).
5. The recommendation is to provision for external pullups on GPMC0_CSn0-3 (depending on the configuration) to prevent the attached device inputs from floating until driven by the host.
6. Series resistor (0Ω) provision for GPMC0_CLK (close to processor clock output pin to control possible signal reflections) and external pulldown (10kΩ) for GPMC0_CLK (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state).
7. Supply rails connected to the IO supply for IO group VDDSHV3 referenced to (powered by) GPMC0 peripheral and attached device IO supply are sourced from the same source and follow the ROC.

8. Open-drain output type signal active high ready and active low busy (R/B#) outputs from the NAND flash are connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). The recommendation is to provide the pullup (commonly used value 10kΩ) close to the attached device.
9. Boot mode inputs configured for alternate function (GPMC interface) through a 0Ω to be able to isolate to check boot mode functionality.

7.4 External Communication Interface (Ethernet (CPSW3G0), USB2.0, UART and MCAN)

Note

Refer the linked section for implementing series resistors and parallel pulls: *Processor-Specific SK Versus Data Sheet*.

7.4.1 Ethernet (MAC) Interface

The processor family supports x2 (two) independent Ethernet interface with individual MAC IDs (using CPSW3G0 peripheral). Each of the MAC interface supports RGMII or RMII interface.

For more information on the Ethernet interface, see the following FAQs:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 and AM2434, AM2432, AM2431 (ALV, ALX) Custom board hardware design - Ethernet

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RGMII interface and RGMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RMII interface and RMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Ethernet PHY RGMII synchronous clock

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

7.4.1.1 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G0)

The processor family supports x1 instance of CPSW3G0 Ethernet switch (with 2 external ports) that can be configured either as a 3-port switch (interfaces to 2 external Ethernet ports (port 1 and 2)) or dual independent MAC interface having individual MAC address.

CPSW3G0 supports RGMII (10/100/1000) or RMII (10/100) interface for each of the external Ethernet interface port. In RGMII interface, both TDx (data transmitted by processor) data path and RDx (data received by processor) data path are completely independent on each other, where each have own clock and data signals that perform source synchronous data transfers.

7.4.1.1.1 IO Power Supply

Processor MAC interface (CPSW3G0) signals (IOs, used for Ethernet interface with EPHy) are referenced to (powered by) VDDSHV2 supply rail (IO supply for IO group 2). The recommendation is to connect VDDSHV2 and the IO supply rail of the attached device (EPHy) to the same supply source.

VDD (CORE voltage) of the attached device (EPHy) can be powered from (by) an independent (different power supply source) supply source.

7.4.1.1.2 MAC (Data, Control and Clock) Interface Signals Connection

Provisioning for series resistors (0Ω) is recommended for the processor Ethernet MAC interface signals (For TDx signals the recommendation is to place near to the processor MAC interface pins). The recommendation is to use the smallest possible package (0402 or smaller) and place series resistors close to source. The resistor value can be adjusted during testing. For the RDx signals internal impedance control (in case EPHY supports) option provided by EPHy can be used. The recommendation is to provide provision for external series resistors (0Ω) on the RDx signals in case space is not a constraint or EPHY does not support internal impedance control.

The interrupt output of the EPHy can be connected to the processor EXTINTn (interrupt) pin. The recommendation is to connect a pullup (10kΩ or 47kΩ) for the EXTINTn close to processor.

7.4.1.1.3 EPHy Reset

A 3-input ANDing logic can be used to implement the attached device (EPHY) reset. Processor GPIO (used to locally reset the EPHY) is connected as one of the input to the ANDing logic AND gate with provision for pullup (10kΩ or 47kΩ) (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other two inputs to the AND gate are the MAIN domain POR (cold reset) status output (PORz_OUT) and MAIN domain warm reset status output (RESETSTATz).

In case a dual input ANDing logic is considered PORz_OUT (pin strapping on power-up) or RESETSTATz can be connected as one of the input with the processor GPIO input connected as the other (second) input. When more than one (x2) EPHy are used, the recommendation is to provide provision to reset the EPHy individually.

A pullup or pulldown (10kΩ) at the output of the ANDing logic can be used based on the EPHY reset input polarity. The EPHY is required to be held in reset for a specified minimum time after the clock is valid.

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used to reset the EPHY (attached device), the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the EPHY reset input can be slow and introduce too much delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.4.1.1.4 Ethernet PHY (and MAC) Operation and Media Independent Interface (MII) Clock

The recommendation is to match the clock specifications for the EPHy and the processor.

7.4.1.1.4.1 Crystal Used as Clock Source for Processor and EPHy

In case a crystal is used as the clock source for the EPHy, the recommendation is to match crystal (clock) specifications with the processor clock specifications.

7.4.1.1.4.2 External Oscillator Used as Clock Source

An external (LVCMOS) oscillator can be used as the clock source for the processor (and the EPHy). A x1 (single) oscillator or multiple oscillators (separate oscillator for each of the EPHy and processor) can be used. When using x1 (single) oscillator, the recommendation is to buffer the oscillator clock output (use individual buffer for each attached device clock input) before connecting to the processor and EPHy.

A single channel (with single input and single output) buffers, or single input with dual or multiple output buffer can be used to connect the clock output of the oscillator to the processor and EPHy. For a specific use case (requirement for some of the industrial applications using a Time Sensitive Networking (TSN)), single input and two or more output (based on number of EPHy used) buffer is recommended for the processor and the EPHy.

The recommendation is to verify that the XO of the EPHY is connected according to the recommended guidelines.

7.4.1.1.4.3 Processor Clock Output (CLKOUT0)

For optimizing the custom board design, the processor clock output (CLKOUT0) can be used as clock source (input) to the EPHy. CLKOUT0 is buffered internally and is intended to be connected in a point-to-point clock topology. Buffering of the CKLOUT0 (individually) is recommended before connecting to the clock input of the attached devices (EPHy). A series resistor (0Ω, adjust after testing) is recommended at the source end of the CLKOUT0 to control possible signal reflections.

EPHY using RGMII interface requires a 25MHz clock input that is not synchronous to any other signals. 25MHz clock does not have any timing requirements, but is important the EPHy does not receive any non-monotonic transitions on the clock input.

When EPHY is configured for RMII interface, clocking option depends on the EPHY configuration.

When EPHY is configured as a controller, many of the RMII EPHy use a 25MHz input clock that is not synchronous to any other signals, the 25MHz clock signal does not have any timing requirements, but is important to make sure the EPHY does not receive any non-monotonic transitions on the clock input.

The RMII EPHY provides the 50MHz clock output to the MAC. For RMII use case, the 50MHz data transfer clock is delayed (hardware delay) to the MAC relative to the EPHY. The delay shifts clock to data timing relationship which can erode the timing margin. Eroded timing margin can be a concern for some designs if the delay is large.

When EPHY is configured as a device, the MAC and the EPHY uses a 50MHz common clock that is synchronous to both transmit and receive data. The 50MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the EPHY, where transitions are expected to arrive simultaneously at the MAC and EPHY device pins. The common clock provides better timing margin for both transmit and receive data transfers. Important requirement is that the MAC and EPHY do not receive any non-monotonic transitions on the clock inputs. To control the clock signal integrity, the recommendation is to route the common clock signal through a single input, two-output phase aligned buffer. The recommendation is to use equal length signal traces that are half the length of the data signals for connecting the clock buffer outputs, where one clock output connects to the MAC and the other connects to the EPHY.

For RMII interface, the recommended configuration *RMII Interface Typical Application (External Clock Source)* is explained in the processor-specific TRM. When the *RMII Interface Typical Application (Internal Clock Source)* configuration is used, the recommendation is to validate performance on a board level. The recommendation is to provision for connecting an external clock for initial performance testing and comparison with internal clock.

The Ethernet performance (RGMII) is validated on the processor and the EPHY (used on the SK board) with 25MHz clock frequency.

The CLKOUT0 can be used to source a 25MHz or a 50MHz clock to processor (MAC) and EPHY. The CLKOUT0 output will be available after the software configures the clock output. The CLKOUT0 configuration is not recommended when support for Ethernet boot is required. CLKOUT0 connected as EPHY clock input is likely to glitch anytime the configuration is changed.

WKUP_CLKOUT0 is required to be configured to source the processor reference clock (MCU_OSC0_XO). The clock output does not glitch after the clock begins to toggle. However, the first high or low pulse can be short because reset is released asynchronous to the MCU_OSC0 clock.

Processor clock outputs performance is not defined in the processor-specific data sheet since the clock performance can be influenced by a number of variables unique to each custom board design. The recommendation for custom board designer is to validate timing of all peripherals by using the actual PCB delays, minimum or maximum output delay characteristics, and minimum setup and hold requirements of each device to confirm there is enough timing margin.

7.4.1.1.5 Ethernet PHY Pin Strapping

Some of the TI EPHy configure the outputs as inputs during reset and latch the EPHY configuration (pin strapping done through resistors) when the EPHY reset is released. Applying appropriate pullup or pulldown (as per EPHY recommendations) on strap inputs (IOs) is recommended (strap inputs also connects to processor IOs). TI EPHY used on the processor-specific SK use a combination of pullup and pulldown allowing multiple configuration modes to be configured with each pin. During processor reset, the IO buffers and internal pullup or pulldown are disabled, and minimizes any concern of a mid-supply voltage being applied to the processor input buffer by the EPHY. The EPHY is required to be configured to normal state from reset state to drive a valid logic state before enabling any of the associated processor input buffers.

7.4.1.1.6 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type fail-safe IO buffer. The recommendation is to connect external pullup (10kΩ or 47kΩ) when a PCB trace is connected and an external input is not being actively driven. Open-drain output type IO buffer has slew rate requirements specified when pulled up to 3.3V. An RC (delay) is recommended to limit the input slew rate. The capacitor is recommended to be placed near to the processor pin.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection

7.4.1.1.6.1 External Interrupt (EXTINTn) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Electrical characteristics (fail-safe and slew rate requirements when pulled to 3.3V).
3. Connection of pullup for EXTINTn IO.
4. Connection of pullup for EXTINTn IO when pulled to 3.3V.

Schematic Review

Follow the below list for the custom schematic design:

1. Pullup value used. The recommendation is to compare with the SK schematic implementation as a starting point.
2. Pullup referenced to (powered by) the processor VDDSHV0 (pullup connected to correct IO voltage level).
3. EXTINTn is an open-drain output type fail-safe IO buffer. An external pullup is recommended when a trace or external input is connected.
4. Open-drain output type IO buffer, EXTINTn has slew rate requirements specified when pulled to 3.3V supply. The recommendation is to add an RC at the input to limit the input slew rate. Refer TMDS64EVM.
5. RC value used for slew rate control. Refer TMDS64EVM. The recommendation is to connect capacitor near to the processor pin.

7.4.1.1.7 MAC (Media Access Controller) to MAC Interface

When implementing EPHY-less (MAC-to-MAC) connection between x2 processors, RGMII interface is recommended (check with TI if the MAC-to-MAC interface is officially supported on the selected processor family) since the clocks are source synchronous.

When MAC-to-MAC interface between x2 processors is implemented, the recommendation is to verify fail-safe operation, matching of clock specifications, and IO level compatibility.

7.4.1.1.8 MDIO (Management Data Input/Output) Interface

The processor IOs used for MDIO interface are referenced to (powered by) VDDSHV2 supply rail (IO supply for IO group 2).

The recommendation is to connect an external pullup (2.2kΩ (Follow EPHY recommendations), close to the EPHY) for the MDIO0_MDIO (MDIO data) signal.

For the MDIO_MDC, the recommendation is to verify if the EPHY supports internal pull (pulldown).

7.4.1.1.9 Ethernet MDI (Medium Dependent Interface) Including Magnetics

In case the EPHY and MDI (copper or fiber) interface including the magnetics and the RJ45 connector are implemented on the processor board, the recommendation is to follow the SK implementation for MDI interface connections, recommended magnetics (recommending using the magnetic used on the SK or similar) and connection of RJ45 connector shield to circuit ground. Provision for external ESD protection is recommended.

7.4.1.1.10 Capacitors for the Power Supply Rails

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDSHV2 supply rail and the attached device (CORE, ANALOG and IO supplies).

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.4.1.1.11 Ethernet Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. MAC interface configuration - RGMII or RMII.
3. IO level compatibility between processor MAC interface signals and EPHY (attached device).
4. Matching of processor and EPHY clock specifications.
5. Clocking of EPHy and processor MAC for RMII interface.
6. MAC-to-MAC interface connections.
7. MDIO interface and EPHY address configuration.
8. Implementation of EPHY reset logic.
9. Implementation of x2 EPHy reset logic.
10. Pullup on the MDIO interface MDC (clock signal) can be optional (EPHY can have internal pulldown; the recommendation is to verify the availability of pull in the EPHY data sheet).

Schematic Review

Follow the list below for the custom schematic design:

1. The recommendation is to compare the bulk and decoupling capacitors used for process and the EPHy supply rails with SK schematic implementation (when TI EPHY is used).
2. The recommendation is to provision for a series resistors (on the TDx signals near to processor MAC TDx output pins).
3. The recommendation is to verify the attached device IO supply and the IO supply for IO group VDDSHV2 referenced by (powered by) the processor MAC interface signals are connected to the same supply source and follow the ROC.
4. MDIO interface connection including pullup (2.2kΩ (Follow EPHY recommendations)) for MDIO data signal added near to the EPHY. MDIO connection to multiple devices and the addition of pullup near each EPHY. When more than x1 EPHY are used, configuration of EPHY address for MDIO interface.
5. A crystal with internal oscillator or an external oscillator for each EPHy or a common external oscillator with buffers (outputs are use case dependent) can be used.
6. The recommendation is to match the EPHy and the processor clock specifications.
7. Clocking of EPHy and processor MAC for RMII interface including addition of buffers (based on the EPHY configuration) and clock architecture (use of common Oscillator and Buffer with multiple outputs). In case processor clock output is connected to more than one input, each of the clock input is recommended to be the buffered output of the clock.
8. When MAC-to-MAC interface is used, the recommendation is to verify IO level compatibility, fail-safe operation (when x2 processor MACs are referenced to (powered by) different power sources) and matching of clock specifications.
9. The recommendation is to verify the EPHY reset implementation including ANDing logic, AND gate input pullup and EPHY reset input pull with the SK implementation when TI EPHY is used. A 3-input ANDing logic can be used to implement the attached device (EPHY) reset. Processor GPIO (used to locally reset the EPHY) is connected as one of the input to the ANDing logic AND gate with provision for pullup (to support boot) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other two inputs to the AND gate are the MAIN domain POR (cold reset) status output (PORz_OUT) and MAIN domain warm reset status output (RESETSTATz).
10. When more than one (x2) EPHy are used, the recommendation is to provide provision to reset the EPHy individually.

Additional

1. The recommendation is to follow the steps below recommended when TI EPHY is used:
    - Obtain a review of the implementation done with the EPHY business unit or product line.
    - The recommendation is to verify recommended bulk and decoupling capacitors are added and the power sequence requirements are followed.

    - The recommendation is to verify RBIAS resistor value & tolerance, selection of the RJ45 connector, external ESD protection provision for MDI signals and connection of RJ45 connector shield to circuit ground
2. A single channel (with single input and single output) buffers, or single input with dual or multiple output buffer can be used to connect the clock output of the oscillator to the processor and EPHy. For a specific use case (requirement for some of the industrial applications using a Time Sensitive Networking (TSN)), single input and two or more output (based on number of EPHy used) buffer is recommended for the processor and the EPHy.
3. When EPHY is configured as RMII peripheral, a single input (common clock input), two-output phase aligned buffer is recommended.
4. Consider adding 0Ω (optional and recommended when space is not a constraint) series resistors near to the attached device (EPHY) for the RDx signals.
5. To optimize the ANDing logic, it is ok to use a dual input AND gate with RESETSTATz and the processor GPIO as inputs. ANDing logic additionally performs IO level translation. The recommendation is to verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause supply leakage and affect board performance.
6. In case Ethernet boot is considered, the recommendation is to review the silicon errata, verify the supported EPHY interface configurations, MAC interface port used versus recommended, and the recommended clock and interface connection.

7.4.2 Universal Serial Bus (USB2.0)

The processor family supports x2 (two) instances of USB 2.0 interface ports. The USB interfaces (USB0, USB1 ports) can be configured as host or device or Dual-Role Device (DRD).

USBn_VBUS (n = 0-1) is recommended to be connected as per the *USB Design Guidelines* section of the processor-specific data sheet. The supply voltage range for the USBn_VBUS pins is defined in the *Recommended Operating Conditions* section of the processor-specific data sheet. The nominal input voltage applied is equal to the resistor divider output when VBUS supply voltage level is 5V.

USBn_ID functionality can be implemented using any of the processor GPIOs.

Note

USBn_VBUS are fail-safe inputs. The fail-safe input is valid only if the VBUS supply is connected through the recommended *USB VBUS Detect Voltage Divider / Clamp Circuit*.

7.4.2.1 USBn (n = 0-1) Interface When Used

The recommendation is to connect the USB supplies VDDA_CORE_USB (USB0 and USB1, core supply), VDDA_1P8_USB (USB0 and USB1, 1.8V analog supply), and VDDA_3P3_USB (USB0 and USB1, 3.3V analog supply) to the recommended power supply rails as per the processor-specific data sheet.

The recommendation is to connect USBn_DM (n = 0-1) and USBn_DP (n = 0-1) signals directly (without any series resistor or filter capacitor). The recommendation is to route USBn signals with traces that does not include any stubs or test points.

The recommendation is to connect a calibration resistor between USBn_RCALIB (n = 0-1) pin (close to processor RCALIB pin) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

7.4.2.1.1 USB Interface Configured as Host

The recommendation is to implement a USB power switch to control the VBUS supply to externally connected USB device. The power switch protects the on-board supply from overload (excess current draw).

The power switch output connects to the USB type A connector. The recommendation is to connect a capacitor (minimum value of 120µF) on the VBUS supply close to the connector.

The USBn_DRVVBUS (n = 0-1) signals (internal pulldown enabled during and after reset) can be used to enable the VBUS power switch. An external pullup near to the power switch enable (EN) pin is not recommended. External pulldown (10kΩ) is optional.

The recommendation is to use a USB power switch with OC (over current) indication, add a pullup (10kΩ or 47kΩ) and connect to the processor IO (input) to detect VBUS overload.

Connection of USBn_VBUS (VBUS supply input including Voltage Divider, Clamp) input is optional (not a requirement).

7.4.2.1.2 USB Interface Configured as Device

The VBUS power supply is sourced from an external host. USB standard recommends connecting < 10µF capacitor to the VBUS close to the USB Type-B connector.

The recommendation is to follow the *USB VBUS Design Guidelines* section of the processor-specific data sheet to divide the USB VBUS voltage (supply near the USB interface connector using resistor divider and zener diode protection) before connecting to USBn_VBUS input.

The zener diode protection (recommended) can be considered to be optional if custom board designer is absolutely sure that the board never sees a VBUS voltage > 5.5V (sourced on-board).

Connecting an on-board supply that is not switched (permanent) or connecting a permanent 3.3V supply with equivalent divider or connecting a permanent 1.65V directly to USBn_VBUS is not recommended or allowed. A switched supply that can be disconnected at the end of the session and switched back during the start of the next session is recommended.

7.4.2.1.3 USB Interface Configured as Dual-Role-Device

If the custom board uses USB Micro-AB connector, the USBn_ID signal from the connector is recommended to be routed to any of the processor pin. The GPIO pin used can be specified in the board device tree file, including the pinmux setting of the GPIO pin.

Note

Full compliant USB On-The-Go (OTG) feature is not supported. The USB ID pin is not bonded out.

7.4.2.1.4 USB Type-C

If the custom board design uses a USB Type-C® connector, the USBn_ID signal connection is not a requirement. The DRD mode switching is controlled by the USB Type-C companion device.

DRP (Dual Role Port) requires a controller, primarily to switch power based on the negotiated role. In a Device Mode only, USB2.0 only, USB Type-C implementations where the device is not powered by the USB Type-C connector, no USB Type-C controller is required.

- The CC pins at the connector are required to be independently grounded via 5.1kΩ resistors.
- The USB DP and USB DM connector pins are shorted on the PCB (DM=B7:A7, DP=B6:A6). Shorting allows for USB2.0 connectivity regardless of cable orientation. The recommendation is to keep the resulting stubs short.

Refer to the *USB VBUS Design Guidelines* section of the processor-specific data sheet for more information on USBn_VBUS input scaling recommendations.

The AM62x SK USB0 interface design can be a reference for implementation of the USB Type-C interface.

See the following FAQ:

[FAQ] SK-AM62A-LP: Is USB OTG possible without PD controller?

The FAQs are generic and can also be used for the AM62P, AM62P-Q1 processor family.

7.4.2.2 USBn (n = 0-1) Interface When Not Used

When USB0 and USB1 interfaces are not used in the custom board design, the recommendation is to provide provision to connect the USB interface signals (for the supported USB boot configuration (USB0 - DFU)) on the USB0 interface and also add provision to connect the required processor USB supplies for the initial board builds.

When both USB0 and USB1 are not used or USB0 or USB1 is not used, the interface signals and the supplies have specific connectivity requirements.

For connecting the USB0 and USB1, interface signals and supply pins, see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The recommendation is to connect the USB supplies (VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB) to VSS through separate 0Ω resistors.

In case USB0 or USB1 is planned to be used for future expansion, the recommendation is to connect the signals (USBn_DM, USBn_DP, USBn_RCALIB and USBn_VBUS) to a USB connector following the USB interface routing guidelines. The recommendation is to provide provision to connect the required supplies.

7.4.2.3 Additional Information

The recommendation is to connect USBn_DM and USBn_DP signals directly from the processor to the USB hub upstream port. The hub then distributes USBn signals to the downstream ports. As each hub has different implementation requirements, the recommendation is to follow the hub manufacturer recommendations.

For more information on USB2.0 interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – USB2.0 interface

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.4.2.4 USB Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Required USB interface configuration (Host or Device) and recommended connections.
3. Connection of USBn_VBUS. USB VBUS design guidelines based on the USB interface configuration.
4. Connection of USB supplies including filtering.
5. Connection of USB interface signals between processor and external USB interface connector.
6. Connection of recommended USBn calibration resistor.
7. Implementation of USB VBUS supply control power switch when USB interface is configured as host.
8. Implementation of pull for USBn_DRVVBUS.
9. USB power switch, EN using USBn_DRVVBUS and connection of power switch OC output to processor IO.
10. Provision for recommended capacitors on the USB VBUS pin near to the USB connector.
11. Provision for external ESD protections for the USB interface.
12. In case USB boot is implemented, the recommendation is to verify the silicon errata, supported interface configuration, USB port and the connections.
13. Fail-safe operation of USBn_VBUS and USB interface signals.

Schematic Review

Follow the list below for the custom schematic design:

1. The USB interface can be configured for Host (refer relevant SK schematics) or device or DRD.
2. Direct connection of the USB signals from the processor to the USB connector. USB interface connection matches the required USB interface configuration (Host or Device). Compare the implementation with SK schematic.
3. Any of the processor GPIO can be used to support DRD.
4. USBn_VBUS connection is optional for USB Host configuration.

5. The recommendation is to follow the processor-specific data sheet recommendations for VBUS voltage divider values and tolerance (±1%). Use of multiple resistors is allowed provided the total resistance value, tolerance and divider ratio is maintained over temperature and voltage. VBUS supply input protection (Zener protection and value) and VBUS capacitor values follow USB standards (refer SK).
6. USBn_DRVVBUS has an internal pulldown enabled during and after reset. Connecting pullup drives the attached device to mid-supply.
7. Power switch enable connection (in case processor USBn_DRVVBUS is used, pullup is not recommended or allowed since the USBn_DRVVBUS has an internal pulldown enabled during reset and after reset).
8. Connection of power switch OC output to the processor IO and IO level compatibility (pullup connection).
9. Connection of power supplies (core, peripheral and IO). A filtered supply (ferrite and capacitors) is used for VDDA_CORE_USB and VDDA_1P8_USB. VDDA_3P3_USB can be connected to the 3V3_SYS voltage. Refer to specific and latest SK for implementation as filters are being continuously optimized.
10. Processor USB peripheral supply rails connected follow the ROC.
11. Connection of 499Ω ±1% resistor to USB0 and USB1 RCALIB pins.
12. Connecting 5V supply from the USB connector directly to the USBn_VBUS pin is not recommended or allowed. Changing the processor-specific data sheet recommended VBUS divider and zener value is not recommended or allowed. Fail-safe capability support for VBUS input is valid only when the recommended divider values as per processor-specific data sheet is implemented.
13. Connection of the recommended capacitor based on the USB configuration. Refer SK schematics for implementation. For USB host, the recommendation is to connect a capacitor (minimum value of 120µF) on the VBUS supply close to the connector. For USB device, the VBUS power supply is sourced from an external host. USB standard recommends connecting < 10µF capacitor to the VBUS close to the USB Type-B connector.
14. The recommendation is to follow the pin connectivity requirements for connecting the USB core and peripheral when USB0 or USB1 is not used and USB0 and USB1 are not used.
15. USBn_VBUS capability is supported when the VBUS configuration as per the processor-specific data sheet is implemented.
16. USB interface signals are not fail-safe. No interface signals are recommended to be applied before the supplies ramp.

Additional

1. In case Type-C USB interface is implemented using TI devices, the recommendation is to obtain a review of the implementation with the relevant business unit or product line.
2. The recommendation is to verify fail-safe operation of USB interfaces. Applying an external interface signal before processor supply ramps can cause voltage feed and can affect the custom board functions.
3. Common-mode chokes (CMC) can be used on the USB interface signals for EMI control. CMC can reduce the signal amplitude and degrade USB interface performance (speed, data throughput, communication errors). Provision to bypass the CMC using 0Ω resistors is recommended. When a CMC is used on the USB interface signals, the recommendation is to verify the connections including the polarity. Reversing the CMC connection polarity can short the USB interface data signals.
4. DNI external pullup and pulldown connected to USBn_DRVVBUS pin to implement wakeup from deep sleep functionality.
5. The recommendation is to consider marking of differential signals and the differential impedance value.
6. In case USB interfaces are not used, the recommendation is to provide provision for USB0 DFU boot interface for the initial boards.

7.4.3 Universal Asynchronous Receiver/Transmitter (UART)

Note

The processor peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. The recommendation is to verify and use the correct IOSET in the custom board design. Timing closure for the interface is based the IOSETs.

The processor family supports x9 (nine) (x7 MAIN domain, x1 MCU domain, x1 WKUP domain) instances of UART interface and supported functions include data transfer (TXD, RXD), Modem control functions (CTS, RTS) and extended modem control signals (DCD, RI, DTR, DSR - supported by MAIN domain UART1).

For the number of UART instances supported, see the processor-specific data sheet. The recommendation is to refer the *Signal Descriptions* section of the processor-specific data sheet for the supported functionalities for each of the UART instances.

The recommendation is to verify the application requirements for UART interfaces (external communication interface or debug) and functions (configuration, 2-wire or 4-wire with flow control).

When an external RS232 transceiver is used, the recommendation is to match the external interface signal IO level and the dual-voltage IO supply for IO group operating voltage level. The recommendation is to power the IO supply of the external transceiver and the processor IO supply for IO group VDDSHVx from the same source. The recommendation is to verify fail-safe operation of the UART inputs and the voltage level connected to the external pull resistor.

The recommendation is to provision for series resistors (0Ω) on the interface signals, close to source, for isolation (debug) or control possible signal reflections.

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pullup (10kΩ or 47kΩ) is recommended on the processor UART receive inputs (UARTn_RXD [n = 0-6], MCU_UART0_RXD, and WKUP_UART0_RXD) in case the processor IOs can float (to prevent the attached device inputs from floating until driven by the host). The recommendation is to verify the availability of pulls on the external interface signal and populate the pulls accordingly. A pullup (47kΩ) is recommended on the processor UART transmit signals (UARTn_TXD [n = 0-6], MCU_UART0_TXD, and WKUP_UART0_TXD) in case the processor or the attached device outputs can float.

One of the common error observed when UART interface is used is UART interface signals polarity being reversed. The recommendation is to connect the signals as below:

- TX to RX
- RX to TX

The recommendation is to verify the connections, IO level and matching of polarity when additional UART interface flow control signals are used.

When external UART interface signals are connected directly to the processor UART interface, the recommendation is to verify IO level compatibility and fail-safe operation. The recommendation is to provide provision for external ESD protection.

The recommendation is to provision for connecting UART boot (UART0) for early board builds for board bring-up and debug.

7.4.3.1 UART Interface When Not Used

When UART interfaces are not implemented on the custom board design, the recommendation is to provide provision for connecting external UART interface signals for debug. The recommendation is to follow the below priority for provisioning the UART interface signals:

- UART0
- MCU_UART0
- WKUP_UART0

The recommendation is to add TPs on the processor board for connecting external inputs. The recommendation is to provide parallel pulls (10kΩ or 47kΩ) for the IOs that can float (to prevent the attached device inputs from floating until driven by the host). Provision for adding external ESD protection is recommended and can be populated when the UART interface is used.

The UART interface signals are not fail-safe. No external inputs (UART interface signals) is recommended to be applied before the processor supplies ramp.

7.4.3.2 Universal Asynchronous Receiver/Transmitter (UART) Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Provision for series resistors for interface signals near to the source.
3. Parallel pull provision added for the processor or attached device IOs.
4. Interface signals (data, direction control) connections.
5. Required communication speed (Baud rate) versus supported baud rates.
6. Required communication errors (%) versus calculated communication errors (%) due to internal clock divider mismatch.
7. Processor IO supply for IO group and the attached device IO supply connection.
8. Fail-safe operation of UART interface signals.
9. External ESD protection when the interface signals are connected directly to external inputs.

Schematic Review

Follow the below list for the custom schematic design:

1. Provision for series resistors (22Ω) near to source added for the interface signals to control possible signal reflections or isolate for testing.
2. Parallel pull (10kΩ or 47kΩ) provided for the interface signals that can float (to prevent the attached device inputs from floating until driven by the host).
3. Pullup referenced to (powered by) the processor VDDSHVx for corresponding UART instance and signals matches.
4. Interface signals (data, direction control) connections including signal polarity matching.
5. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) UART peripherals and attached devices IO supply are connected to the same power source and follow the ROC.
6. Provision for parallel pull added for any of the processor or attached device IOs that can float.
7. UART interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps.

Additional

1. The recommendation is to verify fail-safe operation when external interface signals are connected directly and are sourced from a different supply with respect to the processor IO supply for IO group.
2. Applying an external input signal to the processor UART inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
3. The recommendation is to provision for external ESD protection for the interface signals when external inputs are connected directly.
4. In case UART interfaces are not used, the recommendation is to provide provision for connecting the UART0, MCU_UART0 or WKUP_UART0 for debug.

7.4.4 Modular Controller Area Network (MCAN) with Full CAN-FD Support

Note

The processor peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. The recommendation is to verify and use the correct IOSET in the custom board design. Timing closure for the interface is based the IOSETs.

The processor family supports x4 (four) (x2 MAIN domain, x2 MCU domain) instances of Modular Controller Area Network (MCAN) with Full CAN-FD support.

The MCAN module supports both classic CAN and CAN-FD (CAN with Flexible Data-Rate) specifications.

The MCAN interface, interfaces to the attached device supporting MCAN interface through external MCAN transceiver.

In case an external transceiver is used, the recommendation is to match the external interface signal IO levels with the dual-voltage IO supply for IO group voltage level. The recommendation is to power the IO supply of the transceiver and the processor IO supply rail from the same source.

The recommendation is to provision for series resistors (0Ω) on the interface signals, close to source, for isolation (debug) or control possible signal reflections. Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pullup (47kΩ) is recommended on the processor MCAN transmit (receive) signals in case the processor or the attached device outputs can float.

The recommendation is to provide the recommended terminations for the MCAN transceiver external interface inputs.

7.4.4.1 Modular Controller Area Network Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Provision for series resistors added for all the interface signals near to the source.
3. Provision for parallel pull added for the processor or attached device interface IOs.
4. Connection of IO supply for IO group and attached device IO supply.
5. Fail-safe operation of MCAN interface signals.

Schematic Review

Follow the below list for the custom schematic design:

1. Series resistor value used (22Ω) and the placement (near to source).
2. Parallel pull value (10kΩ) added for any of the processor or attached device IOs that can float (to prevent the attached device inputs from floating until driven by the host).
3. Pullup referenced to (powered by) the processor VDDSHVx for corresponding MCAN instance and pins matches.
4. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) MCAN peripherals and attached devices IO supply are connected to the same power source and follow the ROC.
5. Provision for parallel pull added for any of the processor or attached device IOs that can float.
6. MCAN interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps.

Additional

1. Processor IOs are not fail-safe. No external input is recommended to be applied before the processor supply ramps. The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor MCAN inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. External ESD protection when the interface signals are connected directly to external inputs.

7.5 On-board Synchronous Communication Interface (MCSPI, MCASP and I2C)

7.5.1 Multichannel Serial Peripheral Interface (MCSPI) and Audio Peripheral - Multichannel Audio Serial Port (MCASP)

Note

The processor peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. The recommendation is to verify and use the correct IOSET in the custom board design. Timing closure for the interface is based the IOSETs.

Multichannel Serial Peripheral Interface (MCSPI):

The processor family supports x5 (five) (x3 MAIN domain, x2 MCU domain) instances of MCSPI. The MCSPI module is a multichannel transmit/receive, synchronous serial bus and can operate in controller mode or peripheral mode. In controller mode, the processor SPI interface sources the clock to the attached device. In peripheral mode, the attached device is required to source the SPI clock to processor.

A series resistor 22Ω is recommended (as a starting point) for the MCSPI clock output signals. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown (10kΩ) is recommended close to the attached device clock input pin. A pullup (10kΩ) is recommended for the chip select (CS) pin close to the attached device.

The MCSPI peripheral does not support boot. The OSPI0 interface supports SPI boot.

For the MCSPI interface SPIx_D0 and SPIx_D1 are the data lines. The data lines support programming the signals either to transmit data (transmission, output) or receive data (reception, input).

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A parallel pull (10kΩ or 47kΩ) is recommended for the processor or attached device data lines that can float (to prevent the attached device inputs from floating until driven by the host).

The recommendation is to connect the SPI interface to x1 (single) memory device. When connecting to multiple memory devices, the recommendation is to follow high-speed design practices and perform simulations to make sure the layout is not going to generate non-monotonic clock transitions when the single clock source is connected to multiple SPI attached devices.

See the following FAQs:

[FAQ] SK-AM64B: MCSPI Integration Guide

[FAQ] AM6412: AM64x SPI D0 and D1 - MISO/MOSI

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

Audio Peripheral - Multichannel Audio Serial Port (MCASP):

The processor family supports x3 (three) (x3 MAIN Domain) instances of Audio peripheral - Multichannel Audio Serial Port (MCASP). MCASP supports up to 4/6/16 Serial Data Pins (serializer) across x3 MCASP with Independent TX and RX Clocks. MCASP supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats. A series resistor 22Ω is recommended (as a starting point) for the MCASP clock output. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown (10kΩ) is recommended close to the attached device clock input pin.

Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A parallel pull (47kΩ) is recommended for the processor or attached device data lines that can float (to prevent the attached device inputs from floating until driven by the host).

The MCASP functions as a general-purpose audio serial port and are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Custom board hardware design - Queries related to MCASP

7.5.1.1 Connection of MCSPI and MCASP Interface Signals

For the MCSPI interface, the recommendation is to provide series resistors (22Ω) for SPI clock output signals SPI0..2_CLK (MCSPI 0..2) and MCU_SPI0..1_CLK (MCU_MCSPI 0..1 close to processors clock output pin (processor MCSPI is configured as controller) since the clock output is used for retiming.

For the MCASP interface, the recommendation is to provide series resistors (22Ω) for transmit clock (Transmit Bit Clock) output signals MCASP0..2_ACLKX and Transmit Frame Sync signals MCASP0..2_AFSX close to processors clock output pin (processor MCASP is configured to source the clock) since the clock output is used for retiming.

The recommendation is to add a pulldown (10kΩ) (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) for all IOs configured for MCSPI and MCASP interfaces.

The recommendation is to provide series resistors (22Ω) for receiver clock (Receive Bit Clock) output signals MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device).

For a number of processor IOs (LVCMOS or SDIO), the IO buffers TX (Output) and RX (Input) are disabled and internal pulls (pullup and pulldown) are turned off during reset and after reset. The recommendation is to verify if external pullups (10kΩ or 47kΩ) are provided for SPI Chip Select SPI0..2_CS0..3 (MCSPI 0..2) and MCU_SPI0..1_CS0..3 (MCU MCSPI 0..1) (close to attached device). The recommendation is to add pulls (10kΩ or 47kΩ) to the processor and the attached device signals (data interface - data in, data out) that can float (to prevent the attached device inputs from floating until driven by the host).

Two (x2) or more devices (common clock connection, different data signals connection, working simultaneously) are allowed to be connected to MCASP interface. The MCASP can be configured to have the transmit and receive sections operate synchronously to the transmit section clock and transmit frame sync signals. The BCLK and frame sync need to be the same for all target devices if using dedicated serializers, not an issue if using TDM. During custom board design, the potential of signal quality/signal reflections (signal reflections caused by driving multiple inputs from a single MCASP clock output) is something to be considered.

7.5.1.2 MCSPI Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Interface configuration and connections
3. Series resistor provision for clock output and placement
4. Series resistors provision for the interface signals near to the source
5. Connection of parallel pulls for clock, data and chip select
6. External SPI Chip Selects connection
7. Connection of IO supply for IO group and attached device IO supply.
8. Interface performance and signal integrity
9. Configuration of SPI data signals
10. Fail-safe operation of interface signals

Schematic Review

Follow the below list for the custom schematic design:

1. Interface configuration and recommended connections (including IOSET).
2. Series resistor 22Ω added to the clock output signal near to processor clock output pin (used for retiming).
3. Provision for series resistors added (optional) for the interface signals (to isolate for testing or to control possible signal reflections).
4. Pullup referenced to (powered by) the processor VDDSHVx for corresponding MCSPI instance and signals.

5. Processor VDDSHVx and the attached device IO supply are sourced from the same supply.
6. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) MCSPI peripherals and attached devices IO supply follow the ROC.
7. Pulldown (10kΩ) provision for MCSPI clock (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) for all IOs configured for MCSPI interfaces.
8. Provide provision for external pullups for SPI Chip Select SPI0..2_CS0..3 (MCSPI 0..2) and MCU_SPI0..1_CS0..3 (MCU MCSPI 0..1) (close to attached device). The recommendation is to add pulls to the processor and the attached device signals (data interface - data in, data out) that can float (to prevent the attached device inputs from floating until driven by the host). Pullup values used (10kΩ or 47kΩ).
9. Configuration of processor SPIx data bits D0 and D1 bits (data direction) matches the attached device and required pulls are added for signals that can float.
10. Parallel pull added for the processor or attached IOs that can float.
11. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices.
12. MCSPI interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps.

Additional

1. The recommendation is to verify fail-safe operation when processor IOs are directly connected to external interface signals or connector (through carrier board or add-on board). Applying an external input signal to the processor MCSPI inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. External ESD protection when the interface signals are connected directly to external inputs.

7.5.1.3 MCASP Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. MCASP interface configuration and connections.
3. Series resistor provision for clock output and placement.
4. Series resistors provision for the interface signals near to the source.
5. Connection of parallel pulls for clock and data.
6. Connection of IO supply for IO group and attached device IO supply.
7. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns.
8. Parallel pull for processor or attached IOs.
9. Connection of MCASP signals when connected to multiple attached devices.
10. Fail-safe operation of MCASP interface.

Schematic Review

Follow the below list for the custom schematic design:

1. MCASP interface configuration and recommended connections (including IOSET).
2. Series resistor (22Ω) added to the clock output signals (transmit bit clock, frame sync) near to the processor clock output pin (used for retiming).
3. Provision for series resistors added (optional) for the interface signals (to isolate for testing or to control possible signal reflections).
4. Pulldown (10kΩ) provision for the MCASP clock (close to attached device clock input pin) to hold the attached device in low state (there are cases where the clock is stopped or paused in a low logic state and the pulldown option is consistent with this logic state) for all IOs configured for MCASP interfaces.
5. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) MCASP peripherals and attached devices IO supply are sourced from the same supply and follow the ROC.

6. Pullup referenced to (powered by) the processor VDDSHVx for corresponding MCASP instance and signals.
7. Provide provision for external pullups for MCASP interface (Transmit or Receive) close to attached devices. The recommendation is to add pulls to the processor and the attached device signals (data interface - data in, data out) that can float (to prevent the attached device inputs from floating until driven by the host). Pullup values used (10kΩ or 47kΩ).
8. Interface performance (speed, data throughput, communication errors) and signal integrity related concerns have been analyzed (simulated) when connecting to multiple attached devices.
9. Connection of MCASP signals when connected to multiple attached devices. Follow general design guidelines to minimize stubs.
10. Parallel pull added for the processor or attached device IOs that can float.
11. MCASP interface signals are not fail-safe. The recommendation is to apply the inputs only after the processor supply ramps.

Additional

1. The recommendation is to verify fail-safe operation when connected to external signals. Applying an external input signal to the processor MCASP inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.
2. Connecting Two (x2) or more devices (common clock connection, different data signals connection, working simultaneously) to MCASP interface is supported. The recommendation is to follow good or recommended layout practices when routing the bit clock (transmit bit clock and receive bit clock). Perform simulations using IBIS model. The x2 devices (Example: Codec and amplifier) are recommended to be running with the same format (TDM/I2S/etc) and Codec and amplifier are recommended to be running with the same format (TDM/I2S/etc) and word size setup are synchronized with the bit clock and frame Sync.
3. External ESD protection when the interface signals are connected directly to external inputs.

7.5.2 Inter-Integrated Circuit (I2C)

Note

The processor peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. The recommendation is to verify and use the correct IOSET in the custom board design. Timing closure for the interface is based the IOSETs.

The processor family supports x6 (six) (x2 (two) I2C compliant, fail-safe open-drain output type IO buffer and x4 (four) LVCMOS buffer type emulated open-drain output type IO) instances of I2C interfaces. The supported I2C interfaces include x4 MAIN domain (LVCMOS IO buffers are used to emulate open-drain output type IO), x1 MCU domain (I2C compliant open-drain output type IO buffer) and x1 WKUP domain (I2C compliant open-drain output type IO buffer) I2C interfaces.

The MCU_I2C0 and WKUP_I2C0 interfaces are fail-safe, true open-drain output type IO buffers, and are fully compliant to the I2C specifications (Refer to the Philips I2C-bus specification version 2.1 for timing details).

The processor family includes multi controller Inter-Integrated Circuit (I2C) controllers, each of which provides an interface between a local host (LH, AM62Px processor) and any I2C-bus-compatible device that connects via the I2C bus.

Each I2C instance can be configured to be an I2C-compatible target or controller device. I2C interface can be implemented with dedicated, I2C compliant, open-drain output type IO buffers, or with standard LVCMOS IO buffers. The I2C instances associated with open-drain IO buffers support HS-mode (up to 3.4Mbps when the IO buffers are operating at 1.8V and support up to 400Kbps when the IO buffers are operating at 3.3V). The I2C instances associated with LVCMOS IO buffers support Fast-mode (up to 400Kbps).

7.5.2.1 I2C Interface Signals Connection

Note

For I2C interfaces with open-drain output type IO buffers (MCU_I2C0 and WKUP_I2C0), a pullup (4.7kΩ) is recommended irrespective of IO configuration. An external pullup is recommended even when the I2C interface (peripheral) is not used for alternate functions and is expected to be left unconnected.

Refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet. A pullup (4.7kΩ, adjust after testing) is recommended for the I2C interfaces. I2C interfaces support clock stretching. The clock output frequency (relative to the set frequency) has bus loading dependency. When difference is observed between the set frequency and the measured clock frequency, adjust the pullup (reduce) and measure the clock frequency.

Open-drain output type IO buffer I2C interface when pulled to 3.3V supply, have slew rate requirements specified. An RC (capacitor placed near to the processor I2C interface pins) is recommended to limit the slew rate. For RC implementation, see the AM64x EVM schematic and see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

For more information, see the *Connection of Supply Rails to External Pullups* section.

In applications where a number of I2C interfaces are required, I2C0, I2C1, I2C2, and I2C3 interfaces can be considered.

I2C0, I2C1, I2C2, and I2C3 interfaces use LVCMOS type IO buffer to emulate an open-drain output type IO and are not fully compliant with the I2C specification, in particular falling edges are fast (< 2ns). Review the exceptions (for I2C0, I2C1, I2C2, and I2C3 interface) in the processor-specific data sheet. A series resistor (47Ω, adjust after testing) is recommended to be placed near to the processor for the interface signals to control the fall time. The series resistor value is recommended to be finalized during testing.

Pullups (4.7kΩ, adjust after testing) are recommended for LVCMOS IOs when the IOs are configured for I2C functionality. The recommendation is to connect the pullups with the shortest stub.

For more information, see the following FAQs:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – I2C interface

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 and AM62D-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

Note

When I2C2 and I2C3 interfaces are used, refer to the I2C2 and I2C3 note (can be multiplexed to more than one pin) in the *Timing and Switching Characteristics, Peripherals, I2C* section of the processor-specific data sheet.

Note

The recommendation is to verify the *Exceptions* sub-section in the *Timing and Switching Characteristics, I2C* section of the processor-specific data sheet during the custom board design. Take note of the exceptions for the emulated open-drain output type IOs I2C interface. **The recommendation is to add a series resistor to control the fall time.**

7.5.2.2 I2C (Open-drain Output Type IO Buffer) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Timing and switching characteristics, and any additional information available.
3. I2C interface configuration, recommended connections and I2C interface pullup.
4. Slew rate requirements and connections for slew rate control.
5. Open-drain output I2C interface connections when interface is not used.
6. I2C instances and connection to multiple attached devices.
7. Terminations for attached device address inputs.

Schematic Review

Follow the below list for the custom schematic design:

1. WKUP_I2C0 and MCU_I2C0 I2C interfaces (controllers) are complaint open-drain output type IO buffers.
2. During processor cold reset and after reset, RX buffers are enabled, a pullup (4.7kΩ) is recommended irrespective of IO configuration.
3. During processor cold reset and after reset, RX buffers are enabled, a pullup is recommended irrespective of IO usage (including use case where I2C interface signals are planned to be left as NC).
4. The recommendation is to verify the pullup values used for the I2C interfaces with the SK schematic implementation or calculate the pullup value based on the load. A pullup (4.7kΩ, adjust after testing) is recommended for the I2C interfaces.
5. The I2C pullup supply voltage connected follows the steady-state maximum voltage specified for fail-safe IOs. The supply threshold depends on the supply voltage connected to IO supply for IO group.
6. RC for open-drain output type IO buffer for limiting the input slew rate when interface operates (pulled) at 3.3V. Capacitor connected near to the processor I2C interface pins when RC for input slew rate control is implemented. Verify the effect of RC on the I2C interface speed and adjust the RC as required.
7. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) I2C peripherals and attached devices IO supply are sourced from the same supply and follow ROC.
8. Attached device address inputs connected to IO supply through a resistor (> 1kΩ).
9. Processor supports multiple I2C instances. The recommendation is to verify that there are no I2C address conflicts on any of the I2C interface. In case additional I2C interfaces are required, an I2C switch can be used.

Additional

1. The recommendation is to review the *Timing and switching characteristics*, *I2C Exceptions* section of the processor-specific data sheet during the design stage and include the required circuit.
2. The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
3. The recommendation is to not place more than one set of pullup resistors on the I2C bus, the pullups can result in excessive loading and potential incorrect operation. Adjust the pullup value based on the bus speed configured.
4. The recommendation is to make sure IO supply for IO group powering the processor I2C IOs matches the supply voltage used for the pullup and the attached I2C devices IO supply. Connecting the pullups to proper supply level can prevent incorrect I2C interface operation.
5. I2C interfaces support clock stretching. The recommendation is to adjust the pullup in case the measured clock frequency does not match the configured frequency due to the bus loading or signal slew rate.

7.5.2.3 I2C (Emulated Open-drain Output Type IO) Interface Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Timing and switching characteristics, and any additional information available.
3. I2C interface configuration, I2C interface pullup requirements and connections.
4. I2C pullup when interface is not used.

5. I2C instances and connection to multiple attached devices.
6. Terminations for attached device address inputs.
7. Emulated open-drain output type I2C interface exceptions and connection requirements.

Schematic Review

Follow the below list for the custom schematic design:

1. I2C0, I2C1, I2C2 and I2C3 I2C interfaces are LVCMOS buffer type emulated open-drain output type IO.
2. I2C interface configuration and recommended connections (including grouping of the interface signals as per IOSET). I2C interface type and pullup requirements.
3. A pullup (4.7kΩ) is recommended when IO is configured as I2C interface.
4. The recommendation is to verify the pullup values used for the I2C interfaces with the SK schematic implementation or calculate the pullup value based on the load. A pullup (4.7kΩ, adjust after testing) is recommended for the I2C interfaces.
5. Pullup referenced to (powered by) the processor VDDSHVx (I2C pullup connected to correct voltage).
6. When I2C interface is not used, these IOs can be configured for alternate functions and the pulls are dependent on the IO function.
7. Supply rails connected to the IO supply for IO group VDDSHVx referenced to (powered by) I2C peripherals and attached devices IO supply are sourced from the same supply and follow the ROC.
8. Processor supports multiple I2C instances. The recommendation is to verify that there are no I2C address conflicts on any of the I2C interface. In case additional I2C interfaces are required, an I2C switch can be used.
9. Attached device address pin connected to IO supply through a resistor (> 1kΩ).
10. Note the I2C exceptions in the *Timing and Switching Characteristics* section of the processor-specific data sheet for emulated open-drain output type I2C interface. Series resistor (47Ω, adjust after testing) is recommended near to the processor I2C interface signals to control fall time.

Additional

1. I2C0, I2C1, I2C2, and I2C3 interfaces use LVCMOS type IO buffer to emulate an open-drain output type IO and are not fully compliant with the I2C specification, in particular falling edges are fast (< 2ns).
2. The recommendation is to review the *Timing and switching characteristics*, *I2C Exceptions* section of the processor-specific data sheet during the design stage.
3. The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
4. The recommendation is to not place more than one set of pullup resistors on the I2C bus, the pullups can result in excessive loading and potential incorrect operation. Adjust the pullup value based on the bus speed configured.
5. The recommendation is to make sure IO supply for IO group powering the processor I2C IOs matches the supply voltage used for the pullup and the attached I2C devices IO supply. Connecting the pullups to proper supply level can prevent incorrect I2C interface operation.
6. I2C interfaces support clock stretching. The recommendation is to adjust the pullup in case the measured clock frequency does not match the configured frequency due to the bus loading or signal slew rate.
7. Fail-safe interface support (emulated open-drain output type IOs are not fail-safe, no external input is recommended to be applied recommended to be applied before the processor IO supply ramps). The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor I2C inputs before processor supply ramps can cause voltage feed and can affect the custom board functions.

7.6 User Interface (CSIRX0, DPI, OLDI0, DSI), GPIO and Hardware Diagnostics

7.6.1 Camera Serial Interface (CSI-RX, CSI-2, CSIRX0)

The processor family supports x1 Camera Serial interface (CSI-RX, CSI-2, CSIRX0), x4 Lane with D-PHY (DPHY, DPHY_RX) and are MIPI CSI-2 v1.3 Compliant + MIPI D-PHY 1.2 compliant (CSIRX0). CSIRX0 supports up to x4 (1, 2, 3, or 4) Data Lane connection to D-PHY (DPHY_RX). For maximum supported data rate, see the *Multimedia, Camera Serial interface (CSI-2) Receiver with Lane D-PHY* section in the *Features* chapter of processor-specific data sheet.

The DPHY_RX (CSI-RX) supports a x1 (single) clock lane and all the data lanes are clocked at the same frequency. The frame rate is determined by start-of-frame, end-of-frame signaling and allows handling the input sources with different frame rates per channel.

7.6.1.1 CSIRX0 Peripheral When Used

The processor CSIRX0 peripheral is referenced to (powered by) VDDA_CORE_CSI_DSI and VDDA_CORE_DSI_CLK (CSIRX0 and DSITX0 core supplies), and VDDA_1P8_CSI_DSI (CSIRX0 and DSITX0 1.8V analog supply).

The recommendation is to connect a parallel resistor between CSI0_RXRCALIB (close to processor RXRCALIB pin) and VSS. Refer to the processor-specific data sheet for recommended resistor value and tolerance.

For more information on CSIRX0, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625SIP / AM625-Q1 / AM62Ax / AM62Px Custom board hardware design – CSI-2 capabilities

The FAQ includes information related to the allowed data lane and clock lane swapping.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.6.1.2 CSIRX0 Peripheral When Not Used

CSIRX0 peripheral when not used has specific connection requirements for interface signals and power supplies.

For connecting the interface signals, power supplies (core and analog), see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

When boundary scan function is used, CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) are recommended to be connected to the relevant (respective) supplies. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When boundary scan function is not used and DSITX0 interface is not used, the recommendation is to connect CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) to VSS through separate 0Ω resistors. Decoupling capacitors, bulk capacitors and ferrites can be deleted or depopulated.

CSI0_RXRCALIB resistor can be DNI when CSIRX0 interface is not used.

7.6.1.3 CSIRX0 Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the CSIRX0 peripheral signals to the attached device.
3. Connection of recommended external calibration resistor CSI0_RXRCALIB.
4. Connection of core and analog supply.
5. Fail-safe operation of CSIRX0 interface.

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the CSIRX0 peripheral signals with attached devices including the polarity.
2. Connection of 499Ω ±1% to CSI0_RXRCALIB pin and ground.

3. Ferrite and capacitors used for CSIRX0 analog and core supply, when CSIRX0 peripheral is used. Follow SK schematics.
4. Supply rails connected to the CSIRX0 peripheral supply rail and attached device IO supply are sourced from the same supply follow the ROC.
5. Pin connectivity requirement followed when CSIRX0 peripheral is not used and boundary scan functionality is required. IO calibration resistor can be DNI when CSIRX0 interface is not used, but boundary scan functionality is required.
6. Pin connectivity requirement followed when CSIRX0 peripheral is not used and boundary scan functionality is not required.
7. CSIRX0 inputs are not fail-safe. The recommendation is to not apply any CSIRX0 input until the processor peripheral supply ramps.

Additional

1. The recommendation is to provision for external ESD protection (based on the use case).
2. The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor CSIRX0 inputs before processor supply ramps can cause voltage feed and affect the board performance.
3. The recommendation is to include marking (optional) (100Ω) of differential signals and the differential impedance value.

7.6.2 Display Subsystem (DSS)

7.6.2.1 Display Parallel Interface (DPI)

Note

Refer to processor-specific data sheet and TRM for information related to supported data formats including BT656.

7.6.2.1.1 AM62P, AM62P-Q1 Processor Family

The processor family supports x1 24-bit per pixel, RGB/YUV422 modes, LVCMOS output, DPI (parallel) display interface instance.

For more information on DPI, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB- display interface

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

7.6.2.1.1.1 IO Power Supply

The processor DPI is referenced to (powered by) VDDSHV3 supply rail (IO supply for IO group 3).

7.6.2.1.1.2 Connection

Verifying display (RGB) connections.

DPI display interface support includes 12-, 16-, 18-, and 24-bit RGB active matrix displays. When connecting 16-bit data to an 18-bit panel (BGR565 to BGR666), the recommendations is to connect D0-D4 to B1-B5 of the LCD module input, D5-D10 to G0-G5 of the LCD module input, and D11-D15 to R1-R5 of the LCD module input connector. For the 18-bit interface, on the LCD module input side, the recommendations is to connect B0 to B5, R0 to R5, and R0 to R5.

7.6.2.1.1.3 DPI (Attached Device) Reset

The recommendation is to implement the attached device (LCD module) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup or pulldown (10kΩ or 47kΩ) (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (without ANDing logic) to reset the attached device,the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the DPI reset input can be slow and introduce too much delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.6.2.1.1.4 DPI Signals Connection

The recommendation is to provide provision for connecting a series resistor (0Ω) for VOUT0_PCLK (Pixel Clock Output) (close to processor clock output pin to control possible signal reflections). In case space is not a constraint, the recommendation is to add series resistors (0Ω) for all other control and data signals near to the processor pins.

7.6.2.1.1.5 Capacitors for the Power Supply Rail

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDSHV3 (supply rail referenced to (powered by) DPI interface signals) supply rail and the attached device.

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.6.2.1.1.6 DPI (VOUT0) Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Addition of series resistor for the pixel clock output signal.
3. Series resistors for the display interface DPI control and data interface signals.
4. Implementation of attached device reset logic.
5. External ESD protection.

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the interface signals including mapping of DPI pins of the processor with the attached device (RGB display) and display control signal.
2. Supply rails connected to the IO supply for IO group VDDSHV3 referenced to DPI peripheral and attached device IO supply follow the ROC.
3. The recommendation is to compare the decoupling capacitor of DPI IO supply with relevant SK.
4. Connection of series resistor (0Ω) for the clock output signal near to the processor clock output pin PCLK (to control possible signal reflections).
5. Series resistors for the display interface DPI control and data interface signals is optional. Adding the series resistors is recommended when space is not a constraint.
6. The recommendation is to implement the attached device (LCD module) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup or pulldown (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
7. The recommendation is to provision for external ESD protection (based on the use case).

7.6.2.2 Open LVDS Display Interface (OLDI0)

7.6.2.2.1 AM62P, AM62P-Q1 Processor Family

The processor family supports configuring the OLDI display interface for x2 OLDI-SL single-link (x4 (four) data lanes and x1 (single) clock lane) or x1 OLDI-DL dual-link (x8 (eight) data lanes and x2 (dual) clock lane) display mode. For OLDI-DL dual-link A0 through A3 correspond to the ODD pixels and A4 through A7 correspond to the even pairs.

When OLDI0 interface is configured for x2 OLDI-SL single-link display mode, the OLDI0 interface supports (can be configured) independent display streams (non-duplicate mode, non-mirrored mode).

Refer to the processor-specific data sheet for supported display resolution.

7.6.2.2.1.1 OLDI0 Display Interface Used

Refer below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62P / AM62P-Q1 Custom board hardware design – OLDI (Open LVDS Display Interface) capabilities

7.6.2.2.1.1.1 OLDI0 Interface Compatibility

For verifying the IO voltage level compatibility, see the *OLDI LVDS (OLDI) Electrical Characteristics* section of the processor-specific data sheet.

7.6.2.2.1.1.2 IO Power Supply

The processor OLDI0 interface is referenced to (powered by) VDDA_1P8_OLDI0 (OLDI0 1.8V analog supply rail).

7.6.2.2.1.1.3 OLDI0 (Attached Device) Reset

The recommendation is to implement the attached device (OLDI module) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup or pulldown (10kΩ or 47kΩ) (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (without ANDing logic) to reset the attached device,the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO level. A resistor divider can be used alternatively for level shifting, provided optimum value of the resistor divider is selected. If too high the rise/fall time of the OLDI0 reset input can be slow and introduce too much delay. Use of too low value resistors as divider causes the processor to source too much steady-state current during normal operation.

7.6.2.2.1.1.4 Capacitors for the Power Supply Rail

The recommendation is to verify (use recommended capacitors when recommendations are available or follow the relevant SK implementation) bulk and decoupling capacitors have been provided for VDDA_1P8_OLDI0 supply rail.

The recommendation is to follow the processor-specific SK implementation when recommendations are not available.

7.6.2.2.1.2 OLDI0 Peripheral Not Used

OLDI0 peripheral when not used has specific connection requirements. For connecting the OLDI0 peripheral see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

The OLDI0 1.8V analog supply rail (VDDA_1P8_OLDI0) is recommended to be connected to (powered by) a valid 1.8V source. Ferrite and bulk capacitors are optional.

7.6.2.2.1.3 Additional Information

The OLDI0 data and clock signals are recommended to be connected as point-to-point from the processor to the connector (display) without stubs.

Any board-level implementation is required to comply with the physical layer definition of *IEEE1596.3* standard and *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) interface Circuits)*.

7.6.2.2.1.4 OLDI0 Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the OLDI0 interface signals with attached devices.
3. Marking of differential signals and the differential impedance (100Ω) value.
4. Configuration of interface termination.
5. Connection of supply rail and addition of capacitors.
6. Implementation of attached device logic.
7. OLDI0 interface when not used.
8. The recommendation is to provision for external ESD protection (based on the use case).

Schematic Review

Follow the below list for the custom schematic design:

1. Supply rail connected to the OLDI0 interface peripheral rail on the processor and the attached device IO supply are sourced from the same supply and follow the ROC.
2. Connection of OLDI0 signals x1 8 lane (dual-link mode) and x2 4 lane (single-link mode) (supports independent display streams (non-duplicate mode, non mirrored mode))
3. Configuration of the required terminations (internal to the processor or attached devices).
4. Connection of the OLDI0 interface signals with attached devices including the polarity of the signals.
5. The recommendation is to implement the attached device (OLDI module) reset using a 2-input ANDing logic. Processor GPIO is connected as one of the input to the AND gate with provision for pullup or pulldown (pullup enabled) near to the ANDing logic AND gate input and provision for 0Ω to isolate the GPIO output for testing or debug. The other input to the AND gate is the MAIN domain warm reset status output (RESETSTATz).
6. When OLDI0 interface is not used, connection of the recommended power supply and signals as per the pin connectivity requirements.

7.6.2.3 Display Serial Interface (DSI)

7.6.2.3.1 AM62P, AM62P-Q1 Processor Family

The processor family supports display interface with x4 (four) data lanes and x1 (single) clock lane.

Refer processor-specific data sheet for supported display resolution.

7.6.2.3.1.1 DSITX0 Peripheral Used

The processor DSITX0 interface is referenced to (powered by) VDDA_CORE_CSI_DSI and VDDA_CORE_DSI_CLK (CSIRX0 and DSITX0 core supplies) and VDDA_1P8_CSI_DSI (CSIRX0 and DSITX0 1.8V analog supply).

The recommendation is to connect a parallel resistor between DSI0_TXRCALIB (close to processor) and VSS. Refer processor-specific data sheet for recommended resistor value and tolerance.

The recommendation is to follow the OLDI0 or the DPI0 attached device reset implementation in case the attached device is required to be reset.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.6.2.3.1.1.1 DSITX0 Peripheral Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the DSITX0 peripheral signals to the attached device.
3. Connection of recommended external calibration resistor DSI0_TXRCALIB.
4. Connection of core and analog supply.
5. Fail-safe operation of DSITX0 interface.

Schematic Review

Follow the below list for the custom schematic design:

1. Connection of the DSITX0 peripheral signals with attached devices including the polarity.
2. Connection of 499Ω ±1% to DSI0_TXRCALIB pin and ground.
3. Ferrite and capacitors used for DSITX0 analog and core supply, when DSITX0 peripheral is used. Follow SK schematics.
4. Supply rails connected to the DSITX0 peripheral supply rail and attached device IO supply are sourced from the same supply follow the ROC.
5. Pin connectivity requirement followed when DSITX0 peripheral is not used and boundary scan functionality is required. IO calibration resistor can be DNI when DSITX0 interface is not used, but boundary scan functionality is required.
6. Pin connectivity requirement followed when DSITX0 peripheral is not used and boundary scan functionality is not required.
7. DSITX0 inputs are not fail-safe. The recommendation is to not apply any DSITX0 input until the processor peripheral supply ramps.

Additional

1. The recommendation is to provision for external ESD protection (based on the use case).
2. The recommendation is to verify fail-safe operation when connected to external interface signals. Applying an external input signal to the processor DSITX0 inputs before processor supply ramps can cause voltage feed and affect the board performance.
3. The recommendation is to include marking (optional) (100Ω) of differential signals and the differential impedance value.

7.6.2.3.1.2 DSITX0 Peripheral Not Used

DSITX0 peripheral when not used has specific connection requirements for interface signals and power supplies.

For connecting the DSITX0 peripheral signals, power supplies (core and analog), see the *Pin Connectivity Requirements* section of the processor-specific data sheet.

When boundary scan function is used, CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) are recommended to be connected to the recommended supply rails. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When boundary scan function is not used and CSIRX0 interface is not used, the recommendations is to connect CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) to VSS through separate 0Ω resistors. Decoupling capacitors, bulk capacitors and ferrites are not recommended to be populated.

DSI0_TXRCALIB resistor can be DNI when DSITX0 interface is not used.

7.6.3 General Purpose Input/Output (GPIO)

Note

Read the note at the end of *Pin Connectivity Requirements* section of processor-specific data sheet for connecting processor IOs.

The processor family supports x2 GPIO module instances (GPIO0 and GPIO1) in the MAIN domain and x1 GPIO module instance MCU_GPIO0) in MCU domain. The general-purpose input/output (GPIO) peripheral supports signals (pins) that can be configured as either inputs or outputs. When configured as an output, software can write to internal registers to control the state driven on the output pins. When configured as an input, software can read the state of the input by reading the internal registers. In addition, the GPIO peripheral can generate host CPU interrupts and DMA synchronization events in different interrupt/event generation modes. The *Pin Attributes* and *Signal Descriptions* sections of the processor-specific data sheet provides information on the processor pins that can be configured as GPIOs (push-pull type) supporting LVCMOS and SDIO buffer types. Other type of IOs supported by the processor are also described in the *Pin Attributes* section.

Refer below FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to GPIO

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – Queries related to LVCMOS input Hysteresis

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Data sheet Pin Attributes and Pin connectivity related queries

7.6.3.1 Availability of CLKOUT on Processor GPIO

MCU_OSC0_XO can be configured as WKUP_CLKOUT0 output.

7.6.3.2 GPIO Connection and Addition of External Buffer

The recommendation is to add a series resistor (with a value that is use case dependent and limits the current as per the processor-specific data sheet). When loads that draw (require) higher currents (above the processor-specific data sheet values) are connected to the processor GPIO, the recommendation is to buffer the processor IO before connecting to the load.

Common processor LVCMOS IO interface guidelines:

1. A number of processor IO(s) are not fail-safe. No external input is recommended to be applied before processor supplies ramp.
2. Processor LVCMOS IOs have slew rate requirements (LVCMOS input slew is <1000ns), specified, applying a slow ramp input or connecting a capacitor directly at the input is not recommended.
3. Connecting a capacitor load > 22pF at the output is not recommended. DNI capacitor or perform simulations (based on the use case).
4. Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pull is recommended near to the attached device being driven by the processor IO that can float (to prevent the attached device inputs from floating until driven by the host).
5. A parallel pull (47kΩ) is recommended for any processor IO (pad) that has a trace connected but not being driven actively. When adding parallel pull is not feasible, the recommendation is to route the traces away from noisy signals.
6. The recommendation is to verify IO level compatibility, and fail-safe operation between the processor IO(s) and attached devices.

7.6.3.3 Additional Information

Pins (or Pads) of unused IOs can be left unconnected, unless otherwise stated. A number of IOs have a *Pad Configuration Register* that provides configuration control over the capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more information, refer to the *Control Module* chapter of the processor-specific TRM. Software can disable the IO receive buffers (that is, RXENABLE=0) that are not used in the design, as part of early initialization. The recommendation is for the software to not unexpectedly enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

Note

For guidance on configuring unused pins (or peripherals), the recommendation is to refer to the *Pin Connectivity Requirements* section of the processor-specific data sheet.

Note

PADCONFIG register bit configuration - ST_EN:

The recommendation is to keep the ST_EN bit enabled in case the PADCONFIG register is modified by the software. The minimum *Input Slew Rate* parameter defined in each *Electrical Characteristics* table is associated with long-term reliability. The parameters are not a function of the ST_EN bit. The schmitt trigger function implemented in the input buffer only changes the output results of the input buffer, by filtering noise pulses that do not exceed the hysteresis. The schmitt trigger function does not change how the input buffer operates when a application applies a slew rate to the IO input that is slower than defined in the processor-specific data sheet.

Note

For guidance on configuring the IOs, refer to the *Pad Configuration Registers* section of the processor-specific TRM.

Note

Specific peripherals and GPIOs support debounce functionality. The recommendation is to look for notes related to debounce functionality for peripherals or GPIOs in the *Signal Descriptions* section of processor-specific data sheet.

For more information on connection of unused processor peripherals and IOs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC peripherals and IOs connection when not used

For information on connecting (used/unused) processor pins, and peripherals, see the following FAQ:

[FAQ] AM62x, AM62Ax, AM62D-Q1, AM62L, AM62Px, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals and add pullup or pulldown? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...)

Refer to the note at the end of *Connectivity Requirements* section of the processor-specific data sheet while using the processor GPIOs.

7.6.3.4 GPIO Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the supplies to IO supply for IO groups (All IO pins referenced to (powered by) VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART to same voltage level).
3. IO level compatibility for the externally applied inputs.
4. Connection of processor IOs to IO supply or VSS.

5. LVCMOS (SDIO) input slew rate, connection of capacitor at the input or at the output of the processor IO.
6. Fail-safe operation of LVCMOS (SDIO) IOs and connection of multiple IOs together.
7. IO current sink or source follows the processor-specific data sheet recommendations. One of the common use case for the IO interface is driving LEDs for indication. The recommendation for custom board designer is to review the LED source or sink current, effect on the processor IO voltage level, and adjust the current. If continuous current draw is expected, the recommendation is to drive the LEDs using an external FET or Transistor based switch.
8. Relevant PADCONFIG register configuration based on the required IO functionality.

Schematic Review

Follow the below list for the custom schematic design:

1. Each IO has an associated supply voltage used to power the IO cell (VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART). In case VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART is sourced from 3.3V (1.8V) supply, all IO referenced to (powered by) VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART rails are recommended to be connected (operate) at 3.3V (1.8V) level.
2. The supply voltage for all pullups that are connected to processor IOs matches the voltage applied to the corresponding IO supply for IO group (VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART). Pulling a signal to a different IO voltage can cause voltage leakage (residual voltage).
3. Supply rail connected to the GPIO group referenced to (powered by) the IO supply for IO group VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART and the external inputs or GPIO pullup voltage level follow the ROC.
4. Directly connecting processor IOs to supply or VSS is not recommended or allowed, (including boot mode inputs). The custom board designer can have errors with the firmware and miss-configure the LVCMOS GPIOs that are intended as inputs, to be outputs driving logic high instead.
5. IO level compatibility for externally applied inputs from add-on or carrier board or external input is directly connected to the IOs through an external connector (provision for external ESD protection added).
6. External pulls are added for any of the processor (or attached device) IOs that can float (to prevent the attached device inputs from floating until driven by the host).
7. Input signal applied to the processor LVCMOS inputs follow the slew rate requirements as per processor-specific data sheet. Connecting a capacitor directly at the input can increase the signal slew and is not recommended.
8. Connection of capacitor load directly to the processor output for control or enabling of attached device is not allowed. Recommend simulation when capacitor load > 22pF (place holder) is used at the output of GPIO.
9. A number of processor IOs are not fail-safe. No external input voltage is allowed to be applied to the processor IOs before the IO supply for IO groups supply VDDSHVx or VDDSHV_MCU or VDDSHV_CANUART ramps (excluding fail-safe IOs).
10. Shorting of multiple IOs together directly is not recommended. Connecting the IOs to supply or ground directly is not recommended.

Additional

1. Provision for external ESD protection for external input directly connected to the IOs.
2. Common processor LVCMOS IO interface guidelines, refer to *GPIO Connection and External Buffering* of user's guide. A number of processor IOs (LVCMOS, SDIO) are not fail-safe. No external input is recommended to be applied before the processor supply ramps.
3. Processor IOs have slew rate requirements specified. Applying a slow ramp input or connecting a capacitor directly at the input is not recommended.
4. Connecting a capacitor load > 22pF (place holder) at the output is not recommended. DNI capacitor or perform simulations (based on the use case).
5. Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and pulldown)) turned off during reset and after reset. A pull is recommended for the attached device being driven by the processor IO that can float (to prevent the attached device inputs from floating until driven by the host).
6. A parallel pull (47kΩ) is recommended for any processor IO (pad) that has a trace connected and not being actively being driven. When adding a pull is not feasible, the recommendation is to route the traces away from noisy signals (Processor IO buffers are (TX (Output) and RX (Input) and internal pulls (pullup and

pulldown)) turned off during reset and after reset. A pullup (47kΩ) is recommended near to the attached device, to hold the attached device inputs that can float in a known state).

7. Fail-safe operation when connected to external signals. Applying an external input signal to the processor GPIO inputs before processor supply ramps can causes voltage feed and affects the board performance.
8. External ESD protection provision is recommended when the IOs are connected directly to external interface signals.
9. Fail-safe IOs include MCU_PORz, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn, and USBn_VBUS (n = 0-1), (when the recommended VBUS voltage divider as per the processor-specific data sheet is used).

7.6.4 On-board Hardware Diagnostics

7.6.4.1 Monitoring of On-board Supply Voltages Using Processor Voltage Monitors

Processor supply voltage monitors can be used to monitor on-board supplies generated using PMIC based or alternate power architecture, and input supply to the custom board connected from an external connector or carrier board. For voltage monitor VMON_VSYS detection to be effective, a 5V or higher (12V or 24V) DC voltage is divided using a resistor divider (0.45V is the monitor input) and connected to VMON_VSYS monitor input. The recommendation is to provide over voltage protection provision (parallel resistor or zener diode) when higher DC voltages are being monitored.

On-board 1.8V or 3.3V supplies can be directly connected to VMON_1P8_SOC and VMON_3P3_SOC.

7.6.4.1.1 Voltage Monitor Inputs Connection When Used

For the voltage monitor pin VMON_VSYS the recommendation is to always provision for external resistors (voltage divider) for early detection (indication) of supply failure irrespective of the software implementation. The recommendation is to connect 5V or above for the detection to be effective. For connecting the on-board voltage (main supply voltage such as 5V or 12V or 24V) through an external resistor voltage divider, see the *System Power Supply Monitor Design Guidelines* section of the processor-specific data sheet. The recommendation is to implement a noise filter (capacitor) at (across) the resistor output connected to the VMON_VSYS input since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients.

The recommendation is to connect VMON_1P8_SOC and VMON_3P3_SOC pins directly to the respective supplies (without any external filter capacitor added). See the *Recommended Operating Conditions* section of the processor-specific data sheet for the allowed supply voltage range.

Note

For VMON_VSYS, fail-safe condition is valid when the recommendations in section *System Power Supply Monitor Design Guidelines* of processor-specific data sheet are followed.

For VMON_1P8_SOC and VMON_3P3_SOC pins, fail-safe condition is valid when the supply voltage connected is within the *Recommended Operating Conditions* section of processor-specific data sheet.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Custom board hardware design – POK VMON Voltage Monitor

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design – Power OK (POK) Module Voltages Monitored and Connection recommendations

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to passive components values, tolerance, voltage rating

7.6.4.1.1.1 Voltage Monitor Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. The recommendation is to always provide provision to connect an external resistor divider as per *System Power Supply Monitor Design Guidelines* section of the processor-specific data sheet for early detect using VMON_VSYS.
3. Voltage level monitored by VMON_VSYS.
4. Connection of voltage to be monitored by processor VMON_VSYS input.
5. Voltage divider recommendations including addition of filter capacitor across the VMON_VSYS divider.
6. Connection of VMON_1P8_SOC and VMON_3P3_SOC.

Schematic Review

Follow the below list for the custom schematic design:

1. For voltage monitor VMON_VSYS detection to be effective, the recommendation is to connect a DC voltage of 5V or higher (12V or 24V) using resistor divider.
2. Resistors with ±1% tolerance are used for the VMON voltage divider resistors.
3. Addition of filter capacitor across the VMON_VSYS divider connected to the processor monitor input. Refer processor-specific data sheet section *System Power Supply Monitor Design Guidelines*. The value of the capacitor is determined by the custom board designer based on the trip time requirement.
4. Connection of 1.8V to VMON_1P8_SOC and 3.3V to VMON_3P3_SOC pins directly without any external filter capacitors.

Additional

1. The recommendation is to always implement (provision on the board) the voltage monitoring functionality using VMON_VSYS for early detection of input supply failure. Voltage monitor VMON_VSYS is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example: 5V, 12V, or 24V. The error associated with the VMON_VSYS voltage monitor requires you to set the threshold significantly lower than the nominal operating range to avoid false trigger and hence the recommendation to monitor input voltage rather than the processor rails. Refer *System Power Supply Monitor Design Guidelines* section of the processor-specific data sheet.

7.6.4.1.2 Voltage Monitor Inputs Connection When Not Used

The recommendation is to always connect (use) voltage monitor VMON_VSYS for early input supply failure detection (indication). When VMON_SYS is not used, the recommendation is to connect VMON_VSYS pin to VSS through a 0Ω resistors and add a test point for future expansion (follow pin connectivity requirements).

For connecting voltage monitor inputs VMON_3P3_SOC and VMON_1P8_SOC when not used, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design – Power OK (POK) Module Voltages Monitored and Connection recommendations

7.6.4.2 Internal Temperature Monitoring

The Voltage and Thermal Manager (VTM) module on the processor supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

Independent temperature sensors are located at designated hotspots on the processor. The recommendation is to read the on-die temperature sensors in Linux and perform thermal management. See the *E2E thread*.

The processor supports one VTM module, VTM0, which is located in the WKUP domain.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x (ALV, ALX) Custom board hardware design – Voltage and Thermal Manager (VTM)

7.6.4.2.1 Internal Temperature Monitoring Checklist

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide.
2. Connection of the recommended supply to the temperature sensor supply pins.
3. Addition of filter capacitors for the TEMPn (n = 0-2) sensor analog supply pins.

7.6.4.3 Connection of Error Signal Output (MCU_ERRORn)

The recommendation is to connect the MCU_ERRORn signal as per the *Pin Connectivity Requirements* section of the processor-specific data sheet for testing or when using the signal for other board level functions.

7.6.4.4 High Frequency Oscillator (MCU_OSC0) Clock Loss Detection

The processor family supports HFOSC0 clock loss detection circuitry to detect HFOSC0_CLK malfunction (stops). Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL [8] CLKLOSS_SWTCH_EN is set, the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the processor to operate with a slower clock.

During clock-loss condition, the processor reports the error to the external device through MCU_ERRORn pin by driving the pin low. The recovery mechanism is up to the external device (such as a PMIC to take action).

Example, doing a full board power cycle for the board to recover. If the board does not recover then the processor has to indicate custom board designer to take alternate actions or perform board level tests such as checking on-board system clocks, external crystal or supply rails.

See the following FAQ:

[FAQ] AM6422: How to Switch Back to External Clock After Clock Loss Detection

The FAQs are generic and can also be used for the AM62P, AM62P-Q1 processor family.

7.6.4.4.1 Crystal or External Oscillator Mal-function

During cold reset (power-on reset), in case the crystal or the external oscillator does not generate the clock, the processor is likely to not start-up.

7.7 SK Specific Circuit Implementation (Reuse)

In case some of the SK implementation listed below are reused:

- DPI to HDMI
- AUDIO CODEC
- FT4232 UART TO USB BRIDGE
- XDS110 DEBUGGER
- CPSW3G RGMII 1 – PHY
- M.2 INTERFACE – SDIO
- CURRENT MONITORING DEVICES
- USB TYPE-C PD CONTROLLER AND POWER SUPPLY

The recommendation is to follow the below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Guidelines for reuse of SK specific implementations listed below on custom board design

7.8 Performing Board Level Testing During Custom Board Bring-up

7.8.1 Processor Pin Configuration Using PinMux Tool

The recommendation is to verify the processor peripheral and IO configuration using the TI *SysConfig-PinMux* tool to take care valid IOSETs have been configured.

For more information, see the PinmuxConfigSummary.csv file provided by the SysConfig-PinMux tool.

7.8.2 Schematics Configurations

The recommendation is to verify the circuit options provided for alternate functionality or testing that are required to be DNI during normal functioning of the board (populating the components can affect or influence custom board performance) are marked as DNI in the custom board design and are not populated on the board before powering the board.

7.8.3 Connection of Supply Rails to External Pullups

Connecting processor IO pullup to a different IO supply rail/operating voltage (does not match the voltage level of IO supply for IO group referenced by the IO group) can cause voltage leakage on the IO rail and affect the custom board performance or processor reliability. Each signal has an associated IO supply for IO group (Example: VDDSHVx [x = 0-3, 5-6]). For more information, see the *Pin Attributes* table in the processor-specific data sheet.

For example, to pullup SPI0_CLK signal in GPIO MUX mode (GPIO1_17), connect the external pullup to supply rail connected to IO supply for IO group VDDSHV0.

7.8.4 Peripheral (Subsystem) Clock Outputs

For any of the processor peripheral that includes a clock output, the recommendation is to configure the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx, CTRLMMR_PADCONFIGy registers. The bit configuration is required for the clock output to work properly.

7.8.5 General Board Bring-up and Debug

Board bring-up tips before starting the board bring-up, includes verifying the following:
- The processor, attached devices and other components assembled matches the design (custom board schematics and the custom board design requirements)
- Assembled boards have been inspected for mounting of components as per BOM (including DNI, Do Not Install components). The assembled board has been inspected for assembly (soldering of the components and soldering workmanship)
- No external inputs are connected to the processor inputs before the custom board supply is applied and the processor supplies ramps

See the following FAQ:

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px)

7.8.5.1 Clock Output for Board Bring-Up, Test, or Debug

The following clock outputs are available on the processor for test and debug purposes only:

MCU_SYSCLKOUT0

MCU_PLL0_HSDIV0_CLKOUT (MCU_SYSCLKOUT0) is divided by 4 and connected to specific pins named MCU_SYSCLKOUT0. The clock output is provided for test or debug purposes only.

SYSCLKOUT0

MAIN_PLL0_HSDIV0_CLKOUT (SYSCLKOUT0) is divided by 4 and connected to specific pins named SYSCLKOUT0. The clock output is provided for test or debug purposes only.

OBSCLK0, OBSCLK1, MCU_OBSCLK0

Observation clock (OBSCLK0, OBSCLK1 and MCU_OBSCLK0) outputs are recommended to be used for test or debug purpose only. Observation clocks can be used to select one of the several internal clocks as output. The observation clock is not expected to be used as a clock source for any external device. As stated in the processor-specific data sheet, OBSCLK0, OBSCLK1 and MCU_OBSCLK0 signals are provided for test or debug purpose only.

The recommendation is to provide TPs and parallel pulls (10kΩ or 47kΩ) when feasible for the processor pins designated MCU_SYSCLKOUT0, SYSCLKOUT0, OBSCLK0, OBSCLK1 and MCU_OBSCLK0.

In case the clock output pins are configured for alternate functions, the recommendation is to insert a TP on the trace and provide provision to isolated the signals from the attached device for test or debug.

7.8.5.2 Additional Information

The recommendation is to provide test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT for testing or debug when not used.

For on-board attached devices (discrete DC/DC or LDO or Temperature sensor or Voltage monitors) that have an alert output, over-current indication output or PG (power good) output, the recommendation is to provide a pullup (10kΩ) and test point for testing or future enhancements (when not used).

7.8.5.3 General Board Bring-up and Debug Checklist

General

Review and verify the following for the custom board schematic design:

1. Provision for isolating the circuit sections.
2. Provision to external debug interface.

Schematic Review

Follow the below list for the custom schematic design:

1. The recommendation is to add provision to isolate the IOs that can be used for debug from alternate function.
2. Provision to connect the debug UARTs have been provided (UART0, MCU_UART0, WKUP_UART0). The recommendation is to add provision for connecting UART interfaces for debug during initial board build.
3. The recommendation is to add provision for JTAG connector or Test points for JTAG interface signals. The recommendation is to place the pulls as per pin connectivity requirements near to the processor JTAG interface pins.
4. The required pullup and series resistors are provided for the UART interface signals.
5. External ESD protection provision added when external interface signals are directly connected to the processor UART signals. The recommendation is to add provision for external ESD protection for the JTAG interface signals.

Additional

1. A number of processor IOs including UARTs are not fail-safe. The recommendation is to connect external inputs only after the processor supplies ramps.
2. The recommendation is to disconnect the external interface signals in case the processor board is powered off.

Refer below FAQ:

[FAQ] SK-AM62: Purpose Of Different UARTs

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

8 Self-Review of Custom Board Schematic Design

Note

During the custom board design cycle, the recommendation is to follow *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processor Family* user's guide along with *Schematic Design Guidelines and Schematic Review Checklist* user's guide.

The next phase of the custom board design once the required schematics updates are complete (following the user's guide, referring to the SK schematic implementation, hardware design considerations user's guide and other collaterals on TI.com), is to perform a self-review following the review checklist provided at the end of each section of the schematic design guidelines. Schematic review checklist in excel format can be used alternatively to perform the review and the schematics in excel format can be used to track the completion of schematic review section wise.

Example of schematic review checklist sections for self-review:

- *Processor Core and Peripheral Core Power Supply Checklist*
- *General Board Bring-up and Debug Checklist*

The below FAQ lists the available collaterals and review steps that can be followed by custom board designer while performing a self-review of custom board schematics:

[FAQ] AM62P / AM62P-Q1 Design Recommendations / Custom board hardware design - Custom board schematics self-review

The below FAQ lists common errors observed (based on review of multiple customer schematics and reference to multiple collaterals). The recommendation is to read the list of errors and make the required updates to the custom board schematics:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - List of errors observed during customer schematics review

9 Custom Board Layout Notes (Added Near to the Schematic Sections) and General Guidelines

The recommendation is to consider adding the required or applicable design notes for the processor, attached devices and other on-board devices to reduce errors during custom board design. The recommendation is to add the required design notes for the processor memory (Example: USB2.0 interface, Ethernet interface, Camera interface, Display (OLDI0, DSITX0) interfaces including eMMC, OSPI, SD card, SDIO and other used processor peripherals including USB, MCSPI, MCASP). The recommendation is to include notes to include custom board boot mode configurations, placement of series and parallel resistors, placement of decoupling and bulk capacitors.

The recommendation is to mark all differential signals, critical signals that can affect performance and specify the target impedance (as required). See the following examples:

- The differential impedance for the USB2.0 data lines is expected to be within the specified tolerance for a nominal value of 90Ω.
- The differential impedance for the CSIRX0, DSITX0 and OLDI0 interface signals is expected to be within the specified tolerance for a nominal value of 100Ω.

Note

Refer to the *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines* for the recommended target impedance for the LPDDR4 clock, address and control signals.

See the following FAQs that includes board layout guideline to follow:

[FAQ] AM625: PCB Pattern Recommendations for Specific Peripherals

[FAQ] AM625: MMC0 PCB Connectivity Requirements

AM6442: PCB layout guidelines for MMCSD0(eMMC) and MMCSD1(SD card)

The FAQs are generic and can also be used for AM62P, AM62P-Q1 processor family.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

9.1 Layout Considerations

General

Review and verify the following for the custom schematic design:

1. Reviewed above "Common checklist for all sections" section of the user's guide
2. Is the custom board designed to be compliant to the PCB trace delay requirements defined in the *Timing Conditions* table found in the *Timing and Switching Characteristics* section of the processor-specific data sheet
3. *Applications, Implementation, and Layout* section of the processor-specific data sheet and followed the relevant sections
4. General high-speed guidelines have been followed

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

10 Custom Board Design Simulation

The baseline drive impedance and ODT settings for attached memory (LPDDR4) are derived from the signal integrity (SI) simulations performed on the SK.

The recommendation is to perform simulation on the custom board design to finalize the values as the configuration values can be different compared to the SK schematic implementation.

The below FAQs can be referenced when simulations are performed:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62L / AM62P / AM62P-Q1 / AM64x / AM243x Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM243x (ALV), AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px

To get an overview of the board extraction, board simulation, and analysis methodologies for high speed LPDDR4 interfaces, see the *LPDDR4 Board Design Simulations* chapter of the *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines* application note.

The drive strength can be adjusted using the *DDR Register Configuration Tool* on SysConfig.

For more information on configuring the DDRSS registers, see the following FAQ:

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design – Processor DDR Subsystem and Device Register configuration

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

For queries related to PDN power SI simulations, see the following FAQ:

[FAQ] AM62A3-Q1: AM62A3-Q1 PDN Power SI SIMULATION Questions

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

10.1 DDR-MARGIN-FW

The DDR margin firmware and supporting scripts allow visualization and measurement of custom board margin in the DDR interface on board. The tools enable probe-less measurement of critical data signals to understand if the custom board design follows the recommended design guidelines of the interface.

DDR-MARGIN-FW - Firmware and scripts to measure system DDR margin

For more information, see the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Question about AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP DDR MARGIN TEST Tool

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

11 Additional References

Additional references include FAQs and *Hardware Design Considerations for Custom Board Design* user's guide for specific processor. Schematics for attached devices including PMIC and EPHY.

11.1 FAQs Covering AM64x, AM243x, AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62Lx Processor Families

The below FAQ summarizes key collaterals that can be referenced during custom board schematic design and custom board schematic review:

[FAQ] AM64x, AM243x (ALV, ALX), AM62x, AM62Ax, AM62Px, AM62D-Q1, AM62L Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

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Note

While using the SK PDF schematics with D-Notes and R-Notes for custom board schematics review, the recommendation is to view the FAQ links added on the schematics for additional information.

11.2 FAQs - Processor Product Family Wise and Sitara Processor Families

Based on TI sitara processor applications and systems team interactions with multiple custom board designers, queries from custom board designers and learnings from queries received from custom board designers and review of internal collaterals, FAQs have been created (related to (detailed explanation and example illustrations added) processor functioning, processor power and IO connections, processor peripherals and interfaces, processor evaluation SK, common errors observed during customer board design reviews, data sheet and pin attributes and commonly asked E2E queries) to support custom board designers during the custom board design phase. Refer the following list of FAQs is recommended during custom board design along with other available design collaterals including *Hardware Design Considerations for Custom Board Design* and *Schematic Design Guidelines and Schematic Review Checklist* on TI.com:

AM62Px Processor Family:

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

AM62Lx Processor Family:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

AM62Ax and AM62D-Q1 Processor Family:

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

AM62x Processor Family:

[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Sitara Processor Families:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

See the following FAQ that provides list of all the available FAQs including software related FAQs for sitara processor families:

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

Note

The FAQs are being updated frequently. The recommendation is to review the FAQs of interest and the FAQ master list at regular intervals for availability of updated information.

11.3 Schematics Review (Self) and Schematic Review Request (Suppliers)

As per of the custom board design cycle, the recommendation is to perform self review, team review and as required external review with the suppliers.

In case a schematics review request is required to be submitted to TI, the recommendation is to follow the below FAQ:

[FAQ] Sitara MPU Hardware Applications Support - Schematics review request

The FAQ is generic and can also be used for AM62P, AM62P-Q1 processor family.

11.4 Processor Attached Devices Checklist

Ethernet PHY PCB Design Layout Checklist

TPS65219 Schematic, Layout Checklist

TPS65931211-Q1 PMIC User Guide for AM62A

Note

The recommendation is to verify availability of device-specific schematic review checklist on TI.com for the attached devices and verify the custom board schematic implementation using the available checklist.

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12 User's Guide Content and Usage Summary

The user's guide includes schematic design guidelines and schematic review checklist for use by custom board designers during the custom board schematic design and custom board schematics review. The recommendations provided in user's guide can be used by custom board designers to optimize the custom board design, reduce schematic design errors, reduce custom board bring-up time, reduce custom board debug time and can possibly minimize future board re-spins.

13 References

13.1 AM62P, AM62P-Q1

- Texas Instruments, *AM62Px Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Px Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Px Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62P-LP*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62P, AM62P-Q1 Processors Family*, user's guide
- Texas Instruments, *AM62P Power Estimation Tool*, application note
- Texas Instruments, *PMIC for Powering AM62Px Devices*, application note
- Texas Instruments, *AM62Px Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *SK-AM62P-LP Design Package Folder and Files List*, product overview
- Texas Instruments, *Sitara AM62P Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.2 AM62L

- Texas Instruments: *AM62Lx Sitara Processors*, Data Sheet
- Texas Instruments: *AM62L Sitara Processors*, Technical Reference Manual
- Texas Instruments: *AM62Lx Sitara Processors Silicon Errata*
- Texas Instruments: *EVM TMDS62LEVM*, product page
- Texas Instruments: *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family*, user's guide
- Texas Instruments: *AM62x, AM62Lx DDR Board Design and Layout Guidelines*, application note
- Texas Instruments: *AM62Lx Escape Routing for PCB Design*, application note
- Texas Instruments: *AM62L Maximum Current Ratings*, application note
- Texas Instruments: *AM62L Power Supply Implementation*, application note
- Texas Instruments: *AM62L Product Overview*, application note
- Texas Instruments: *Sitara AM62Lx Benchmarks*, application note

13.3 AM62A7, AM62A3, AM62A7-Q1, AM62A3-Q1, AM62A1-Q1

- Texas Instruments, *AM62Ax Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Ax Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Ax Silicon Errata*
- Texas Instruments, *Starter Kit SK-AM62A-LP*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 and AM62D-Q1 Processor Families*, user's guide

- Texas Instruments, *AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 & AM62D-Q1 Processor Families Schematic Design Guidelines & Schematic Review Checklist*, user's guide
- Texas Instruments, *AM62Ax Maximum Current Ratings*, application note
- Texas Instruments, *AM62Ax Power Estimation Tool*, application note
- Texas Instruments, *PMIC Solution for AM62Ax*, product overview
- Texas Instruments, *PMIC for Powering AM62Px Devices*, product overview
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*, user's guide
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *SK-AM62A-LP Design Package Folder and Files List*, product overview
- Texas Instruments, *Sitara AM62Ax Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.4 AM62D-Q1

- Texas Instruments, *AM62Dx Sitara Processors*, Data Sheet
- Texas Instruments, *AM62Dx Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62Dx Sitara Processors Silicon Errata, Silicon Revision 1.0*
- Texas Instruments, *AUDIO-AM62D-EVM*, product page
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 and AM62D-Q1 Processor Families*, user's guide
- Texas Instruments, *AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1, AM62A1-Q1 & AM62D-Q1 Processor Families Schematic Design Guidelines & Schematic Review Checklist*, user's guide
- Texas Instruments, *PMIC Solution for AM62Ax*, product overview
- Texas Instruments, *PMIC for Powering AM62Px Devices*, product overview
- Texas Instruments, *AM62Ax/AM62Dx Escape Routing for PCB Design*, user's guide
- Texas Instruments, *AM62Ax, AM62Px, AM62Dx LPDDR4 Board Design and Layout Guidelines*, application note
- Texas Instruments, *Sitara AM62Dx Benchmarks*, application note
- Texas Instruments, *Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs*, application brief

13.5 AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP

- Texas Instruments, *AM62x Sitara Processors*, Data Sheet
- Texas Instruments, *AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*, Data Sheet
- Texas Instruments, *AM62x Sitara Processors*, Technical Reference Manual
- Texas Instruments, *AM62x Silicon Errata*
- Texas Instruments, *Hardware Design Considerations for Custom Board Design Using AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family*, user's guide
- Texas Instruments, *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* , user's guide
- Texas Instruments, *Starter Kit SK-AM62B-P1*, product page
- Texas Instruments, *Starter Kit SK-AM62B for discrete power solution*, product page
- Texas Instruments, *Starter Kit SK-AM62-LP*, product page
- Texas Instruments, *Starter Kit SK-AM62-SIP*, product page
- Texas Instruments, *AM62x Power Consumption*, application note
- Texas Instruments, *AM62x Maximum Current Ratings*, application note
- Texas Instruments, *AM62x Power Estimation Tool*, application note
- Texas Instruments, *Powering the AM62x With the TPS65219 PMIC*, application note
- Texas Instruments, *Powering the AM625SIP With the TPS65219 PMIC*, application note
- Texas Instruments, *Discrete Power Solution for AM62x*, application note
- Texas Instruments, *AM62 Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62x (AMC) Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62x SiP Escape Routing for PCB Design*, application note
- Texas Instruments, *AM62x, AM62Lx DDR Board Design and Layout Guidelines*, application note
- Texas Instruments, *PRU-ICSS Feature Comparison*, application note

- Texas Instruments, *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*, application brief
- Texas Instruments, *AM625SIP: System In Package Explained*, product overview
- Texas Instruments, *SK-AM62B-P1 Design Package Content Overview*, product overview
- Texas Instruments, *SK-AM62-LP Design Package Content Overview*, product overview
- Texas Instruments, *SK-AM62-SIP Design Package Folder and Files List*, product overview
- Texas Instruments, *SK-AM62B Design Package Folder and Files List*, product overview
- Texas Instruments, *Sitara AM62x Benchmarks*, application note

13.6 Common for all Processor Families

- Texas Instruments, *AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1, AM62A3, AM62A7, AM62A7-Q1, AM62D-Q1, AM62P-Q1 Schematic Design Guidelines and Review Checklist* application note
- Texas Instruments, *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note
- Texas Instruments, *High-Speed Interface Layout Guidelines* application note
- Texas Instruments, *High-Speed Layout Guidelines* application note
- Texas Instruments, *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines* application note
- Texas Instruments, *Thermal Design Guide for DSP and Arm Application Processors* application note
- Texas Instruments, *Emulation and Trace Headers Technical Reference Manual* user's guide
- Texas Instruments, *XDS Target Connection Guide* application note
- Texas Instruments, *Interface Circuits for TIA/EIA-644 (LVDS)* design consideration
- Texas Instruments, *General Hardware Design/BGA PCB Design/BGA Decoupling* application note
- Texas Instruments, *MSL Ratings and Reflow Profiles* application note
- Texas Instruments, *Moisture sensitivity level search*packaging search
- Texas Instruments, *Clocking Design Guide for KeyStone Devices* application note
- Texas Instruments, *Hardware Design Guide for KeyStone II Devices* application note
- Texas Instruments, *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design* design guide
- Texas Instruments, *Jacinto 7 DDRSS Register Configuration Tool* application note
- Texas Instruments, *Using IBIS Models for Timing Analysis* application note
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs* application note
- Texas Instruments, *McASP Design Guide - Tips, Tricks, and Practical Examples* application note
- Texas Instruments, *Driving Multiple Loads With a Single LVCMOS Oscillator* application note

13.7 Master List of Available FAQs - Processor Family Wise

A complete list of the FAQs are available that is recommended to quickly view the available list of FAQs for the selected processor or processor families.

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

13.8 Master List of Available FAQs - Sitara Processor Families

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

13.9 FAQs Including Software Related

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

13.10 FAQs for Attached Devices

[FAQ] DP83869-EP: Ethernet compliance Testing failure

[FAQ] List of FAQs for TPS6594-Q1, TPS6593-Q1, LP8764-Q1 PMICs

[FAQ] TPS65219: Benefits of a PMIC vs discrete solution to power Sitara AM62x MPU

14 Terminology

BOM	Bill of Materials
CAN	Controller Area Network
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
CSIRX	Camera Streaming Interface Receiver
DDR0_CAL0	IO Pad Calibration Resistor
DFU	Device Firmware Upgrade
DNI	Do Not Install
DPI	Display Parallel Interface
DRD	Dual-Role Device
DSI	Display Serial Interface
E2E	Engineer to Engineer
ECC	Error-Correcting Code
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EOS	Electrical Over-Stress
ESD	Electrostatic discharge
ESL	Effective Series Inductance
ESR	Effective Series Resistance
FAQ	Frequently Asked Question
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IEP	Industrial Ethernet Peripheral
JTAG	Joint Test Action Group
LDO	Low Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
MAC	Media Access Controller
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interface
MCU	Micro Controller Unit

MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MMC	Multi-Media Card
MMCSD	Multi-Media Card/Secure Digital
ODT	On-die Termination
OLDI	Open LVDS Display Interface
OPN	Orderable Part Number
OSPI	Octal Serial Peripheral Interface
PCB	Printed Circuit Board
PDN	Power Distribution Network
PET	Power Estimation Tool
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROC	Processor-specific Data Sheet Recommended Operating Condition
SD	Secure Digital
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TEN	Test Enable
TMS	Test Mode Select Input
TRC_DATAn	Trace Data n
TRM	Technical Reference Manual
TRSTn	Reset
UART	Universal Asynchronous Receiver/Transmitter
WKUP	Wake-up
XDS	eXtended Development System
ZQ	Memory Device Calibration reference resistor

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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• (User's Guide Usage Guidelines): Added all processor GPNs	3
• Added section Common Checklist for Use With All Schematic Design Guidelines and Schematics Review Sections	3
• Added section Custom Board Schematic Design Implementation Checklist Sub-Sections Description	4
• Added section Common Checklist for Use With All Schematic Design Guidelines and Schematics Review Sections	4
• (Processor-Specific Information): Added Note	6
• (Selection of Processor OPN (Orderable Part Number)): Added packages to all GPNs	6
• (Processor-specific Data Sheet Use Case and Version Referenced for User's Guide Edits): Added more information about data sheet includes and updated data sheet revision (available on TI.com)	6
• (Processor Power Architecture): Added Note	7
• (Discrete Power Devices (DC/DC, LDO) Based Power Architecture): Added Queries related to Discrete power Architecture FAQ and added more information about the MCU_PORz input	10
• (General Recommendations): Added Note	13
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• Added section Processor-Specific SDK	18
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• (Custom Board High-Speed Interface Design Guidelines): Added Links to documents for General High Speed Layout Guidelines FAQ	20
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• (Processor-Specific Recommendations for Power, Clock, Reset, Boot and Debug): Added Note	23
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• (AM62P, AM62P-Q1 Processor Family): Added Queries related to passive components values, tolerance, voltage rating FAQ and more information about MMC0 interface	50

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