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Taking Advantage of Using the dMAX DMA Engine in Conjunction with the McASP Peripheral on the TMS320C67x™ DSP

SEE THE FUTURE
CREATE YOUR OWN

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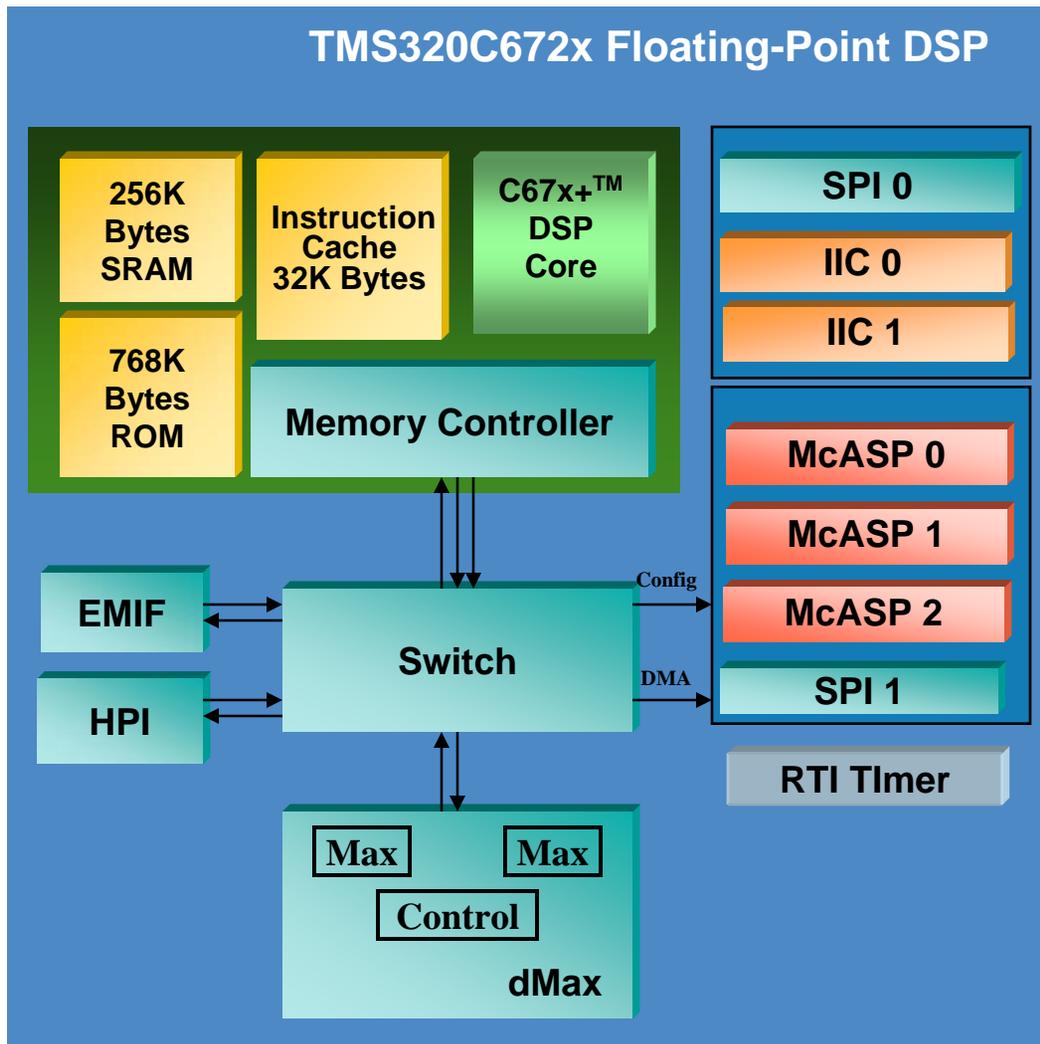Title: Application Engineer
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SPRP498

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TMS320C672x™ Device Overview

TMS320C672x Floating-Point DSP

- 256K Bytes SRAM
- Instruction Cache 32K Bytes
- C67x+™ DSP Core
- 768K Bytes ROM
- Memory Controller
- SPI 0
- IIC 0
- IIC 1
- McASP 0
- McASP 1
- McASP 2
- SPI 1
- RTI TImer
- EMIF
- HPI
- Switch
- Config
- DMA
- dMax
  - Max
  - Max
  - Control

300 MHz DSP core

- 300 MHz 67x+™ core
- 64 Reg + Additional FP instructions
- Code Compatible with 6713 Devices

Large on-chip memory

- 768KB on-chip ROM
- 256KB on-chip RAM
- 32KB Inst. cache (Int Mem + EMIF)
- EMIF for expansion

Enhanced Audio IO

- 16 serial data pins
- Up to 6 different clock rates
- dMAX
  - Support for dma, circular and multi-tap memory delay (for Reverb)
- HPI supports mux A/D and non-mux A/D

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TMS320C6727/C6726/C6722 – High Performance Audio Processors and Low System Cost Options

	C6722 200/250 MHz	**C6726** 250 MHz	**C6727** 250/300 MHz
MFLOPS	1200/1350	1350	1350/1800
Memory	128 K Bytes SRAM 384 K Bytes ROM 32 K Bytes Instr. Cache	256 K Bytes SRAM 384 K Bytes ROM 32 K Bytes Instr. Cache	256 K Bytes SRAM 384 K Bytes ROM 32 K Bytes Instr. Cache
McASP	2	3	3
I²C	2	2	2
SPI	2	2	2
HPI	N/A	N/A	Yes
EMIF	16-bit	16-bit	32-bit
dMax	Yes	Yes	Yes
Availability	Today!	Today!	Today!

Software Compatible

Typical Applications

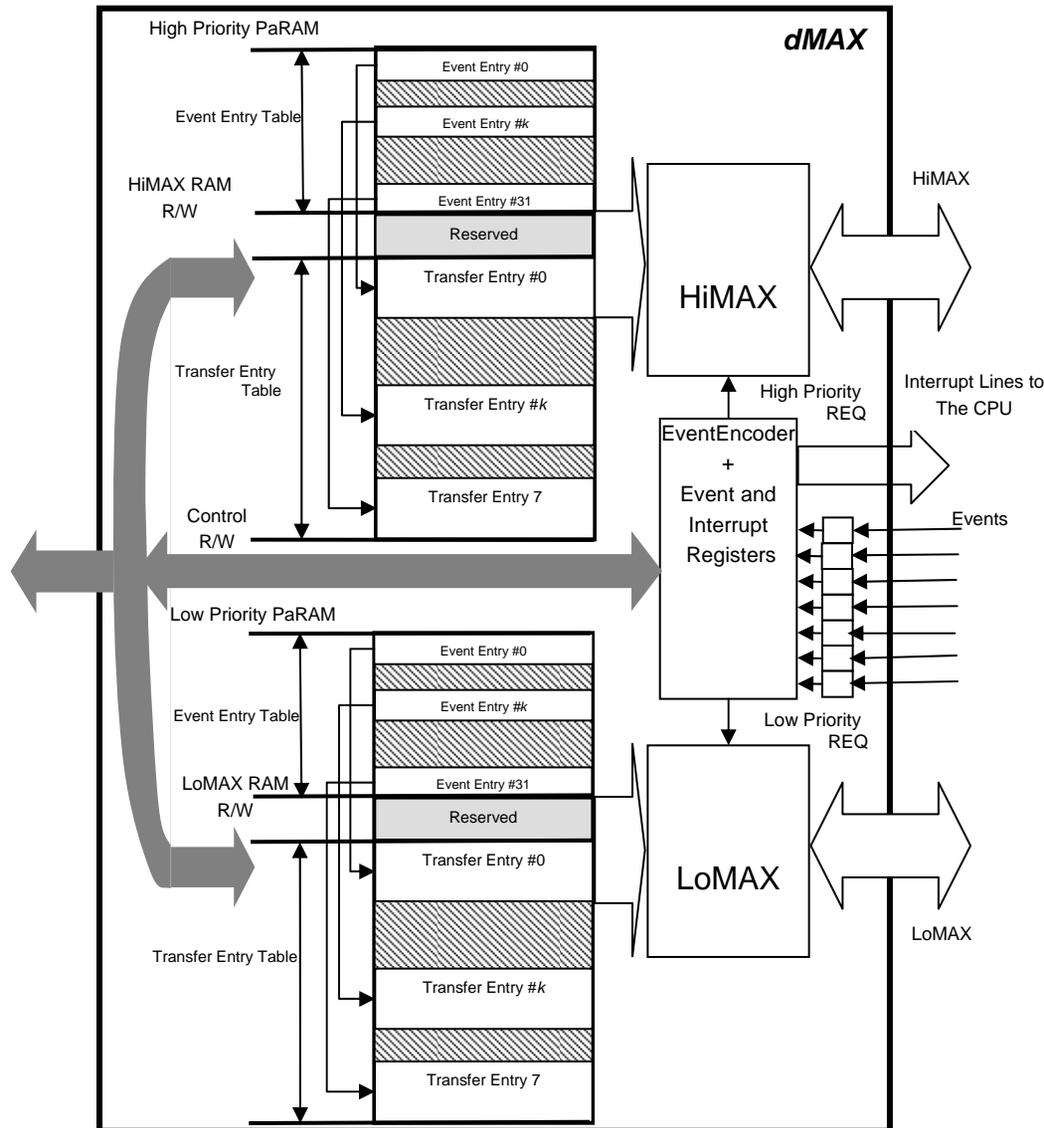Musical Instruments — Sound and musical modification and generation

Audio conferencing

Audio broadcast, encoding and studio applications

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dMAX Block Diagram

The dMAX comprises:

- **Event and interrupt processing registers.**
- **Event encoder.**
- **Address generation hardware for High Priority Event (HiMAX)**
- **Address generation hardware for Low Priority Event (LoMAX).**
- **High priority event Parameter RAM (HiPaRAM).**
- **Low priority event Parameter RAM (LoPaRAM).**

Transfers Supported

- **General Purpose (1D, 2D, 3D)**
- **FIFO Read, FIFO Write**
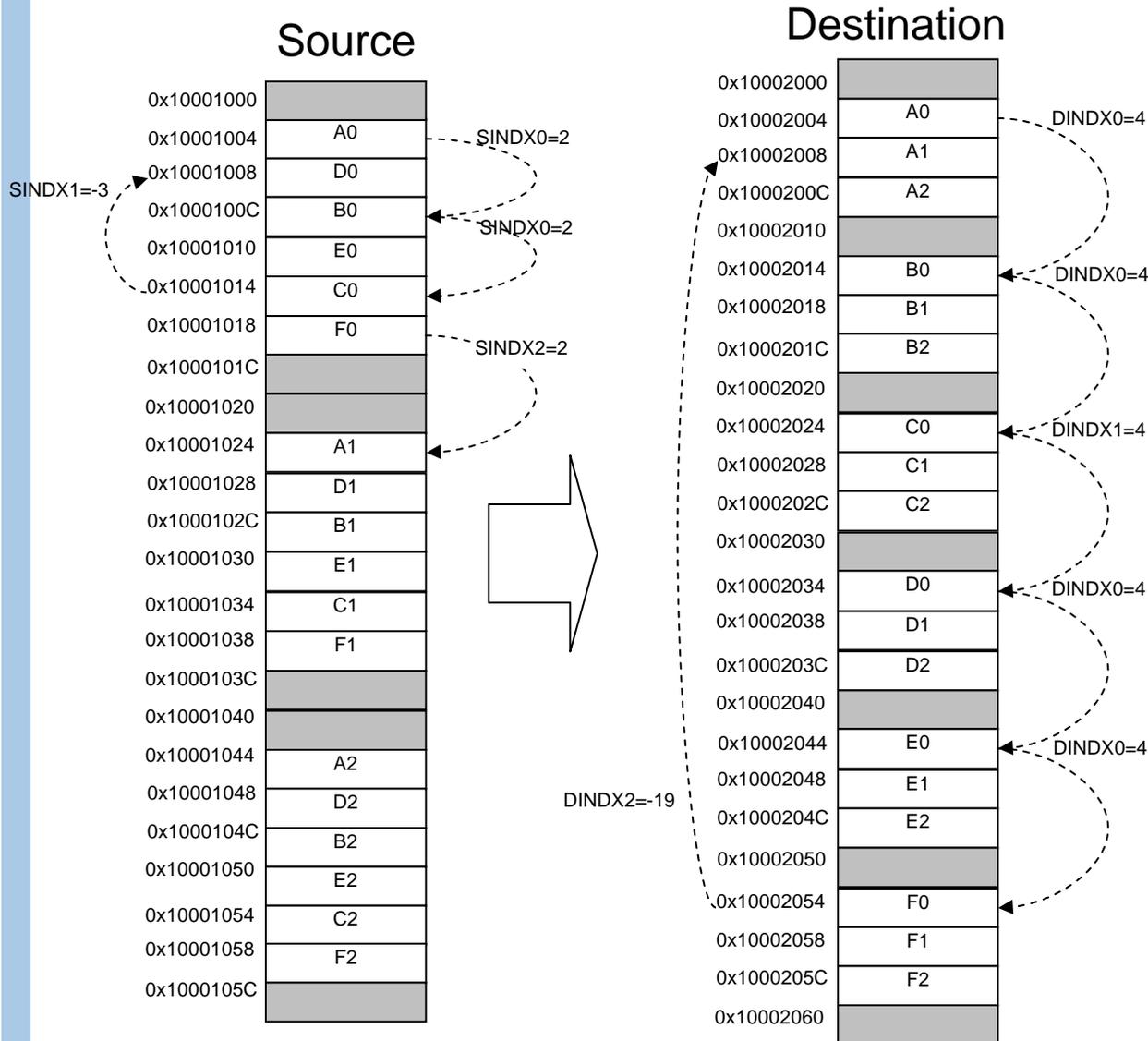- **One Dimensional burst**
- **SPI Slave data transfer**

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McASP Block Diagram
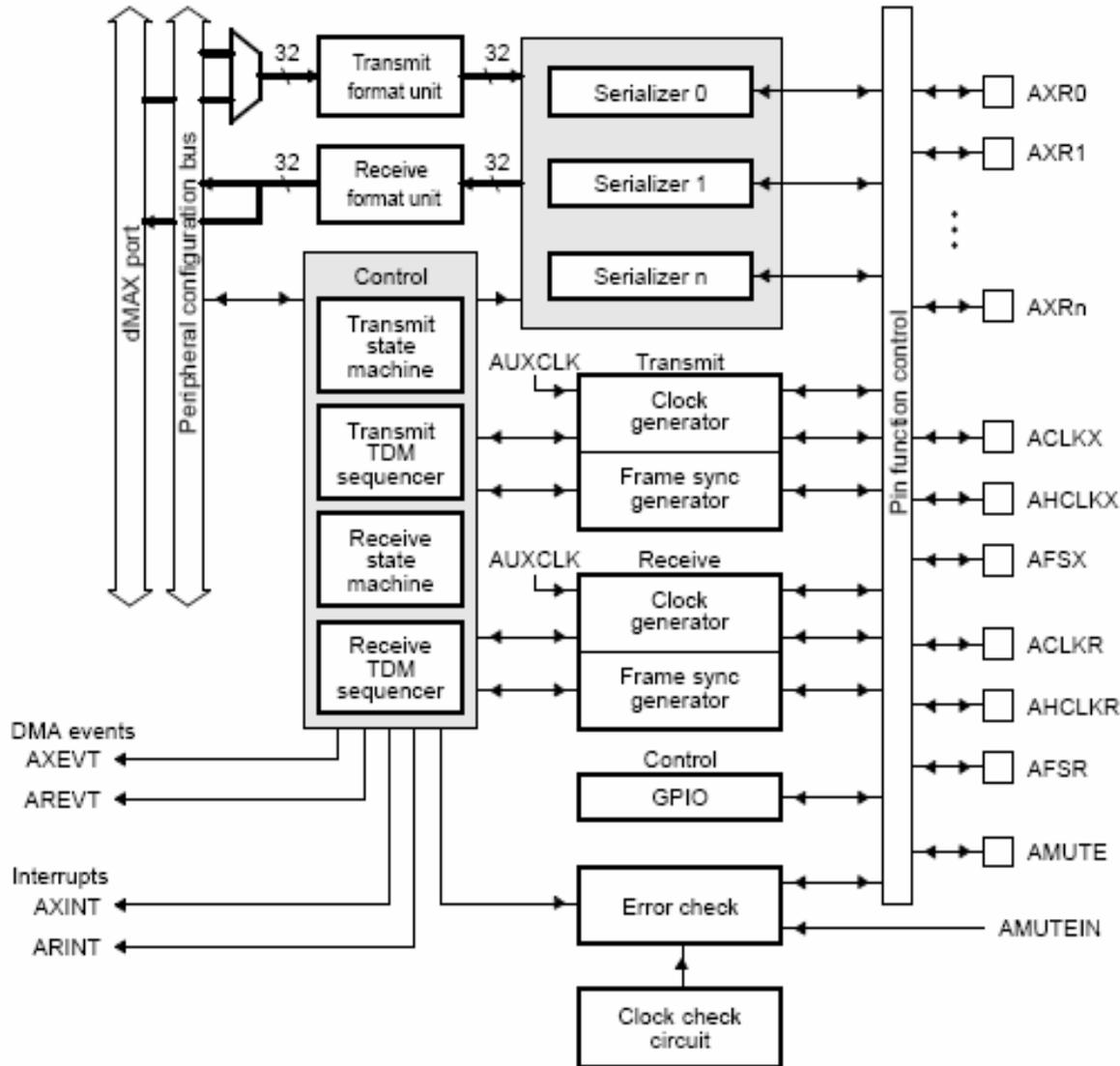
Features:

- **Independent clock generator modules for transmit and receive**

- **TDM streams from 2 to 32, and 384 time slots**

- **Data formatter for bit manipulation**

- **Up to 16 individually assignable serial data pins**

- **Wide variety of I2S and similar bit-stream format**

- **S/PDIF, IEC60958-1, AES-3 formats**
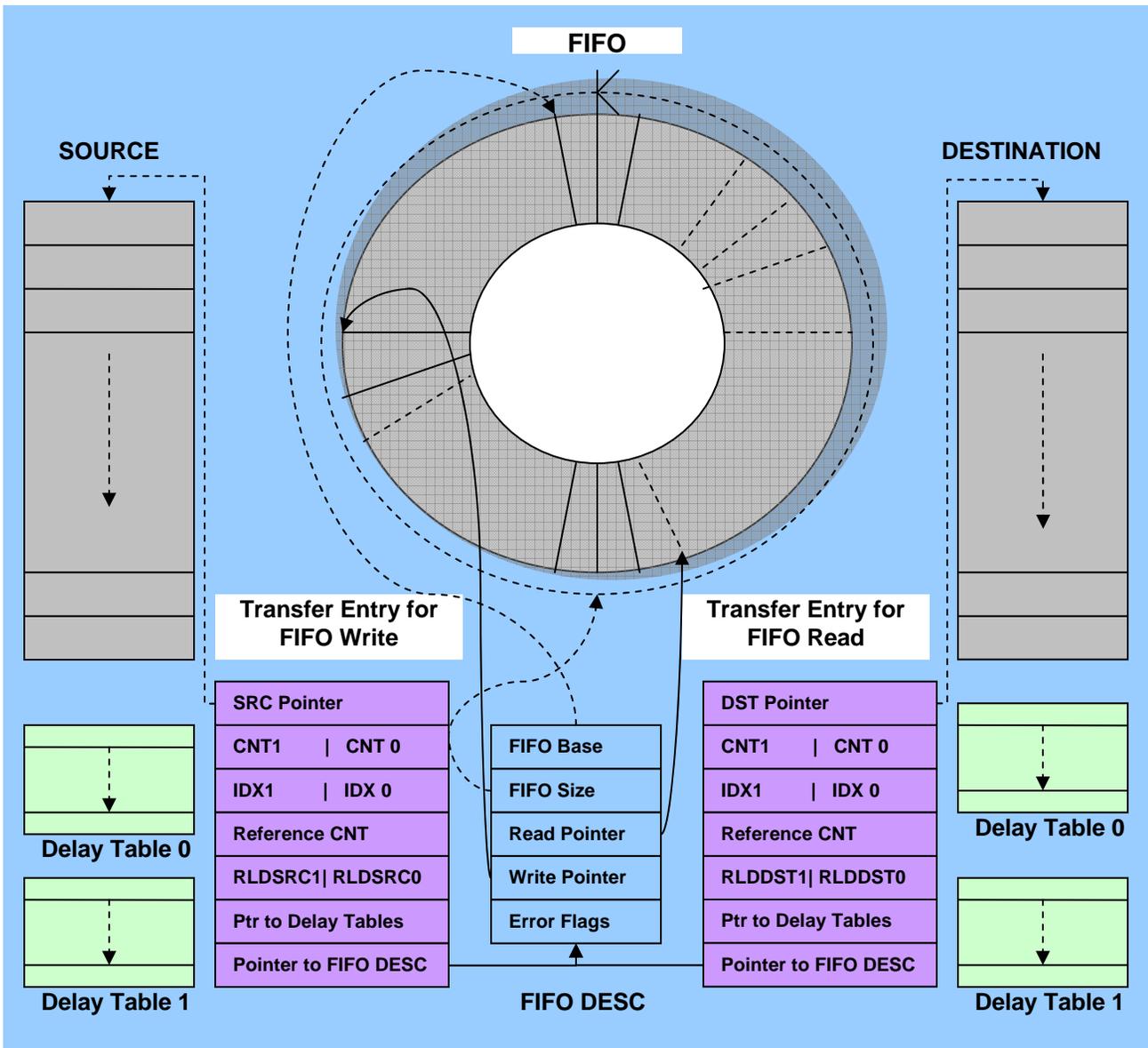
- **Extensive error checking and recovery**

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General Purpose Transfer

Source

Destination

Address	Value
0x10001000	
0x10001004	A0
0x10001008	D0
0x1000100C	B0
0x10001010	E0
0x10001014	C0
0x10001018	F0
0x1000101C	
0x10001020	
0x10001024	A1
0x10001028	D1
0x1000102C	B1
0x10001030	E1
0x10001034	C1
0x10001038	F1
0x1000103C	
0x10001040	
0x10001044	A2
0x10001048	D2
0x1000104C	B2
0x10001050	E2
0x10001054	C2
0x10001058	F2
0x1000105C	

SINDX0=2
SINDX1=-3
SINDX0=2
SINDX2=2

Address	Value
0x10002000	
0x10002004	A0
0x10002008	A1
0x1000200C	A2
0x10002010	
0x10002014	B0
0x10002018	B1
0x1000201C	B2
0x10002020	
0x10002024	C0
0x10002028	C1
0x1000202C	C2
0x10002030	
0x10002034	D0
0x10002038	D1
0x1000203C	D2
0x10002040	
0x10002044	E0
0x10002048	E1
0x1000204C	E2
0x10002050	
0x10002054	F0
0x10002058	F1
0x1000205C	F2
0x10002060	

DINDX0=4
DINDX0=4
DINDX1=4
DINDX0=4
DINDX0=4
DINDX2=-19

Features:

- **1 Dimension (Block Move), 2 Dimension (Sub-frame extraction) 3 Dimension (Data De-Interleaving) transfer support**

- **Separate IDX for 1st, 2nd and 3rd dimension**

- **Separate IDX for source and destination**

- **Transfer first dimension for an event or complete the entire transfer**

- **Supports two reload addresses for source and destination for effective Ping-Pong**

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FIFO Transfers

FIFO

SOURCE

DESTINATION

Transfer Entry for FIFO Write

SRC Pointer
CNT1 | CNT 0
IDX1 | IDX 0
Reference CNT
RLDSRC1| RLDSRC0
Ptr to Delay Tables
Pointer to FIFO DESC

FIFO Base
FIFO Size
Read Pointer
Write Pointer
Error Flags

Transfer Entry for FIFO Read

DST Pointer
CNT1 | CNT 0
IDX1 | IDX 0
Reference CNT
RLDDST1| RLDDST0
Ptr to Delay Tables
Pointer to FIFO DESC

Delay Table 0

Delay Table 1

FIFO DESC

Delay Table 0

Delay Table 1

Features:

- **Moves data b/w two dimensional linear address and a circular buffer.**

- **Circular buffer size need not be 2^n**

- **Table based multi tap delay transfer support**

- **Reload allows Ping-Pong implementation for linear buffer**

- **CPU notification for FIFO Watermark conditions**

- **Error checking for FIFO overflow and underflow**

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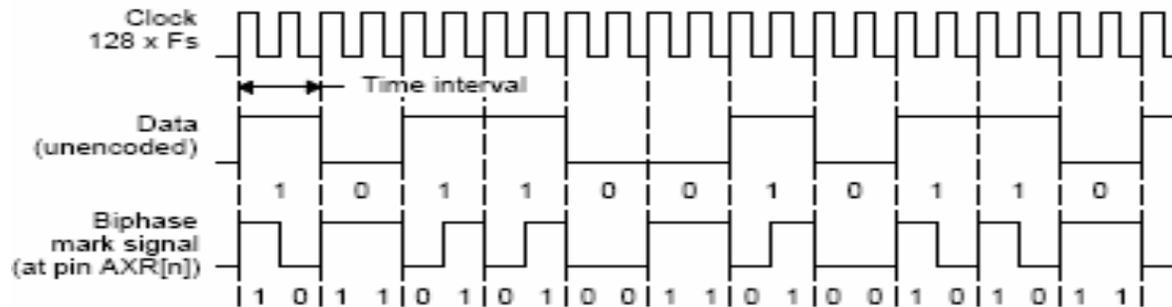# McASP Transfer Format

TDM Format–6 Channel TDM Example

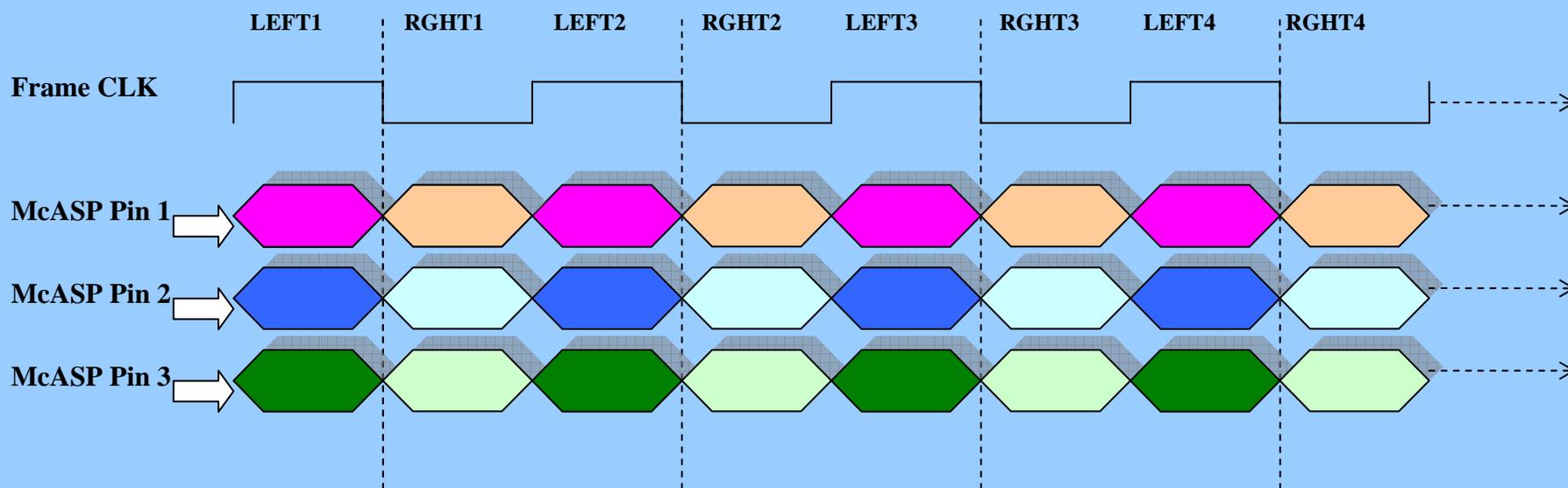Inter-Integrated Sound (I2S) Format
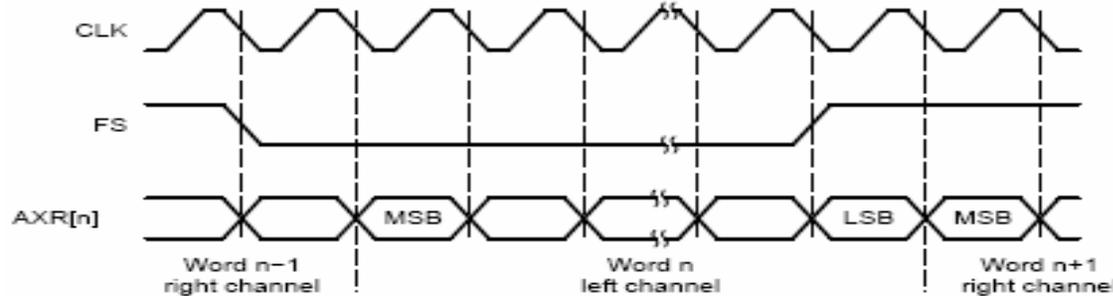
Biphase-Mark Code (BMC)

- ◆ **TDM streams from 2 to 32, and 384 time slots**

- ◆ **Wide variety of I2S and similar bit-stream format**
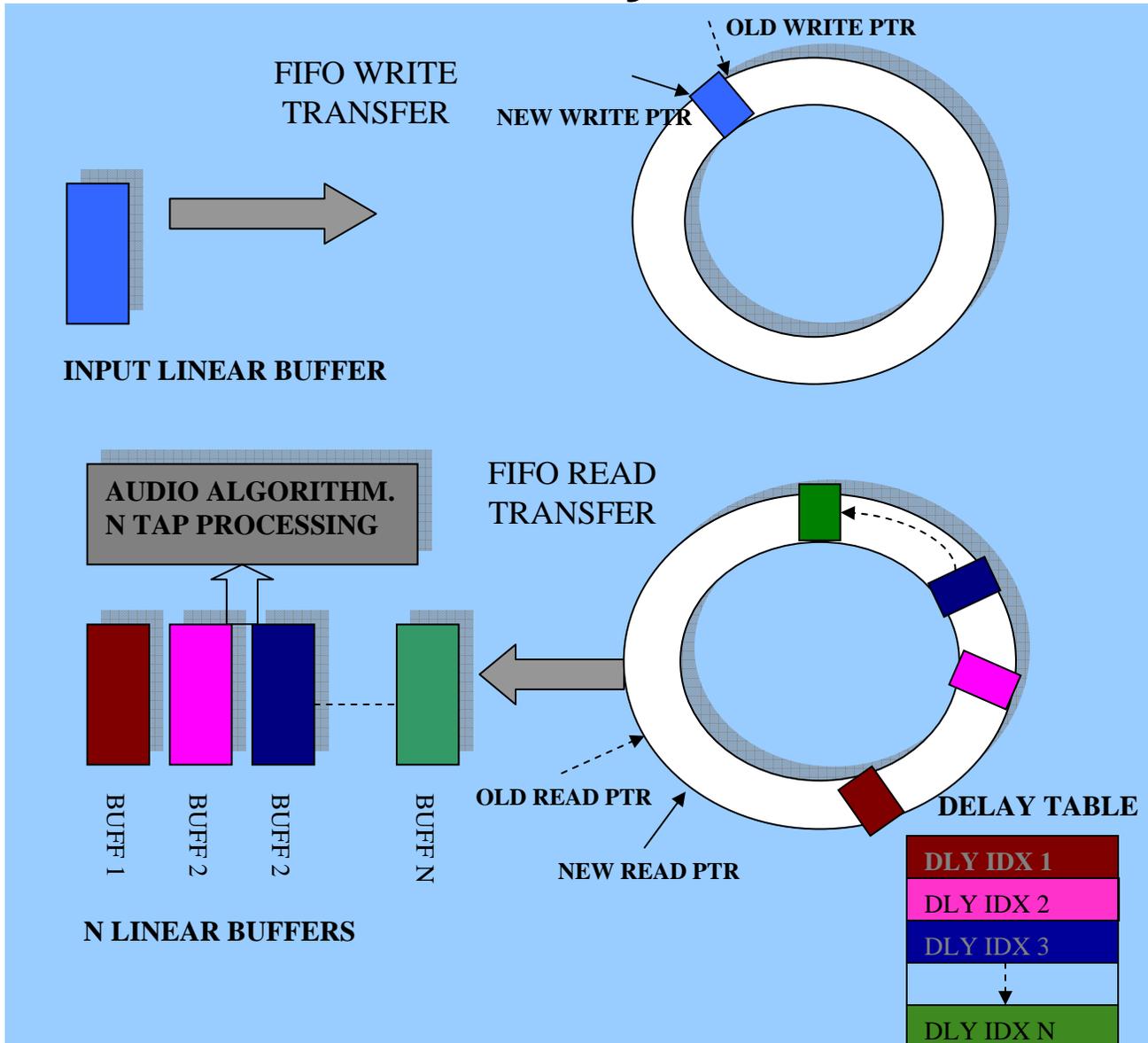
- ◆ **S/PDIF, IEC60958-1, AES-3 formats**

Delay Based Effects

FIFO WRITE TRANSFER

OLD WRITE PTR

NEW WRITE PTR

INPUT LINEAR BUFFER

AUDIO ALGORITHM. N TAP PROCESSING

FIFO READ TRANSFER

BUFF 1
BUFF 2
BUFF 2
BUFF N

N LINEAR BUFFERS

OLD READ PTR

NEW READ PTR

DELAY TABLE

DLY IDX 1
DLY IDX 2
DLY IDX 3
DLY IDX N

- **FIFO Write dMAX transfer updates the FIFO with new data**
- **FIFO Read Transfer reads N TAP data**
- **Read and Write PTR updated by dMAX**
- **dMAX takes care of circular buffering**
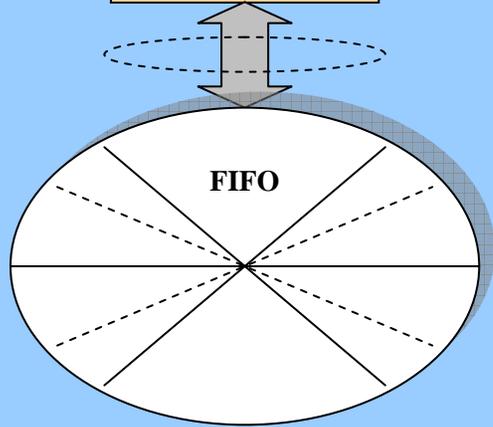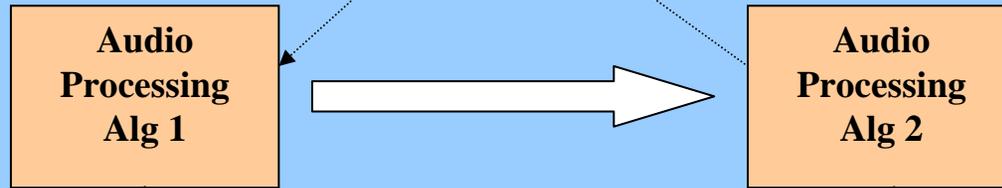- **Error reporting for FIFO under run or overflow**

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Example Audio Processing System

AUDIO THREAD

McASP RX	**Audio I/O Driver RX**	**F/W Audio Thread**	**Audio I/O Driver TX**	**McASP TX**

Audio Data on McASP Pins

Audio Data on McASP Pins

Audio Processing Alg 1

Audio Processing Alg 2

FIFO

PING

PONG
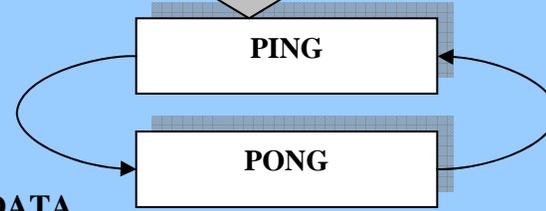
CTRL DATA TRANSFER B/W THREAD

Ctrl data on SPI/I2C

CONTROL THREAD

SPI/I2C	**Control I/O Driver**	**F/W Ctrl Thread**

dMAX TRANSFERS

CPU PROCESSING