TI Developer Conference
March 7-9, 2007 • Dallas, TX

Minds in Motion

# Innovative Solutions for Power Management and Conservation in Next-Generation Wireless Infrastructure Systems

**Brian Narveson**
**Texas Instruments**

# Agenda

- Evolution of power architectures to increase efficiency, save space and reduce cost
- Using T2 power modules to reduce the cost and size of the power system
- Overview of SmartReflex™ technology and how it reduces DSP power dissipation and maintains performance
- Signal chains components that increase performance without increasing power consumption

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# Power Architectures for DSP Boards

# Power System Challenge

- Provide more voltages at higher currents
- Increase power system efficiency
- Produce less noise
- Fit in a smaller space
- Provide all of the above at lower cost

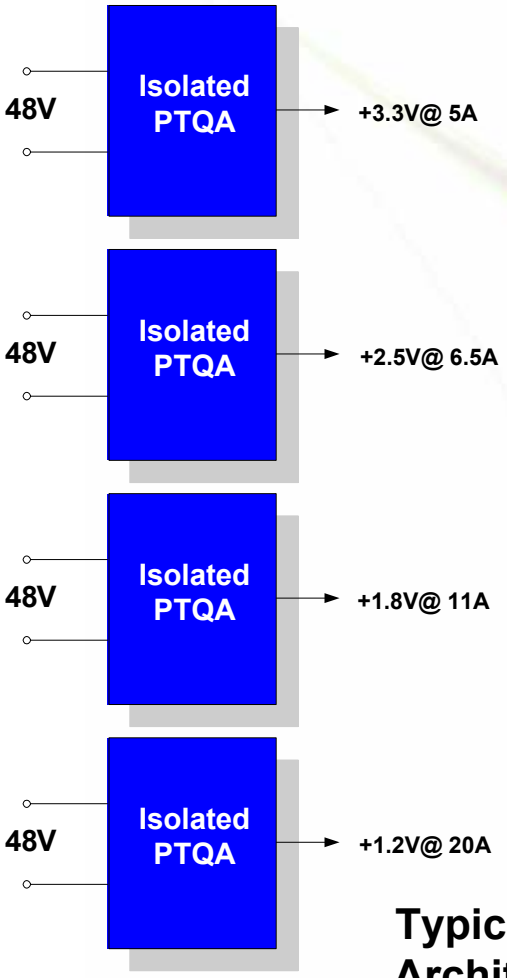
# Overview

- Distributed Power Architecture (DPA) Evolution
  - Individual Isolated Voltages
  - Regulated Intermediate IBC + POL
  - Loosely Regulated IBC + POL
  - Quasi-regulated IBC+POL
- DPA Comparison – Cost and Efficiency Benefits
- Additional System Cost Avoidance and Space Savings
  - Synchronization – Noise Reduction
  - IC Supply Voltage Tolerance Requirements
  - System Sequencing Requirements

# Power System Comparison Example

- Input Voltage Possibilities
  - 18-V DC to 36-V DC
  - 36-V DC to 75-V DC
  - 36-V DC to 55-V DC
- Output Voltages Required
  - 3.3 V @ 5 A
  - 2.5 V @ 6.5 A
  - 1.8 V @ 11 A
  - 1.2 V @ 20 A
- Total Power Requirement 76.55 W

# First Generation – All Isolated Bricks

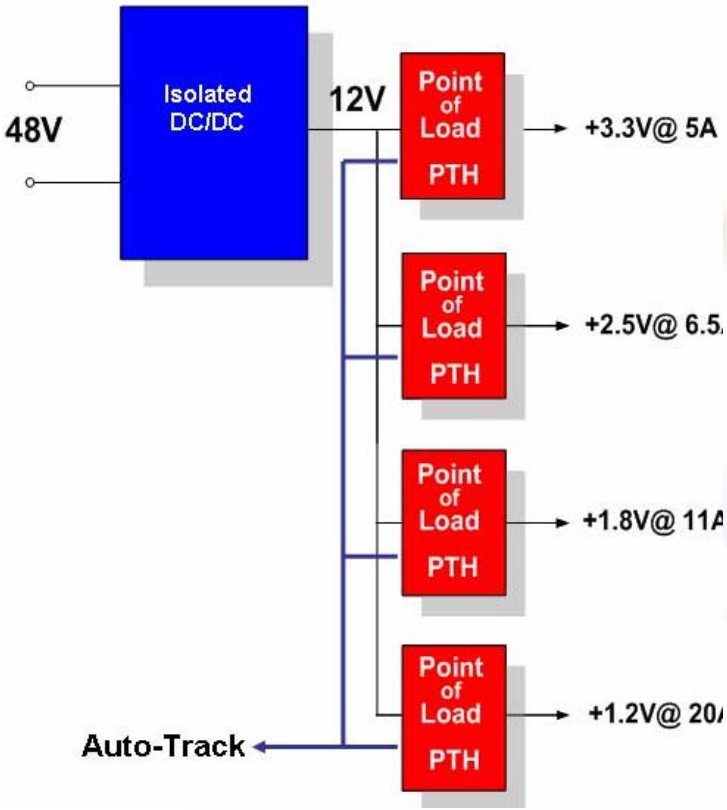



**Typical DPA Architecture**

Distributed Power Architecture (DPA)

- Traditional way of powering telecom/datacom system boards
- Uses all isolated bricks
- Works well with few voltage rails
- As voltage rails increase, costs and PC board space increase
- No sequencing without external circuitry (Lattice or Summit IC) which added cost and board space
- High efficiency due to single conversions

# Second Generation – Regulated IBA



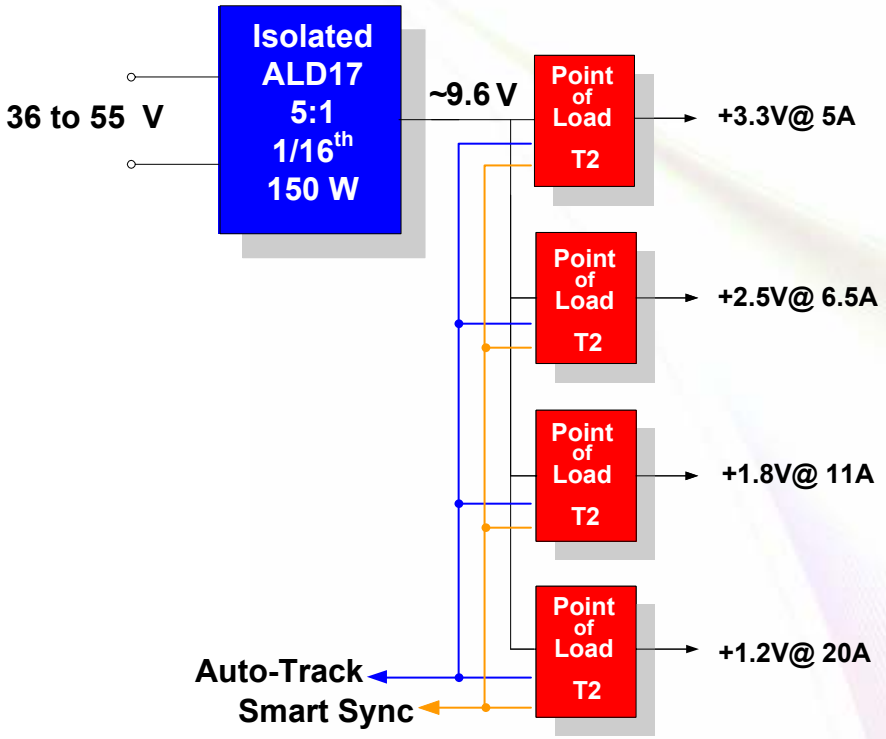

**Regulated Voltage Intermediate Bus Architecture (IBA)**

Regulated (Fixed) Voltage

Intermediate Bus Architecture (IBA)

- Most popular production architecture
- Uses one isolated brick and many non-isolated POLs
- Uses a regulated 3.3 V, 5 V, or 12-V bus
- Results in lower cost, less board space, with less efficiency in some cases
- Simplified sequencing with Auto-Track™
- POL Modules can be replaced with lower cost discrete buck converters

# Third Generation – Unregulated IBA



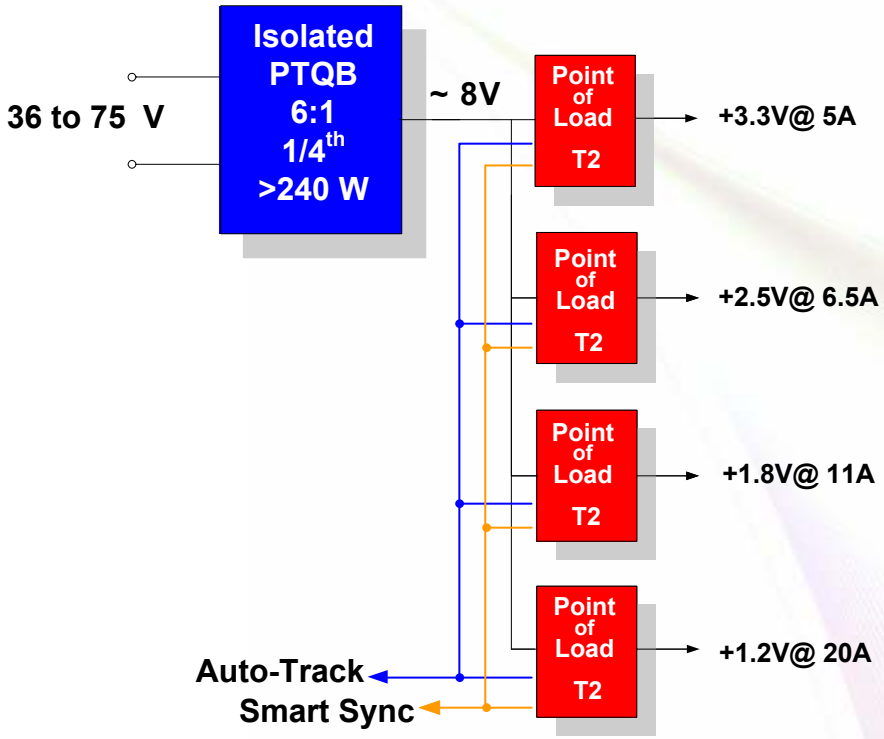

**Unregulated Intermediate Bus Architecture (IBA)**

Unregulated

Intermediate Bus Architecture (IBA)

- Uses quasi-regulated bus converter with 9.6 V nominal (7 to 11 V) bus
- Provides highest isolated converter efficiency ~ 96%
- Limited input voltage range
- Board space consumption minimized
- Provides for optimized conversion efficiency for POLs (9.6 V input)
- Gives highest system efficiency while maintaining cost and size advantages
- Simplified sequencing of all voltage rails with Auto-Track™
- Synchronization using T2 modules

# Third Generation – Quasi-regulated IBA



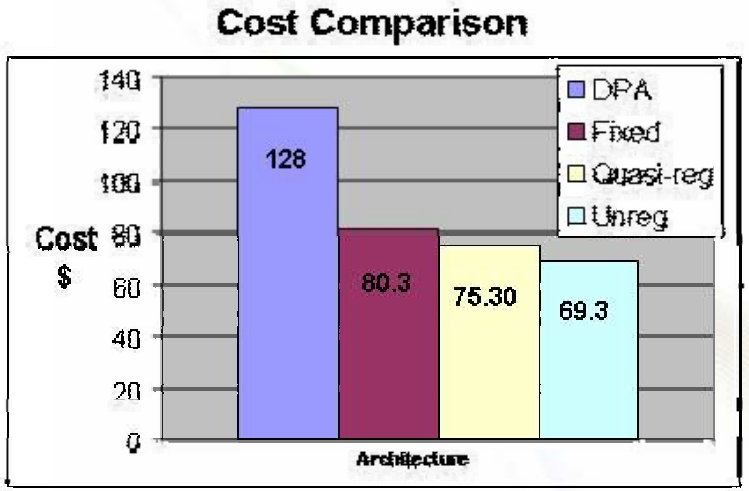

**Quasi-regulated Intermediate Bus Architecture (IBA)**

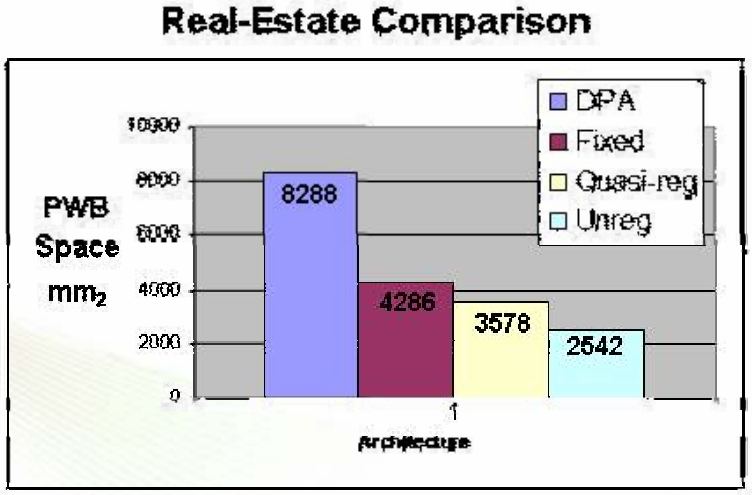
Quasi-regulated

Intermediate Bus Architecture (IBA)

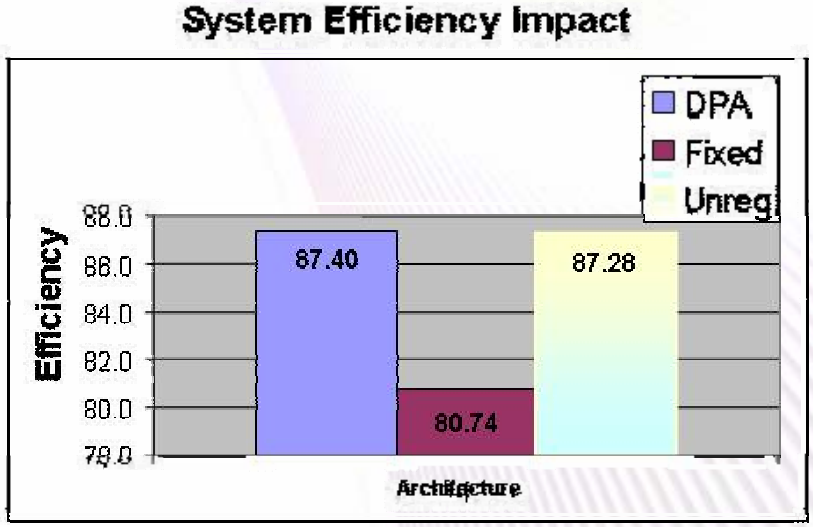
- Uses quasi-regulated bus converter with 8 V nominal (6 to 12.5 V) bus
- Provides highest isolated converter efficiency ~ 96%
- Provides for optimized conversion efficiency for POLs (8 V input)
- Full telecom input voltage range, including input transients (100 V, 100 ms)
- Gives highest system efficiency while maintaining cost and size advantages
- Simplified sequencing of all voltage rails with Auto-Track™
- Synchronization using T2 modules

# Comparison of DPA and IBA Architectures




POL's are 1K Distributor Pricing

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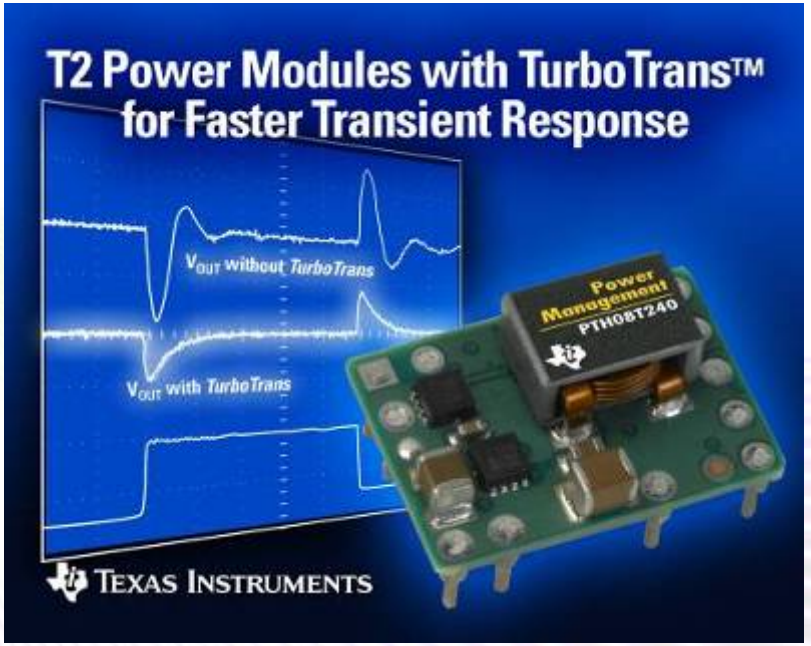
# Additional “System” Cost and Board Space Savings

# T2 Power Modules – Feature Review

- *TurboTrans*™ Technology
- Smart Sync
- 1.5% Regulation
- 50% Smaller Footprint
- Wide Input Voltage
  - 4.5 V to 14 V
- Auto-Track™ Sequencing
- Pb Free and RoHS

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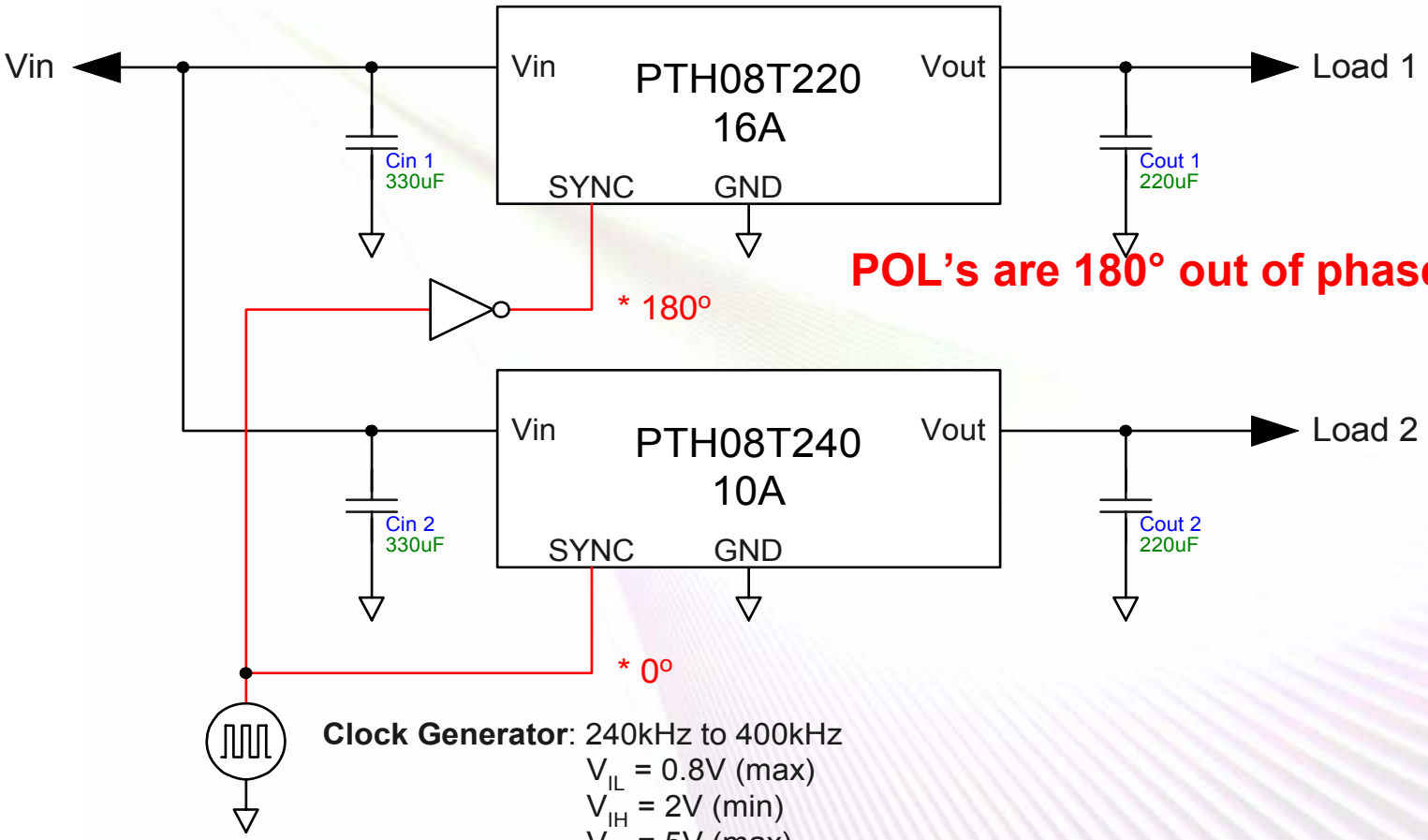
# Smart Sync

- Smart Sync (patent pending) allows the designer to synchronize the switching frequency of multiple T2 power modules.

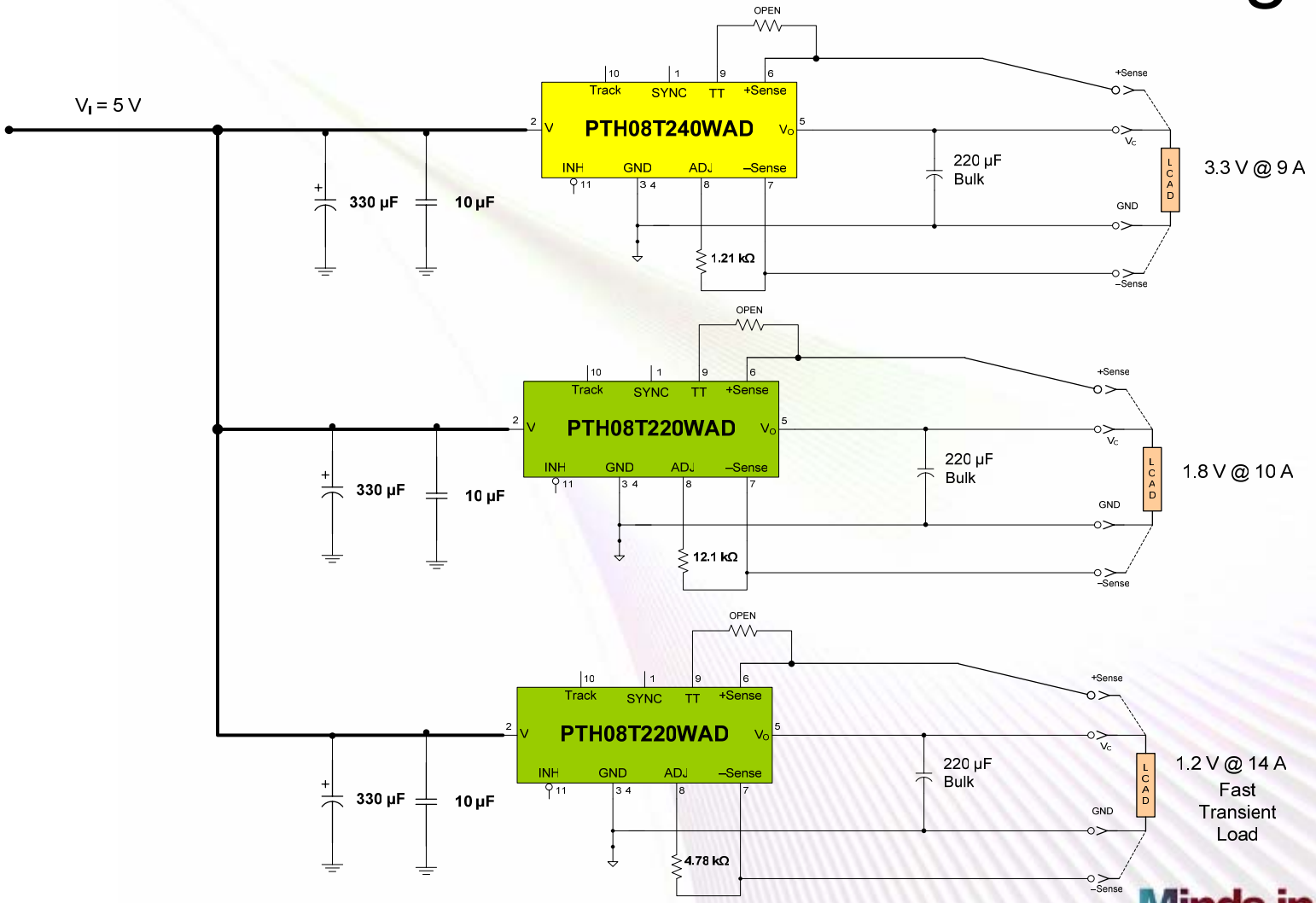
- Smart Sync has three main benefits:
  1. Synchronizing modules **makes EMI filtering easier** by eliminating beat frequencies.
  2. The synchronizing frequency can be higher or lower than the nominal module switching frequency. This allows the designer to synchronize the modules at a frequency that **maximizes efficiency**.
  3. The power modules can be synchronized at different phase angles to help balance source loading and **minimize input capacitance**.

# SMART SYNC with 180° Phase Shift




**How do we minimize the external clock costs?**

# Three T2 Modules Free Running

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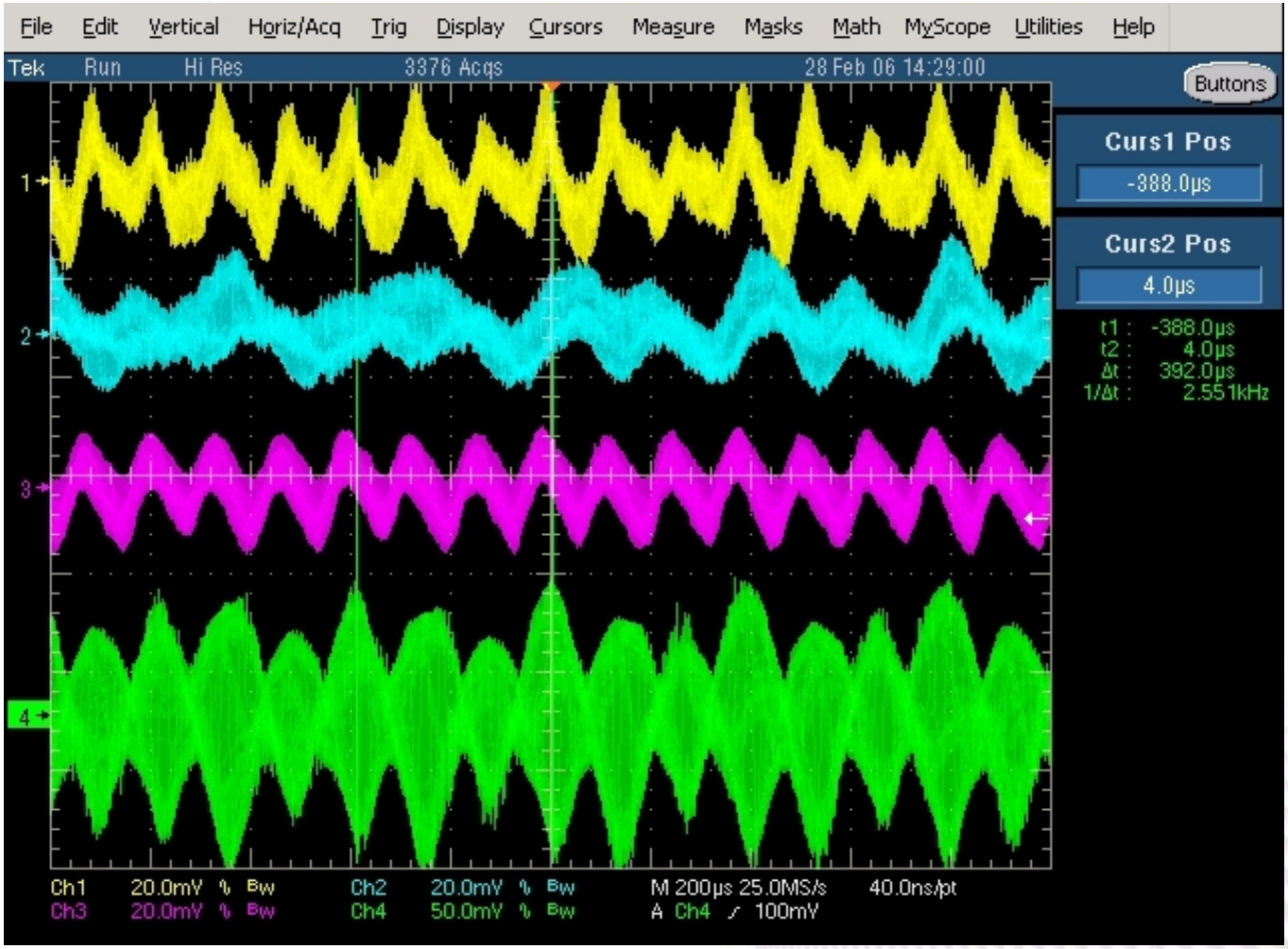
# Three T2 Modules Free Running




**Low (2.5 kHz) Beat Frequency with 150 $mV_{pp}$ Ripple Voltage**

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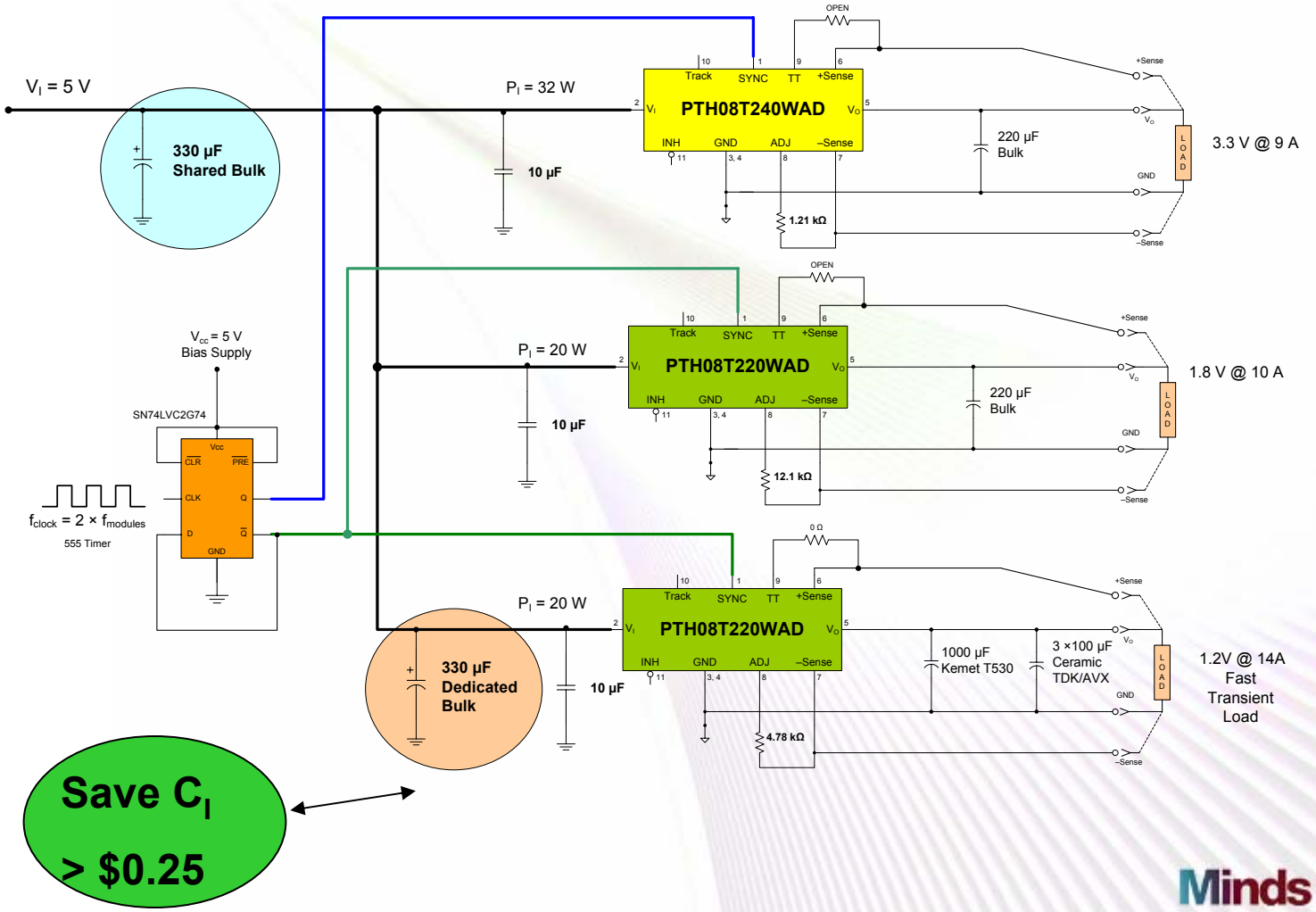
# Dual-Clock Signals Synchronizing Three T2's – The Most Cost Effective Clock Solution

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# Dual-Clock Signals Synchronizing Three T2's


**Beat frequency eliminated. Input voltage ripple reduced to 80 $mV_{pp}$.**

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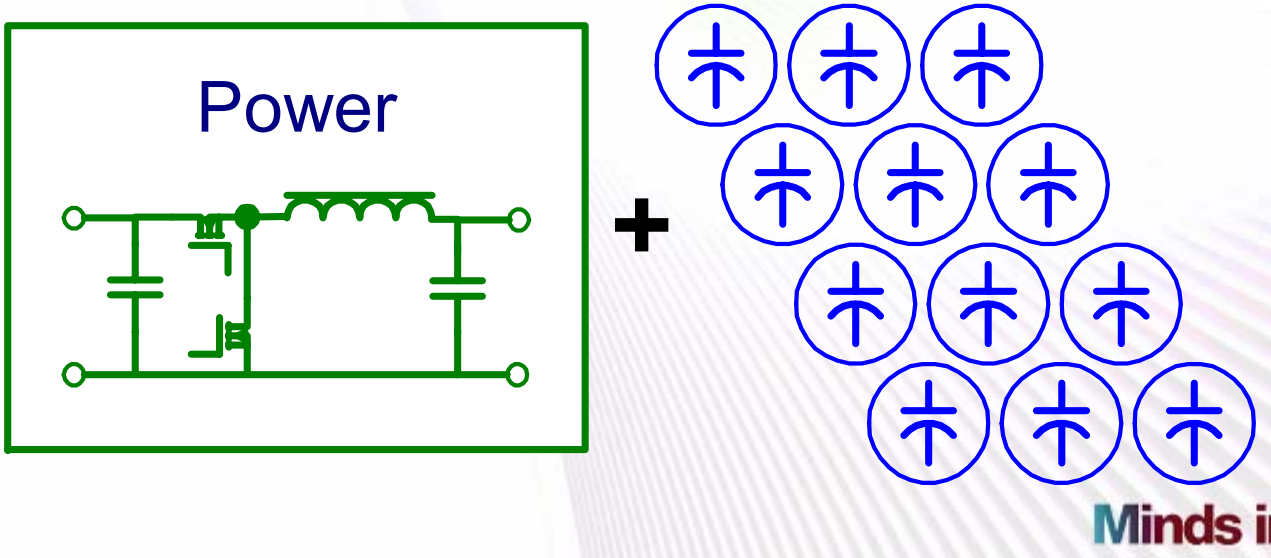
# *TurboTrans*™ Technology

- *TurboTrans*™ Technology is a new feature (patent pending) that allows the designer to custom "tune" the T2 power modules to meet a specific transient load requirement.
- This benefits the designer in three ways:
  1. Up to 8X reduction in output capacitance
     Saves the cost of capacitors and PCB space. In high transient load applications, these savings could easily be as much as the cost of the module itself.
  2. Faster response to transient loads
     For a given value of output capacitance, the designer will see up to a 50 percent reduction in the peak deviation of the output voltage following a load transient.
  3. Enhanced stability when used with ultra-low ESR capacitors
     Designers can safely use newer Oscon, polymer tantalums, or **all ceramic** output capacitors without stability concerns.

# Traditional Solution

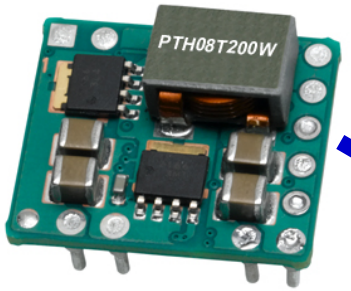
- Traditional power supplies need a large capacitor bank to handle transients.
  - Not high-temperature solder friendly
  - Requires increased PCB space
  - Increased BOM
  - Reduce stability



# *TurboTrans*™ Slashes Required Capacitance

- Requirement: $V_O$ = 1.2 V, $V_{PK}$ =35 mV, and for 8 A total transient. T220 or T210
- A single Kemet T530 1000 uF plus 3X 100uF ceramics will do the job with TurboTrans……Add up to six more without TurboTrans!

**TurboTrans**

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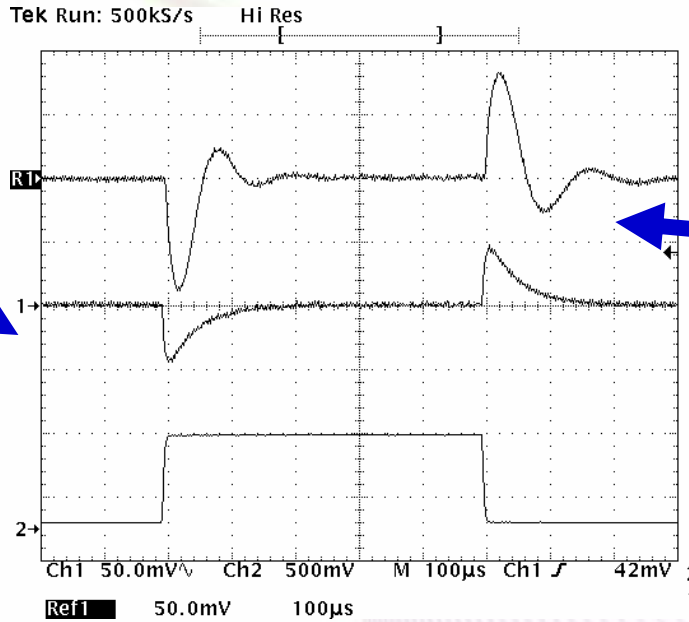


**Without TurboTrans**


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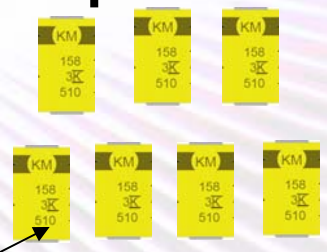

**T530 $C_O$ = $2.50**

**$C_O$ Savings = $15.00**

**T530 $C_O$ = $17.50**

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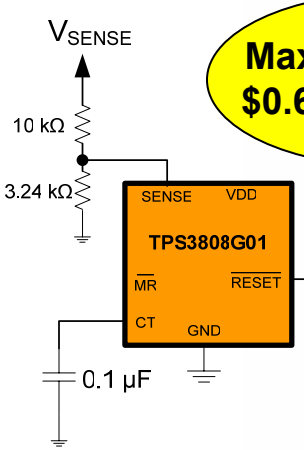
# Supply-Voltage Sequencing

How can I reduce the circuit implementation costs associated with supply-voltage sequencing?

# Supply-Voltage Sequencing
# Supply-Voltage Supervisors vs. Power-Sequencing Controllers

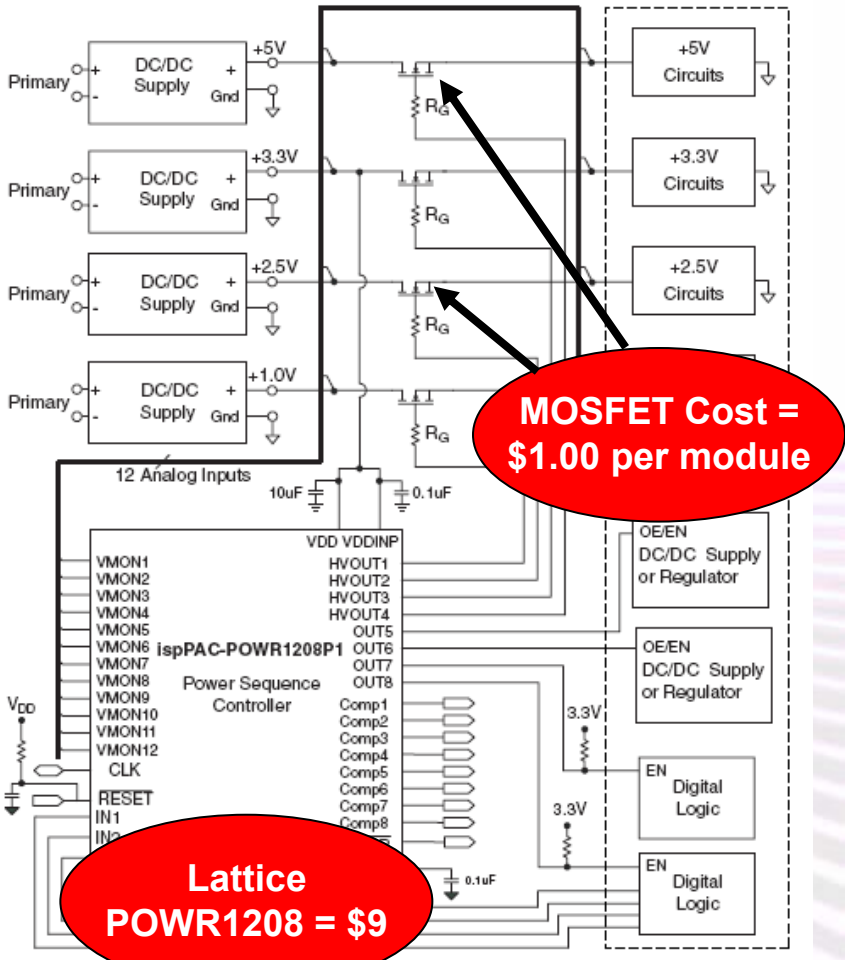



**Maximum Cost = $0.60 per module**

**PTH Auto-Track**

**-VS-**

## Application Block Diagram




**MOSFET Cost = $1.00 per module**

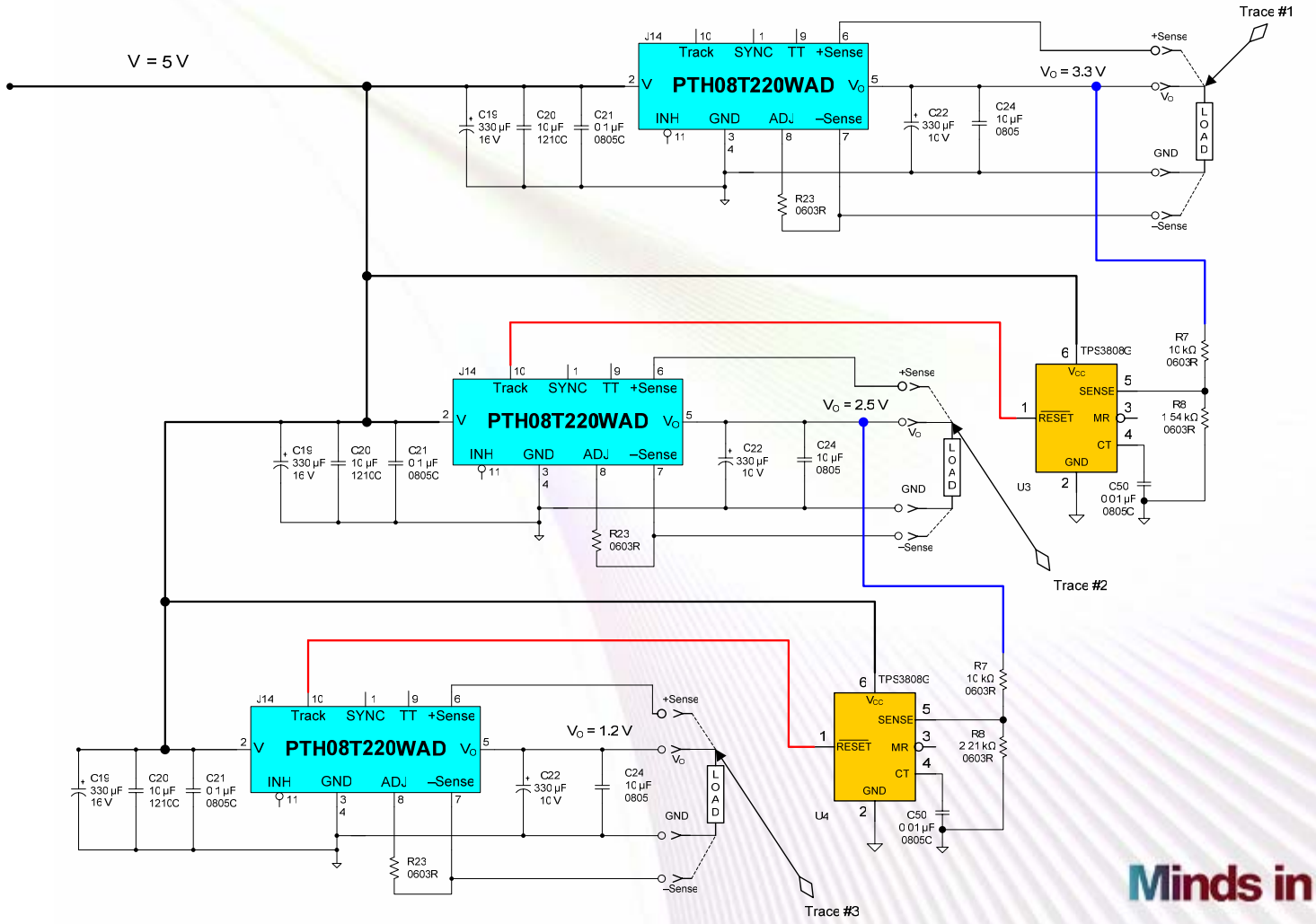
**Lattice POWR1208 = $9**

**For supply voltage sequencing requirements where "power-up" sequencing is the dominant concern, SVS presents a tremendously more cost effective, space saving solution.**

**If designing with at least three modules:** →

**Cost Savings >>$10**

# Sequential Sequencing using AutoTrack™

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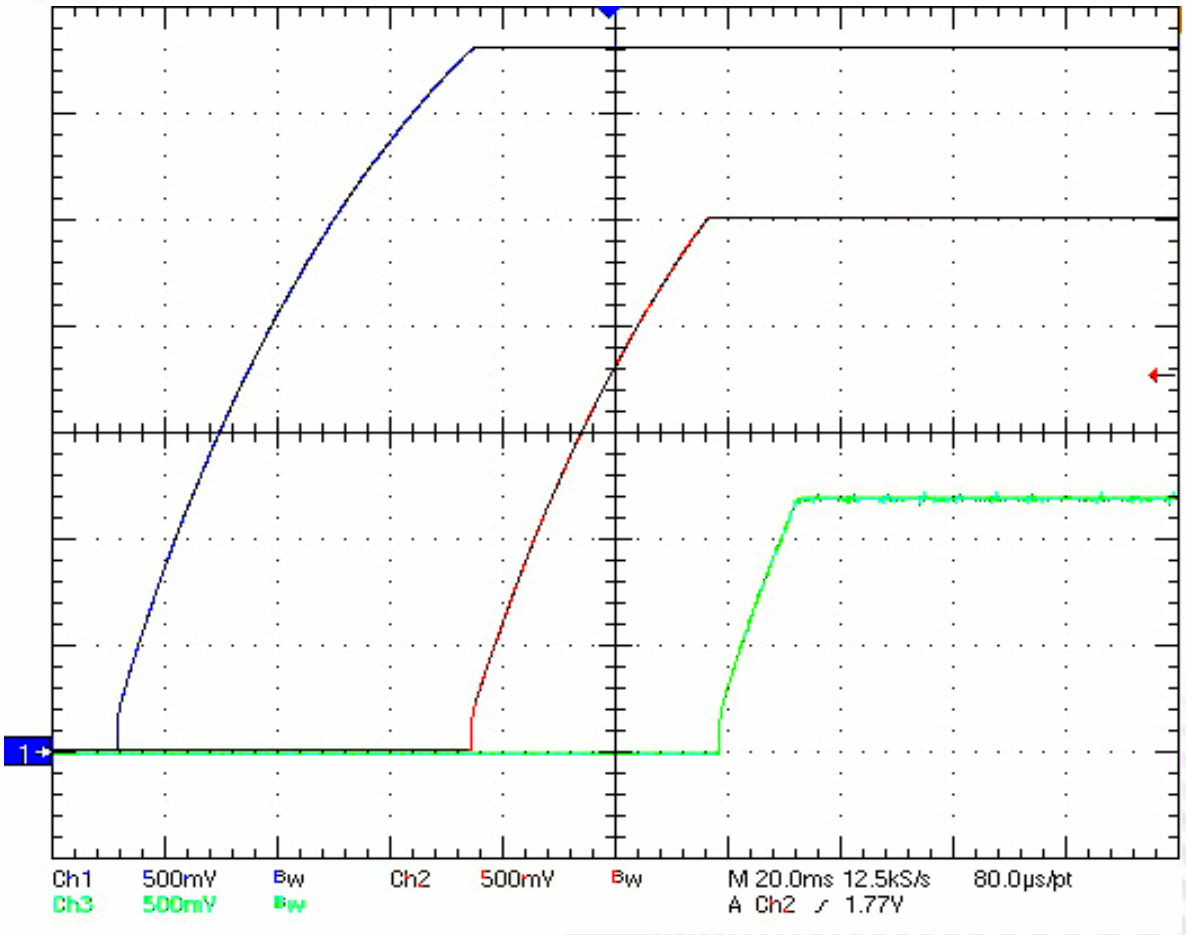
# Sequential Sequencing using AutoTrack™



# Power Summary

- Distributed Power Architecture Evolution
  - Loosely Regulated IBC + POL offer the most cost-effective power solution for today's demanding requirements (performance and cost).
  - Using a 8-V bus offers the optimal conversion efficiency from a 48-Vbus.
- T2 Products
  - Have the highest power densities available in a POL module. Space Savings.
  - SmartSync eliminates the need for external filtering components at the lowest possible cost.
  - TurboTrans reduces the requirement for external output capacitance, offering a huge savings with capacitor costs and board space.
  - Auto-Track combined with SVS allow for low cost implementation of power-up simultaneous and sequential sequencing.

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# Power Saving DSP Innovations

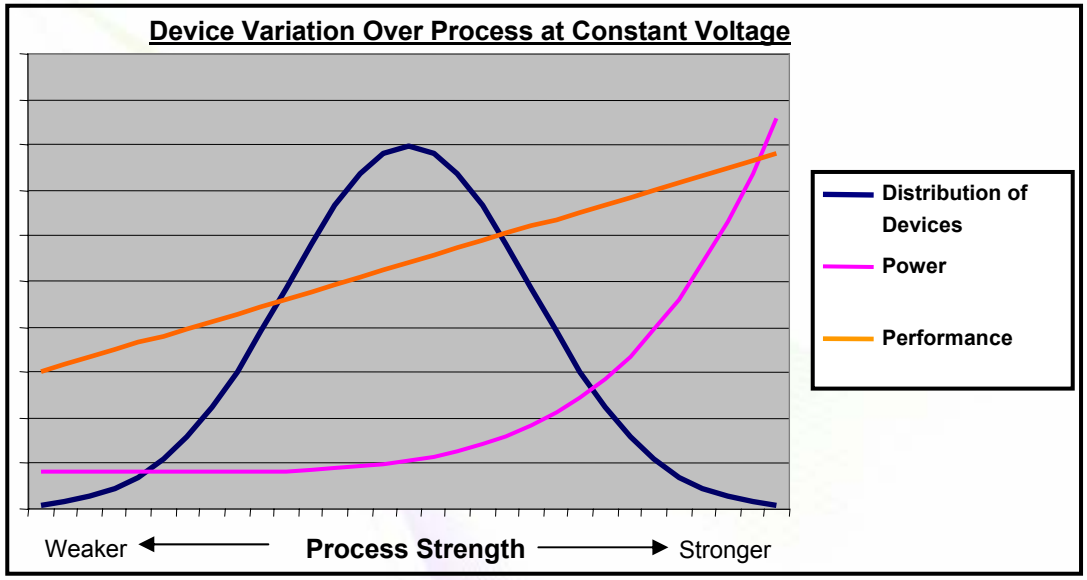
# SmartReflex™ Technology

- **Why SmartReflex™ technology**
  - Confluence of factors on **TCI6487/88**: MHz, density and leakage
  - SmartReflex technology enablement
- **SmartReflex™ technology for TCI6487/88**
  - Overview
  - Leveraging variations over process corners
    - Power without and with SmartReflex voltage scaling
  - SmartReflex temperature component
  - Operation
  - Additional hardware requirements
    - Includes rough cost estimate
  - Silicon junction temp implications
- **Summary**
  - Ensuring success

# SmartReflex Technology on TCI6487/88 DSP

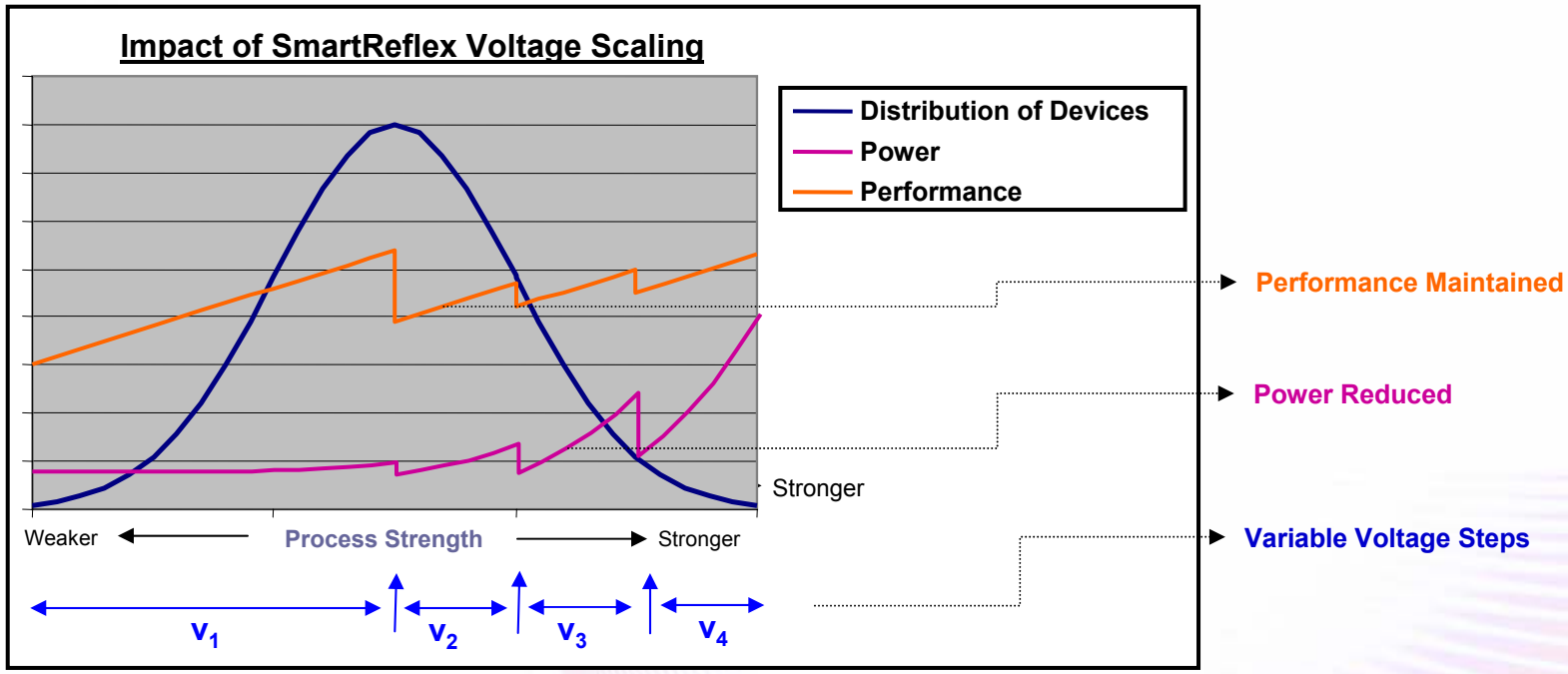
- **SmartReflex technology is ideal on the TCI6487/88**
  - Manufactured on the 65 nm high-performance Si node
  - Very high performance (1-GHz core clock rate)
  - Unprecedented integration (Allows base-band on chip)
  - Power target at 6.25 W
- **SmartReflex technology – Class 0 will be employed to manage the TCI6487/88 DSP power**
- **Used both process and temperature "knobs"**
  - Allows optimized TCI6487/88 operation (i.e. meeting specifications) for maximum power efficiency

# Leveraging Natural Process Variation…




- **Semiconductors produced in any process have inherent variation due to process**
  - *Vary across Weak to Strong depending upon process corner (Blue Line)*
- **Variation across weak to strong silicon creates performance variation**
  - *Vary across Weak to Strong performance depending upon process corner (Orange Line)*
- **SmartReflex technology uses this natural process and performance variation to minimize power**
  - *Selects power/ performance combination to allow each device to meet its performance goals while conserving power (Pink Line)*

# SmartReflex Technology Voltage Scaling




**Strong Process Node**

- *Has slightly higher leakage current*
- *Apply Lower voltage - Desired Performance is maintained, power is conserved*

**Weak Process Node**

- *Has lower leakage current*
- *Apply Nominal voltage - Desired Performance is maintained, power is conserved*

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# SmartReflex Temperature Scaling

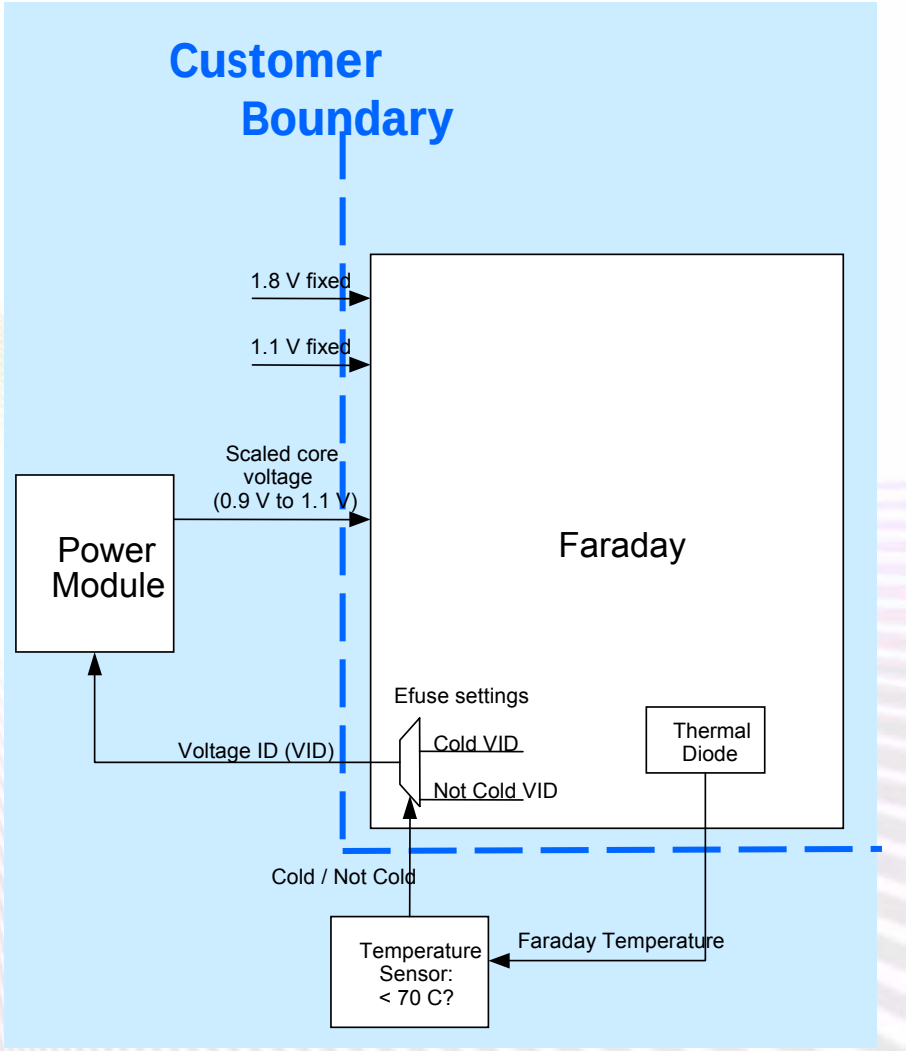
- **Core voltage can be varied based on device temperature**
  - Requires Information about device temperature
  - Voltage (Vdd) to account for device temperature-dependent performance
  - Performed dynamically during device operation
- **Used to compensate for certain transistor types that lose performance at low temperature**.
- **Vdd can be raised to restore performance**
  - At low temperature, voltage can be raised a small amount, ~25 mV, to restore performance, with minimal impact to power
  - Power is not impacted by the higher voltage as power is lower at low temperature

# TCI6487/88 Features Support SmartReflex

- **Customized Circuitry**
  - Assess where the device lies along the strong/weak process continuum
- **Fuse Settings**
  - Internal programmed fuse settings
  - Scaled voltage operational values are associated with fuse settings
- **Voltage ID (VID) Pins**
  - Four pins used to output the settings for the voltage regulator
  - These settings determine appropriately scaled voltage output by voltage regulator
- **Internal Chip Diode**
  - Gauges junction temperature
  - Output pin for temperature region

# SmartReflex Operation

- **Faraday process parameters are sensed**
  - Smart Reflex circuitry senses process corner on device
  - Based on this setting fuses set for two separate set of VIDs
- **Temperature sensor decided high/low temp**
  - Utilizes Faraday temperature circuitry data to calculate high/low setting
  - Setting fed back into Faraday
  - This selects one of two preprogrammed VIDs
- **VID pins set**
  - Final setting has static process and dynamic temperature input
  - Supplies needed operating voltage settings to off chip voltage regulator
  - Up to 16 separate settings
- **The Vreg provides a variable (scaled) 1.1 V supply**
  - The variable supply is the basis of SmartReflex operation
  - Scaled voltage ranges may span ~900 mV to 1.1 V
- **Thus device specs met while minimizing power**

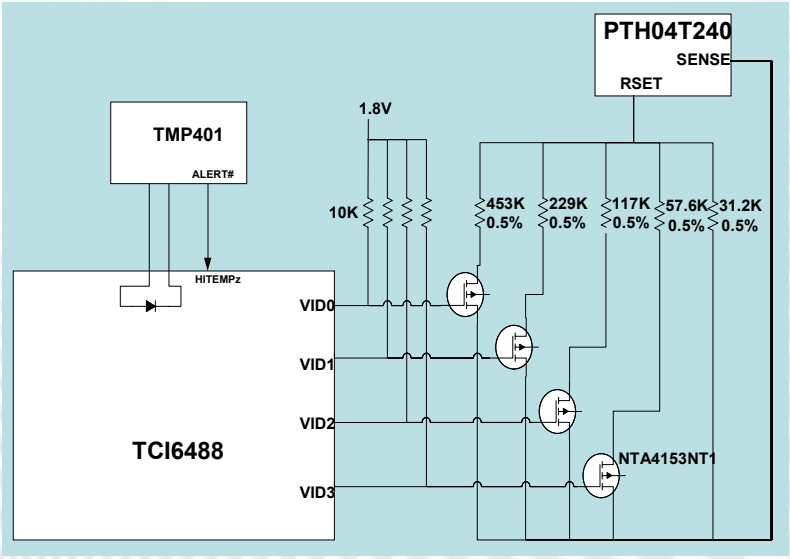


# Additional Hardware Implications (Including TI companion Devices)

- **External Temperature Sensor**
  - Uses temperature region data from diode and converts to scaled voltage setting
    - **25 mV to 50 mV across the range**
  - Feeds directly into Faraday to choose appropriate scaled voltage setting
  - TI's device TMP401 is an LM86 equivalent
    - **Default to optimal levels for Faraday ($I^2C$ not required)**
    - **Has hysterisis to prevent excessive device switching**
    - **Datasheet available**
    - **No reset interruption during switch**

- **External Voltage Regulator**
  - Supplies the required scaled voltage level
  - TI device PTH04T240
    - **Initial samples available**
  - Faraday optimized device PTH04T240F

- **Resistors & FETs**
  - Along with FETs allows four VID pins to adjust voltage regulator output
    - **Mostly generic resistors; Five of these need to be tighter (0.5%) tolerance**
    - **FET selection is critical**



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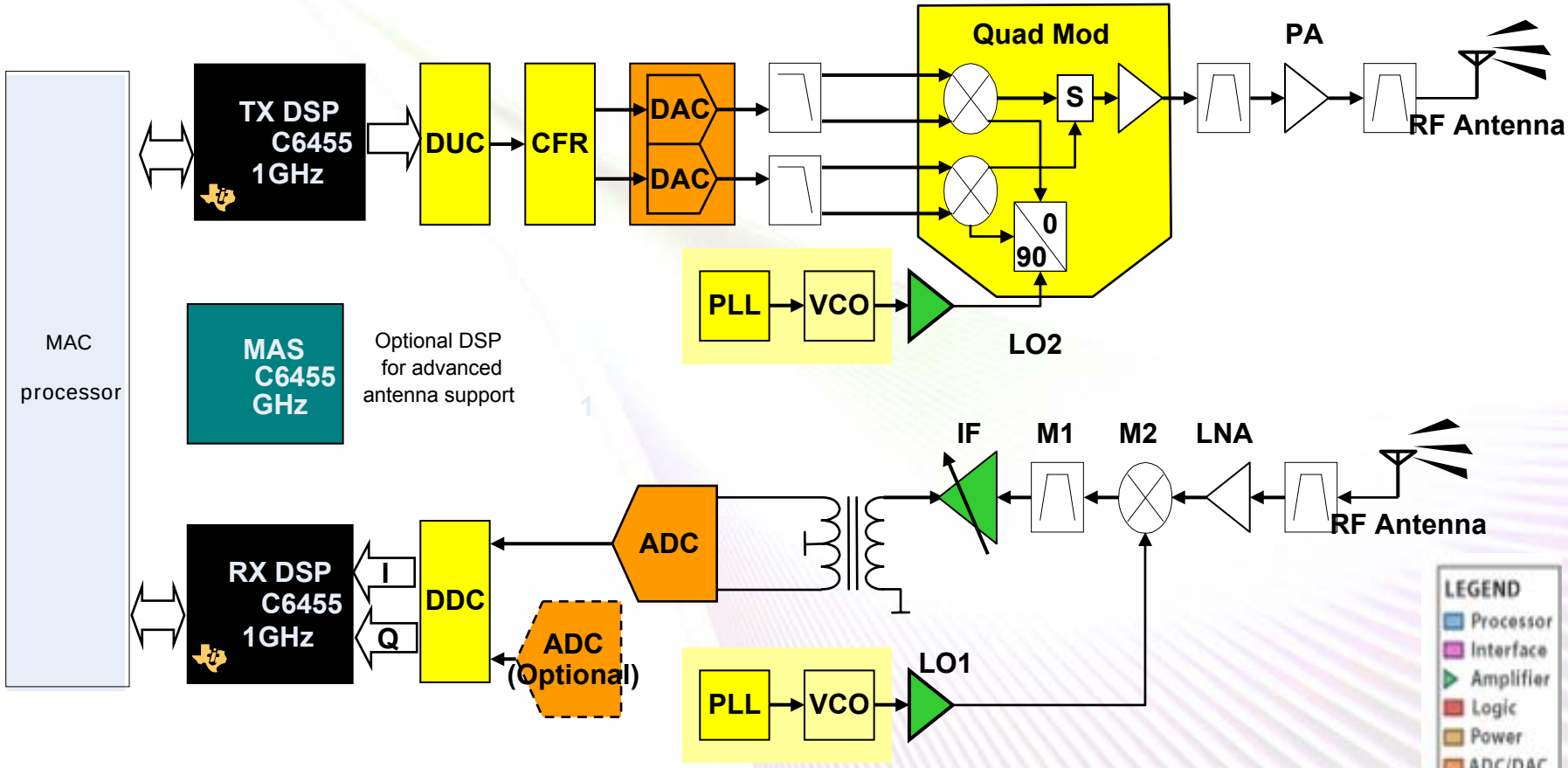
# High Performance Signal Chain with Minimum Power

# Complete BTS Signal Chain Solution

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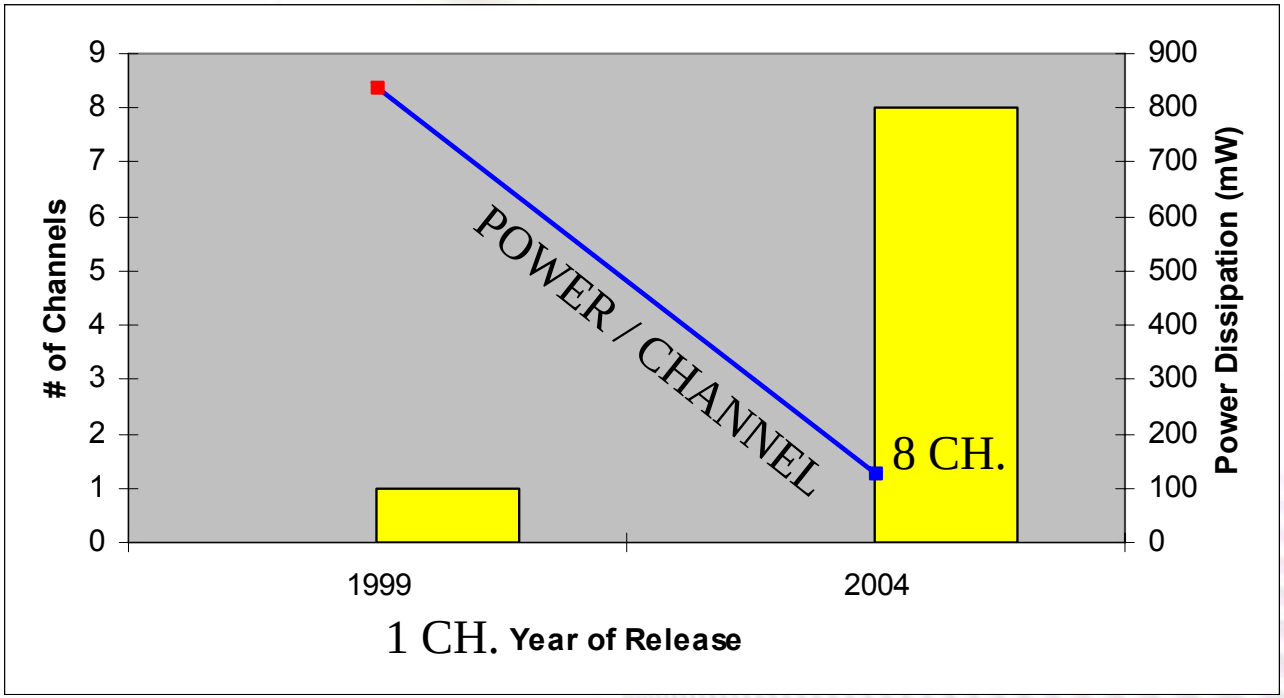
# Advances in Data Conversion

## Multi-Channel Integration Saves Space and Power

## 2004: Industry's First Octal Channel ADC



# Advances in Data Conversion

- **High-Speed ADCs enable wideband systems**
  - 2005: Major advances in technology allow
    - 14-bit ADCs increased in speed by >3X while power dissipation has been reduced (vs. 2000)
    - ADC power dissipation has been halved for same speed/res
- **Gains in speed to support wideband systems without sacrificing power efficiency**
  - 2006: Fastest 14-bit ADC at is >5X faster with less than 50 percent increase in power dissipation vs. average ADC in 2000
    - » ADS5421 (14-bit 40 MSPS) @ 900 mW in 2000
    - » ADS5500 (14-bit 125 MSPS) @ 780 mW in 2005
    - » ADS5547 (14-bit 210 MSPS) @ 1.3 W in 2006

# Summary

- **Innovative unregulated and quasi-regulated power architectures increase efficiency, save space and reduce cost**
- **T2 power modules improve performance and reduce power system cost**
- **SmartReflex technology reduces power dissipation while providing industry leading DSP performance**
- **TI's signal chain components deliver superior performance with less power consumption**

# Acknowledgements


- Adrian Harris for power architecture and T2 lab work
- Zatil Hamid for signal chain content
- Manish Patel for SmartReflex technology content

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