

DSP Solutions For High Quality Video Systems

Todd Hiers
Texas Instruments



TI Video Expertise Enables Faster And Easier Product Innovation

**TI has a long history covering
the video market from end to end**

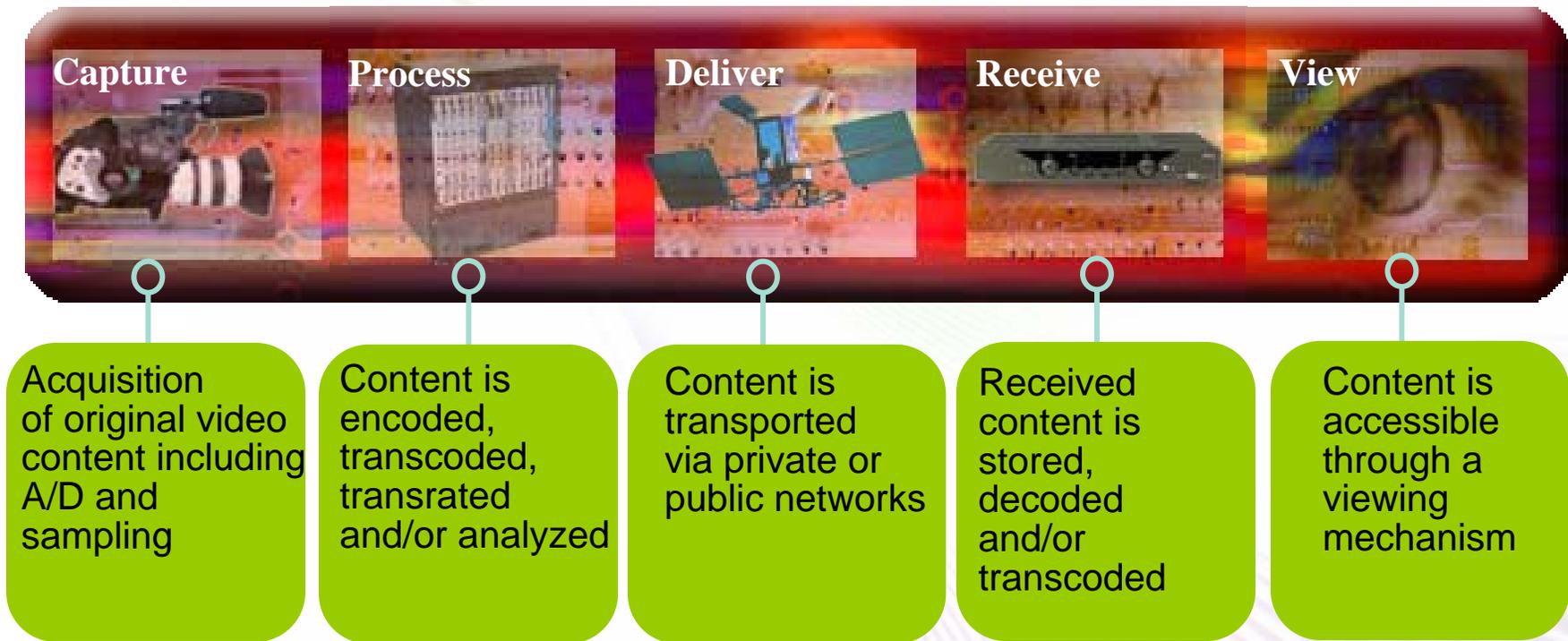
R&D began on image processing in the early 80s

**TI leverages video systems expertise and R&D across
internal design teams to drive innovation
and business development**

**Customers can leverage TI's expertise in end-to-end
video to quickly launch into multiple video markets**

Minds in Motion

Defining the Video Chain



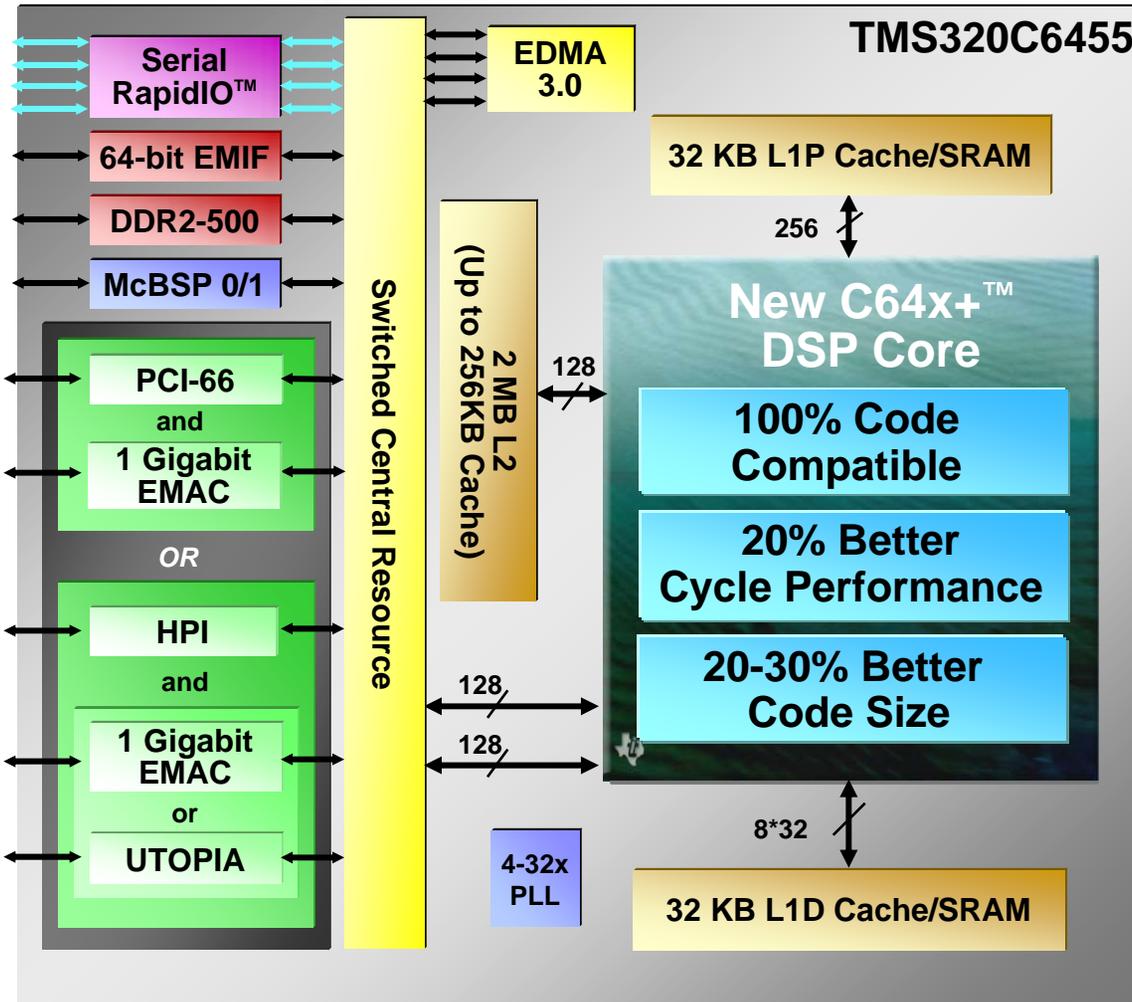
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Platforms & Uses

Likely Uses Platform	Encode	Transcode	Transrate	Decode
Multi 6455	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
645x + FPGA	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
Multi DM643x	<input checked="" type="checkbox"/>			<input checked="" type="checkbox"/>
DM643x + FPGA				<input checked="" type="checkbox"/>
Multi Cat LC			<input checked="" type="checkbox"/>	
C6424 + FPGA			<input checked="" type="checkbox"/>	
DM644x (DaVinci)	<input checked="" type="checkbox"/>			<input checked="" type="checkbox"/>

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C6455 Quick Introduction



Package: 697 BGA, 24 mm, 0.8 mm Pitch, Lead-Free Balls

Serial RapidIO™

- ◆ Up to 10 Gb/s Bi-di communication
- ◆ Connect to any RapidIO device

New C64x+ Core – Up to 1 GHz

- ◆ ISA enhancements for better performance and code size
 - C6455 - 720 MHz: \$179
 - C6455 - 850 MHz: \$219
 - C6455 - 1 GHz: \$259
- (TMS Production prices 2006 / 07 - 10Ku)

Memory Architecture

- ◆ 2 MB L2
 - ❖ 256K Cache/SRAM; Remainder is SRAM only
- ◆ 32 KB L1D Cache/SRAM
- ◆ 32 KB L1P Cache/SRAM

Two EMIFs

- ◆ 32-bit DDR2 (DDR2-500 SDRAM)
- ◆ 64-bit EMIF

GEMAC / UTOPIA / PCI-66 / HPI

- ◆ Multiple connectivity options

C642x Quick Introduction

Features

■ New C64x+™ Core

- 400 MHz, 500 MHz, 600 MHz
- Up to 4800 MMACs performance

■ Memory – C6421

- 16-KB L1D and 16-KB L1P cache/SRAM
- 64-KB L2 cache/SRAM

■ Memory – C6424

- 80-KB L1D and 32-KB L1P cache/SRAM
- 128-KB L2 cache/SRAM

■ Peripherals – C6421

- Two EMIFs – 16-bit DDR2 333MHz; 8-bit EMIF
- VLYNQ™/ EMAC (RMII/MII) or HPI / RMII
- McBSP or McASP – Audio and telecom interfacing
- UART (2), I²C, GPIO, PWM (3), 64-bit timers (2)

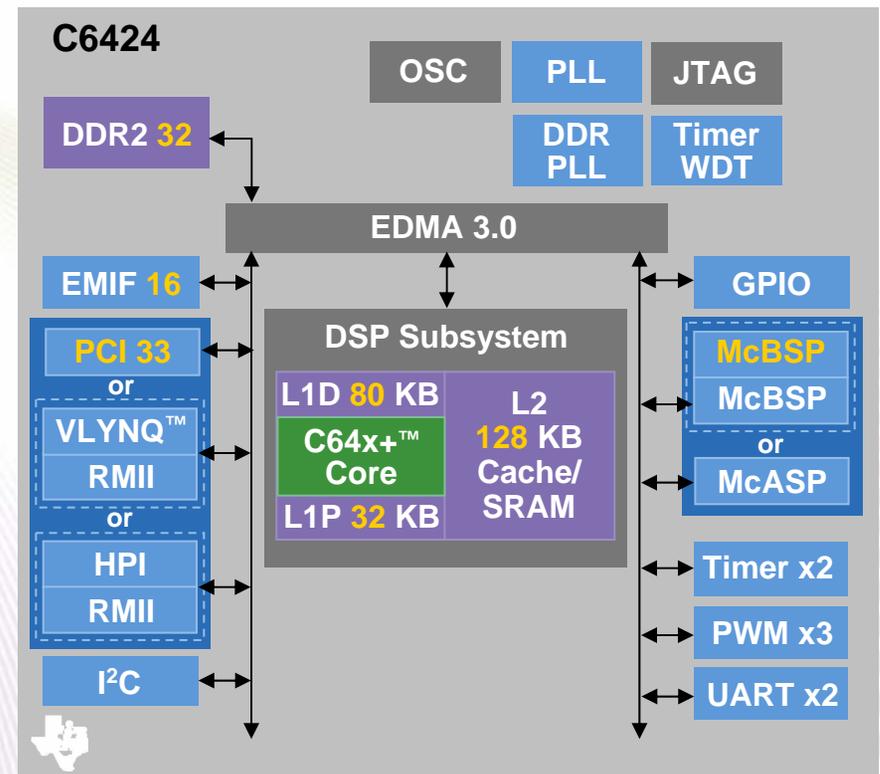
■ Peripherals – C6424 enhancements:

- 32-bit DDR2 333MHz; 16-bit EMIF
- PCI33 or VLYNQ™ / EMAC (RMII) or HPI / RMII
- McBSP (2) or McASP

- Package: 361 pin 16x16-mm BGA, 0.8-mm Pitch, 376 pin 23 x 23 mm BGA, Lead-Free Balls
- Samples: 4Q06; Production: 4Q07
- Price C6421/C6424: \$8.95/\$15.95 at 400 MHz / 10 KU – 2007/08

Benefits

- C6421: Lowest cost DSP with C64x+ performance and Ethernet
- Smallest package C64x DSP
- C6421/24 pin Compatible



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DM643x Quick Introduction

Features

■ New C64x+™ Core

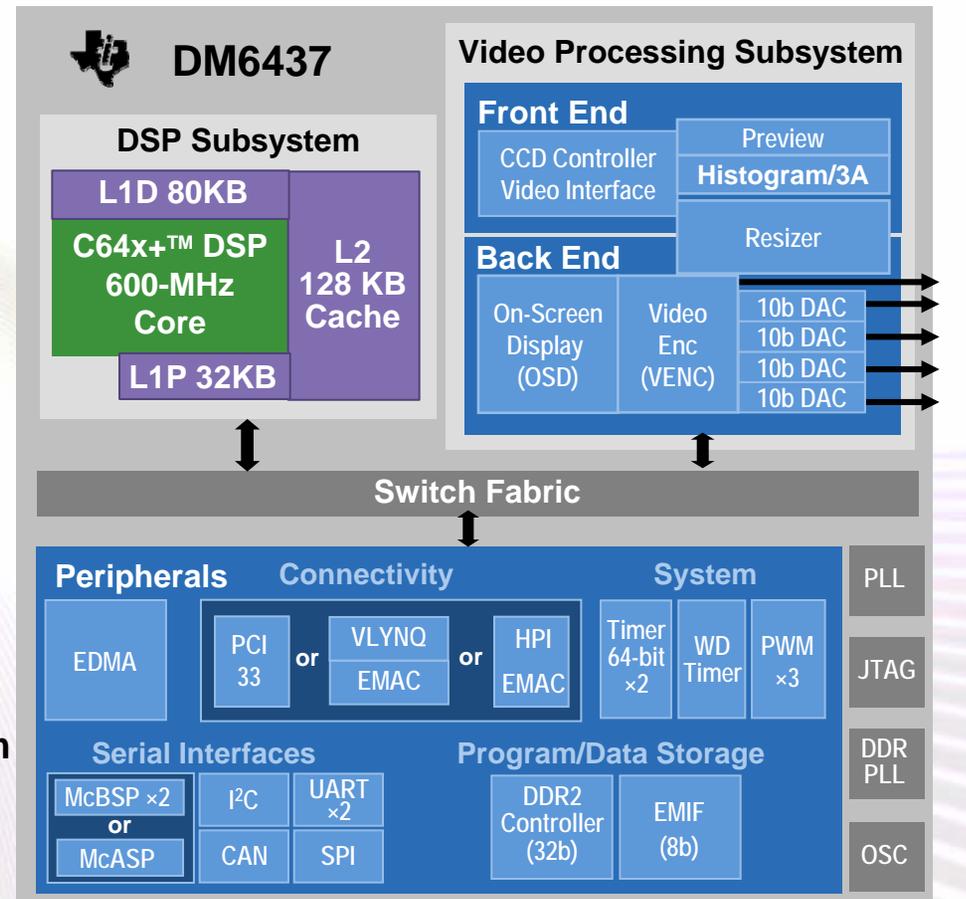
- C64x+™ Core @ Up to 600 MHz

■ Memory

- 80 KB L1D, 32 KB L1P Cache/SRAM
- 128 KB L2 Cache/SRAM

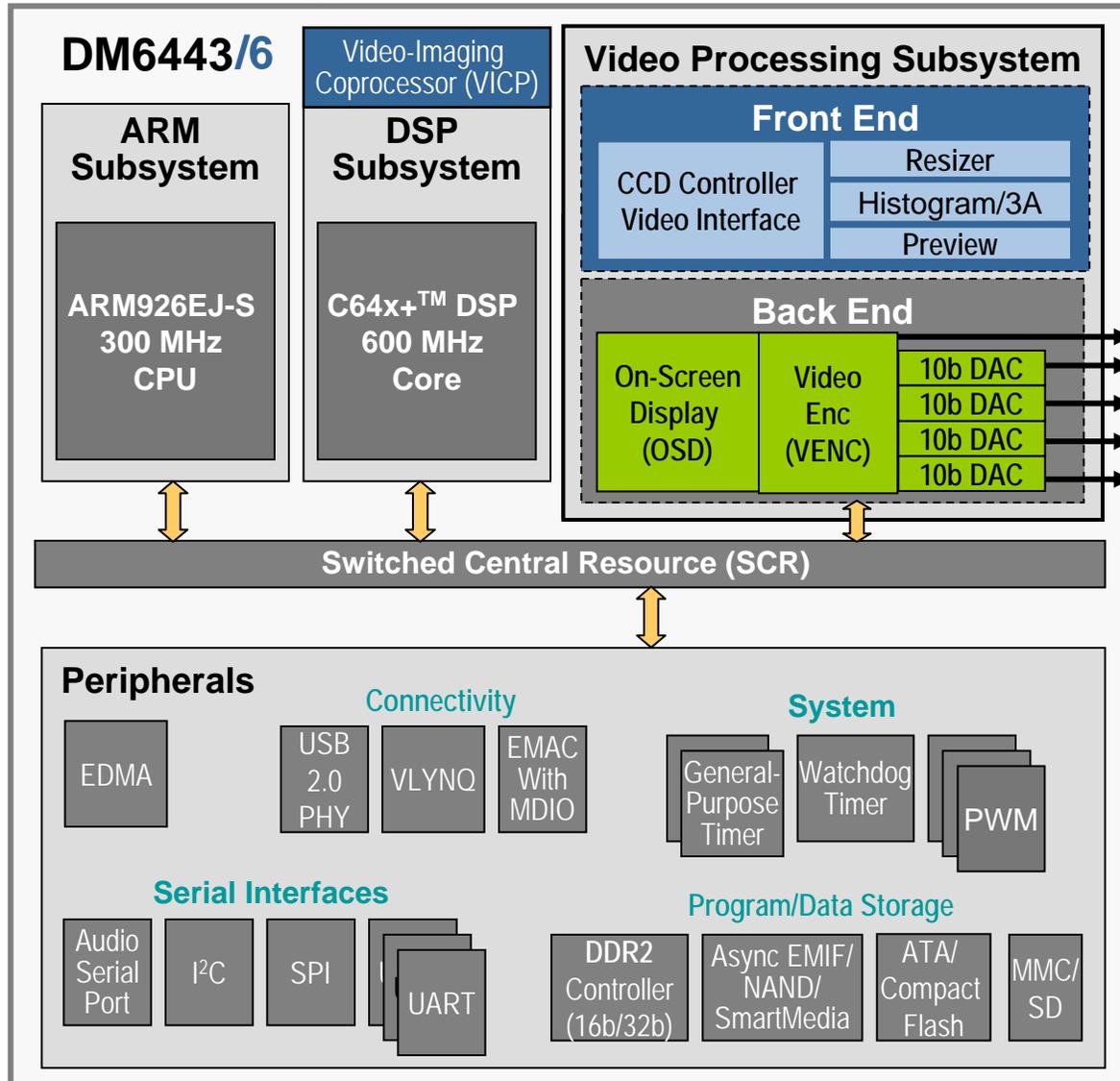
■ Peripherals

- Video Port Sub-System (VPSS): Input (CCDC), Output (w/DACs), Resizer, OSD, and Camera Control
- Two EMIFs: DDR2-266: 32 bits, 133 MHz; EMIF 2.1
- 10/100 Ethernet MAC (MII); PCI 33 MHz; HPI; McASP
- VLYNQ™ – Serial Interface to FPGAs
- UART (2), I²C, SPI, GPIO, PWM (3), CAN (HECC), 64-bit Timers (2)
- **Package: 16x16mm or 23x23mm, 361 Pin, 0.8mm or 376 Pin 1.0mm Pb-Free Balls**
- **Pin Compatible with DM6435/3/1**
- **Samples 4Q06; Production 2Q07**
- **Price: \$22.95 @ 600 MHz, 10 KU – 2007/08**



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DM644x Quick Introduction



Video-Optimized TMS320C64x+™ DSP @ 600MHz

- H.264 MP@L3, 30fps SD Decoding
- VC1/WMV9 Full D1 SD Decoding
- MPEG-2 MP@ML SD Decoding
- MPEG-4 ASP Full D1 SD Decoding

- H.264 BP D1 Encoding
- Simultaneous H.264 BP CIF Coding

Dedicated video processing sub-system

- Back end - Integrated OSD, four video DACs, 24-bit digital RGB output

- Front end - Resizer, Image processing engine, 16-bit digital input

2006 10KU Price:
 TMS320DM6443 \$29.95
 TMS320DM6446 \$34.95

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SRIO Quick Introduction

Serial RapidIO is a high-performance, packet-switched, interconnect technology that addresses the embedded industry's need for:

Reliability

Increased Bandwidth

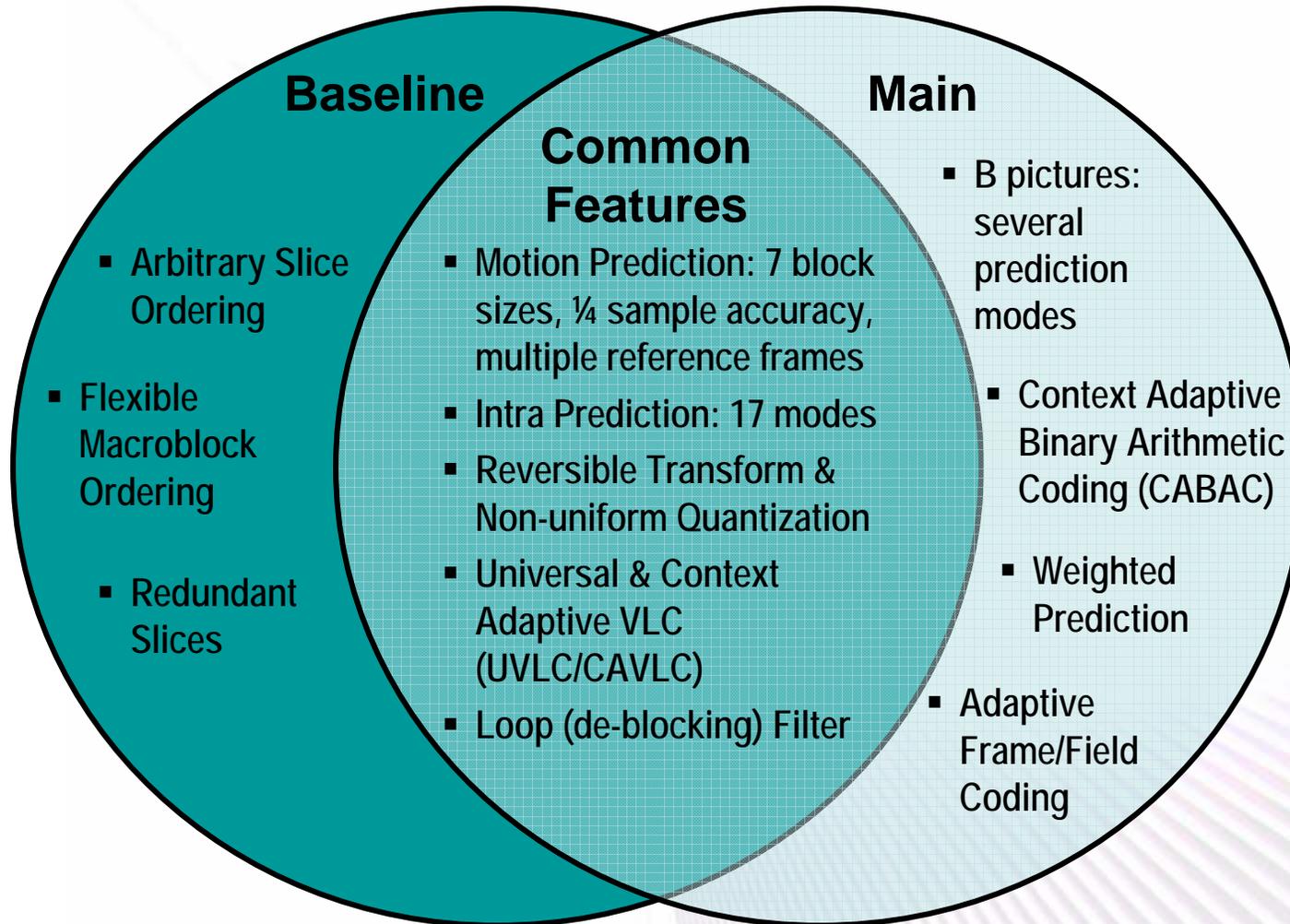
Increased Scalability

Serial RapidIO allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gigabits per second and beyond



- C6455 Serial RapidIO Support – IEEE 1149.6 Compliant
 - 1, 2, or 2.5 GBit/sec per link
 - Up to four 1x links (each 1x link is bidirectional) **--OR--**
 - One 4x link (bi-directional pipe), which provides up to 10 GBit/sec
 - Supports connecting to any other Serial RapidIO device
 - Supports wide variety of network topologies: Rings, Meshes, Stars, & Others
- Benefits
 - 1x Link is fast enough to send HD 1080i raw video between devices
 - 4x Link is easily fast enough to send HD 1080p raw video between devices
 - Reduction in chip count, board area and system cost

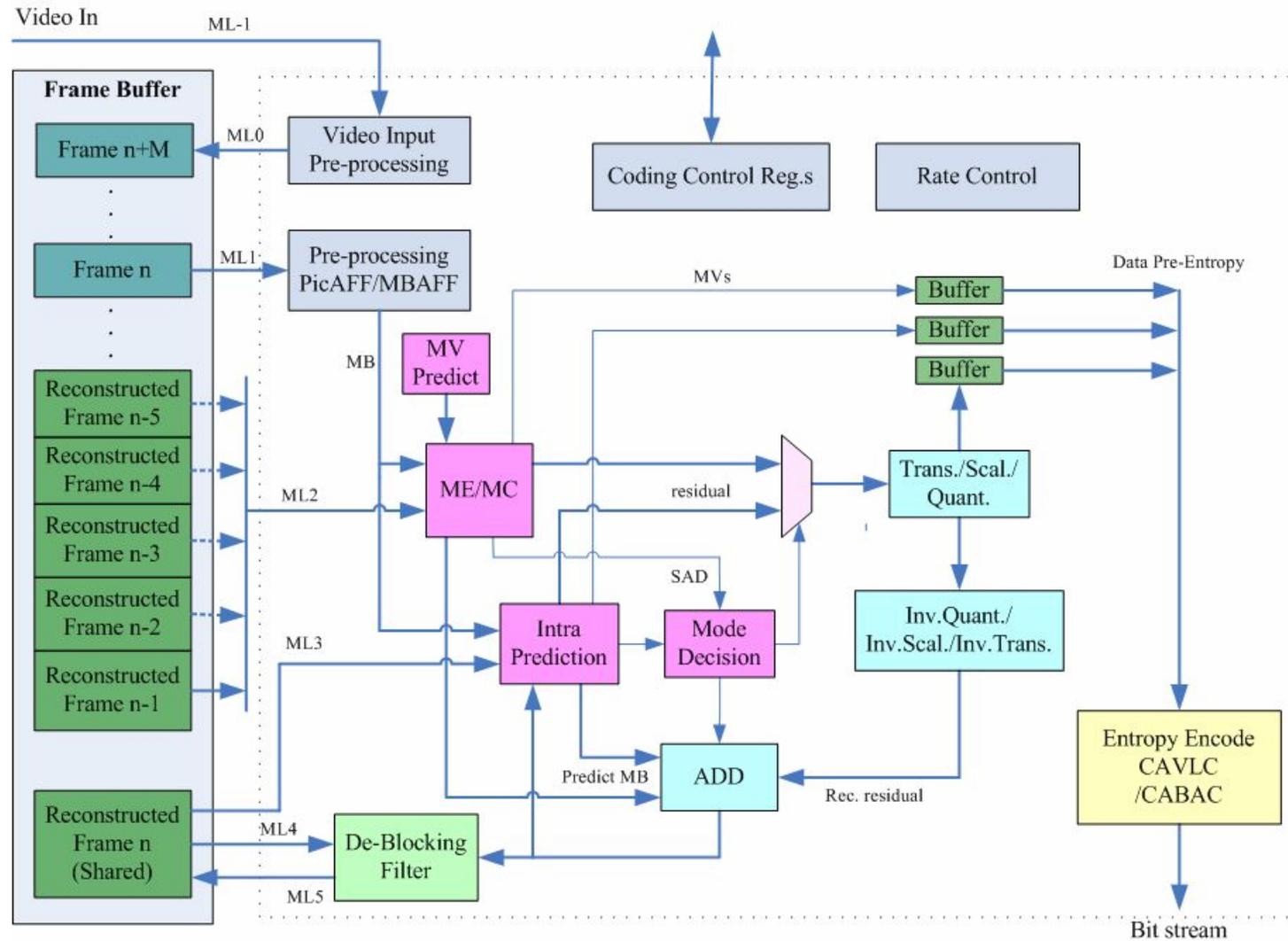
H.264 Quick Introduction



H.264: Baseline & Main Profiles

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H.264 Quick Introduction



Lots of Knobs to Turn

- Resolution
- Frame rate
- Output bitrate
- Encoder Profile (Base, Main, High)
- Encoder Features
 - Search Range
 - Search Algorithm
 - Search Partitions
 - Refinement
 - Number of Reference Frames

All can affect processing load, video quality

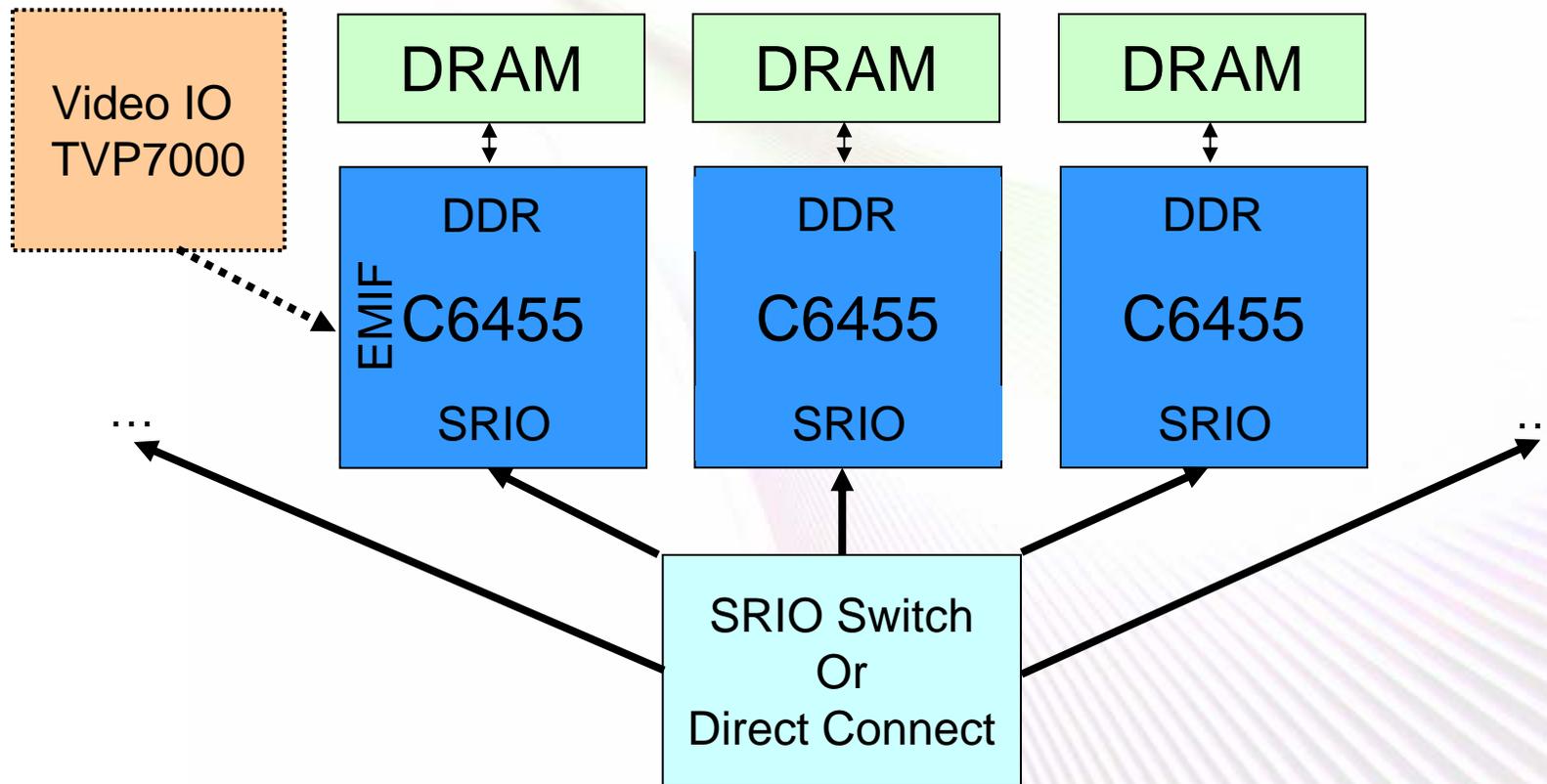
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Multi 6455

- Homogenous processing on “General Purpose” DSP
- Highest Performance
- Most Flexible
- Most Scalable
- Most Software Differentiable

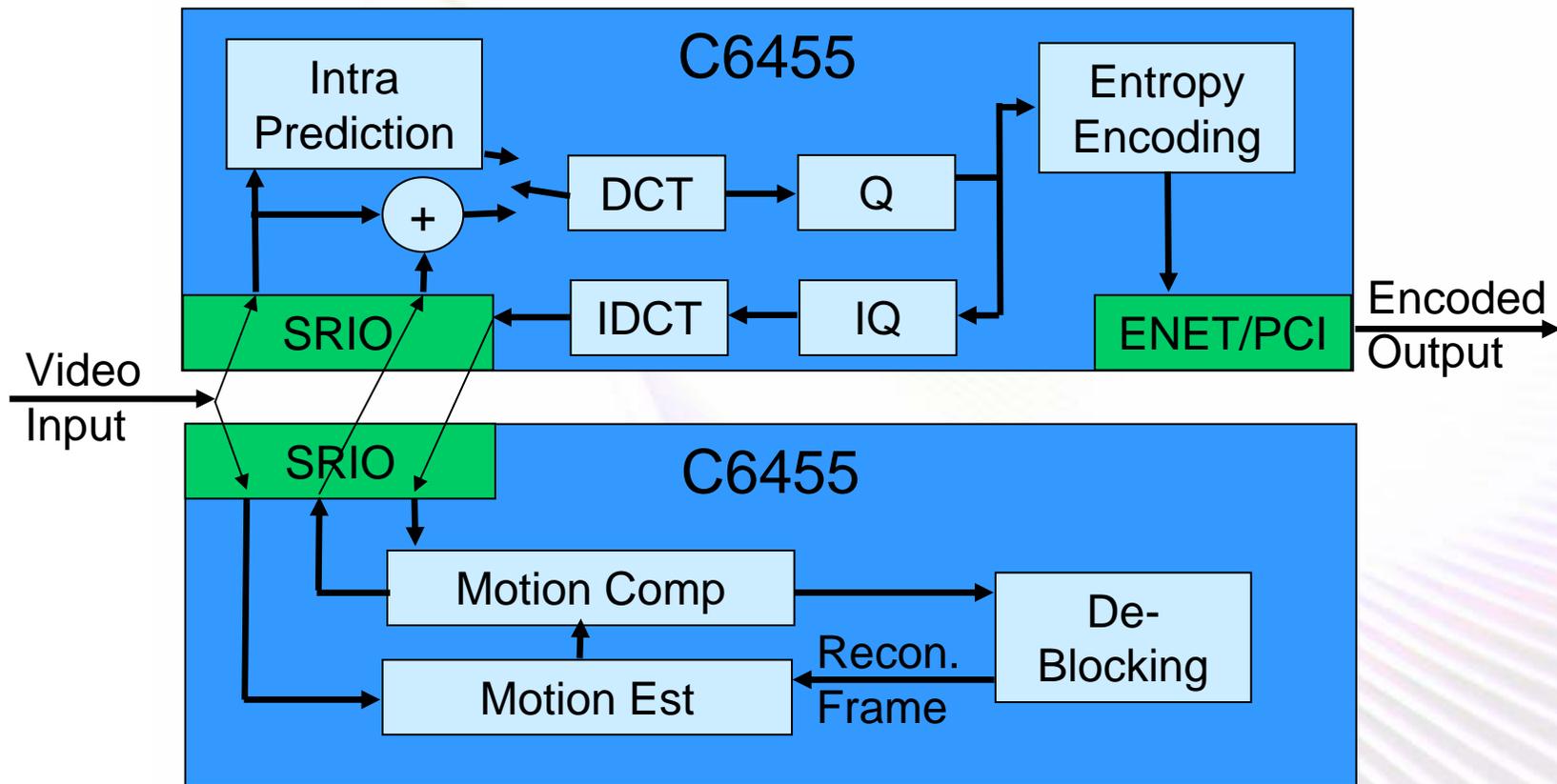
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Multi 6455 - Architecture



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Multi 6455 – Encode Partitioning (Functional Partitioning)



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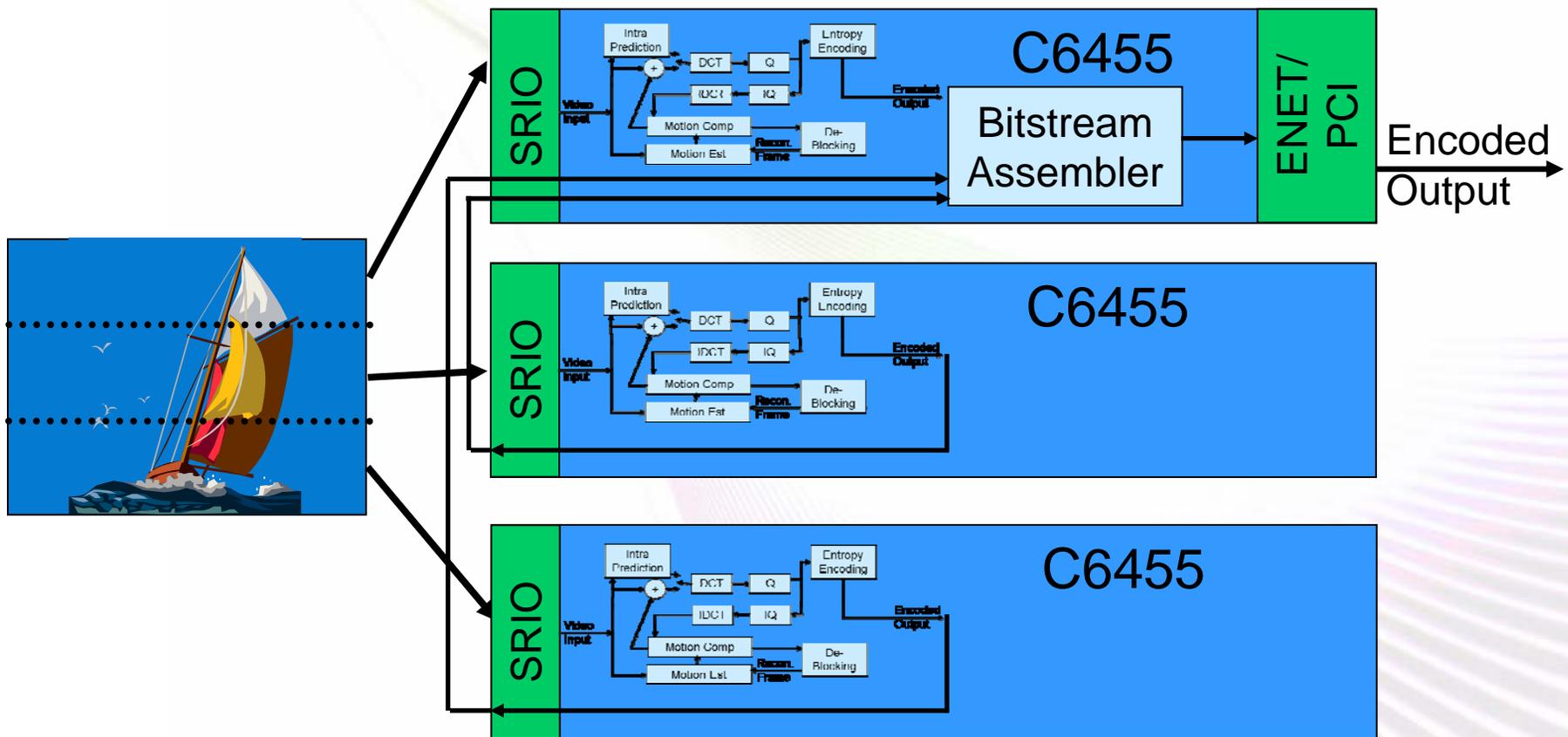
Multi 6455 - Encode Performance (Functional Partition)

Resource \ Est. Utilization	720p30 BP (2 DSPs)	720p30 MP (2 DSPs)
CPU	800 MHz	1200 MHz
SRIO	165 MB/s	165 MB/s
DDR	900 MB/s	1575 MB/s
ENET/PCI	5 Mb/s	5 Mb/s

Resource Utilization is worst case of the DSPs in the system
1 Reference Frame, +/- 64 Search range

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Multi 6455 – Encode Partitioning (Sliced Partition)



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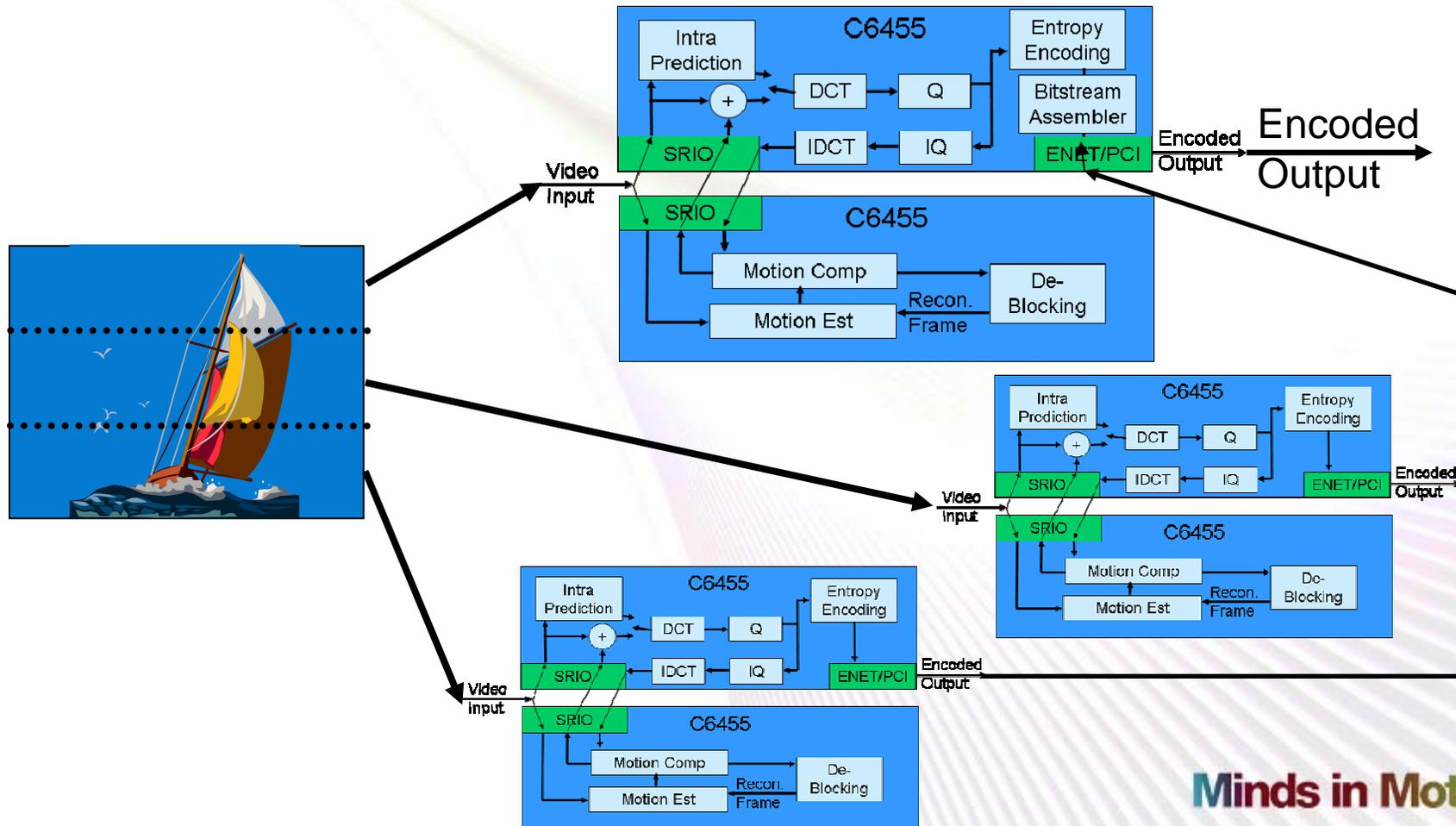
Multi 6455 - Encode Performance (Sliced Partition)

Est. Utilization Resource	720p60 BP (3 DSPs)	720p60 MP (4 DSPs)	1080i60 BP (4 DSPs)	1080i60 MP (6 DSPs)
CPU	880 MHz	1000 MHz	750 MHz	750 MHz
SRIO	210 MB/s	210 MB/s	240 MB/s	240 MB/s
DDR	600 MB/s	790 MB/s	510 MB/s	590 MB/s
ENET/PCI	10 Mb/s	10 Mb/s	10 Mb/s	10 Mb/s

Resource Utilization is worst case of the DSPs in the system
1 Reference Frame, +/- 64 Search range

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Multi 6455 – Encode Partitioning (Combination Partition)



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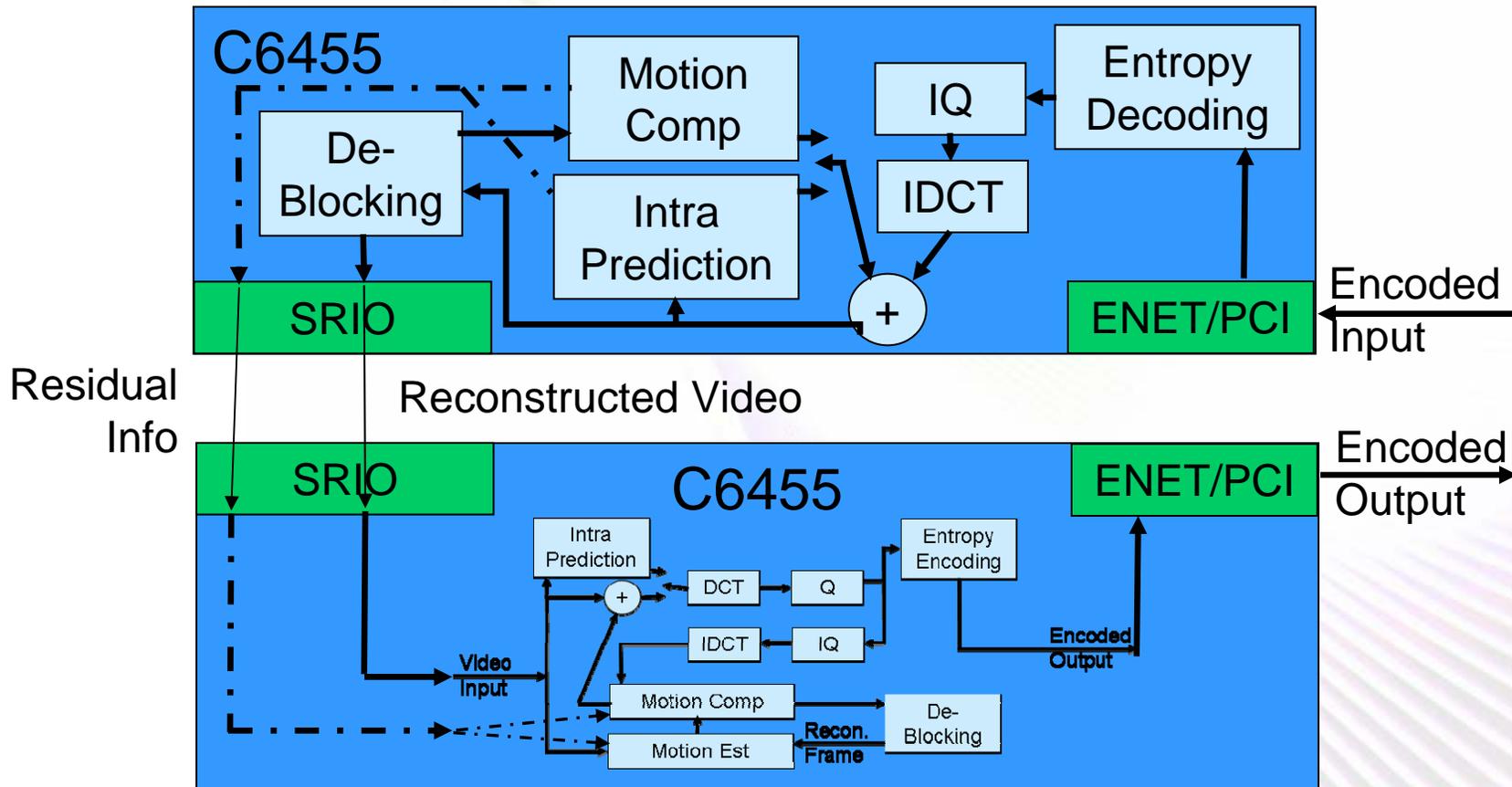
Multi 6455 - Encode Performance (Combination Partition)

Resource \ Est. Utilization	720p60 BP (4 DSPs)	720p60 MP (4 DSPs)	1080i60 BP (4 DSPs)	1080i60 MP (6 DSPs)
CPU	740 MHz	1100 MHz	830 MHz	820 MHz
SRIO	525 MB/s	525 MB/s	600 MB/s	600 MB/s
DDR	600 MB/s	790 MB/s	510 MB/s	590 MB/s
ENET/PCI	20 Mb/s	20 Mb/s	30 Mb/s	30 Mb/s

Resource Utilization is worst case of the DSPs in the system
1 Reference Frame, +/- 64 Search range

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Multi 6455 – Transcode Partitioning



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Multi 6455 - Transcode Performance

Est. Utilization Resource	720p60 BP (3 DSPs)	720p60 MP (4 DSPs)	1080i60 BP (4 DSPs)	1080i60 MP (2 DSPs)
CPU	750 MHz	850 MHz	640 MHz	960 MHz
SRIO	110 MB/s	110 MB/s	120 MB/s	120 MB/s
DDR	120 MB/s	120 MB/s	135 MB/s	135 MB/s
ENET/PCI	20 Mb/s	20 Mb/s	20 Mb/s	20 Mb/s

Resource Utilization is worst case of the DSPs in the system
 1 Reference Frame, Refinement only

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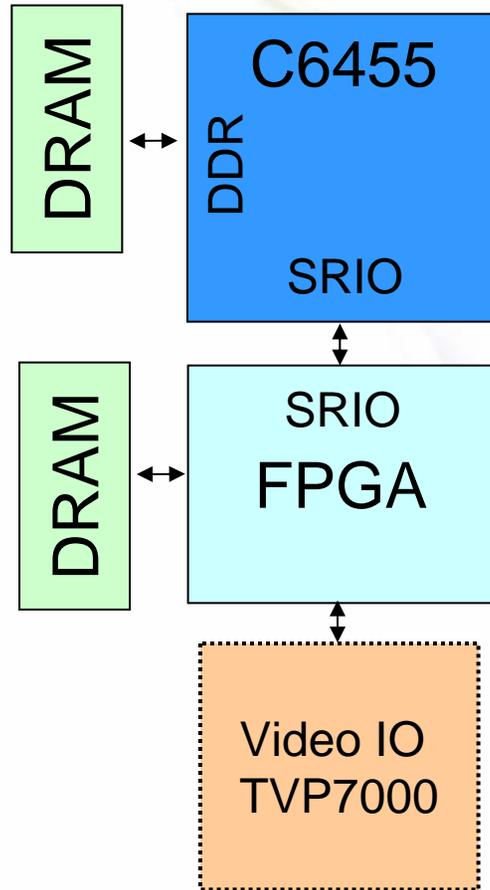
645x + FPGA

- “General Purpose” DSP
- Customizable Acceleration
- Highest Performance
- Flexible
- Scalable
- DSP is ideal for sequential processing steps
- FPGA is ideal for highly parallel processing steps

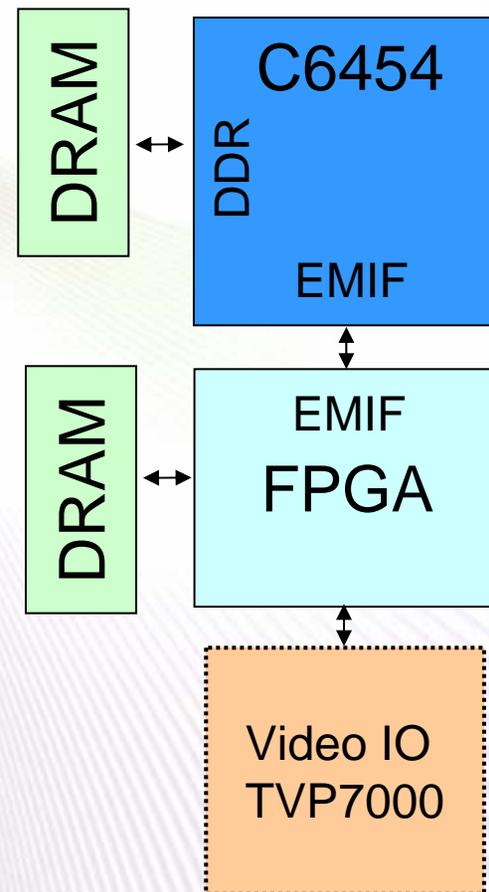
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645x + FPGA - Architecture

With SRIO

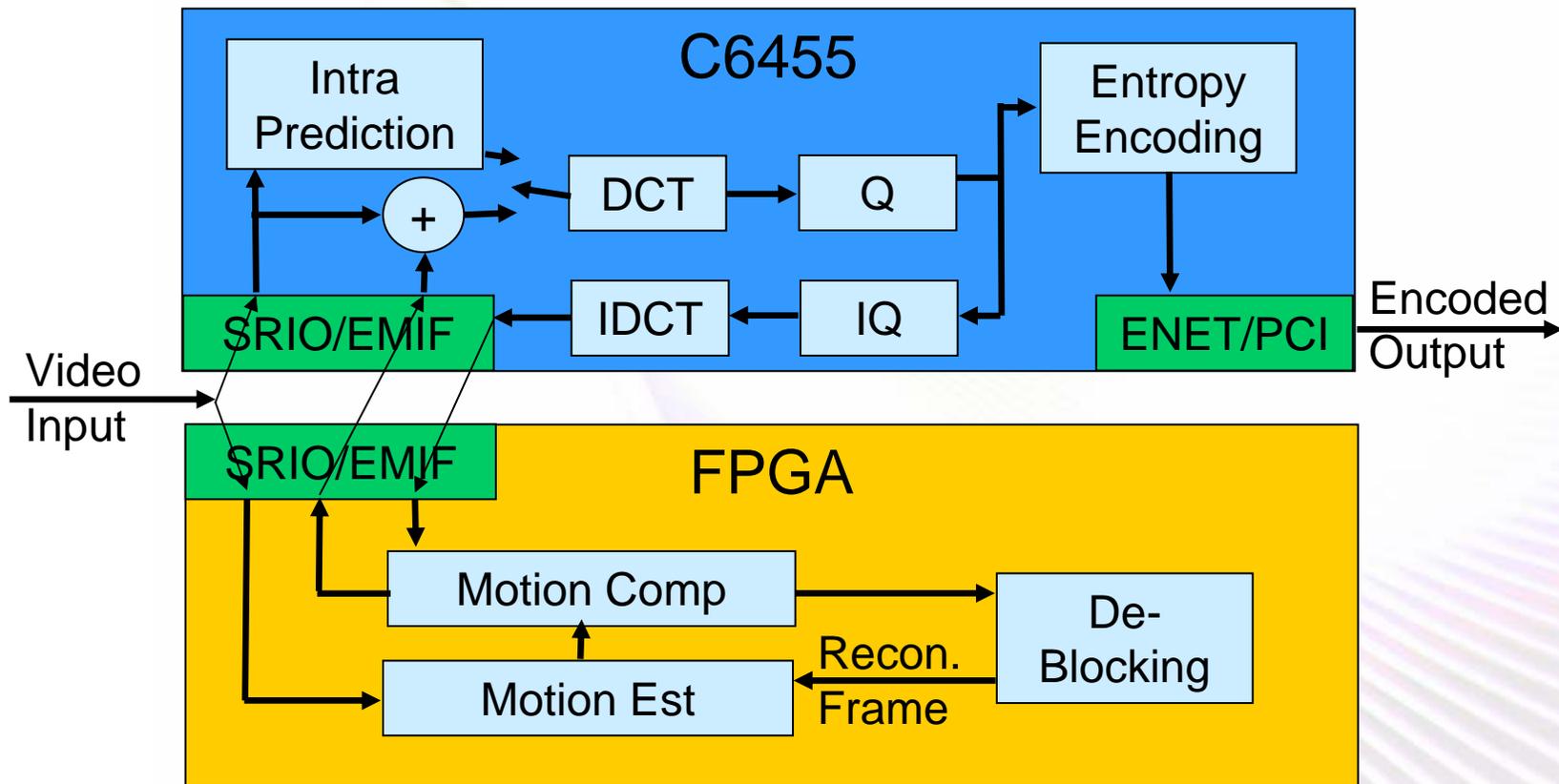


Without SRIO



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645x + FPGA – Encode Partitioning



Minds in Motion

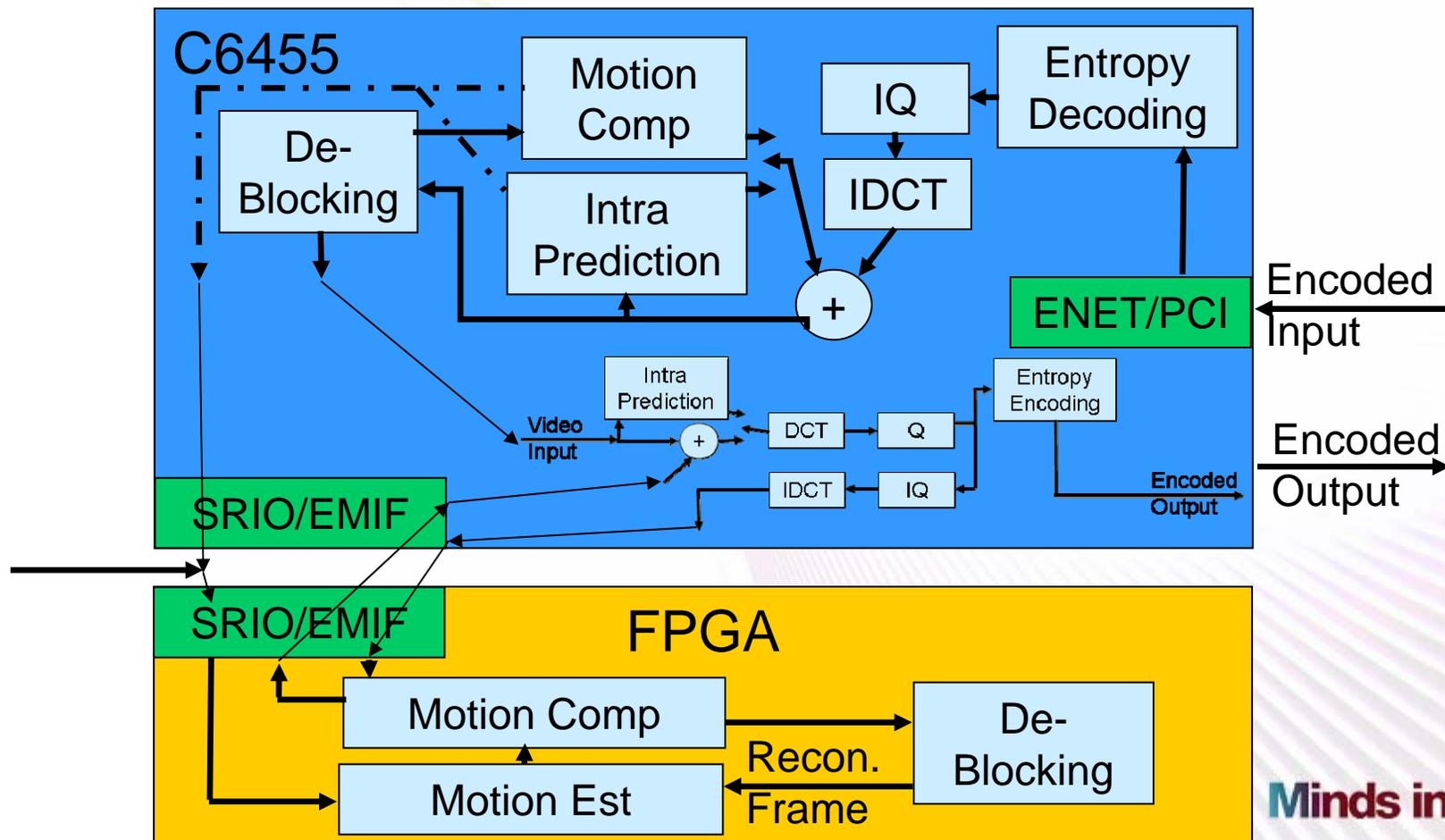
645x + FPGA - Encode Performance

Resource \ Est. Utilization	720p30 BP (1 DSP)	720p30 MP (1 DSP)
CPU	570 MHz	850 MHz
SRIO/EMIF	165 MB/s	165 MB/s
DDR	150 MB/s	165 MB/s
ENET/PCI	5 Mb/s	5 Mb/s

Resource Utilization is worst case of the DSPs in the system
 1 Reference Frame, +/- 64 Search range

Minds in Motion

645x + FPGA – Transcode Partitioning



Minds in Motion

645x + FPGA - Transcode Performance

Resource \ Est. Utilization	720p30 BP (1 DSP)	720p30 MP (2 DSP)
CPU	1170 MHz	850 MHz
SRIO/EMIF	110 MB/s	110 MB/s
DDR	385 MB/s	235 MB/s
ENET/PCI	15 Mb/s	10 Mb/s

Resource Utilization is worst case of the DSPs in the system
 1 Reference Frame, +/- 64 Search range

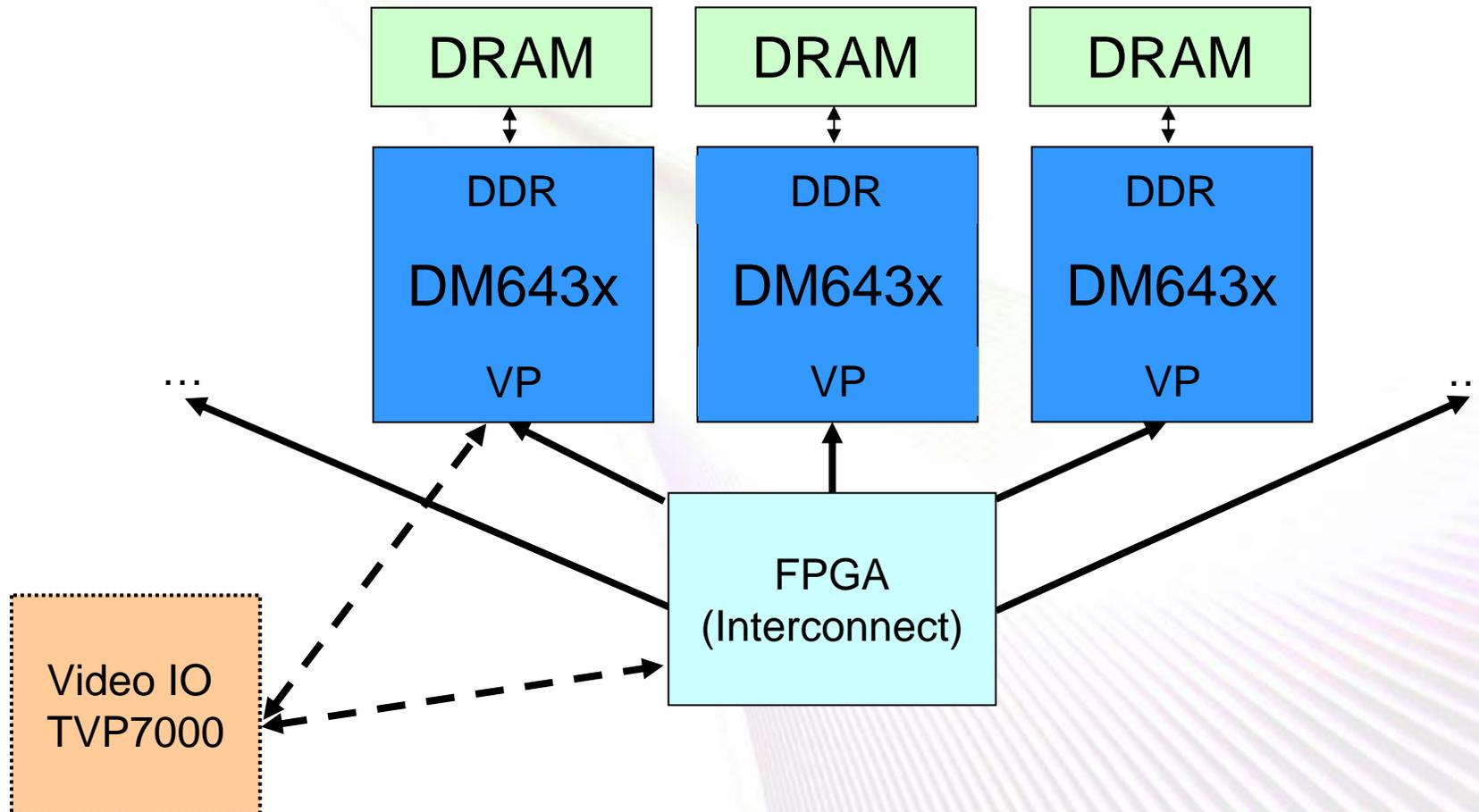
Minds in Motion

Multi DM643x

- Homogenous processing on DSP with Specialized Video IO
- Lower cost
- Flexible
- Scalable
- Software Differentiable

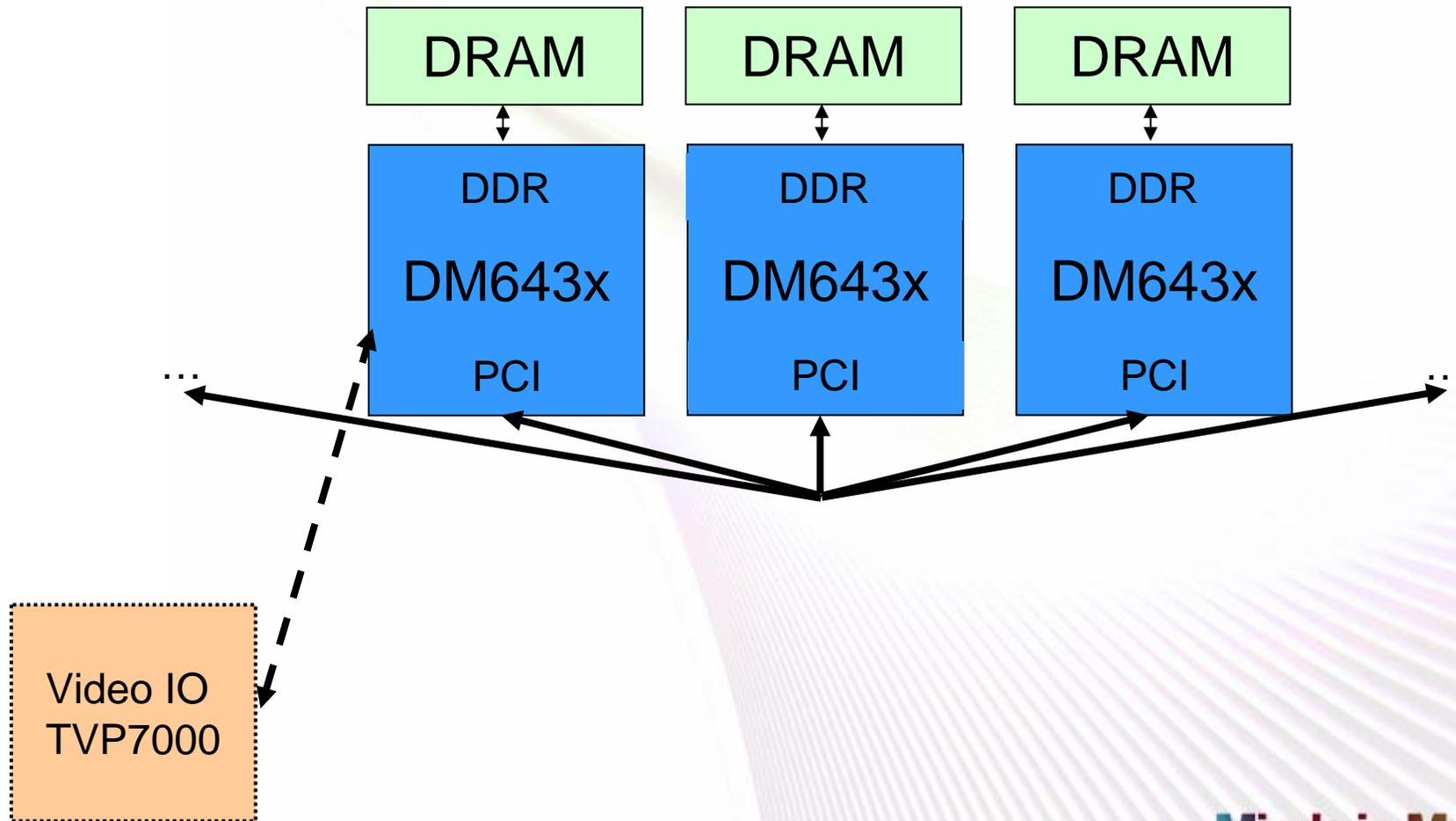
Minds in Motion

Multi DM643x - Architecture



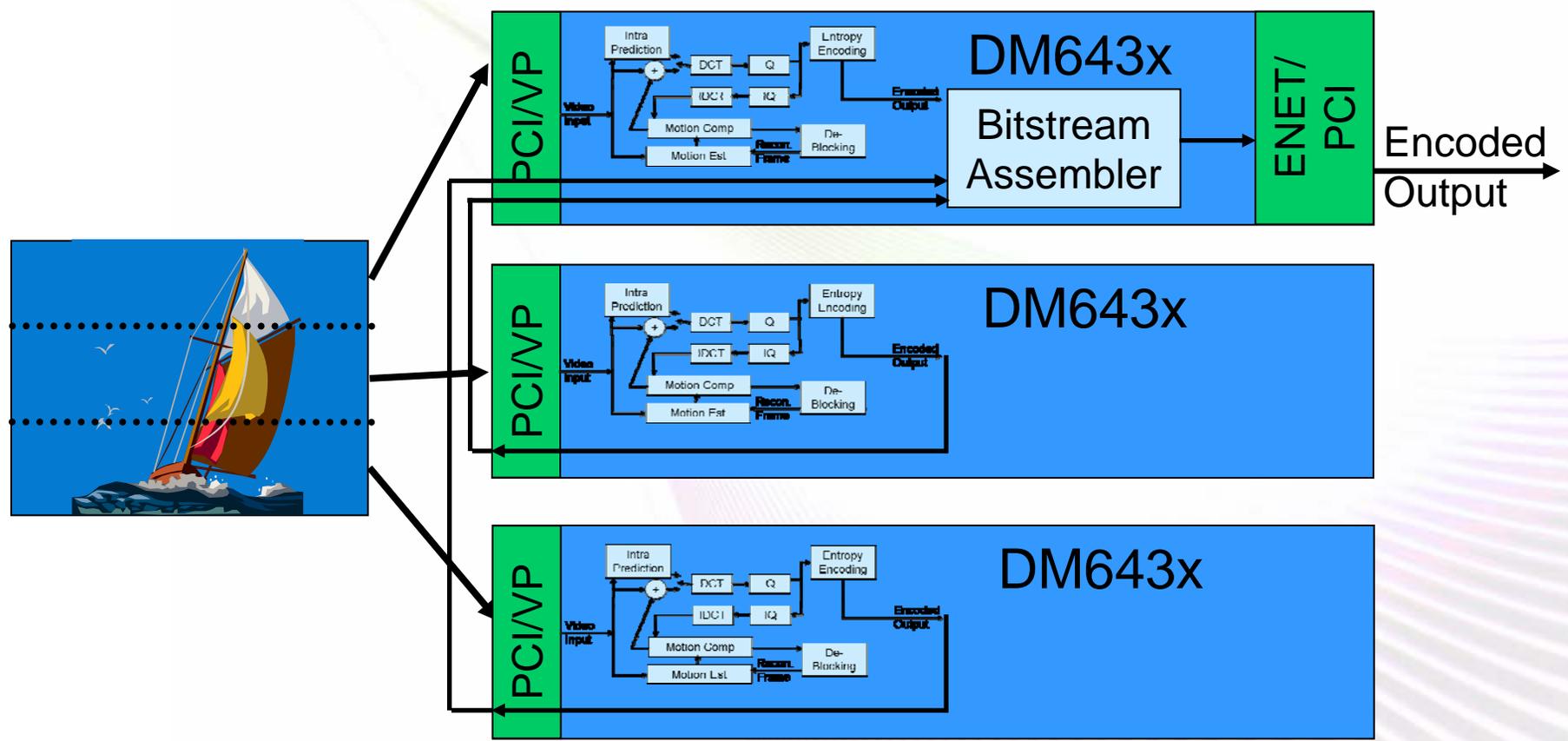
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Multi DM643x - Architecture



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Multi DM643x – Encode Partitioning (Sliced Partition)



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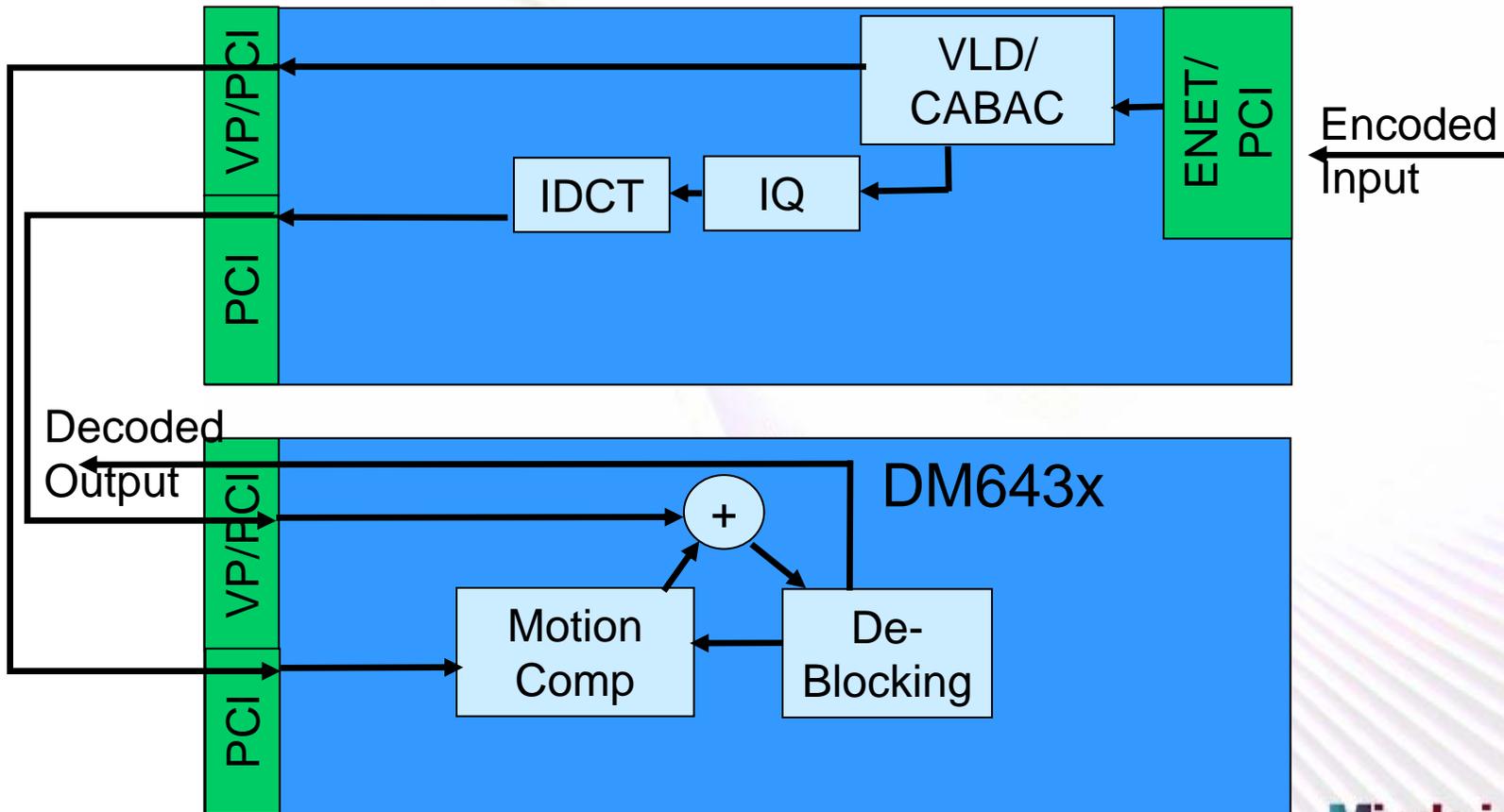
Multi DM643x - Encode Performance (Sliced Partition)

Est. Utilization Resource	480p30 MP (2 DSPs)	720p30 BP (4 DSPs)	720p30 MP (4 DSPs)	1080i60 BP (6 DSPs)
CPU	375 MHz	335 MHz	500 MHz	500 MHz
VP	10 MB/s	15 MB/s	15 MB/s	20 MB/s
DDR	300 MB/s	300 MB/s	520 MB/s	340 MB/s
ENET/PCI	10 Mb/s	20 Mb/s	20 Mb/s	20 Mb/s

Resource Utilization is worst case of the DSPs in the system
1 Reference Frame, +/- 64 Search range

Minds in Motion

Multi DM643x – Decode Partitioning



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Multi DM643x - Decode Performance

Resource \ Est. Utilization	720p30 MP (2 DSPs)	720p60 BP (2 DSPs)	1080i60 BP (2 DSPs)
CPU	330 MHz	440 MHz	500 MHz
VP	110 MB/s	220 MB/s	240 MB/s
DDR	415 MB/s	470 MB/s	530 MB/s
ENET/PCI	10 Mb/s	20 Mb/s	20 Mb/s

Resource Utilization is worst case of the DSPs in the system

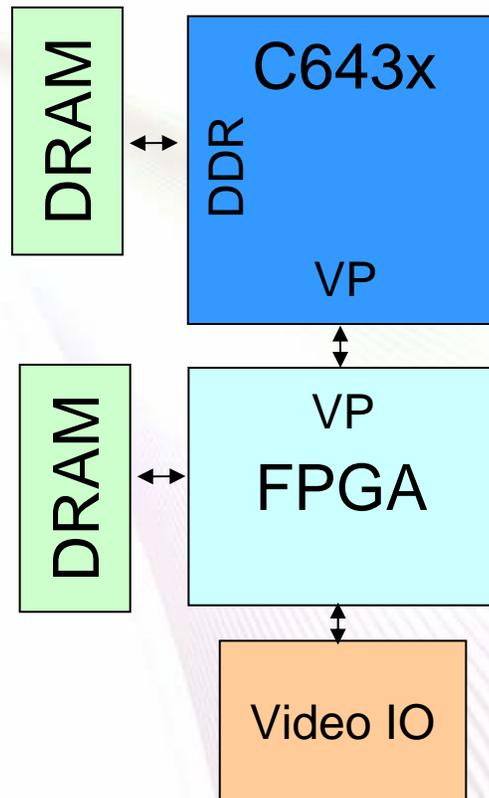
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DM643x + FPGA

- DSP with Specialized Video IO
- Customizable Acceleration
- Lower Cost
- Flexible
- DSP is ideal for sequential processing steps
- FPGA is ideal for highly parallel processing steps

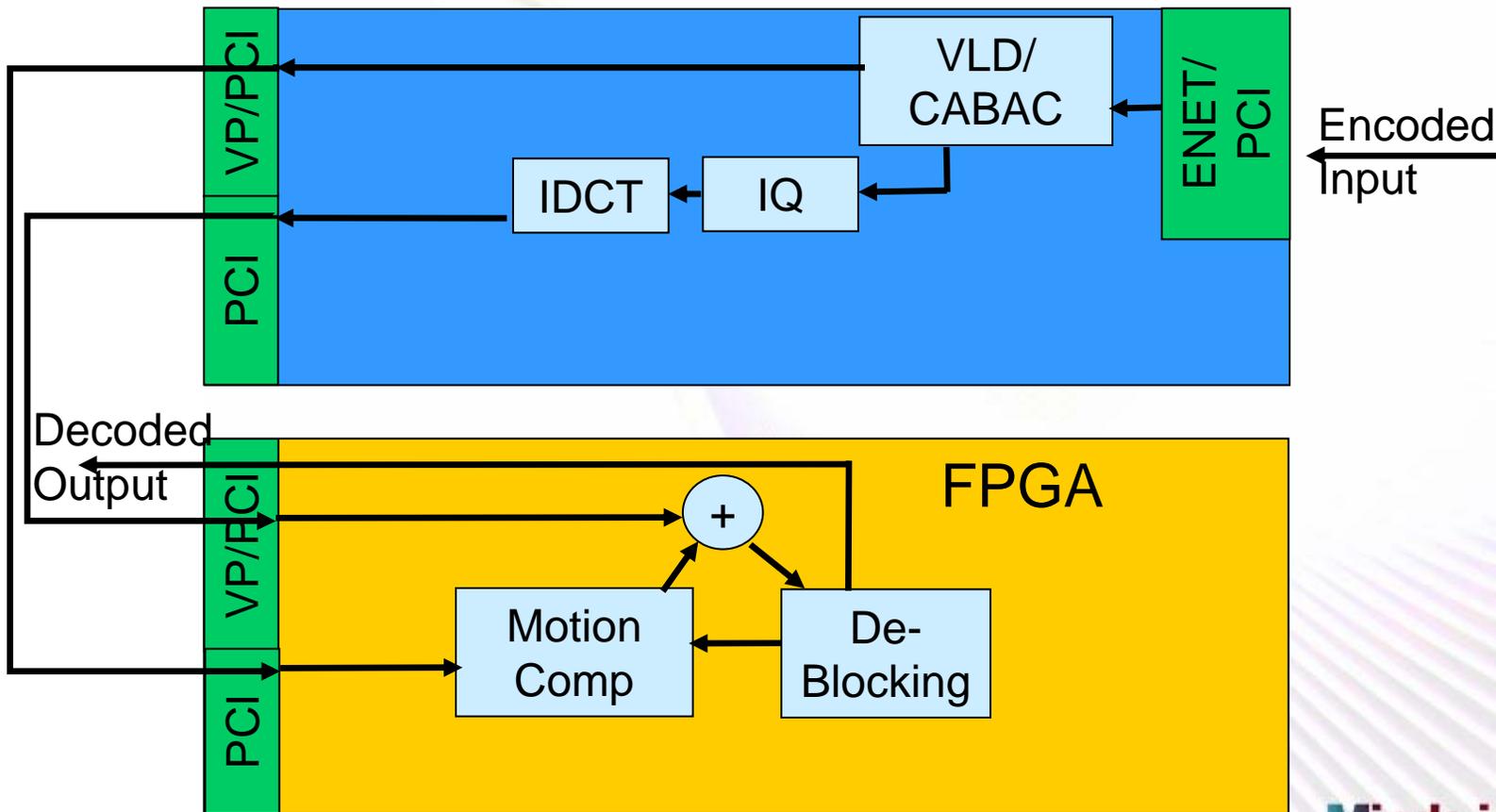
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643x + FPGA - Architecture



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DM643x + FPGA – Decode Partitioning



Minds in Motion

DM643x + FPGA - Decode Performance

Est. Utilization Resource	720p30 MP (1 DSP)	720p60 BP (1 DSP)	1080i60 BP (1 DSP)
CPU	330 MHz	440 MHz	500 MHz
VP	60 MB/s	110 MB/s	120 MB/s
DDR	150 MB/s	150 MB/s	150 MB/s
ENET/PCI	10 Mb/s	20 Mb/s	20 Mb/s

Resource Utilization is worst case of the DSPs in the system

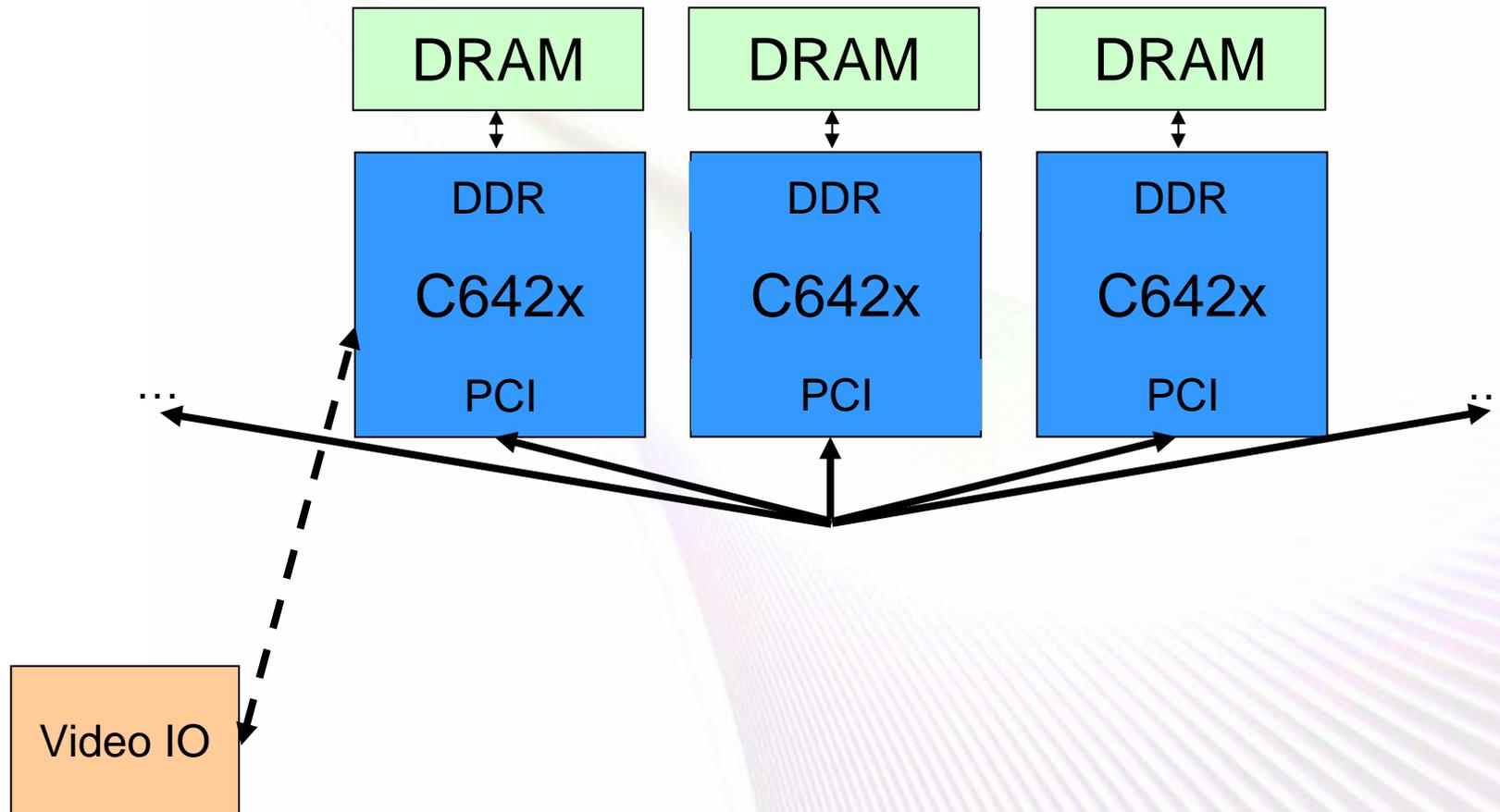
Minds in Motion

Multi C642x

- Homogenous processing on “General Purpose” DSP
- Lowest Cost
- Flexible
- Some Scalability
- Software Differentiable

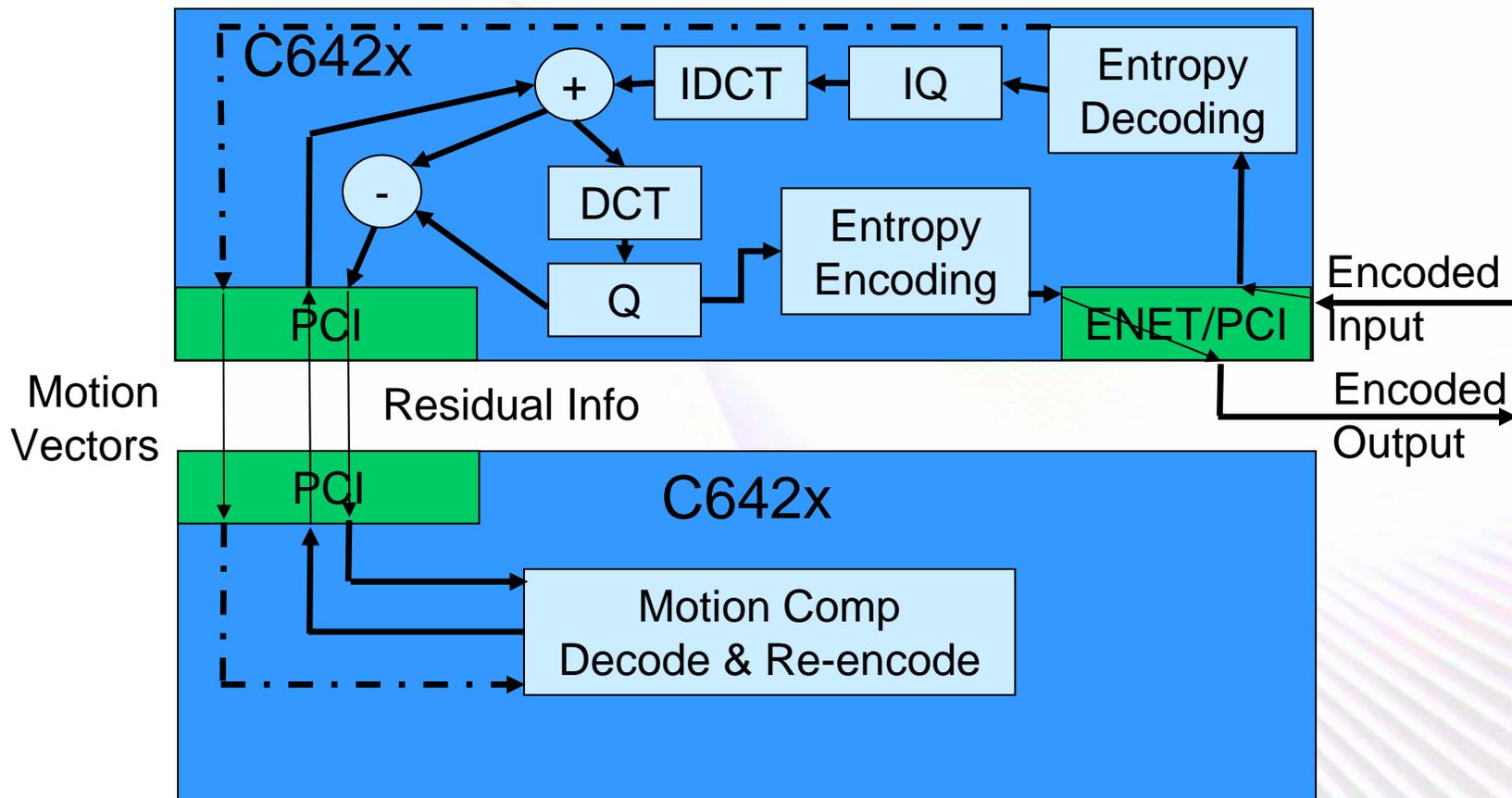
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Multi C642x - Architecture



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Multi C642x – Transrate Partitioning



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Multi C642x - Transrate Performance

Resource \ Est. Utilization	480p30 MP (2 DSPs)	720p30 BP (2 DSPs)
CPU	320 MHz	570 MHz
PCI	40 MB/s	105 MB/s
DDR	155 MB/s	235 MB/s
ENET/PCI	15 Mb/s	30 Mb/s

Resource Utilization is worst case of the DSPs in the system
 No Motion Estimation

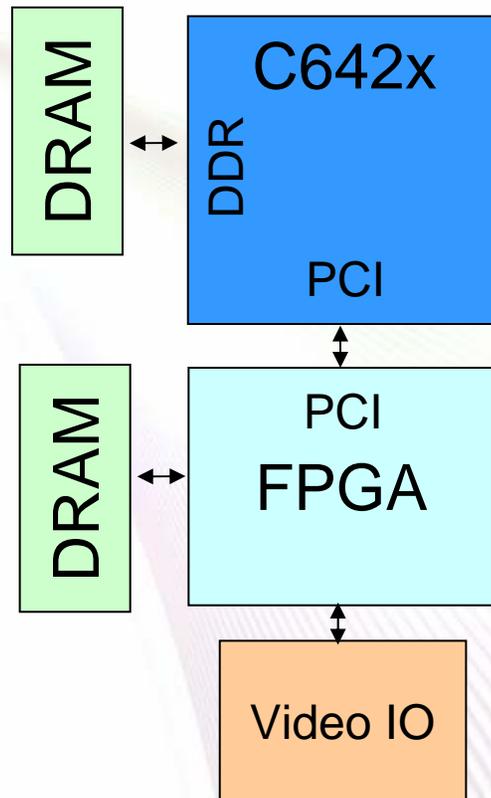
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C642x + FPGA

- “General Purpose” DSP
- Customizable Acceleration
- Lowest Cost

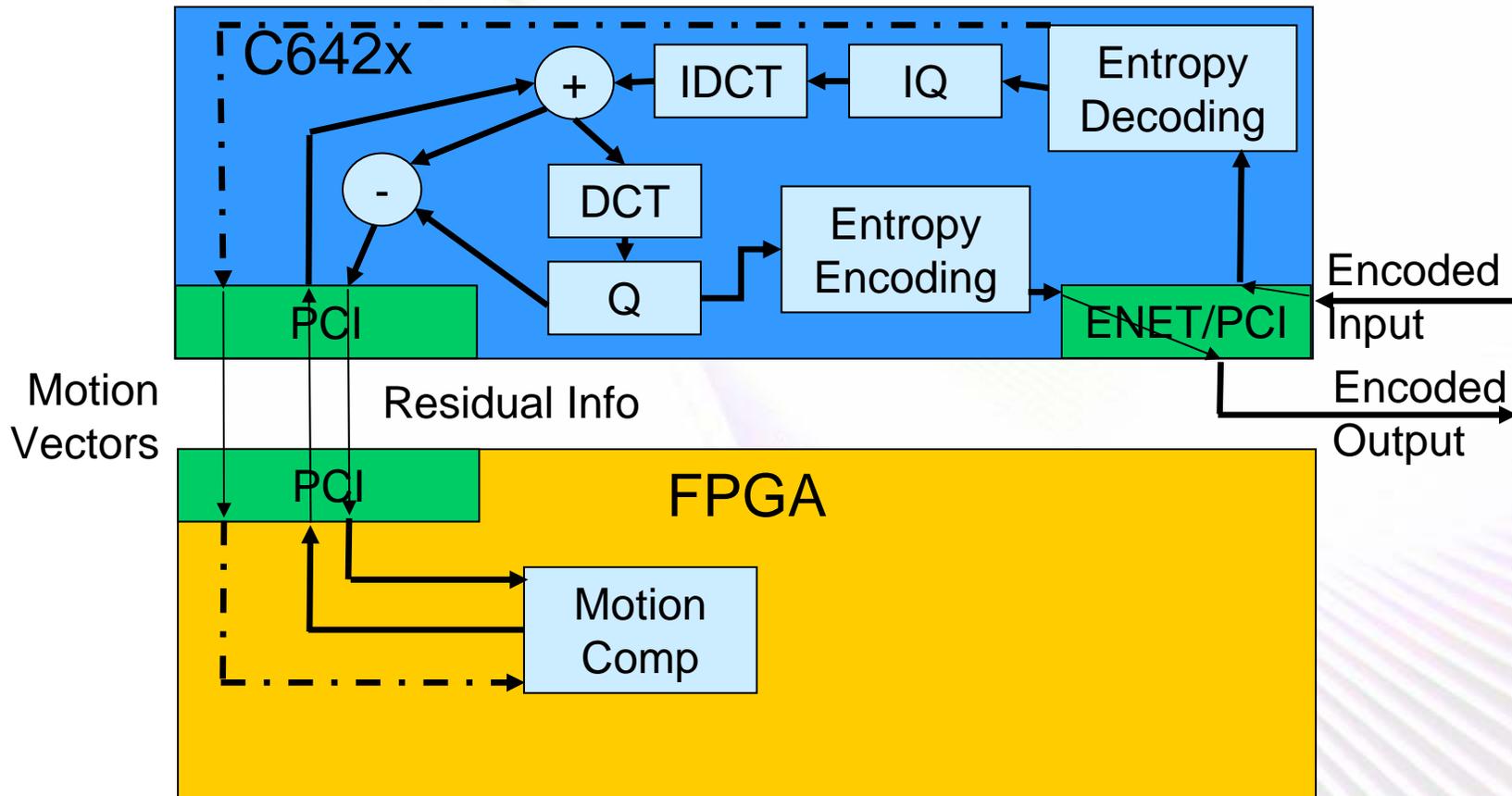
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642x + FPGA - Architecture



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C642x + FPGA – Transrate Partitioning



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C642x + FPGA - Transrate Performance

Resource \ Est. Utilization	480p30 MP (2 DSPs)	720p30 BP (2 DSPs)
CPU	320 MHz	570 MHz
PCI	40 MB/s	105 MB/s
DDR	155 MB/s	235 MB/s
ENET/PCI	15 Mb/s	30 Mb/s

Resource Utilization is worst case of the DSPs in the system
 No Motion Estimation

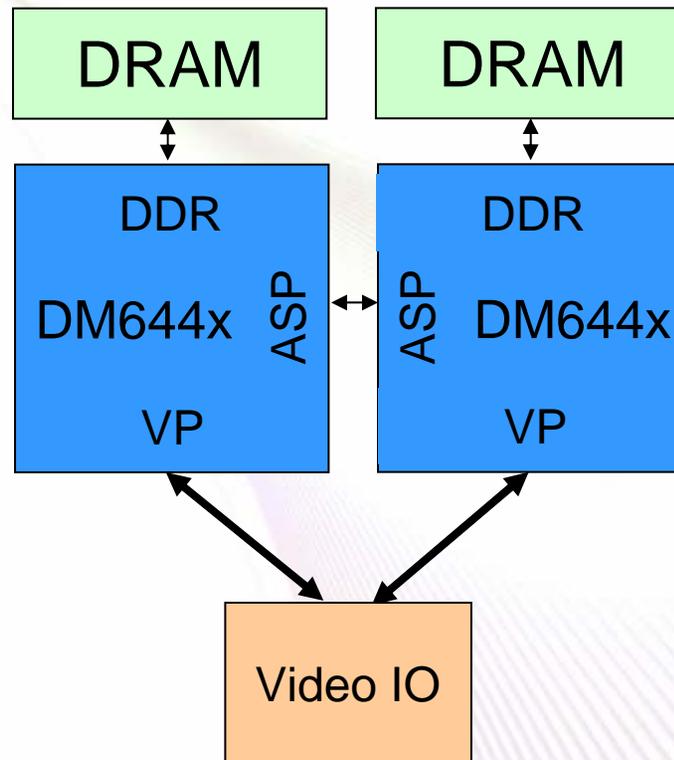
Minds in Motion

Multi DM644x (DaVinci™)

- Homogenous Multiprocessing on Specialized Video DSP
 - On-board accelerators
 - Video IO
- Wide 3rd Party & Video Library Support
- Lower cost

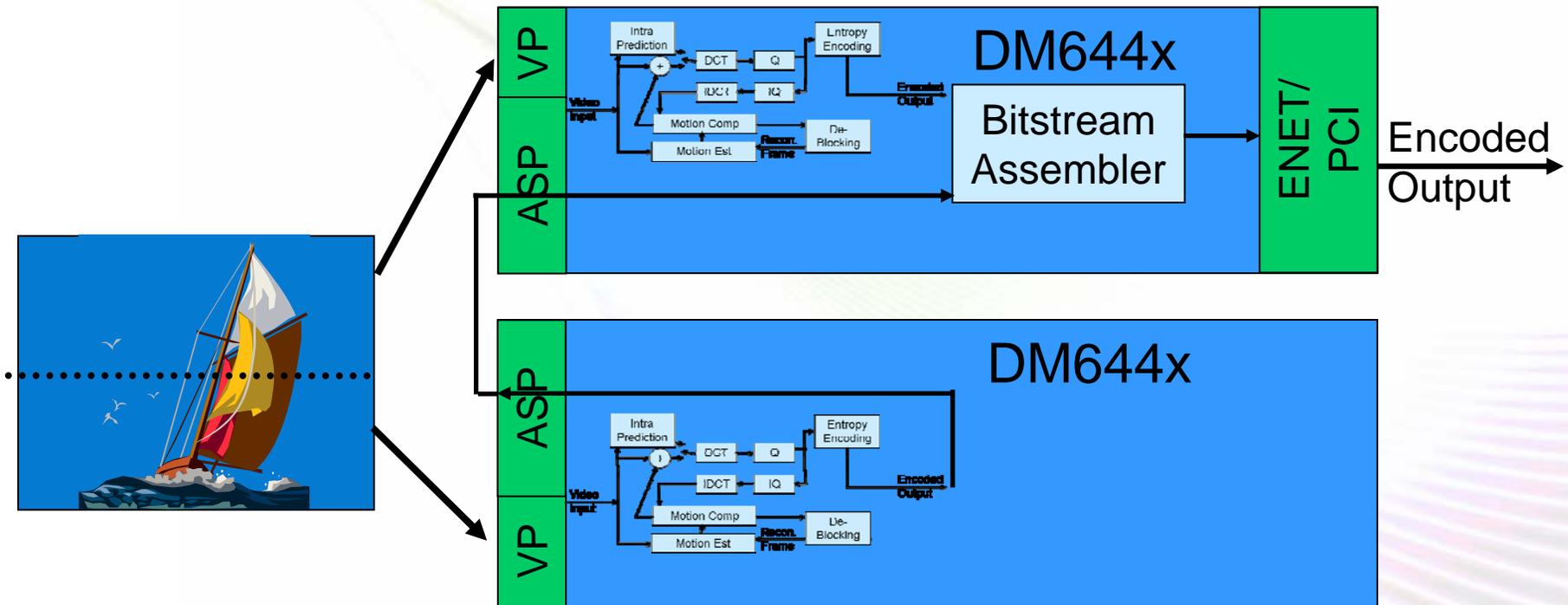
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Multi DaVinci™ - Architecture



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Multi DaVinci – Encode Partitioning (Sliced Partition)



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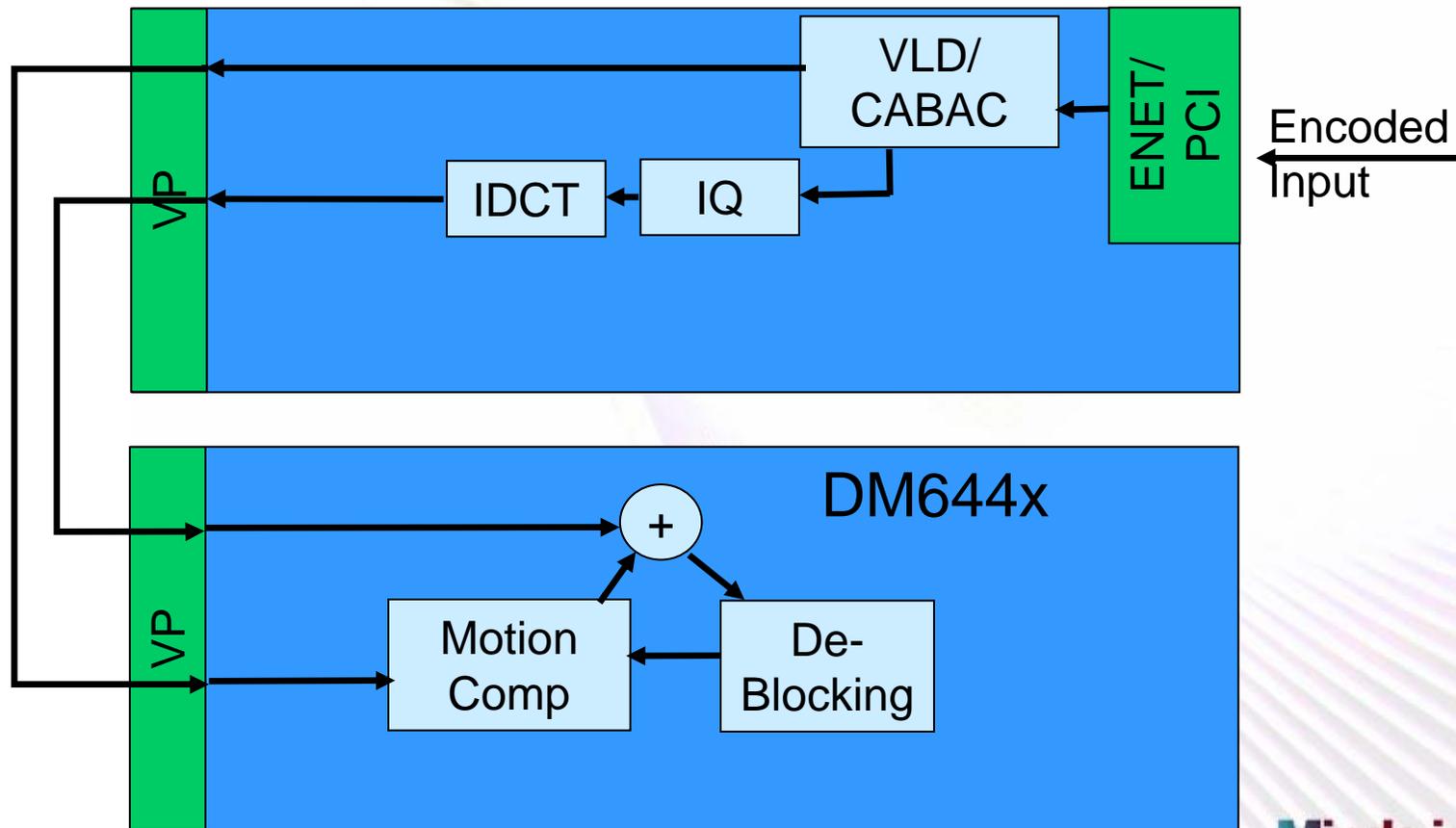
Multi DaVinci™ - Encode Performance

Resource \ Est. Utilization	480p30 MP (2 DSPs)	720p30 BP (2 DSPs)
CPU	310 MHz	550 MHz
VP	10 MB/s	30 MB/s
DDR	150 MB/s	225 MB/s
ENET/PCI	5 Mb/s	10 Mb/s

Resource Utilization is worst case of the DSPs in the system
 1 Reference Frame, +/- 32 Search range

Minds in Motion

Multi DaVinci – Decode Partitioning



Minds in Motion

Multi DaVinci™ - Decode Performance

Resource \ Est. Utilization	480p30 MP (2 DSPs)	720p30 BP (2 DSPs)
CPU	250 MHz	440 MHz
VP	40 MB/s	110 MB/s
DDR	145 MB/s	220 MB/s
ENET/PCI	5 Mb/s	10 Mb/s

Resource Utilization is worst case of the DSPs in the system
 1 Reference Frame, +/- 32 Search range

Minds in Motion

Conclusions

- Elegant solutions exist for video systems that won't fit in one DSP
- Many different solutions for different
 - Resolutions
 - Quality needs
 - Price points
- Mixing and combining examples shown creates an even wider spectrum of solutions

Minds in Motion

DSP Solutions For High Quality Video Systems

Todd Hiers
Texas Instruments

