TI | Developer Conference
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Minds in Motion

ScanExpress JET

Combining JTAG Test with JTAG Emulation to Reduce Prototype Development Time

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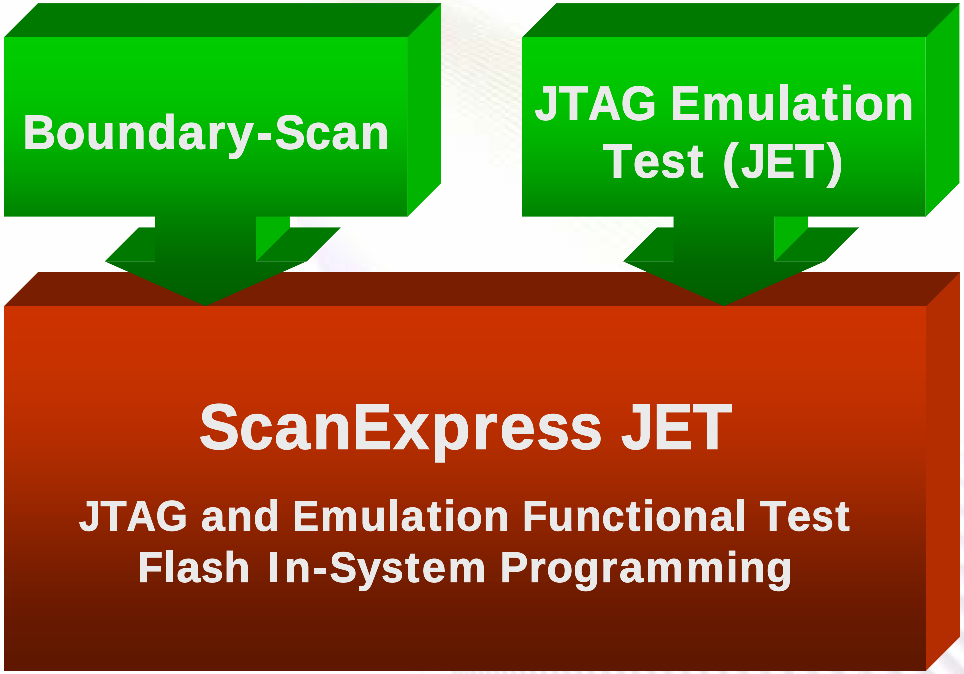
An EWA Technologies Company

Blackhawk™
by EWA Technologies, Inc.

What Is ScanExpress JET?

A powerful combination of boundary-scan structural testing with JTAG in-circuit emulation functional testing within a single tool



Boundary-Scan

JTAG Emulation Test (JET)

ScanExpress JET

JTAG and Emulation Functional Test
Flash In-System Programming

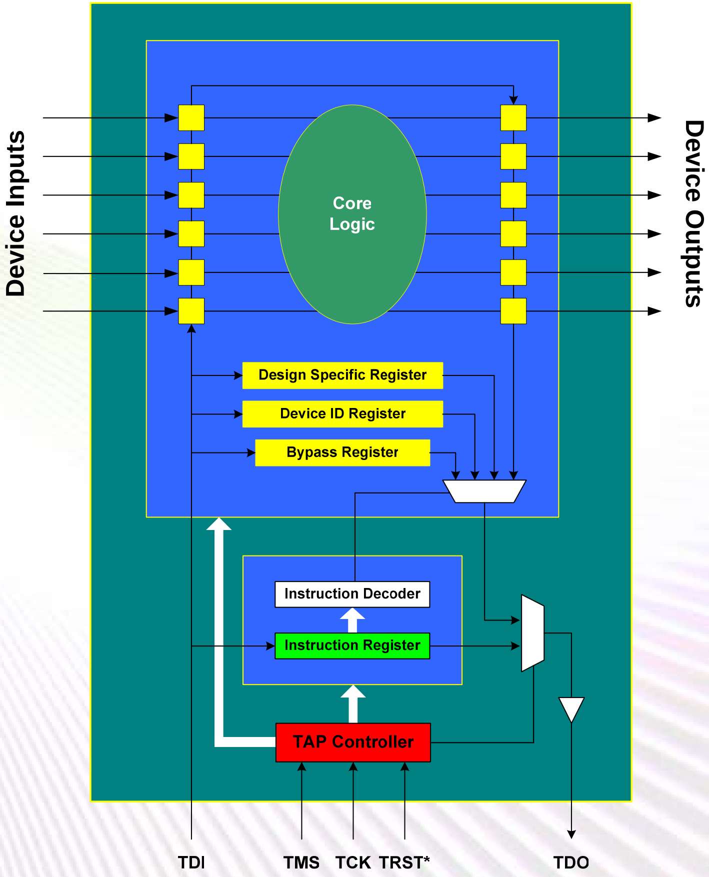
Typical PCB Production Flow

- Structural test is performed via boundary-scan or ICT.
- Functional test is performed at the board level at-speed with various techniques.
- System test is performed on the whole product at-speed before shipment.

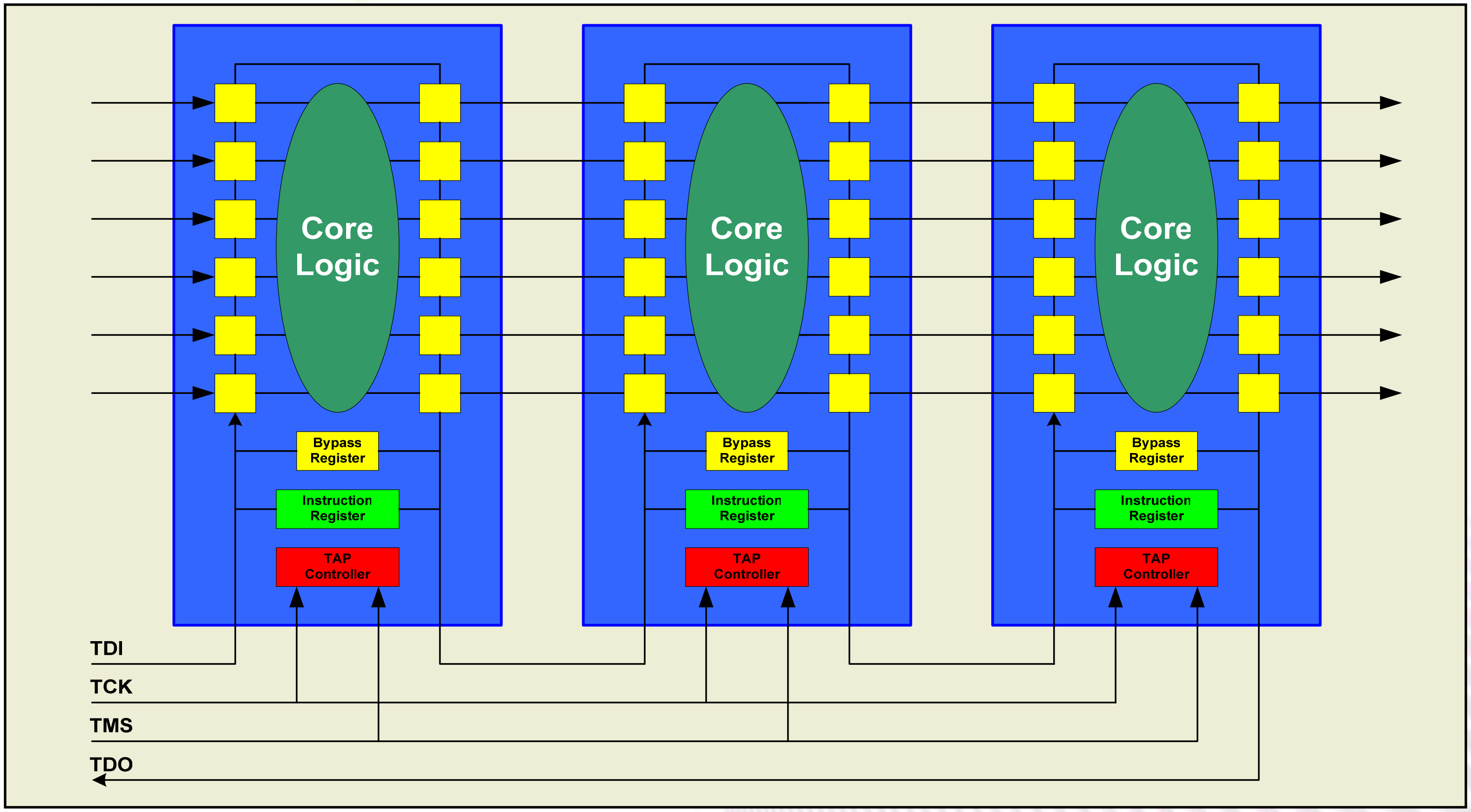
Boundary-Scan Test

Main Building Blocks of a Boundary-Scan Device

- JTAG interface pins
- Test data registers
- Instruction register
- TAP controller



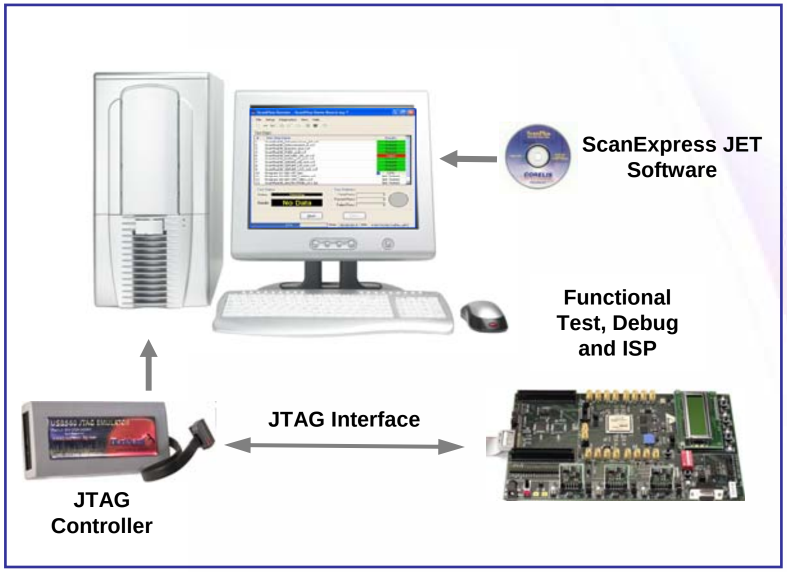
Boundary-Scan Test

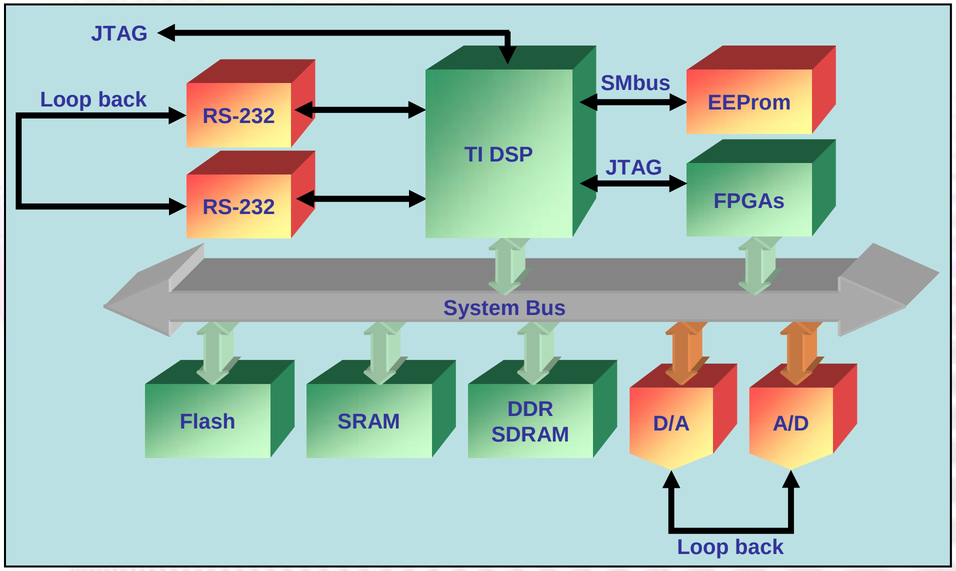


JTAG Emulation Test

JTAG Emulation Test uses a processor’s JTAG debug port to perform:

- At-speed functional testing of boards.
- In-system-programming (ISP) of flash devices.





Why Is JET Necessary?

- Boundary-scan structural testing is incomplete.
  - Does not test interconnects between non-boundary-scan components such as clusters and analog components.
- Boundary-scan is a static test.
  - Tests are not performed at-speed.
  - Boards tested with boundary-scan may fail at-speed system level test,
  - In-system programming time of flash devices may be long.

Capabilities of JET

- Utilizes on-board processor to:
  - Increase test coverage for non-JTAG components by using functional tests of all CPU addressable devices.
  - Initialize devices such as a memory controllers and I/O to test them by applying reads and writes.
- Tests the board at-speed.
  - Tests execute at full UUT processor speed.
- Programs flash memories at their fastest theoretical programming speed.

Capabilities of JET

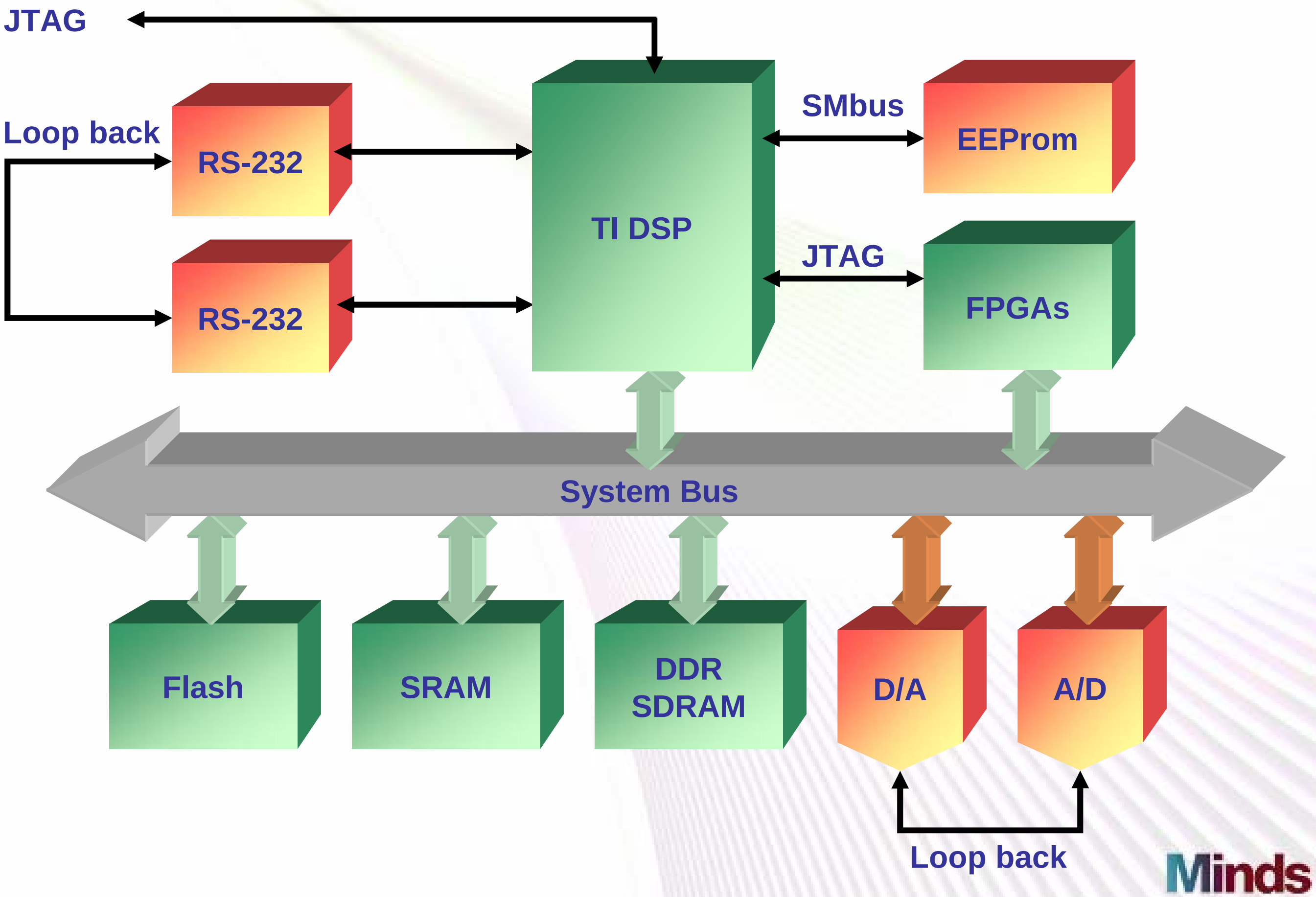
- Integrated CodeRunner/CodeSymphony source level debugger to help debug application code
  - Provides run control (single step, set breakpoints, etc.)
  - High-speed downloading of code.
  - Display and modify system resources.
  - Symbolic debugging.
  - Assists in target debug and fault isolation.
- Integrated Target-Assisted Flash Programmer (TAFP) allows flash programming at theoretical speeds.

ScanExpress JET Coverage

ScanExpress + JET = ScanExpress JET

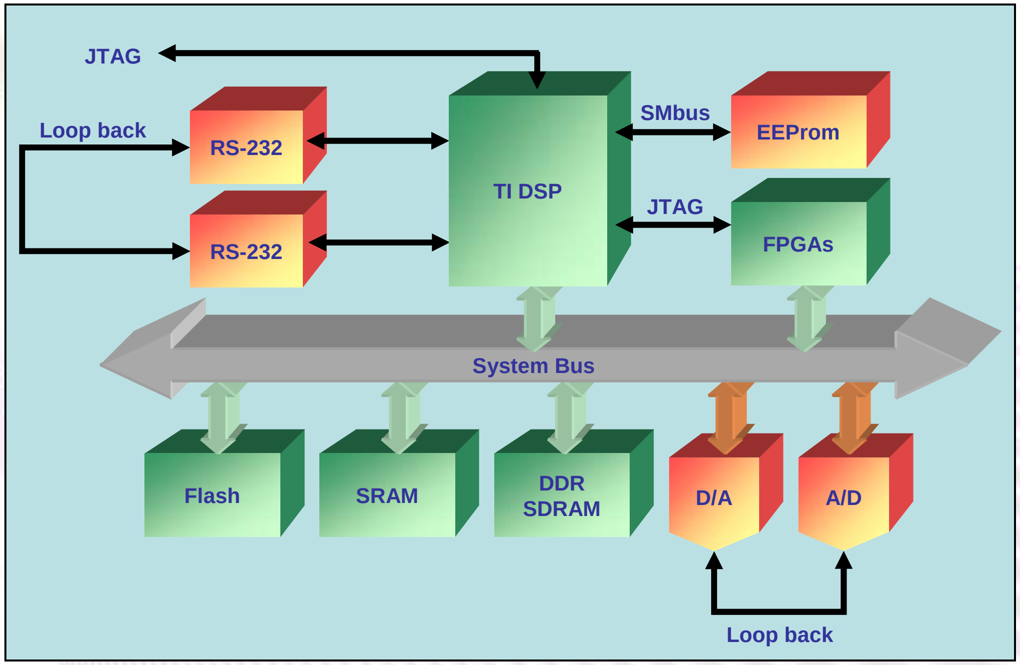
Feature	Boundary-Scan Tests	Functional Test	ScanExpress JET
Structural coverage	Very good	Good	Excellent
Functional coverage	Low	High	High
Programming (ISP) time	Average	Excellent	Excellent
Test time	Fast	Fast	Fast
Test points required	Very few	Very few	Very few
Test development	Automatic	Semi auto	Auto/semi
Diagnostics	Excellent	Average	Excellent

Typical Test Case



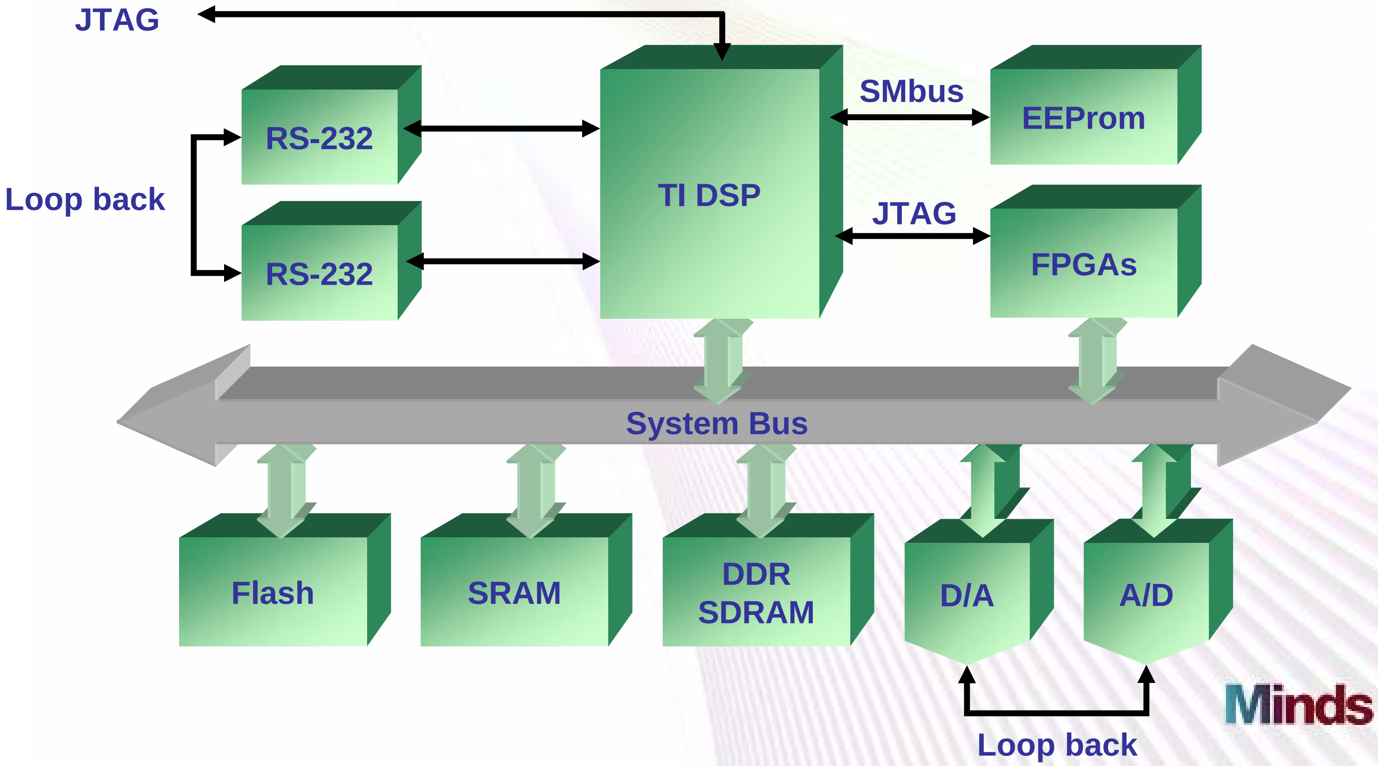
Typical Test Case

- Board includes JTAG and non-JTAG components.
- JTAG components include a CPU with two FPGAs.
- SRAM, SDRAM, and flash memory can be tested using JTAG techniques.
- EEPROM, RS-232 drivers, and D/A and A/D cannot be tested using JTAG.



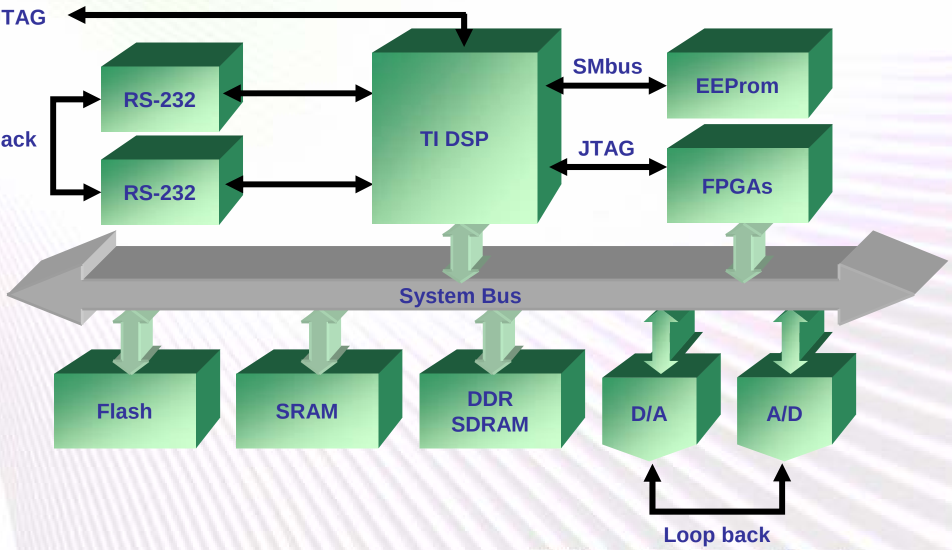
Typical Test Case

- Boundary-scan tests are applied on five components.
- JTAG emulation functional test is performed on additional five components.
- Using ScanExpress JET, all the components in this circuit are tested.



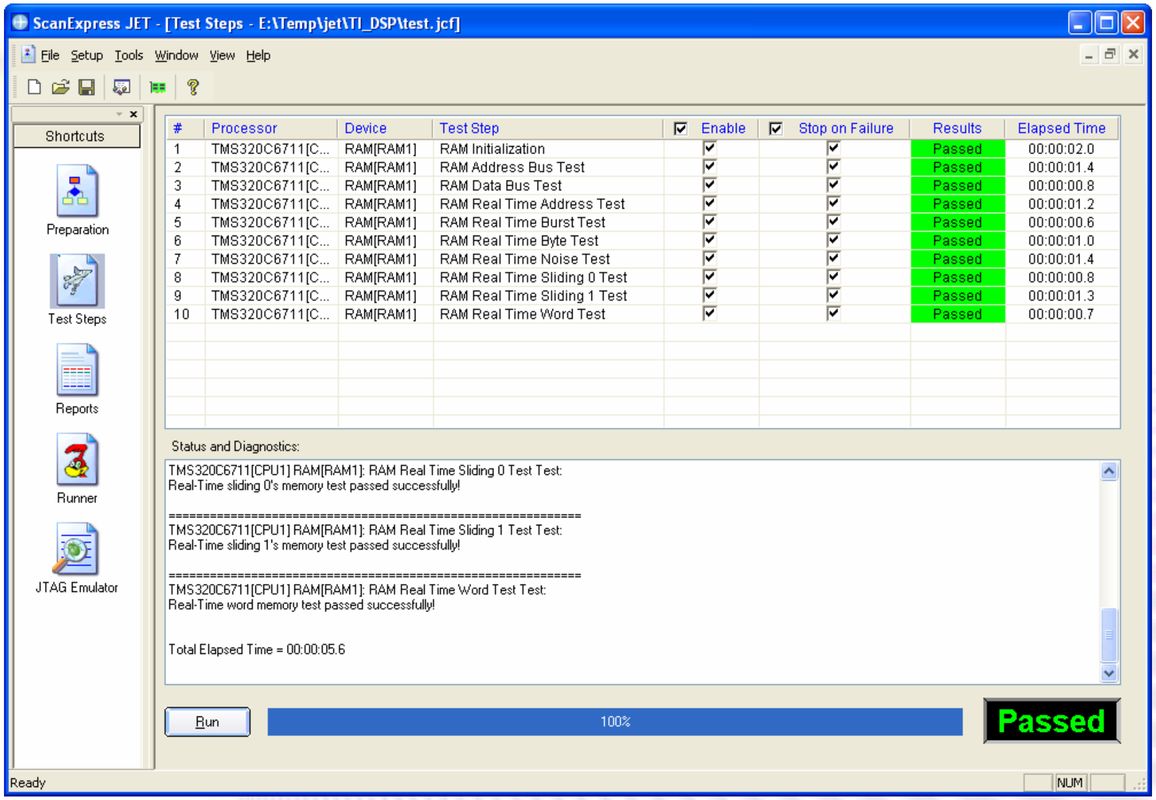
JET Integration

- All Blackhawk XDS560 controllers.
- Tests are designed for prototype development, where fault isolation and identification are important.
- Tests are also reusable in production where test throughput and programming times are important.


JTAG
RS-232
Loop back
RS-232
TI DSP
SMbus
EEProm
JTAG
FPGAs
System Bus
Flash
SRAM
DDR SDRAM
D/A
A/D
Loop back

ScanExpress JET GUI

- Stand-alone development-based software is available to create and execute tests on-the-fly.
- Production-based software is available to execute all the JTAG tests and JET tests in a single test plan.
- All tests can also be invoked from third-party test executives using ScanPlus Runner DLL.



#	Processor	Device	Test Step	☑ Enable	☑ Stop on Failure	Results	Elapsed Time
1	TMS320C6711[C...	RAM[RAM1]	RAM Initialization	☑	☑	Passed	00:00:02.0
2	TMS320C6711[C...	RAM[RAM1]	RAM Address Bus Test	☑	☑	Passed	00:00:01.4
3	TMS320C6711[C...	RAM[RAM1]	RAM Data Bus Test	☑	☑	Passed	00:00:00.8
4	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Address Test	☑	☑	Passed	00:00:01.2
5	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Burst Test	☑	☑	Passed	00:00:00.6
6	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Byte Test	☑	☑	Passed	00:00:01.0
7	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Noise Test	☑	☑	Passed	00:00:01.4
8	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Sliding 0 Test	☑	☑	Passed	00:00:00.8
9	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Sliding 1 Test	☑	☑	Passed	00:00:01.3
10	TMS320C6711[C...	RAM[RAM1]	RAM Real Time Word Test	☑	☑	Passed	00:00:00.7

```
TMS320C6711[CPU1] RAM[RAM1]: RAM Real Time Sliding 0 Test Test:
Real-Time sliding 0's memory test passed successfully!

============================================================
TMS320C6711[CPU1] RAM[RAM1]: RAM Real Time Sliding 1 Test Test:
Real-Time sliding 1's memory test passed successfully!

============================================================
TMS320C6711[CPU1] RAM[RAM1]: RAM Real Time Word Test Test:
Real-Time word memory test passed successfully!


Total Elapsed Time = 00:00:05.6
```

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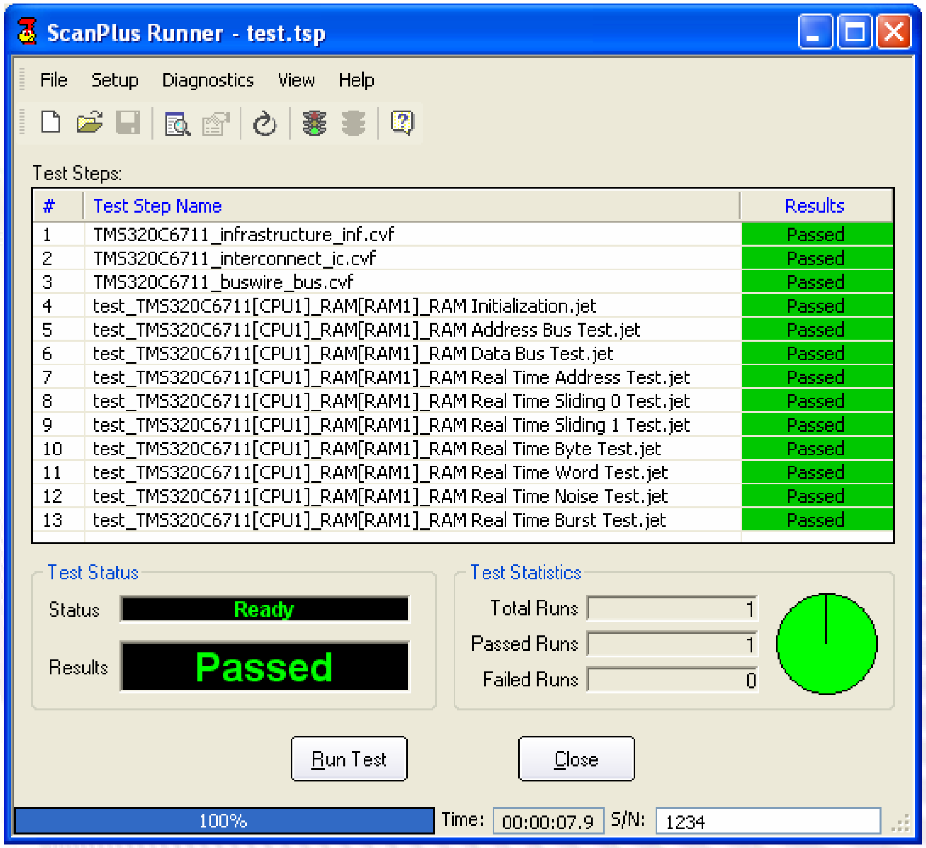
ScanExpress JET Test Steps

- Boundary-scan interconnect tests
  - CPU, system bus, SRAM, SDRAM, FPGAs
  - Flash interconnects are tested for shorts only to minimize test time.
- JTAG emulation tests
  - SDRAM and SRAM are tested again at-speed.
  - Flash is programmed and verified using the Target Assisted Flash module.
  - A/D and D/A are tested by looping the output of the D/A to the input of A/D.
  - UARTs and their RS-232 drivers and receivers are tested by looping TXD and RXD lines.
  - Optionally reset and run the board from its own boot code.



Test Steps:

#	Test Step Name	Results
1	TMS320C6711_infrastructure_inf.cvf	Passed
2	TMS320C6711_interconnect_ic.cvf	Passed
3	TMS320C6711_buswire_bus.cvf	Passed
4	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Initialization.jet	Passed
5	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Address Bus Test.jet	Passed
6	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Data Bus Test.jet	Passed
7	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Address Test.jet	Passed
8	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Sliding 0 Test.jet	Passed
9	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Sliding 1 Test.jet	Passed
10	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Byte Test.jet	Passed
11	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Word Test.jet	Passed
12	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Noise Test.jet	Passed
13	test_TMS320C6711[CPU1]_RAM[RAM1]_RAM Real Time Burst Test.jet	Passed

Test Status

Status: Ready

Results: Passed

Test Statistics

Total Runs: 1

Passed Runs: 1

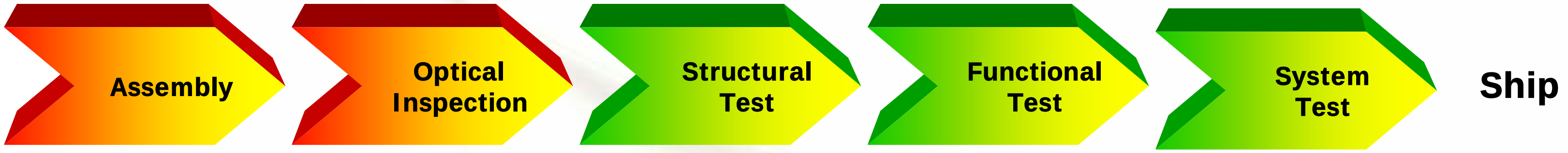
Failed Runs: 0

100%

Time: 00:00:07.9

S/N: 1234

Benefits of JET



Assembly

Optical Inspection

Structural Test

Functional Test

System Test

Ship

- Single test station and GUI for structural and functional testing and in-system programming.
- Higher fault detection and more accurate fault diagnostics.
- Tests components functionality in real-time.
- Reduced use of ICTs and fixture costs.
- Lower cost and faster time to market.

TI-Supported Processors

- TMS320C6711
- TMS320C6713
- TMS320C6416
- TMX320C6455
- TMX320DM642
- OMAP5912
- Others, as required

Other Considerations

- Ideally use boundary-scan where possible as test vectors and diagnostics can be automatically generated and diagnostics are on a net and pin level.
- Increase test coverage using JET for testing non-boundary scan parts. Test generation is semi-automatic, and diagnostic resolution will be on a functional level.
- Analog testing of CPU-accessible parts is possible using JET.
- JET can extend functional test coverage to boundary-scan parts.

Other Considerations

- Memory testing is possible with either method, but boundary-scan can only test interconnects efficiently.
- JTAG emulation test is at full board speed.
- JET can program flash memories at the theoretical speed.
- JET can verify loaded software revisions and check that the board boots under its own software.
- When executed from CPU cache memory, JET can determine why boards don’t boot.

Test Markets and Applications

- Design and Development
  - Design engineers who want to start debugging their prototype before test firmware and test fixtures are available
  - Firmware/software engineers who want to save time and resources to create diagnostic tests automatically
  - Field application engineers who want to verify if customer boards are bad
- Production
  - Test engineers who want to increase their boards’ test coverage and extend their boundary-scan tests with functional tests
  - Repair engineers who want to find board failures quickly and at the lowest cost to the customer

Corelis Advantages

- ScanExpress and JET technologies were developed by a single vendor (Corelis) in the USA.
- Pre-sale, sales and customer support are coming from a single vendor.
- Products are integrated in the test-generation and execution levels and share the same GUI environments.
- Initial functional tests execute from the CPU cache memory when possible. This allows finding failures in boards that do not boot.
- Extensive in-house deep technical knowledge in boundary-scan and JTAG CPU emulation.
- Same parent as Blackhawk, strong third-party relationship with TI.
- Existing Blackhawk customers can reuse emulation hardware in both boundary-scan and JET applications.

JET Demonstration

ScanExpress JET

Demonstration

For a personal demonstration of ScanExpress JET, please see us at the Blackhawk booth #415.

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