TI Developer Conference
March 7-9, 2007 • Dallas, TX

Minds in Motion

Data Converter Basics

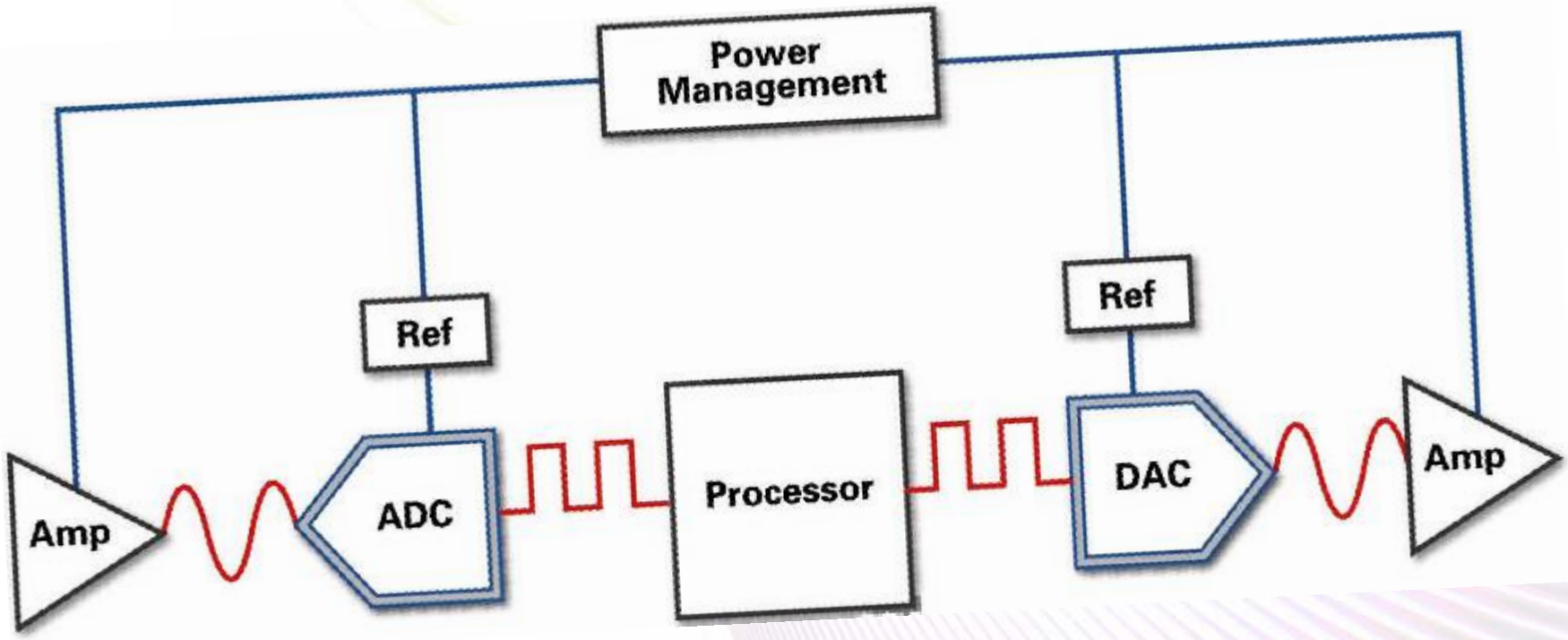
How to Use and Test Data-Acquisition Products

Tom Hendrick,
Texas Instruments, Inc.

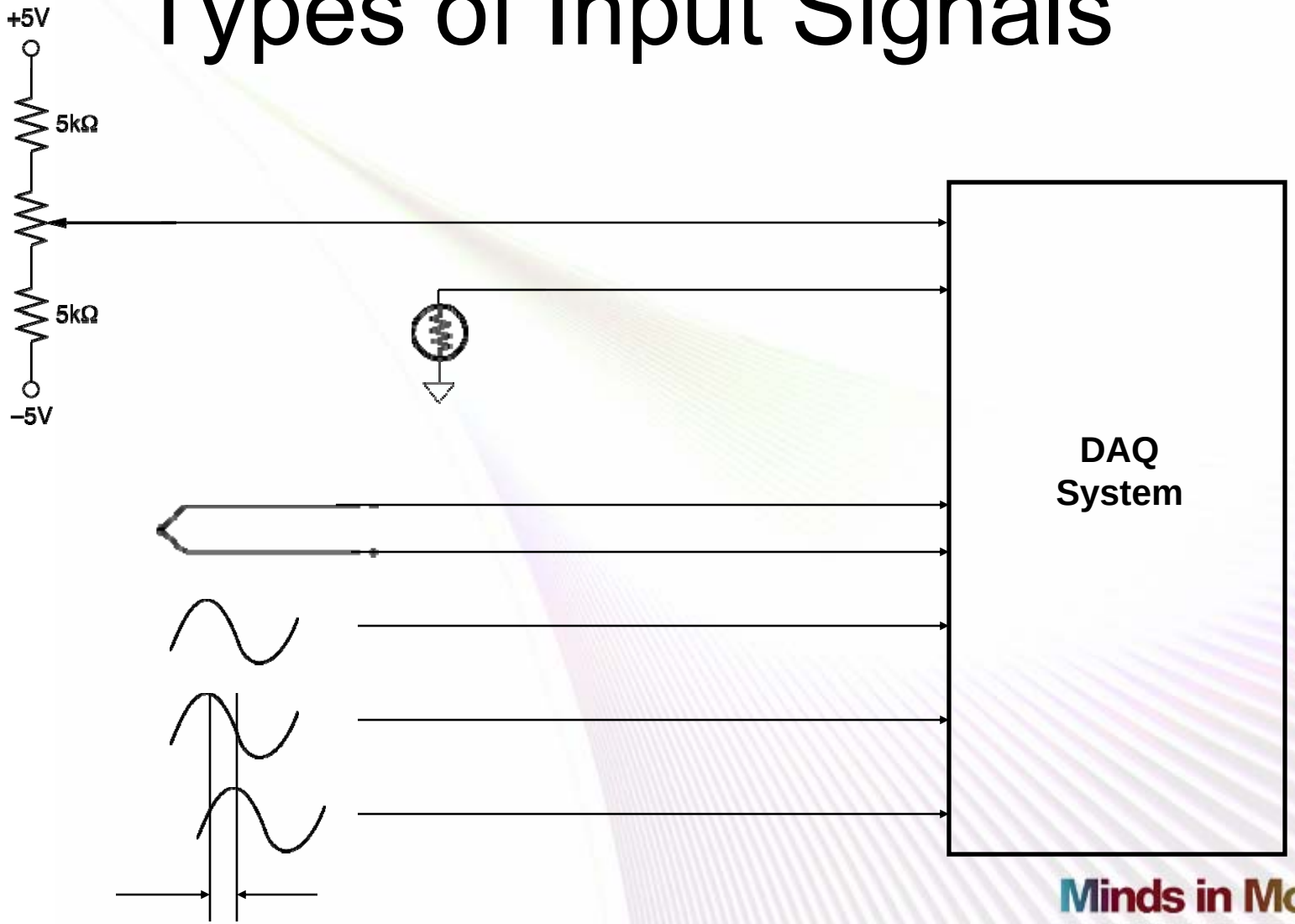
Workshop Agenda

- Data Converter Fundamentals
  - Key concerns when choosing a data converter
  - Data converter and analog design tools
- Design Considerations
  - Input drive considerations
  - Cost and performance tradeoffs
  - PCB layout
- Putting the Pieces Together…
  - Software tool demos
  - Hardware tool demos

Data Acquisition Components



Types of Input Signals



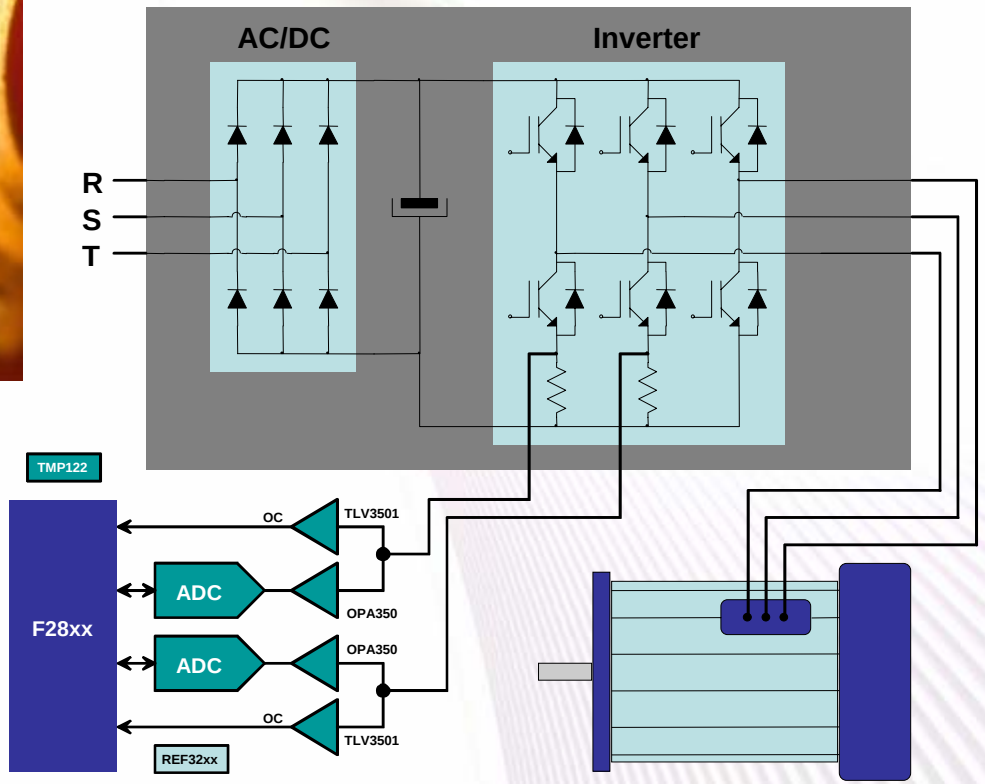
Simultaneous Sampling

- Why do simultaneous sampling?
- Applications for simultaneous sampling converters

Why Sample Simultaneously?

- Preservation of Phase Relationship
  - Speed/position sensors
  - Vibration analysis
- Relative Signals for Various Equations
  - Power
  - Torque, etc.

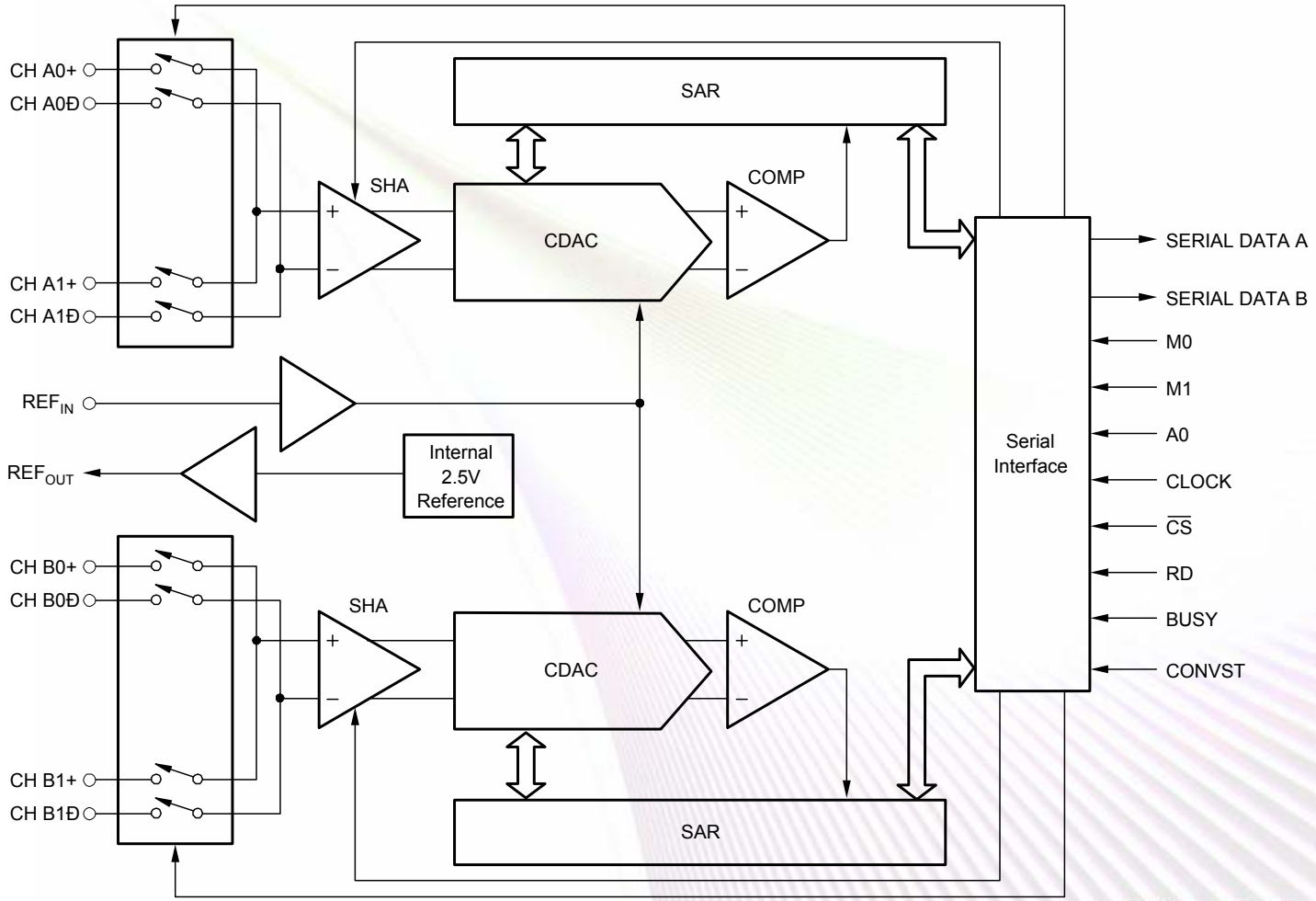
Simultaneous Sampling Applications



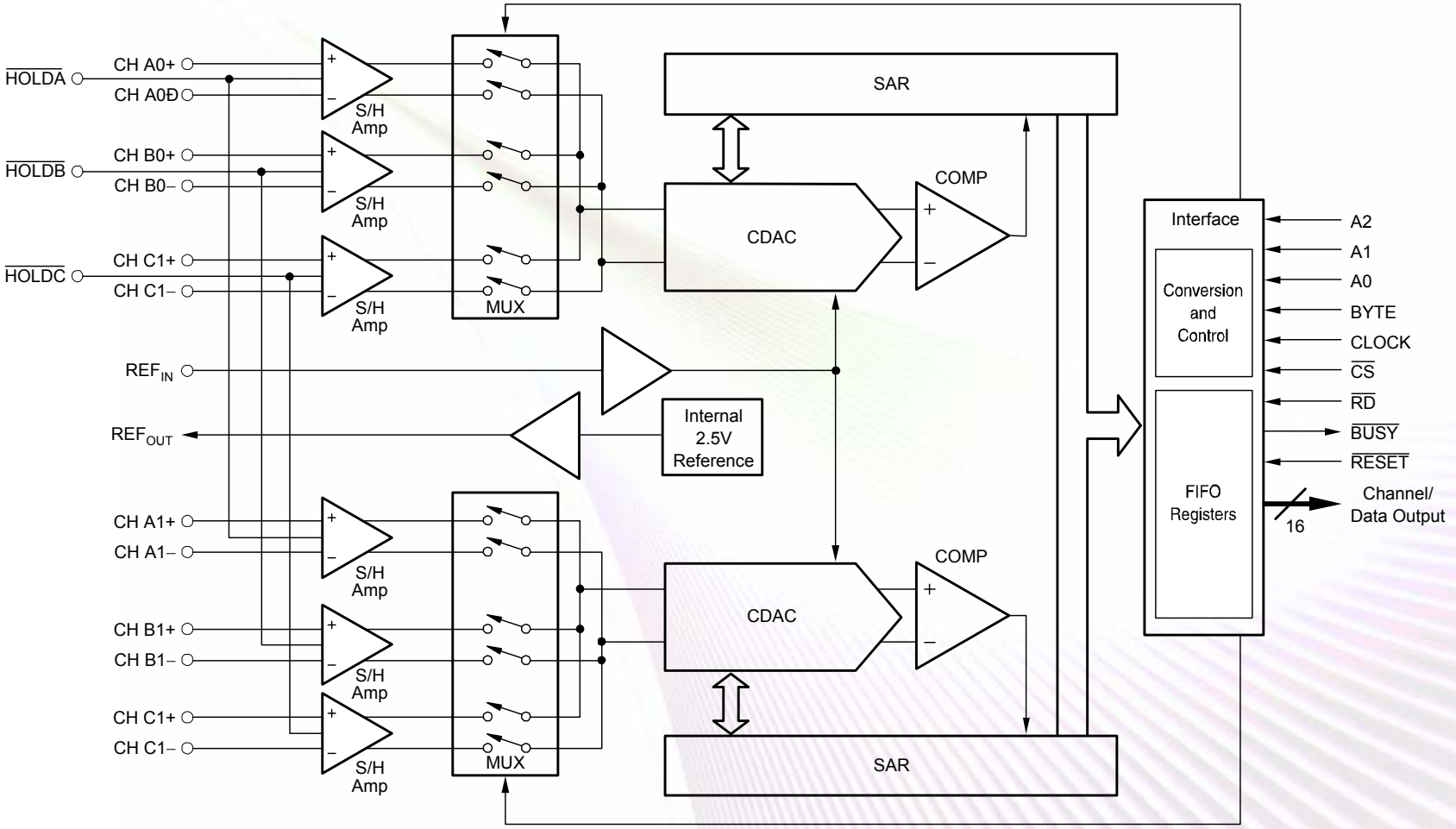
Simultaneous Sampling ADCs

- 2x2 SAR: 2 ADCs with 2 S/H
  - ADS7861, ADS8361
  - ADS7862
- 3x2 SAR: 2 ADCs with 3 S/H
  - ADS7864
- 1x6 SAR: 6 ADCs with 1 S/H
  - ADS8364, ADS8365
- Pipeline
  - THS12xx

2x2 SAR


CH A0+
CH A0Đ
CH A1+
CH A1Đ
SHA
SAR
CDAC
COMP
REF$_{IN}$
REF$_{OUT}$
Internal
2.5V
Reference
CH B0+
CH B0Đ
CH B1+
CH B1Đ
SHA
CDAC
COMP
SAR
Serial
Interface
SERIAL DATA A
SERIAL DATA B
M0
M1
A0
CLOCK
$\overline{CS}$
RD
BUSY
CONVST

3x2 SAR



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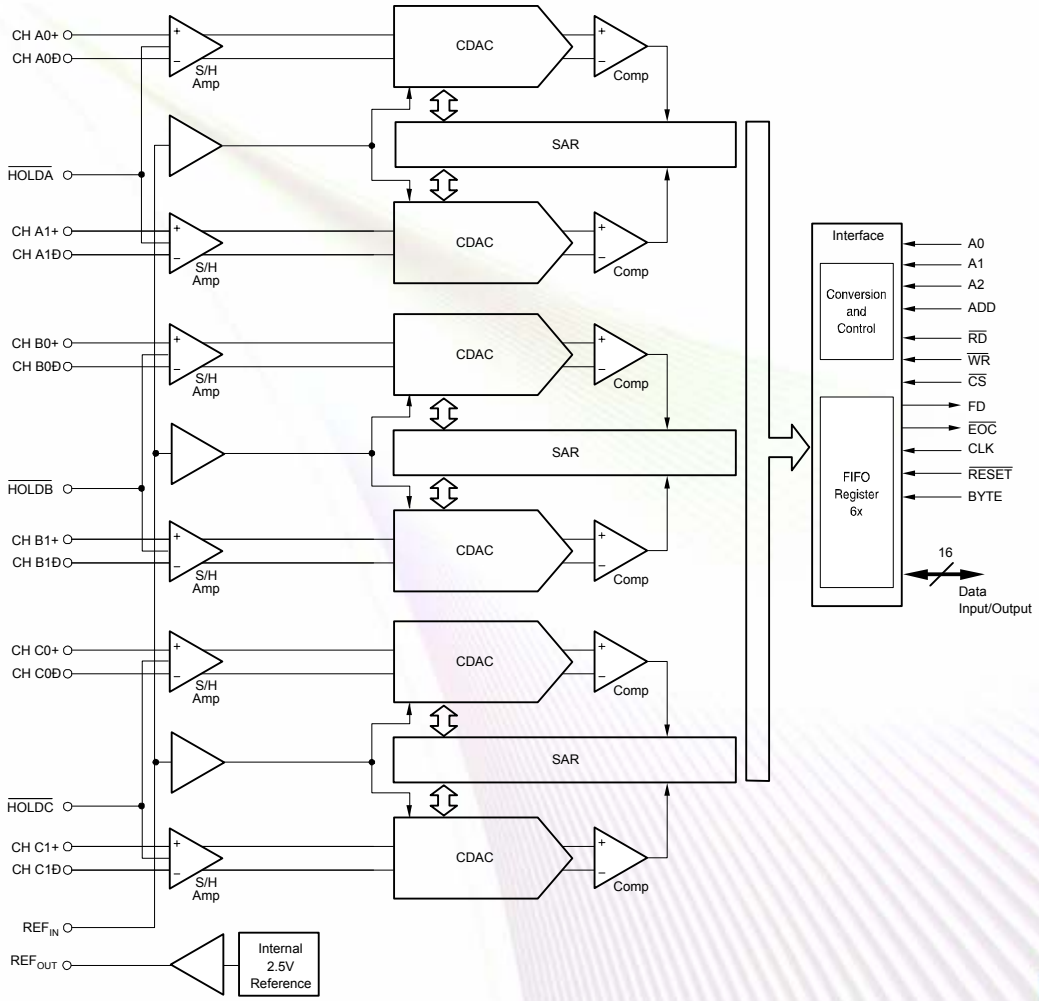
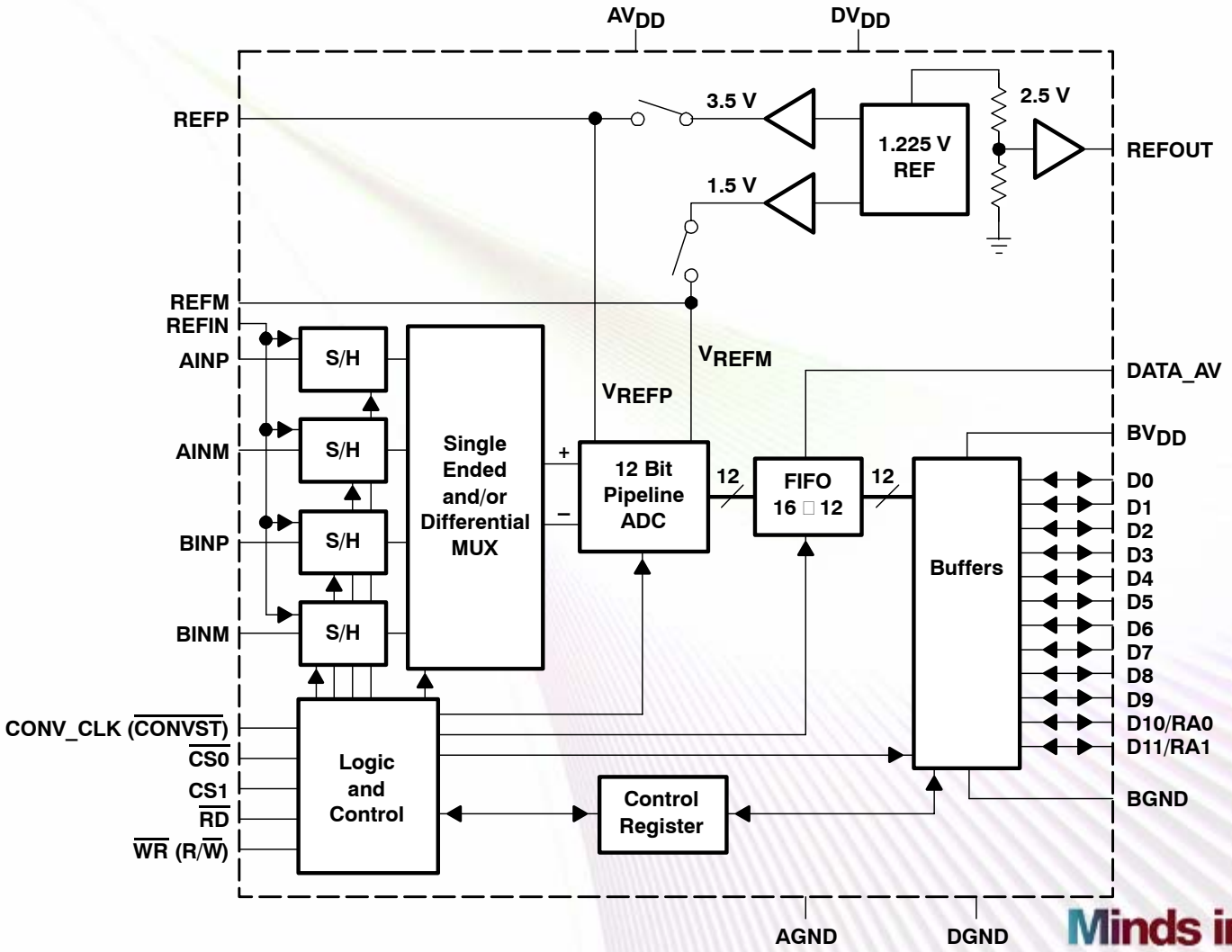
1x6 SAR


CH A0+
CH A0–
S/H Amp
CDAC
Comp
SAR
HOLDA
CH A1+
CH A1–
CH B0+
CH B0–
HOLDB
CH B1+
CH B1–
CH C0+
CH C0–
HOLDC
CH C1+
CH C1–
REF_IN
REF_OUT
Internal 2.5V Reference
Interface
Conversion and Control
FIFO Register 6x
A0
A1
A2
ADD
RD
WR
CS
FD
EOC
CLK
RESET
BYTE
16
Data Input/Output

4X1 Pipeline

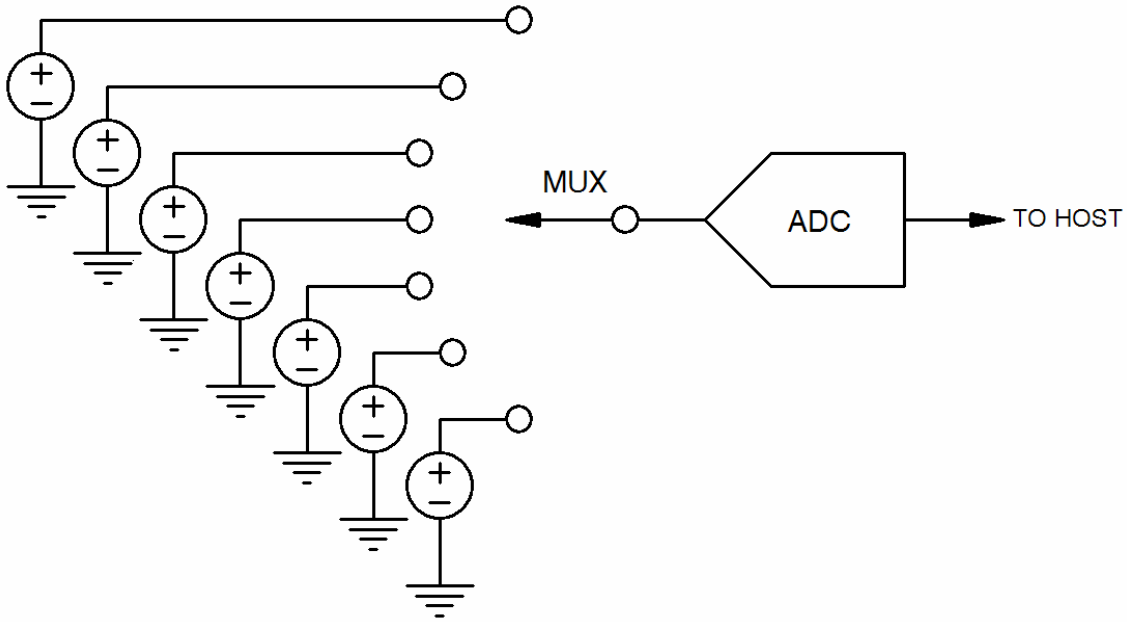


Multiplexed Sampling

- Are there advantages?
- What about using multiple ADCs?
- Applications for multiplexed inputs

Multiplexed Advantages

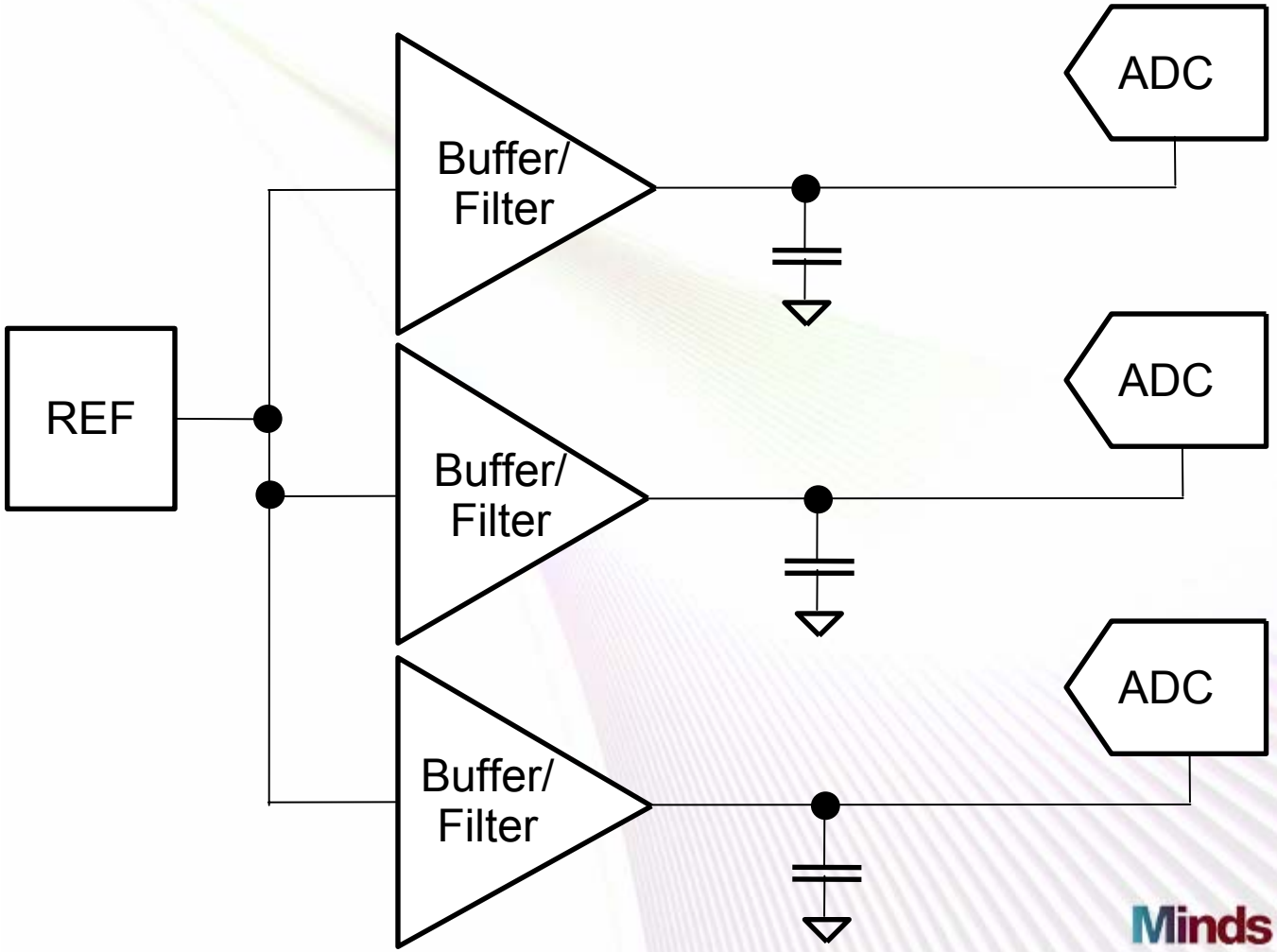
- Fewer converters needed per channel – often only one needed.
- Often lower power
- Often lower cost



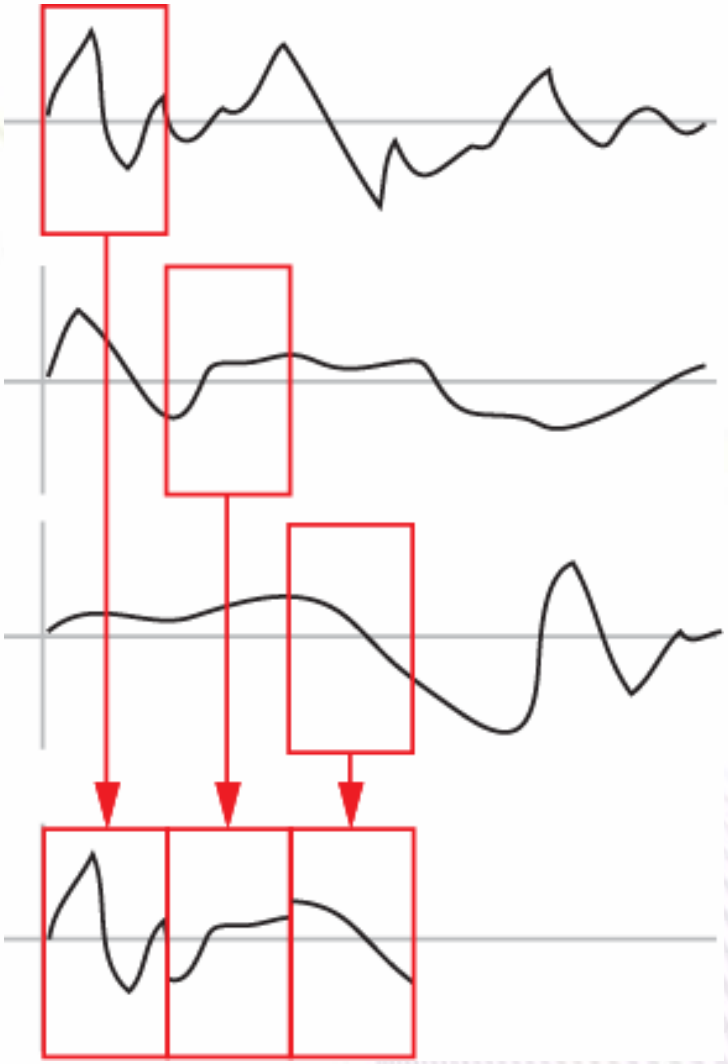
Multiplexed vs. Multi-Chip

- Reference distribution issues
- Input signal issues: One channel has very different input needs from others.
  - Use a single channel device, MUX the others.
- Multiplexing implies time delays between channels – system issues? Simultaneous sampling better?
- Can the processor easily support multiple ADCs?

Reference Distribution



Multiplexing Basics



Multiplexed Applications

- Temperature monitoring
- Multi-point weigh scales
- Pressure monitoring
- Control surface transducer readings (e.g., audio mixer control surface)
- General purpose low-speed sensor data acquisition

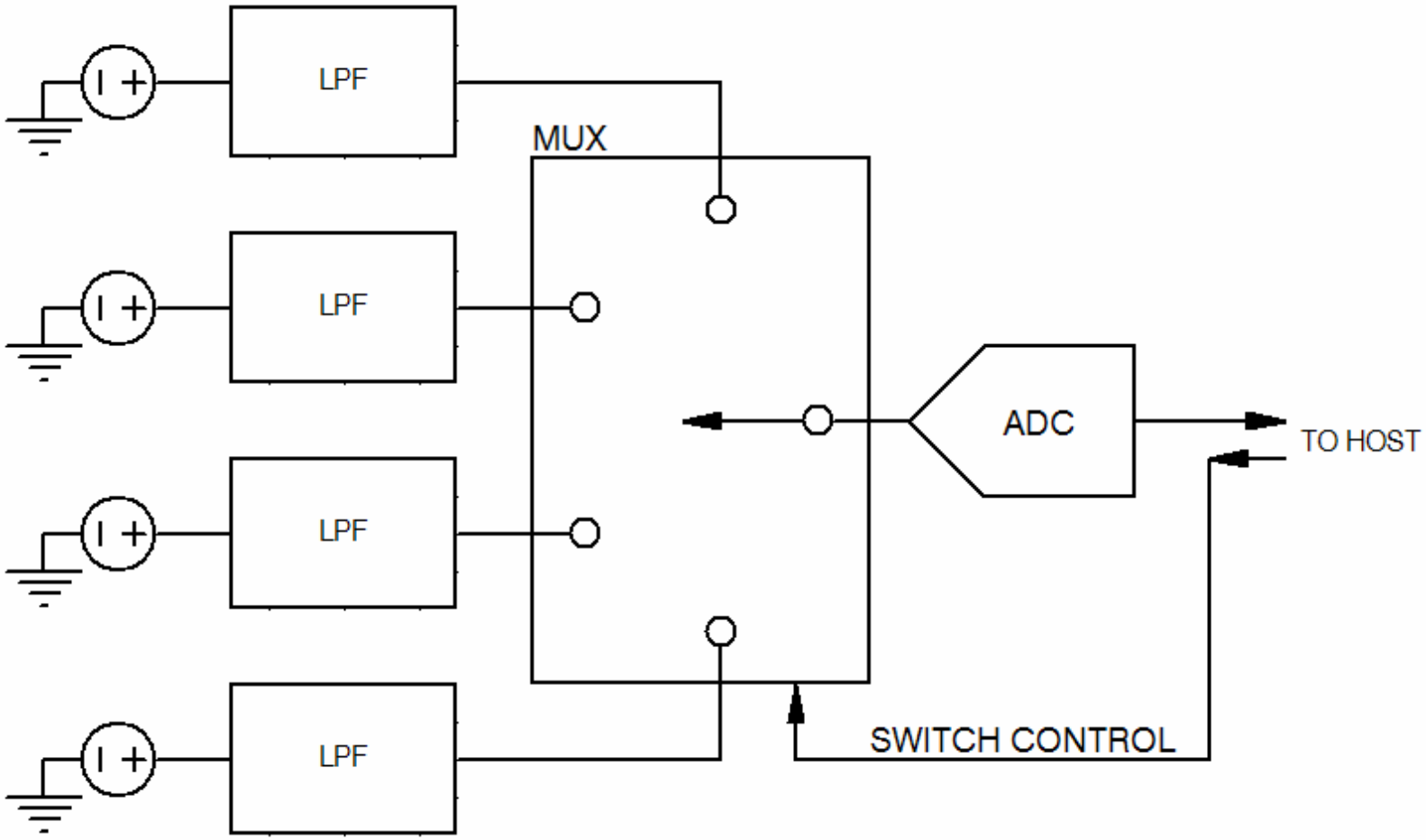
Multiplexing Application Tips

- If converter is available with internal MUX, use it!
  - Available on both SAR and delta-sigma.
- Internal MUXes are tailored to match the ADC performance.
- Don't have to guess about switching and settling time.

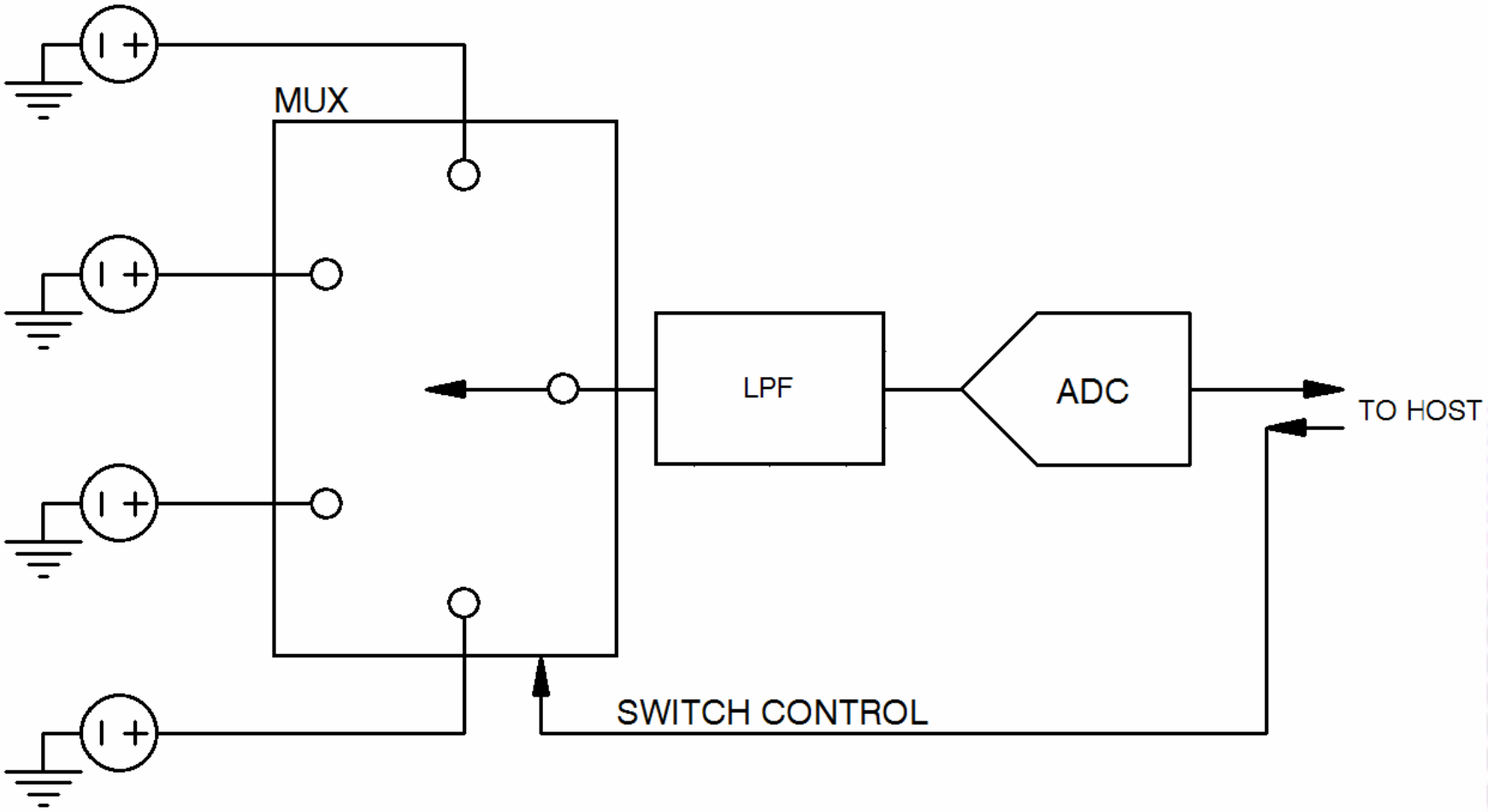
Multiplexing SARs vs. ΔΣs

- SAR-based systems often require low-pass filters on *each channel,* increasing power and cost.
- ΔΣ systems generally offer greater accuracy and lower noise floor.
- SAR designs with a post-multiplexer filter result in a system with settling-time issues almost identical to the ΔΣ design, but with higher noise.

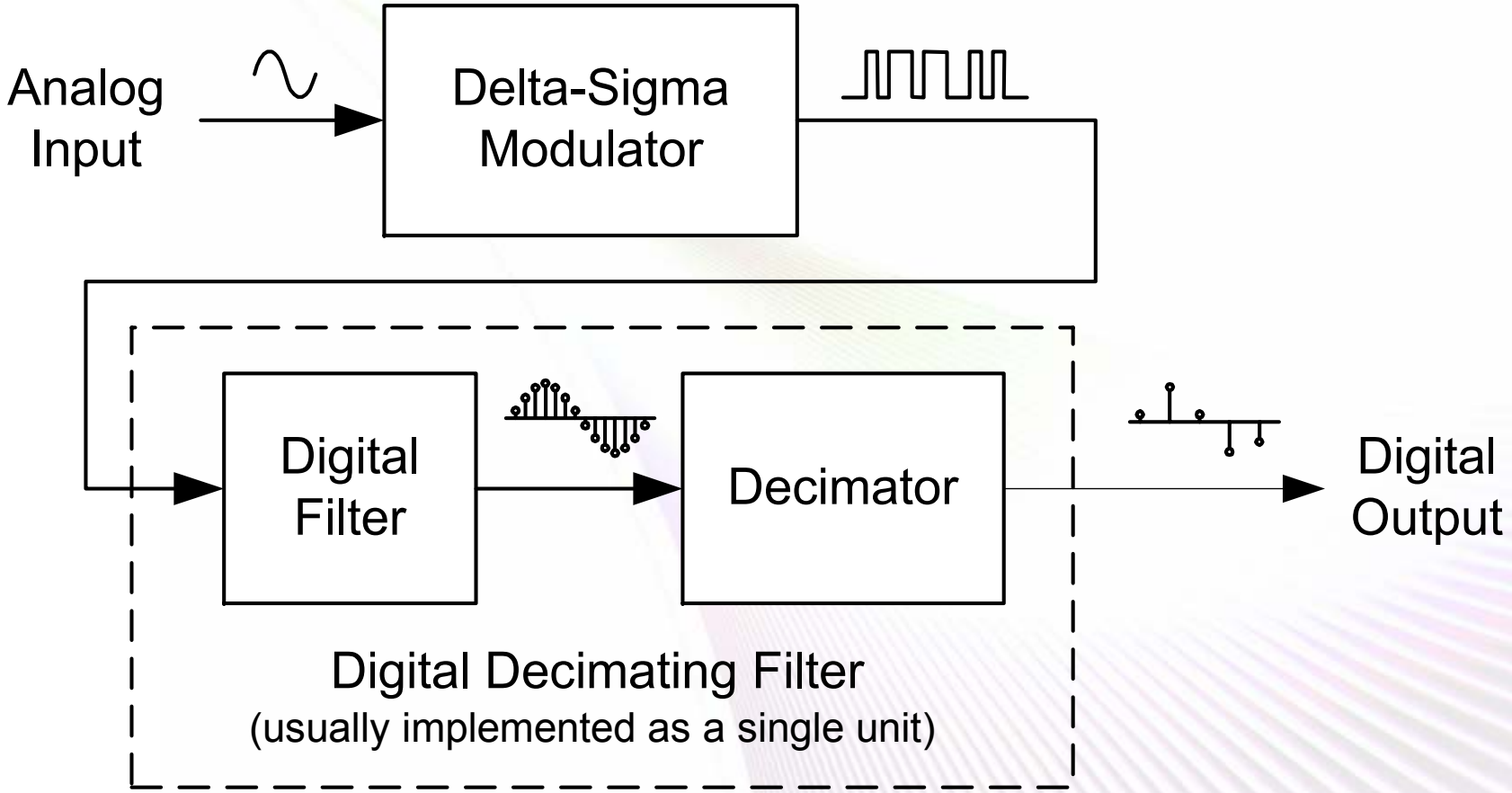
Multiplexing with SARs



Multiplexing with Delta-Sigmas

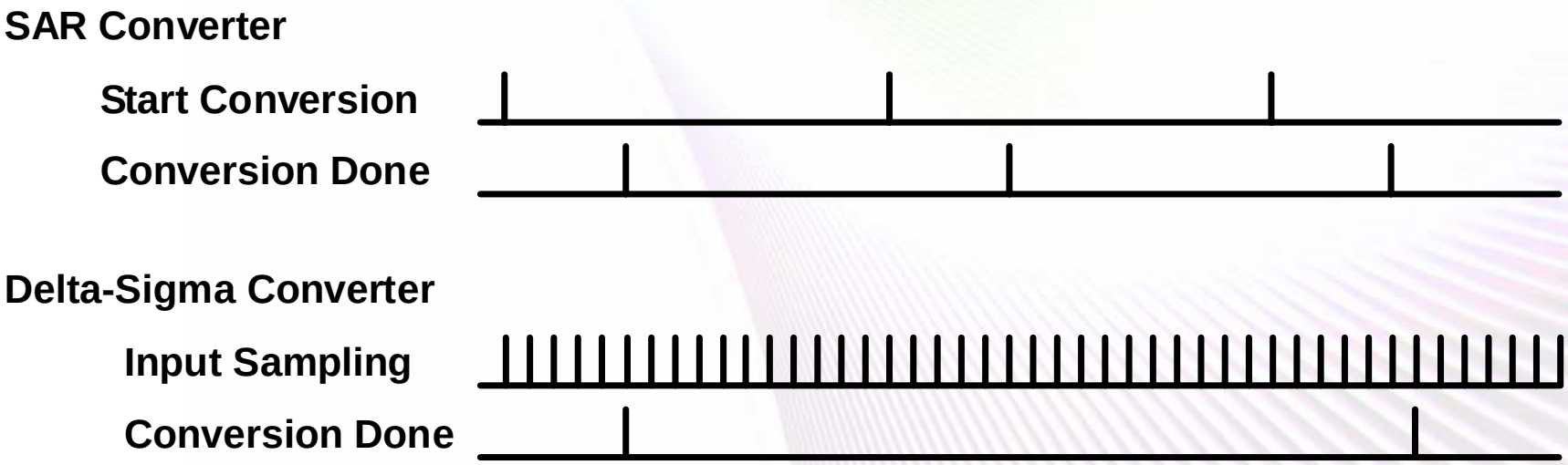


The Delta-Sigma Architecture

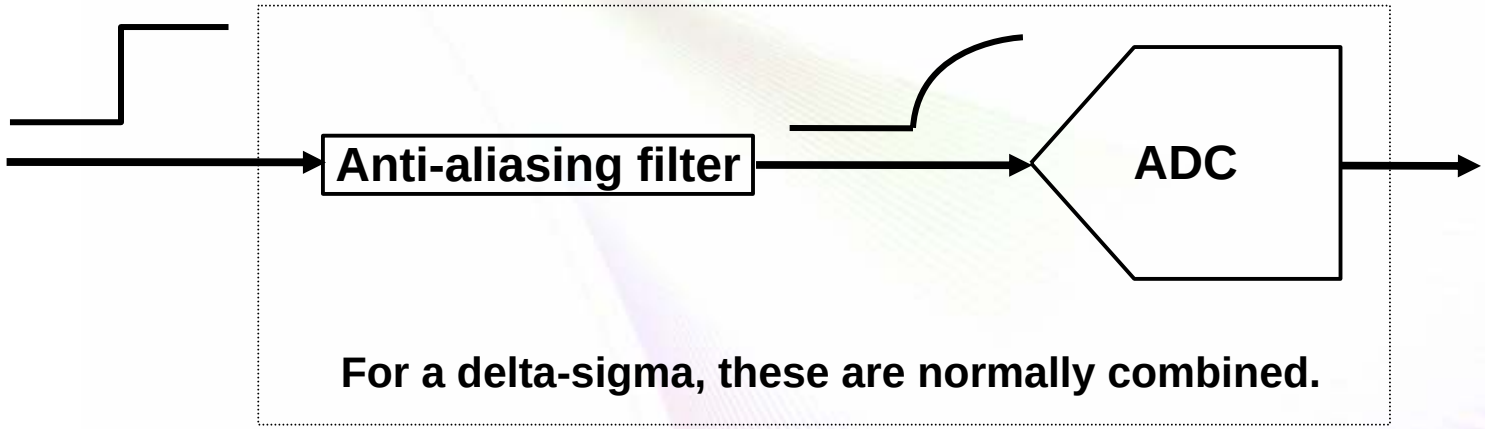


SAR vs. Delta-Sigma Conversions

- SAR conversions have Start Conversion Signal.
- Delta-Sigma is always sampling/converting.

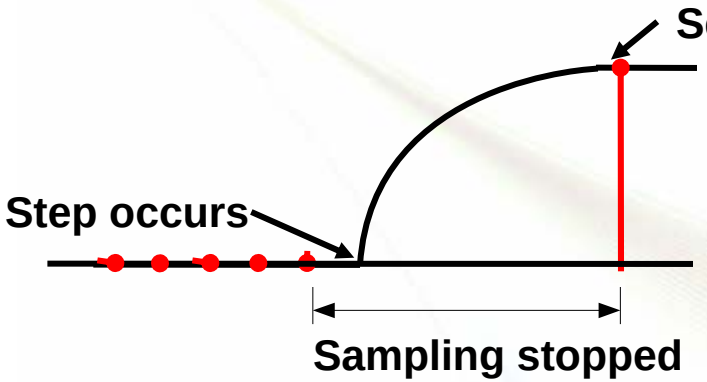


Settling Time

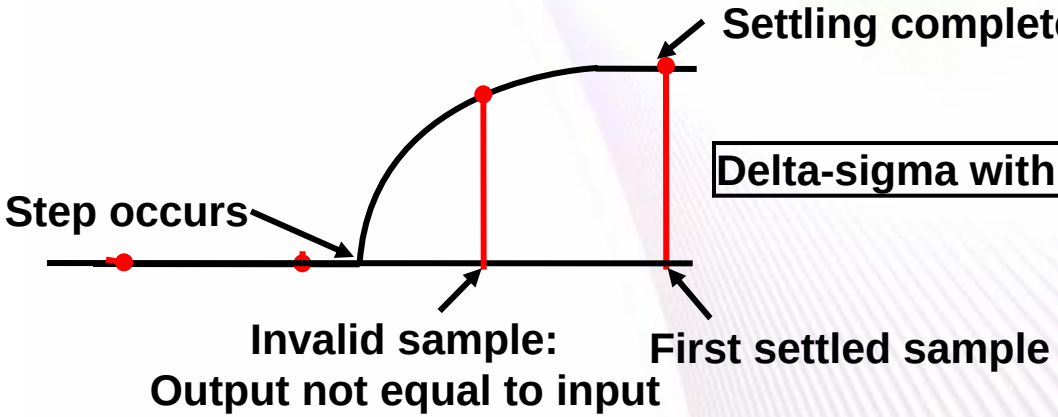


For a delta-sigma, these are normally combined.

Settling Time: SAR vs. ΔΣ

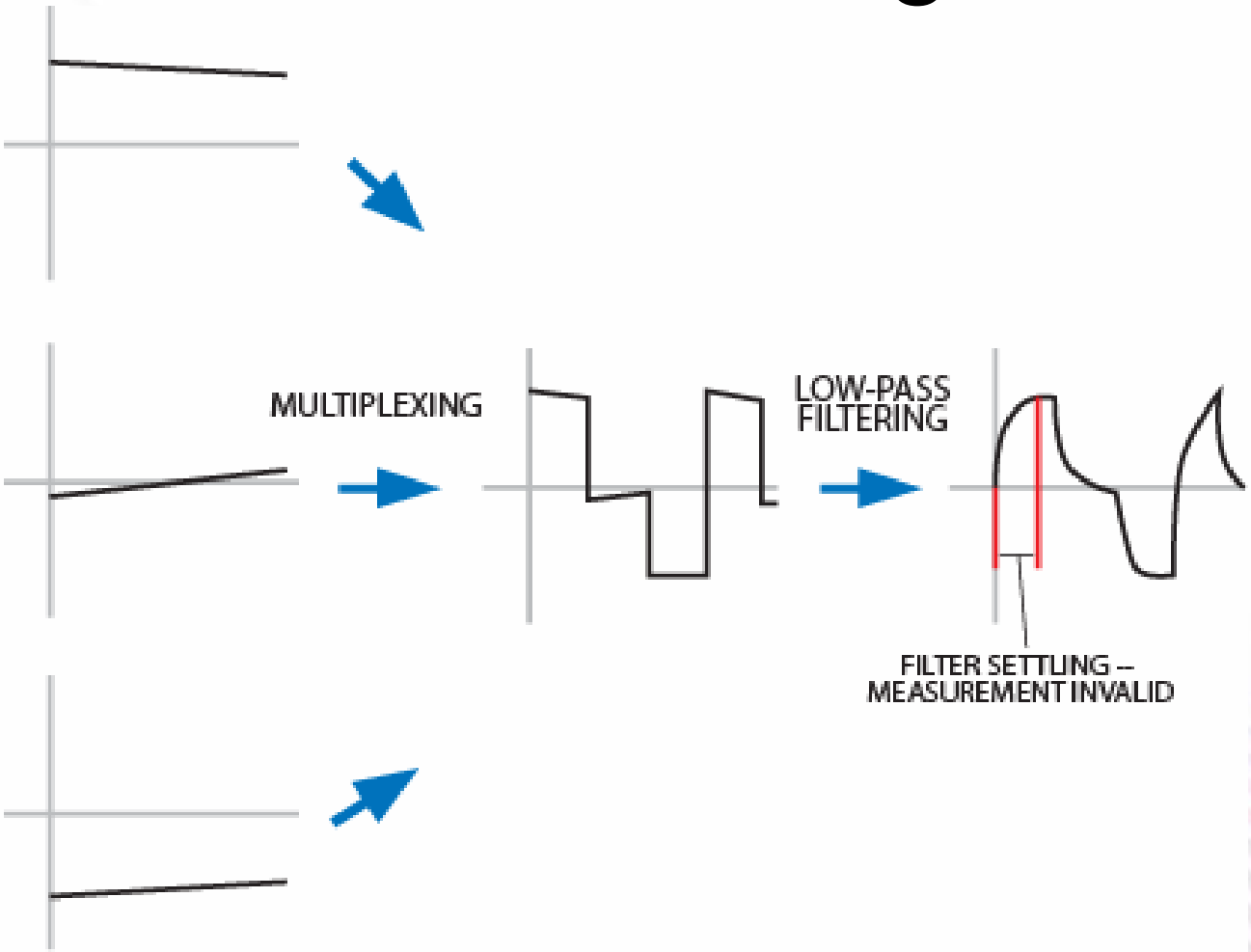


SARs can convert any time, so can be made to resume conversion at just the right moment.

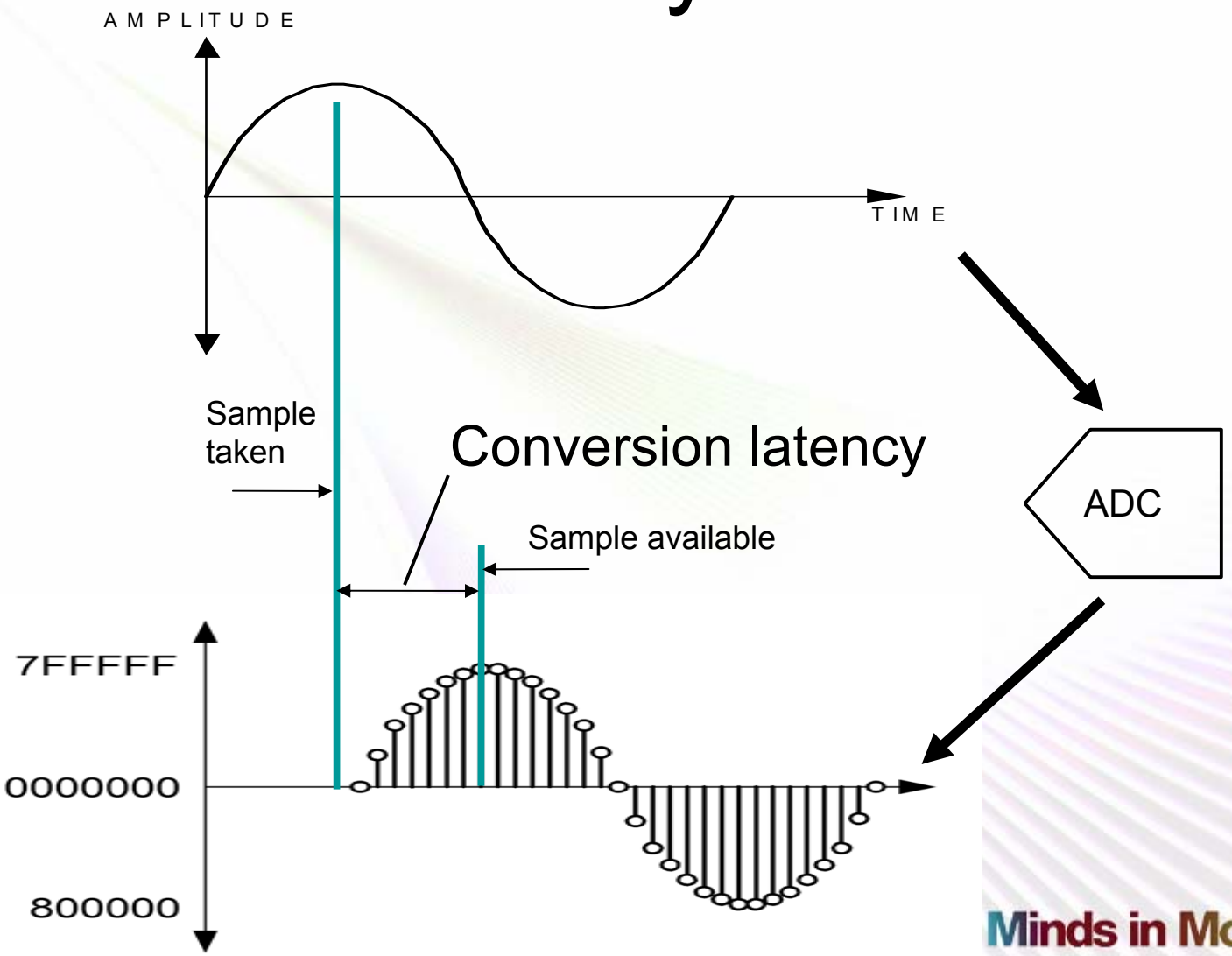


Delta-sigma with 2-cycle settling time.

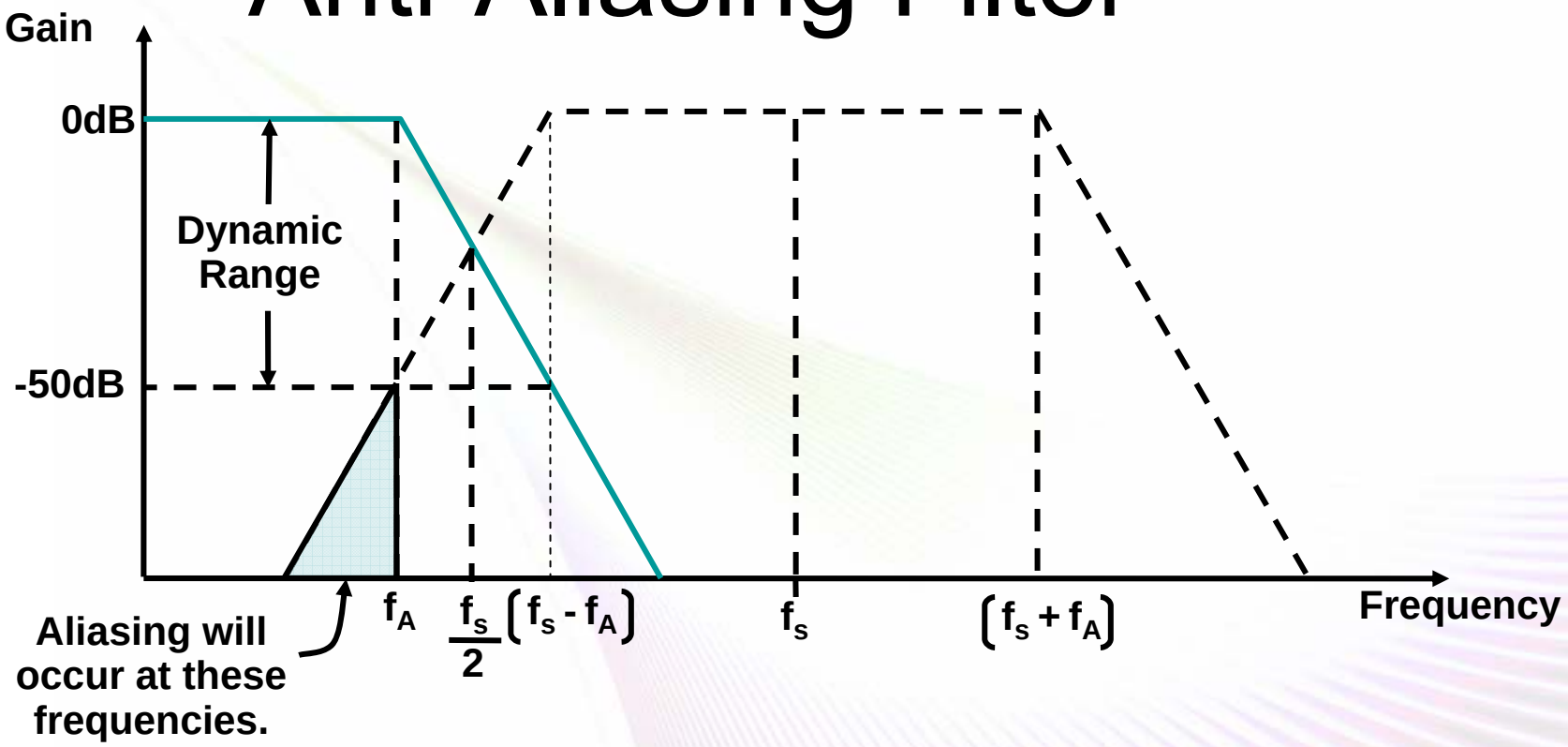
Effects of Settling Time



Latency

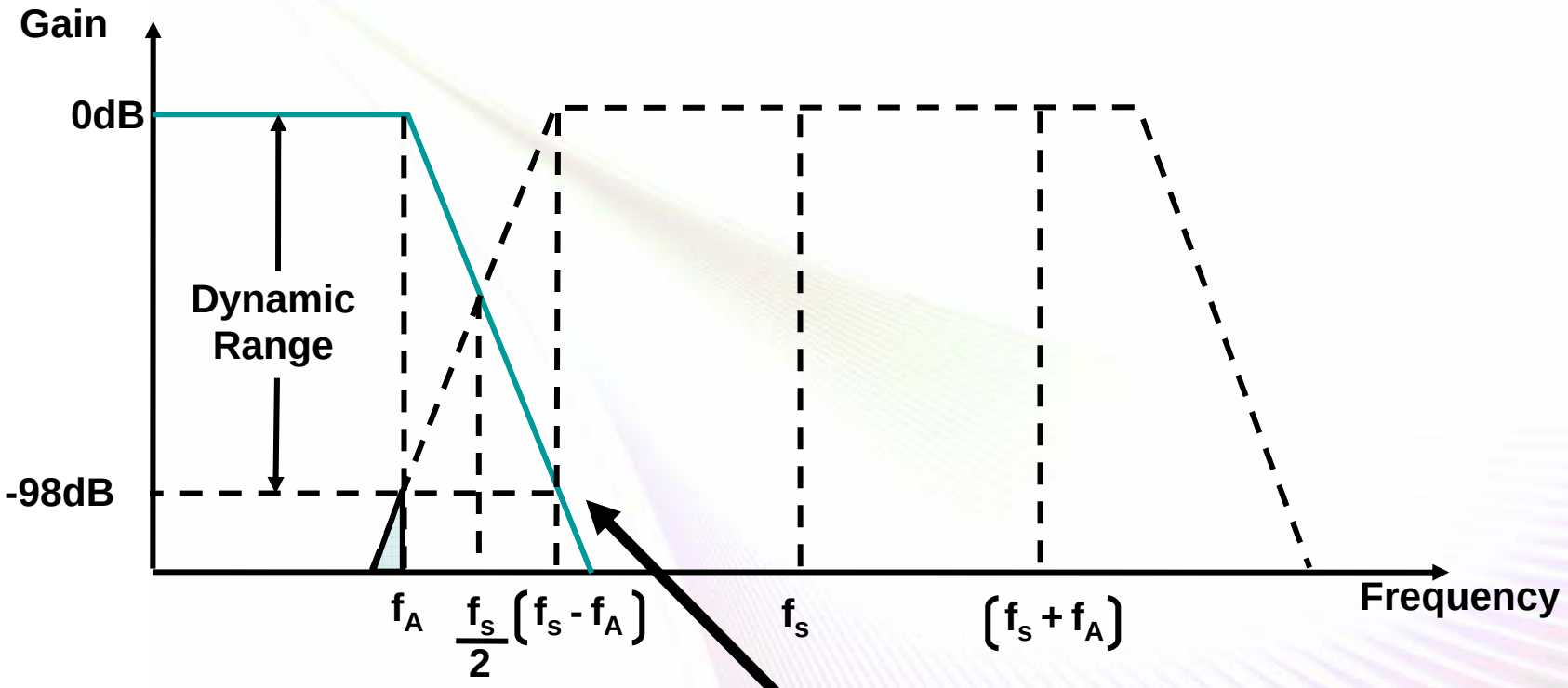

AMPLITUDE
TIME
Sample taken
Conversion latency
Sample available
ADC
7FFFFF
0000000
800000

Anti-Aliasing Filter



50-dB, alias-free range is insufficient for 16 bits.

Improved Anti-Aliasing Filter



An 8-pole filter increases dynamic range to 98 dB!

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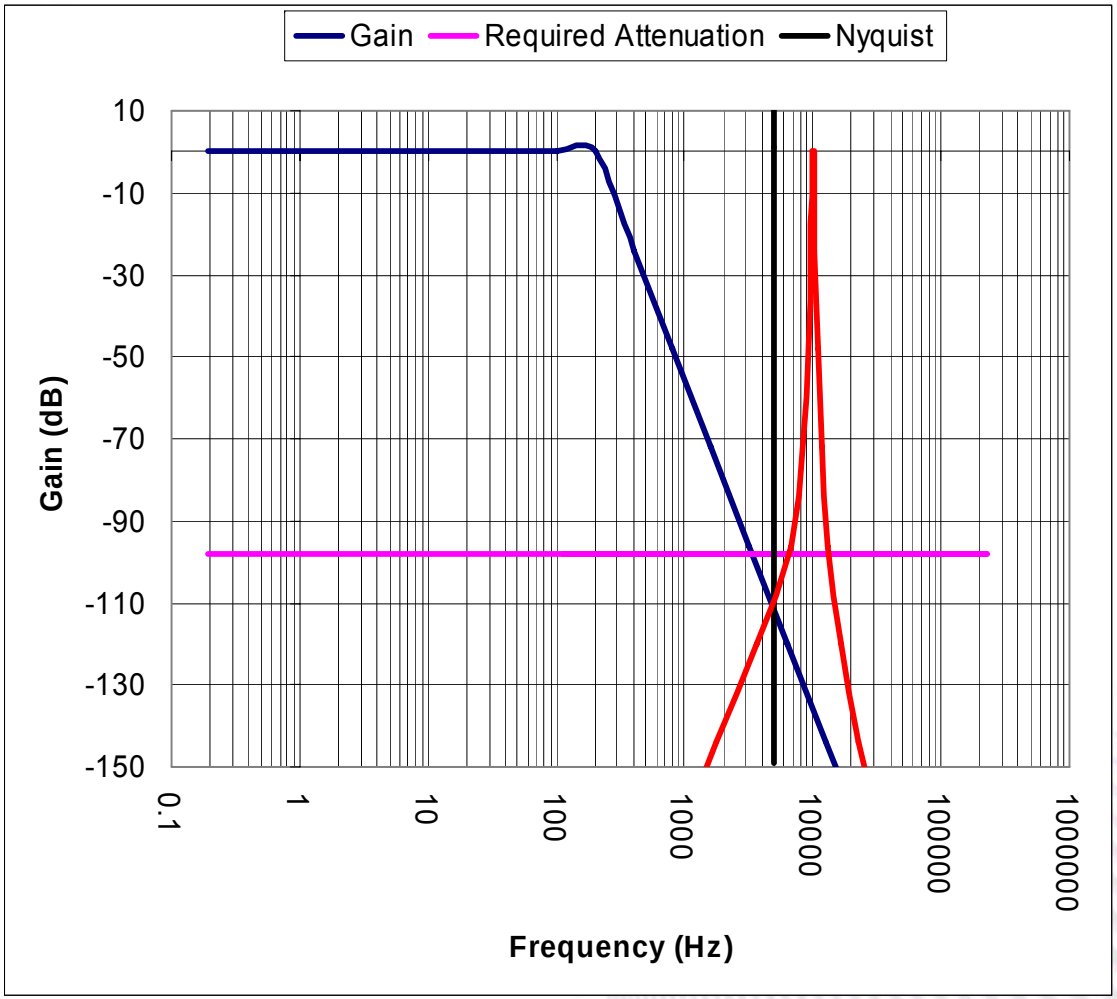
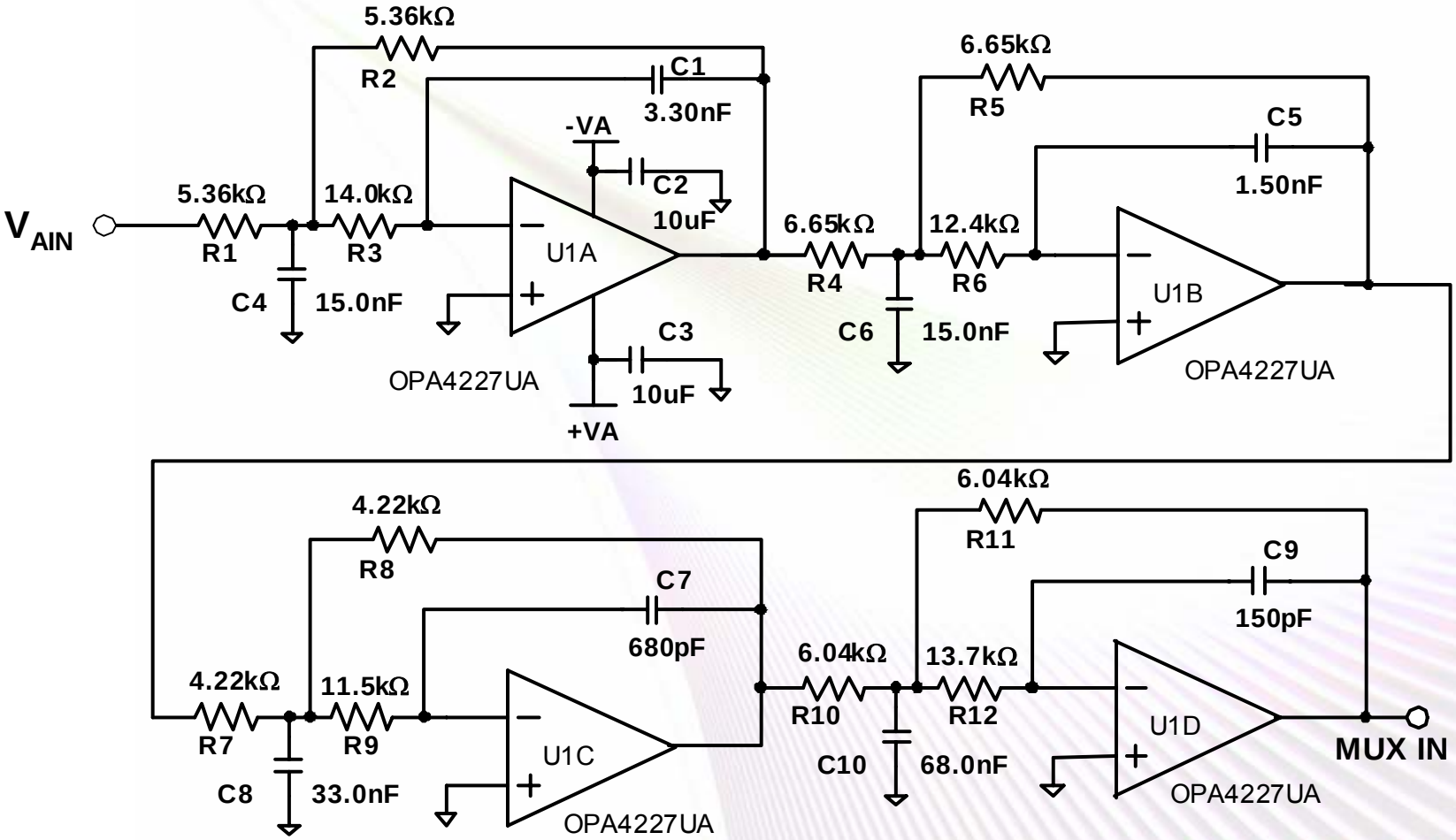
Anti-Aliasing Filter Calculator



8th Order Filter Example



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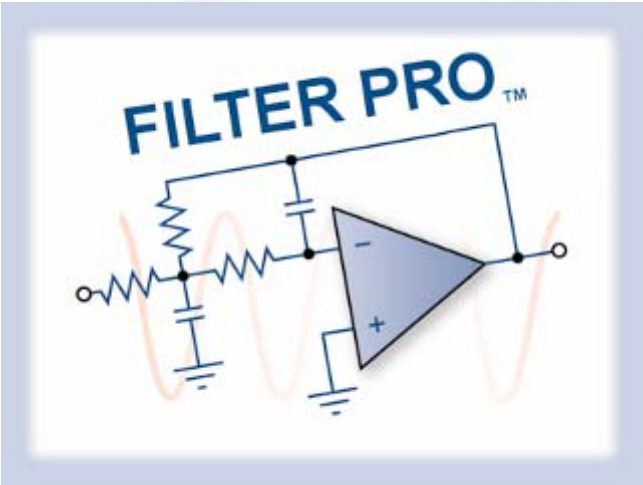
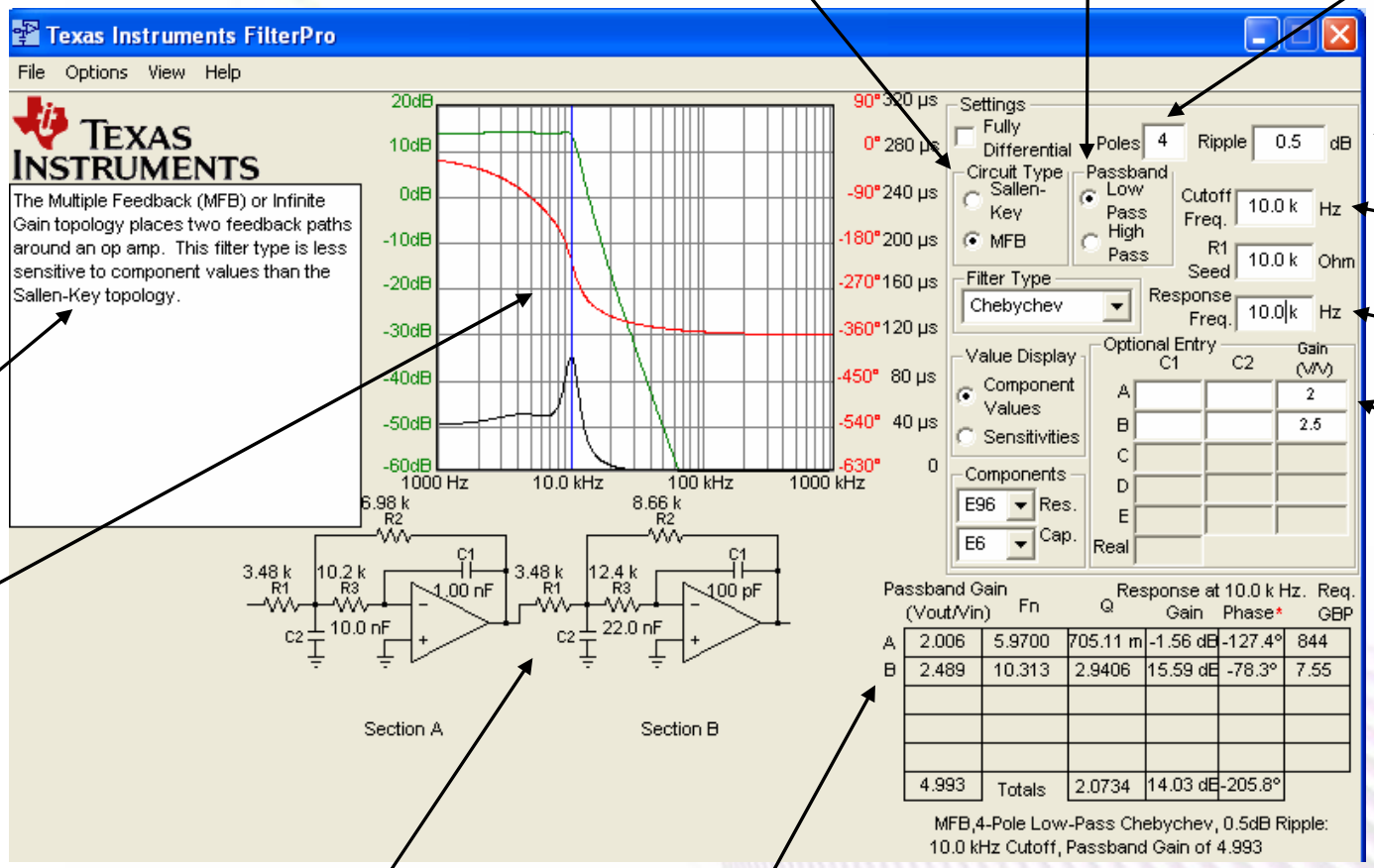
Filter Pro™

- A filter synthesis tool for designing multi-section, low-pass and high-pass active filters.
- Supports 2nd to 10th order, multiple-feedback (MFB) and Sallen-Key filter topologies.



The Filter Pro Worksheet



Filter topology

Pass band

No. of poles

Ripple (Chebychev)

Cutoff freq.

Response freq.

Gain

Topology info

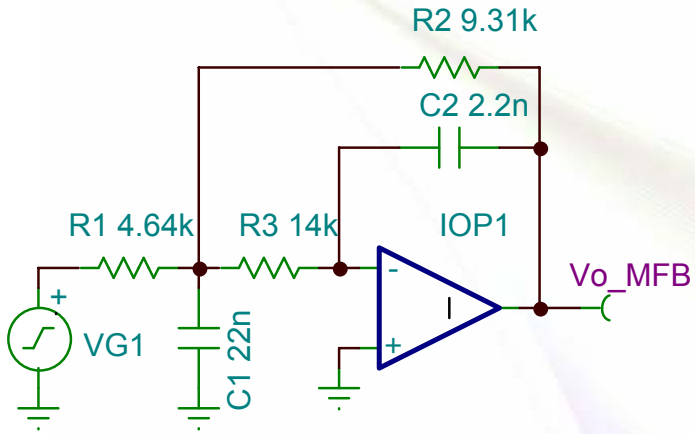
Response plot

Filter schematic with component values

Section Info: G, f_n, "Q"

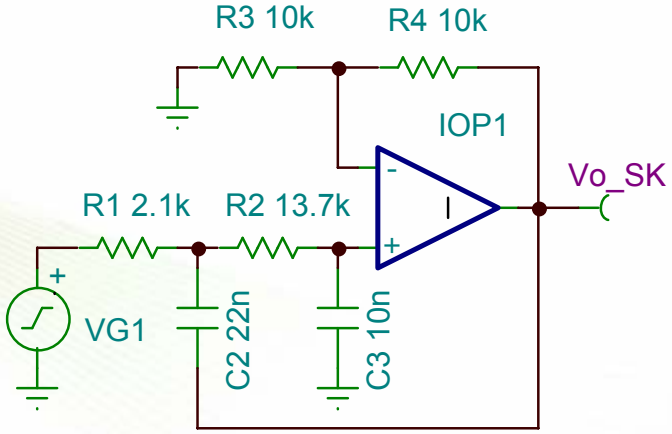
Filter Pro Topologies

Multiple Feedback (MFB)



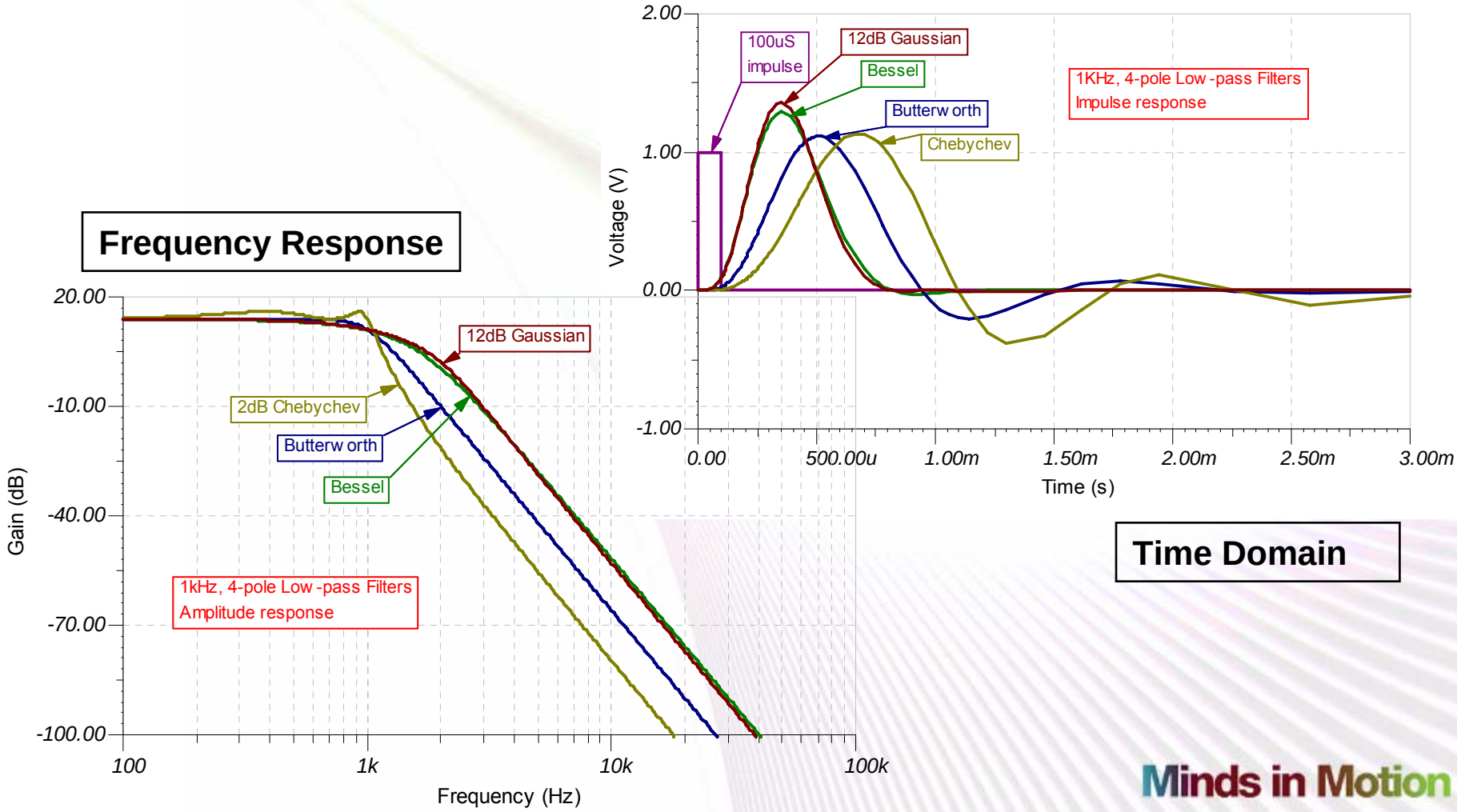
- Inverted stage
- No common-mode error
- Low component sensitivity

Sallen-Key



- Non-inverting stage
- Common-mode input C adds to C3
- G = +1V/V, reduces to follower
- High “Q” sensitivity

Response Characteristics



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ANALOG SIMULATION

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  - Digital
  - Mixed
  - Symbolic
  - Spice
  - Noise
  - Tolerance
  - S-parameters
  - Network Analysis
  - Spectrum Analysis
- Optimization
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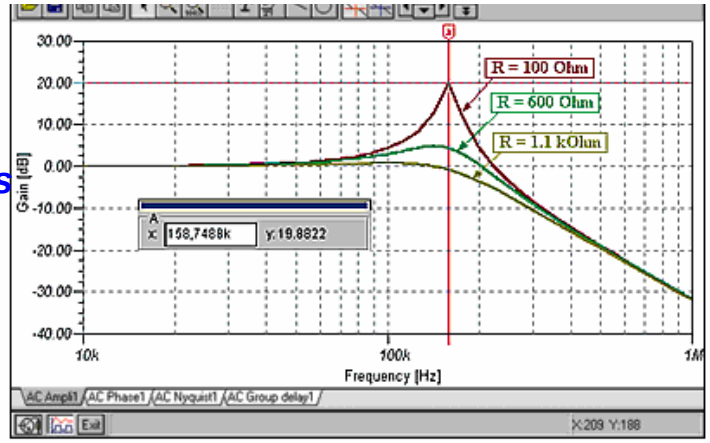
Analog Simulation

Amplifiers and Linear : Tina - Analog Circuit Simulation From Texas Instruments

TINA™

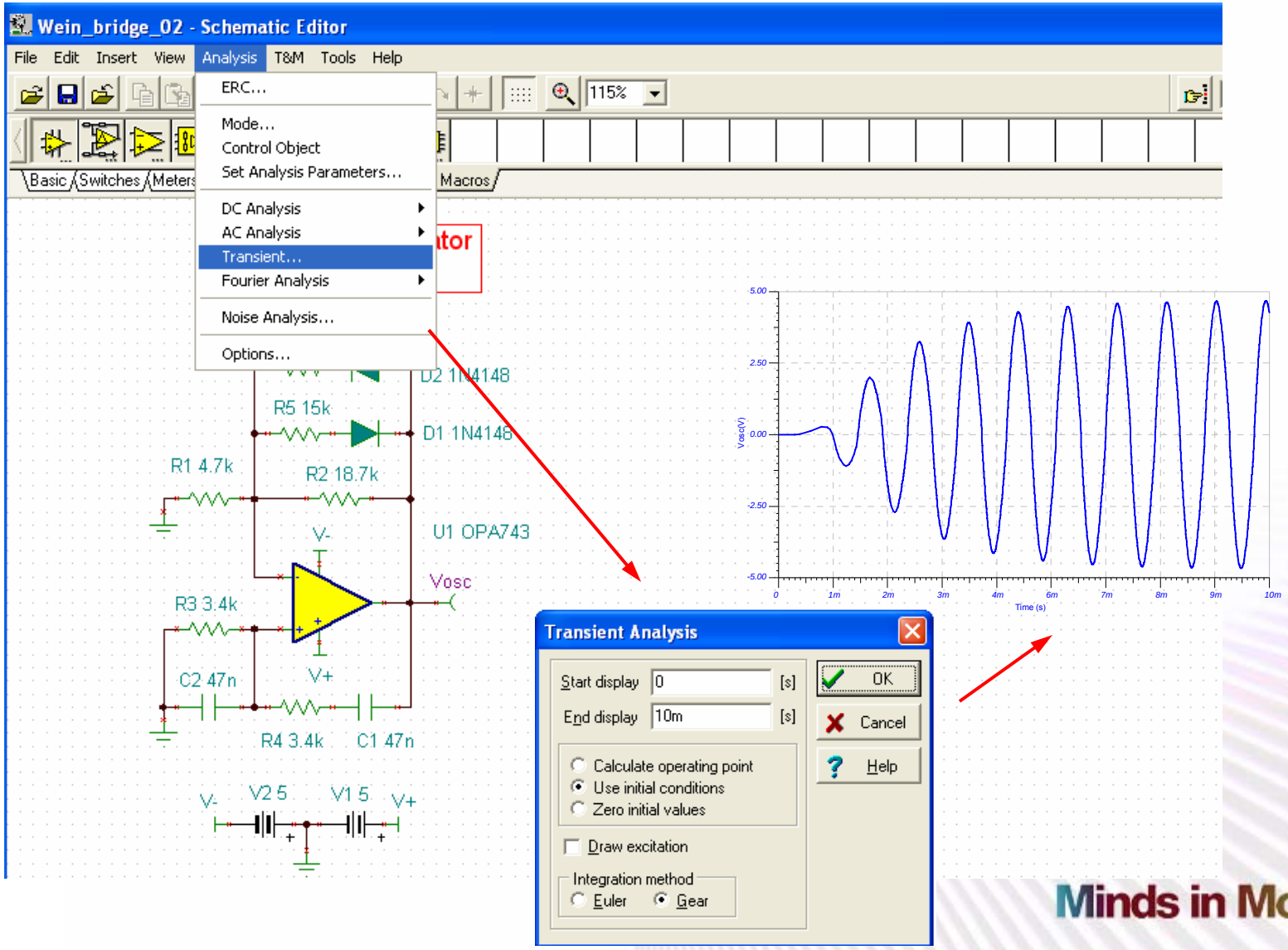
TINA is an easy-to-use, but powerful, circuit simulation program based on a SPICE engine. TINA-TI™ is a fully functional version of TINA, loaded with a library of TI macromodels plus passive and active models. TINA-TI is limited to circuits with two ICs and up to 20 additional nodes.

Screenshot of TINA™ output graphics

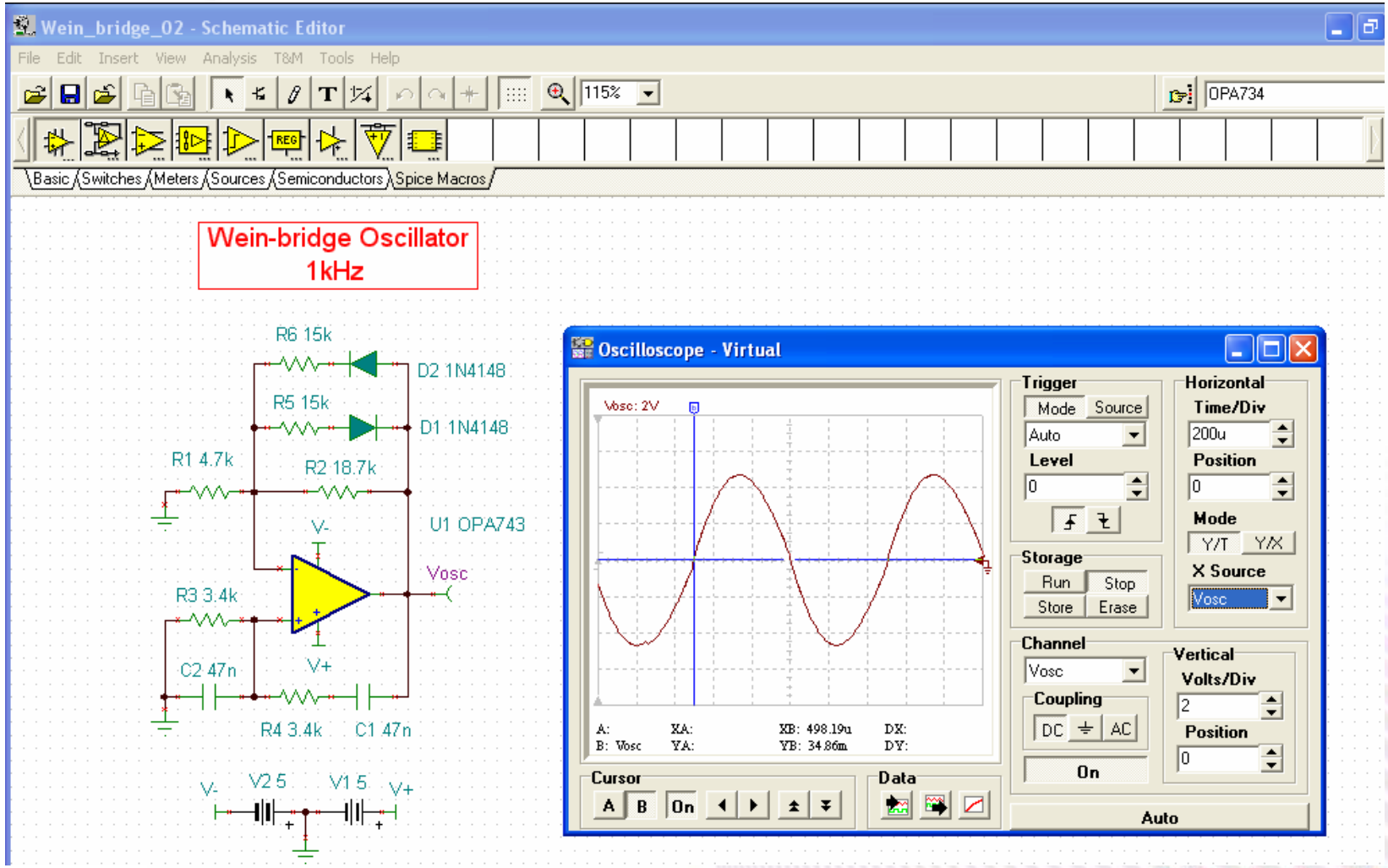


AC Analysis with parameter stepping

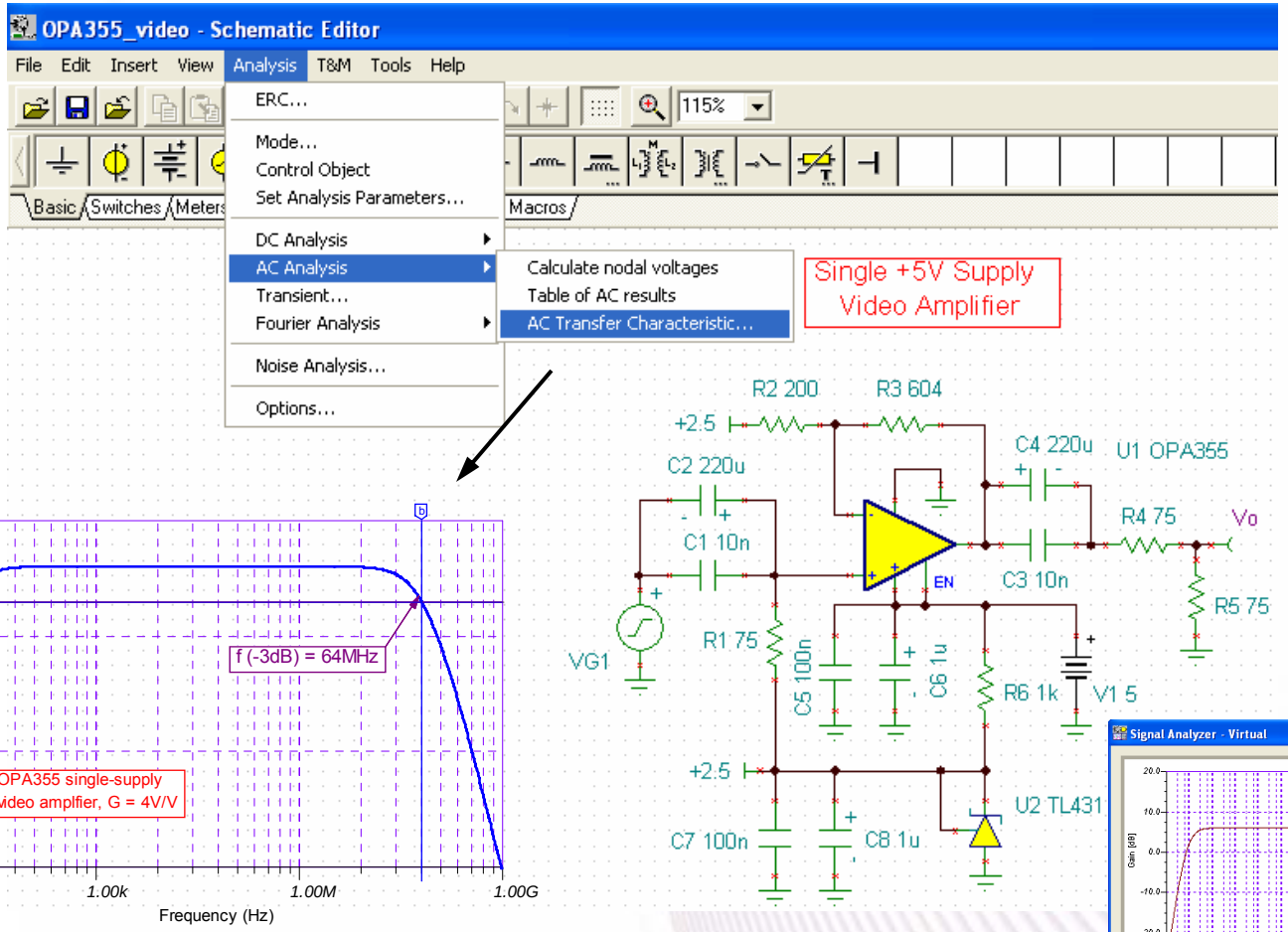
Analysis


Wein_bridge_02 - Schematic Editor
File Edit Insert View Analysis T&M Tools Help
ERC...
Mode...
Control Object
Set Analysis Parameters...
DC Analysis
AC Analysis
Transient...
Fourier Analysis
Noise Analysis...
Options...
Basic Switches Meters Macros
R5 15k
D2 1N4148
D1 1N4148
R1 4.7k
R2 18.7k
U1 OPA743
V-
Vosc
R3 3.4k
C2 47n
V+
R4 3.4k
C1 47n
V- V2 5 V1 5 V+
Transient Analysis
Start display 0 [s]
End display 10m [s]
OK
Cancel
Help
Calculate operating point
Use initial conditions
Zero initial values
Draw excitation
Integration method
Euler Gear
Time (s)

Test and Measurement



TI Example Circuits



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For More on TINA-TI

Where to get TINA-TI:
http://focus.ti.com/docs/toolsw/folders/print/tina-ti.html

Or simply go to www.ti.com
and enter TINA-TI in the keyword search box.

In Summary

- Know Your Input Signals
  - Speed, bandwidth
  - Time relationships to each other
- Choose the Right Scheme
  - Multiplexing
  - Simultaneous sampling
  - Multiple ADCs
- Choose the Right Converter Architecture
  - SAR
    - Input buffering and drive requirements
  - Delta Sigma
    - Settling time of filters

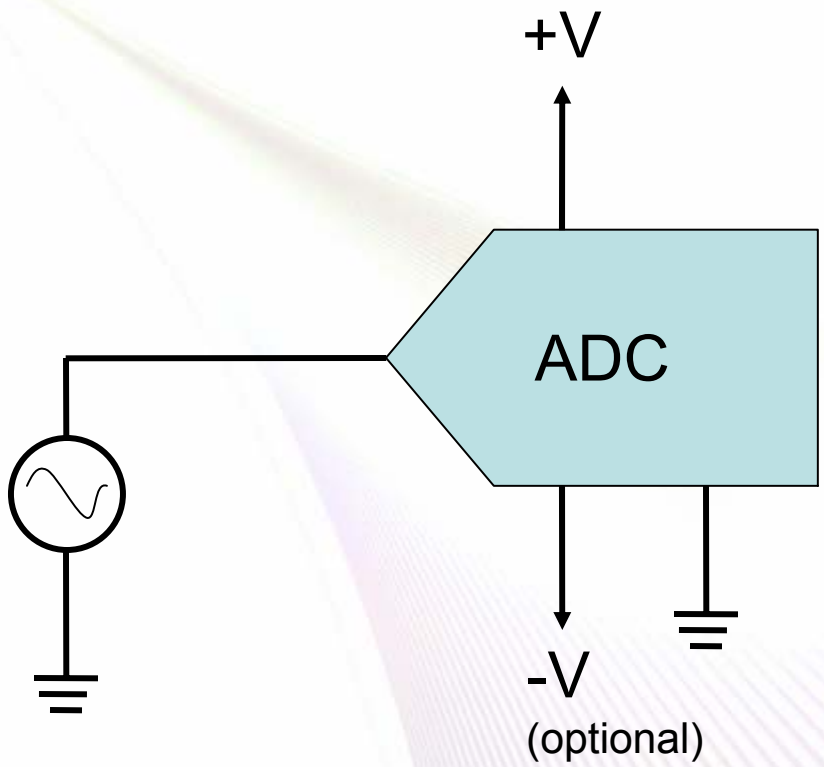
Design Considerations

- ADC Input Drive
- Cost and Performance Tradeoffs
  - Improving embedded ADC performance.
- PCB Layout Considerations
  - Analog and auto routers don't mix.

Input Drive Circuitry

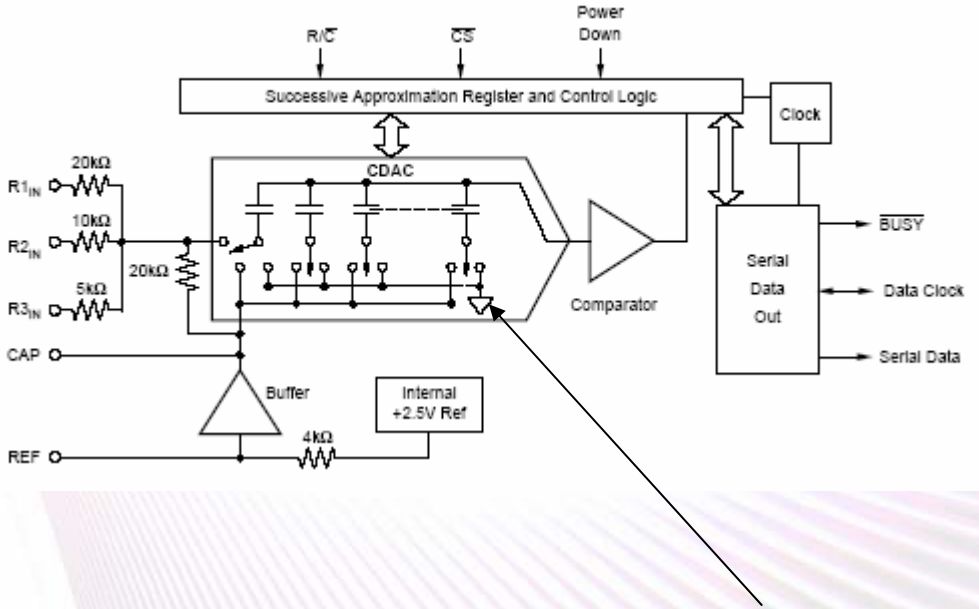
- Input Types
  - Single ended
  - Pseudo-differential
  - Differential
- Buffer Op Amp
  - Rail-to-rail considerations
- RC Circuit
  - Establishing starting criteria
- Modeling the ADC Input Interface

Single-Ended Inputs



Single-Ended Inputs

- A single input pin for a particular channel.
- Input signals are referred to ground.

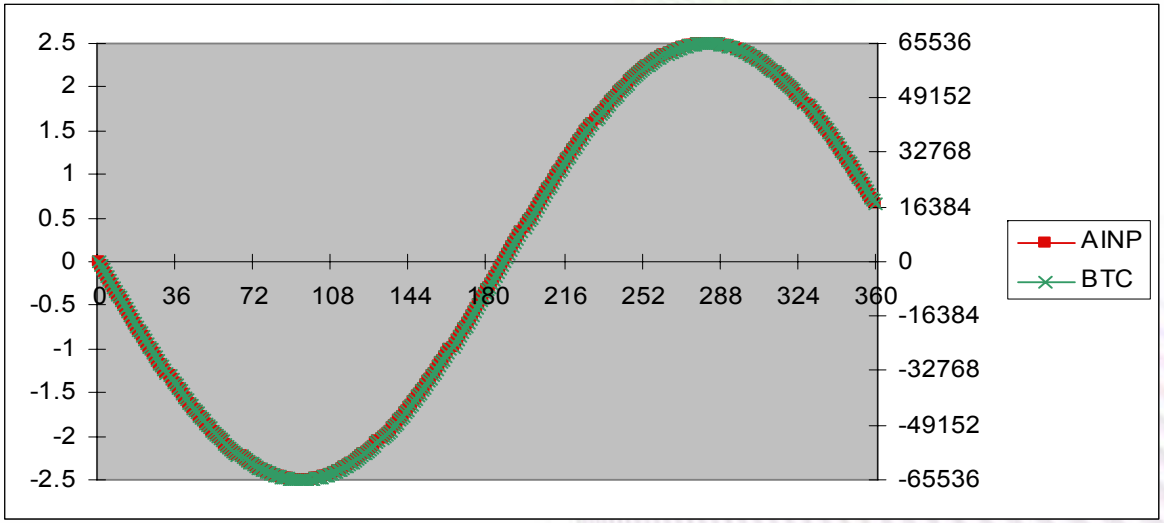


Note: input is referred to GROUND!

True Bipolar Inputs

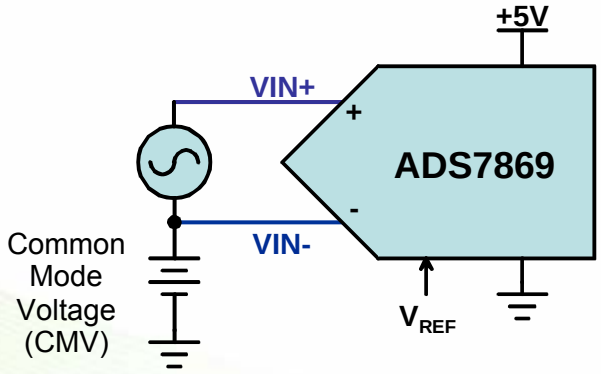
Devices with up to +/-10VDC inputs

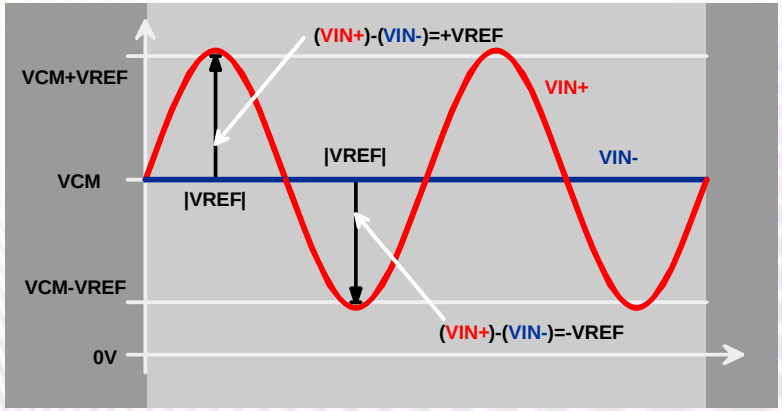
- ADS78xx and ADS85xx Series
- TLC257x and TLC357x Series



Pseudo Differential Inputs

- More like a single-ended input than differential, but with some advantages.
- IN- pin can move, but in a limited range.
- Good for removing common-mode voltages, offsets, etc.
- Provides a “clean” signal reference point.





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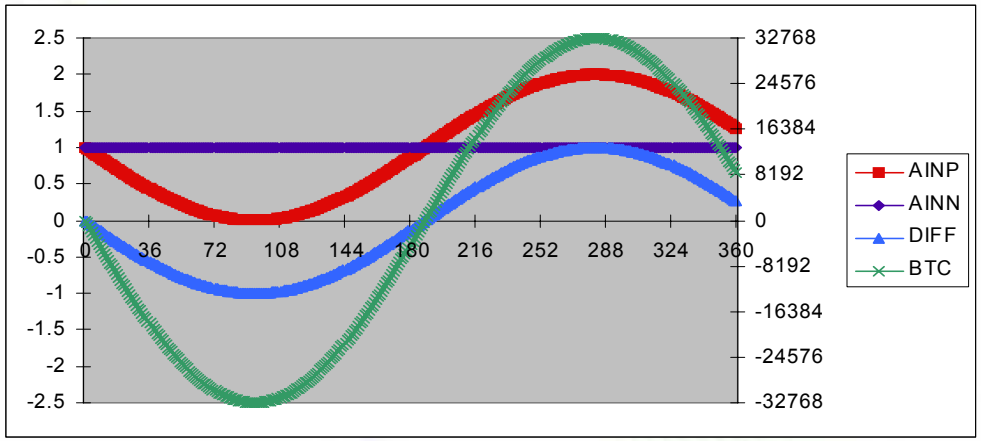
Pseudo Differential Example

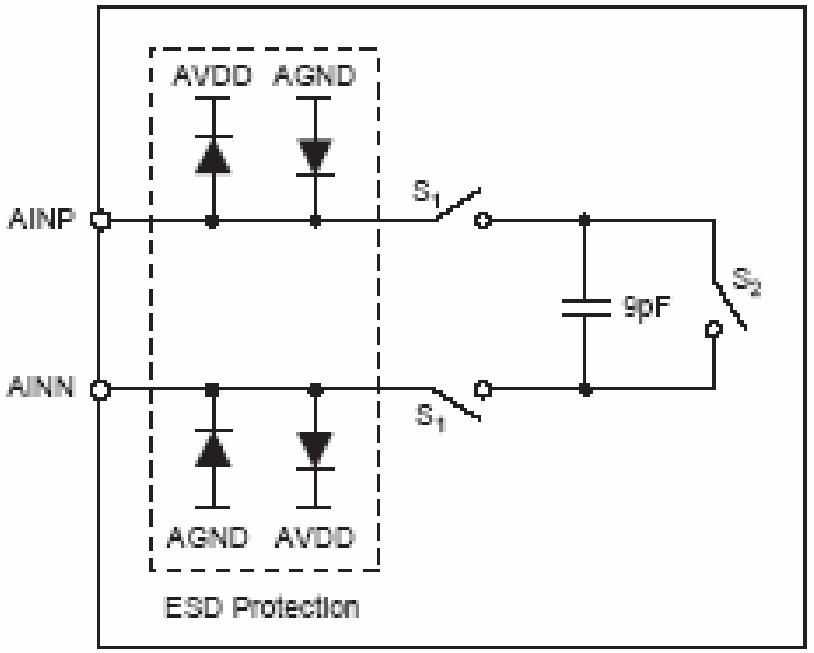


- Example: 0V to 2V sine wave; 1V common mode voltage.
- ADC sees the difference between the two inputs (“differential”).
- Output code may be unipolar or bipolar (bipolar shown here).

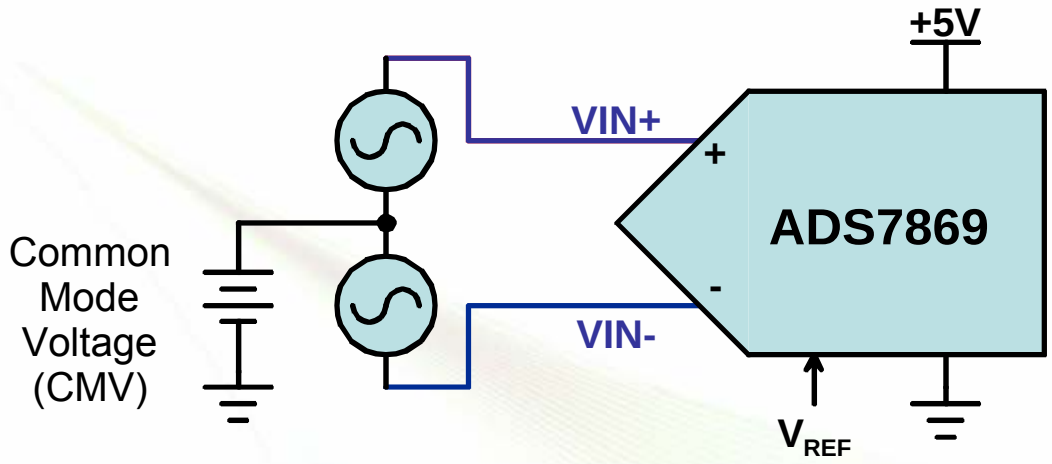
Differential Inputs

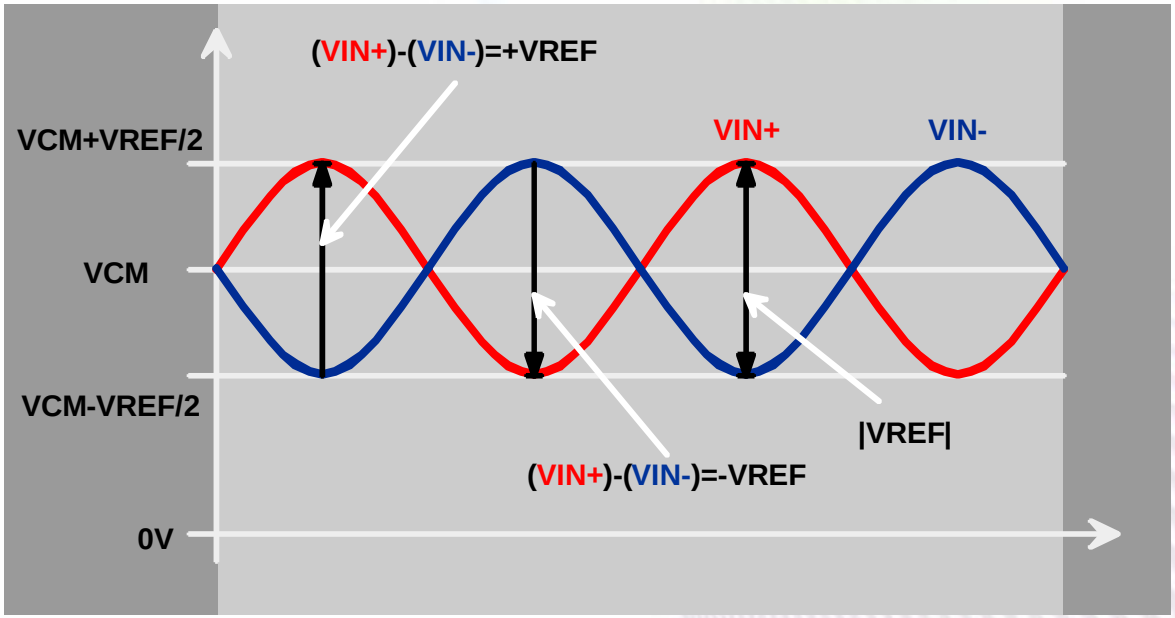
- Sometimes called “fully differential.”
- ADC sees AINP-AINN as input.
- Both inputs can swing from 0V to the full scale – but NOT below ground (in most cases).
- Typically move in a “balanced” fashion.

Example: ADS1271

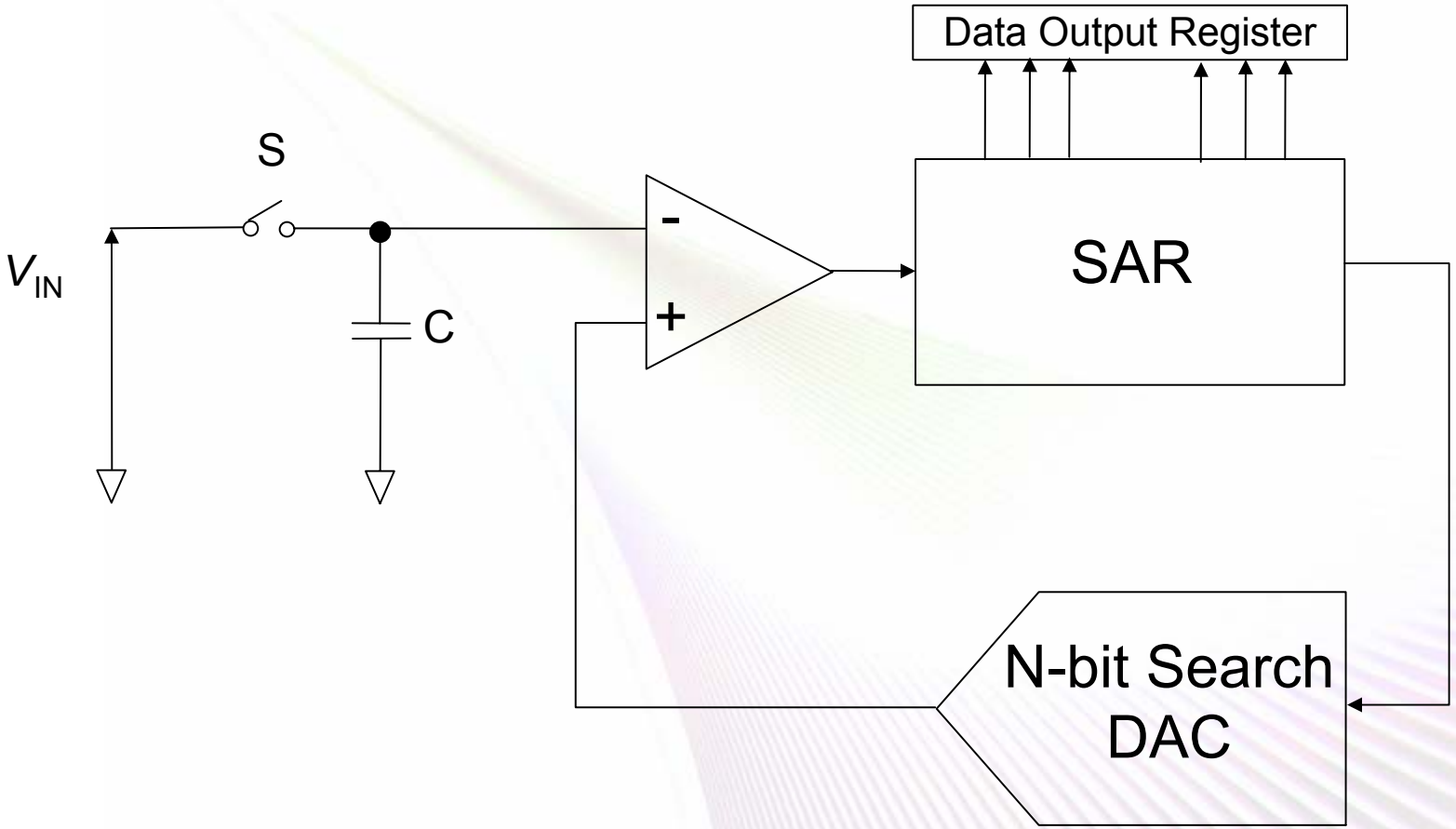


Differential Input Example

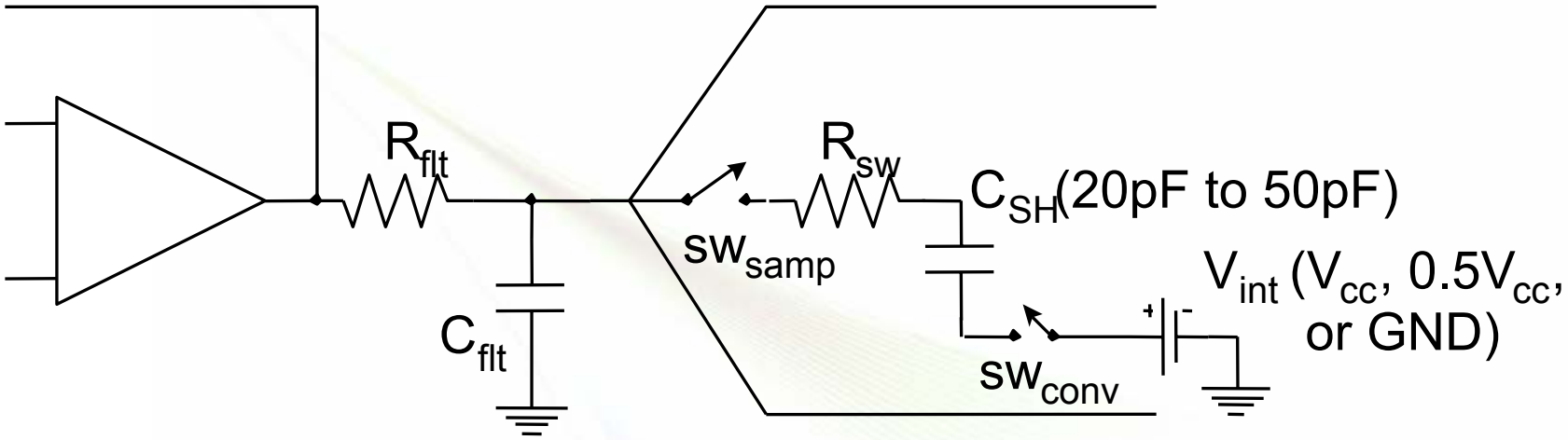




Driving SAR Inputs



Interface Circuit



Op Amp

CMV range, V_{OS} vs CMV

RR out-swing to the rail

Slew rate, Signal BW,

Load transient, Settling time,

Output impedance

Filter

Charge bucket

Filtering,

C_{load} isolation,

A/D

Acquisition time

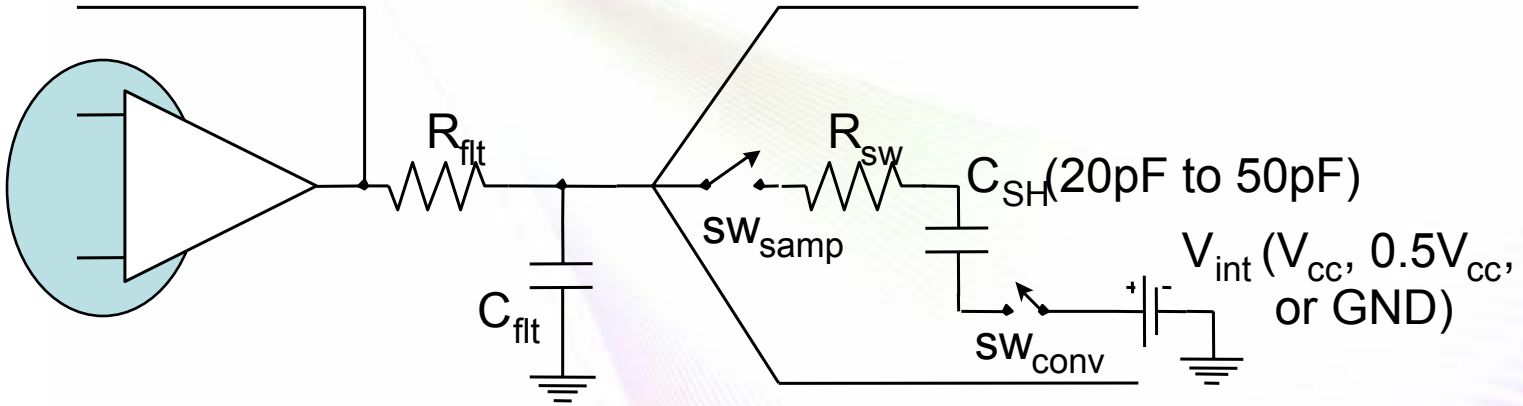
Input circuit parameters

Initial voltage on C_{SH}

Design Checklist Items

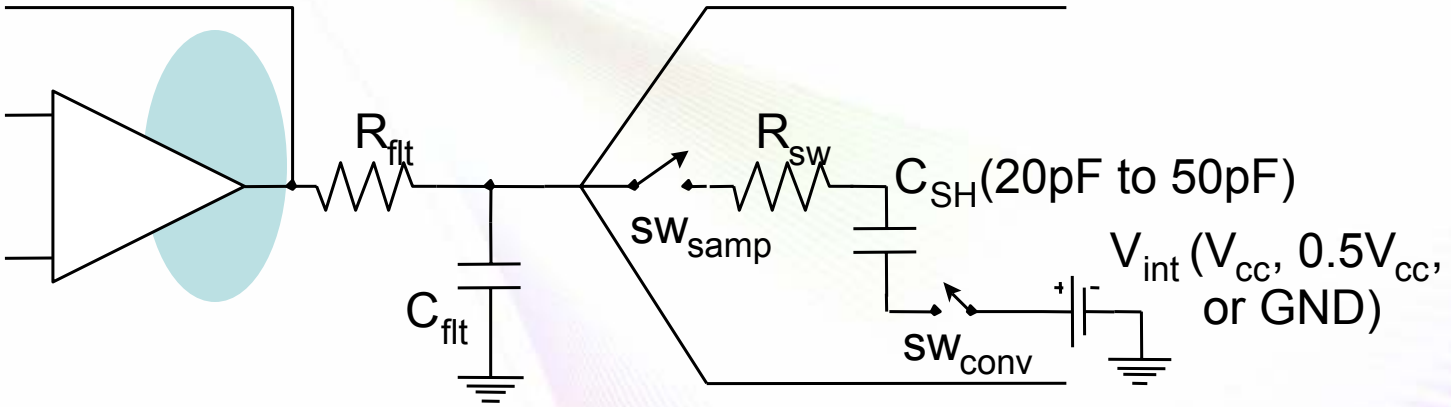
- Op Amp Common Mode Voltage
- Op Amp Output Swing to Rail
- Op Amp Settling Time
- Filter Capacitor Type
- Filter Component Values
- Op Amp Specifications

Amplifier Input Concerns



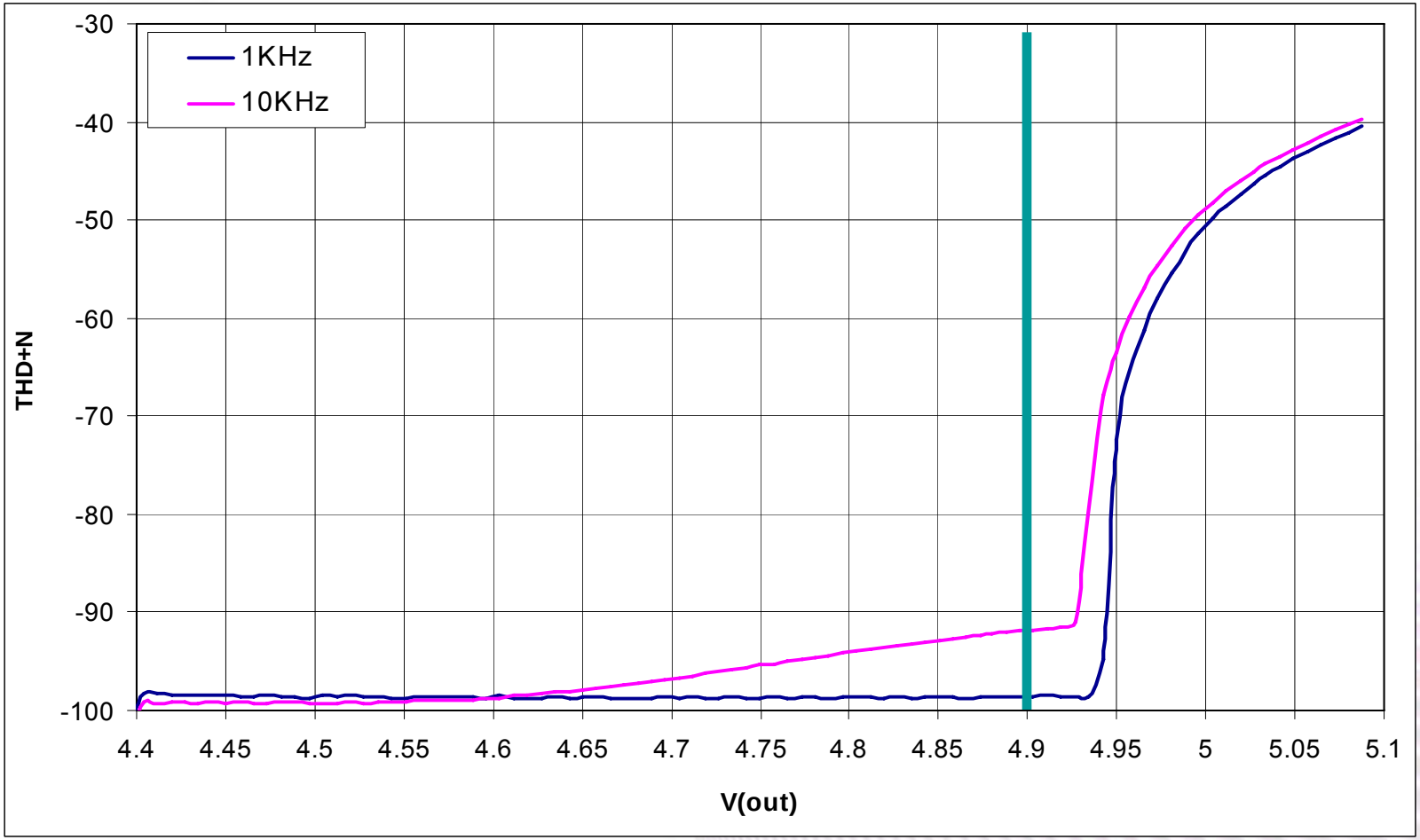
Rail-to-Rail Input

Drive Stage Concerns



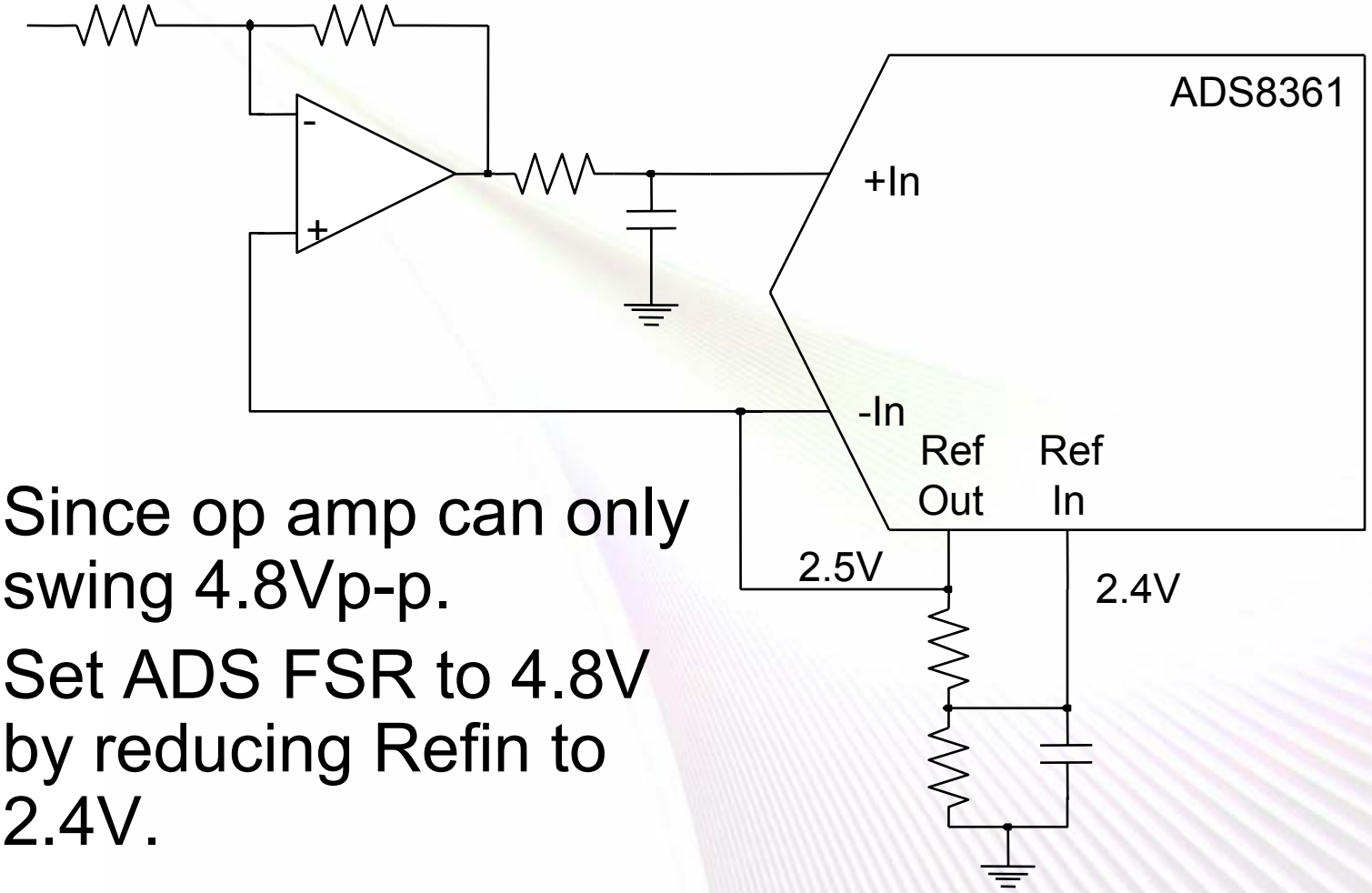
Rail-to-Rail Output

Rail-to-Rail Limitations



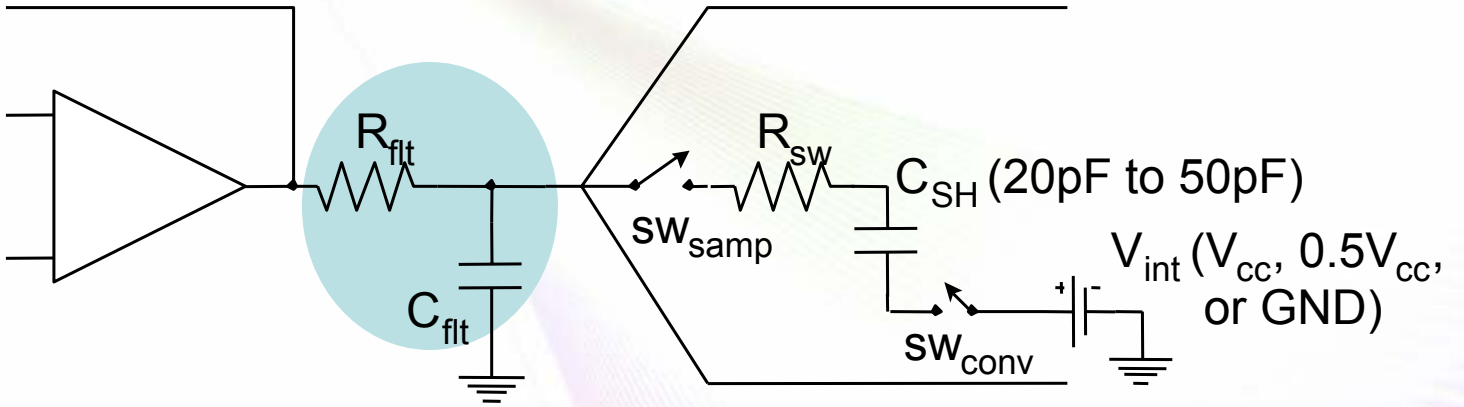
Example: OPA350

A Simple Solution

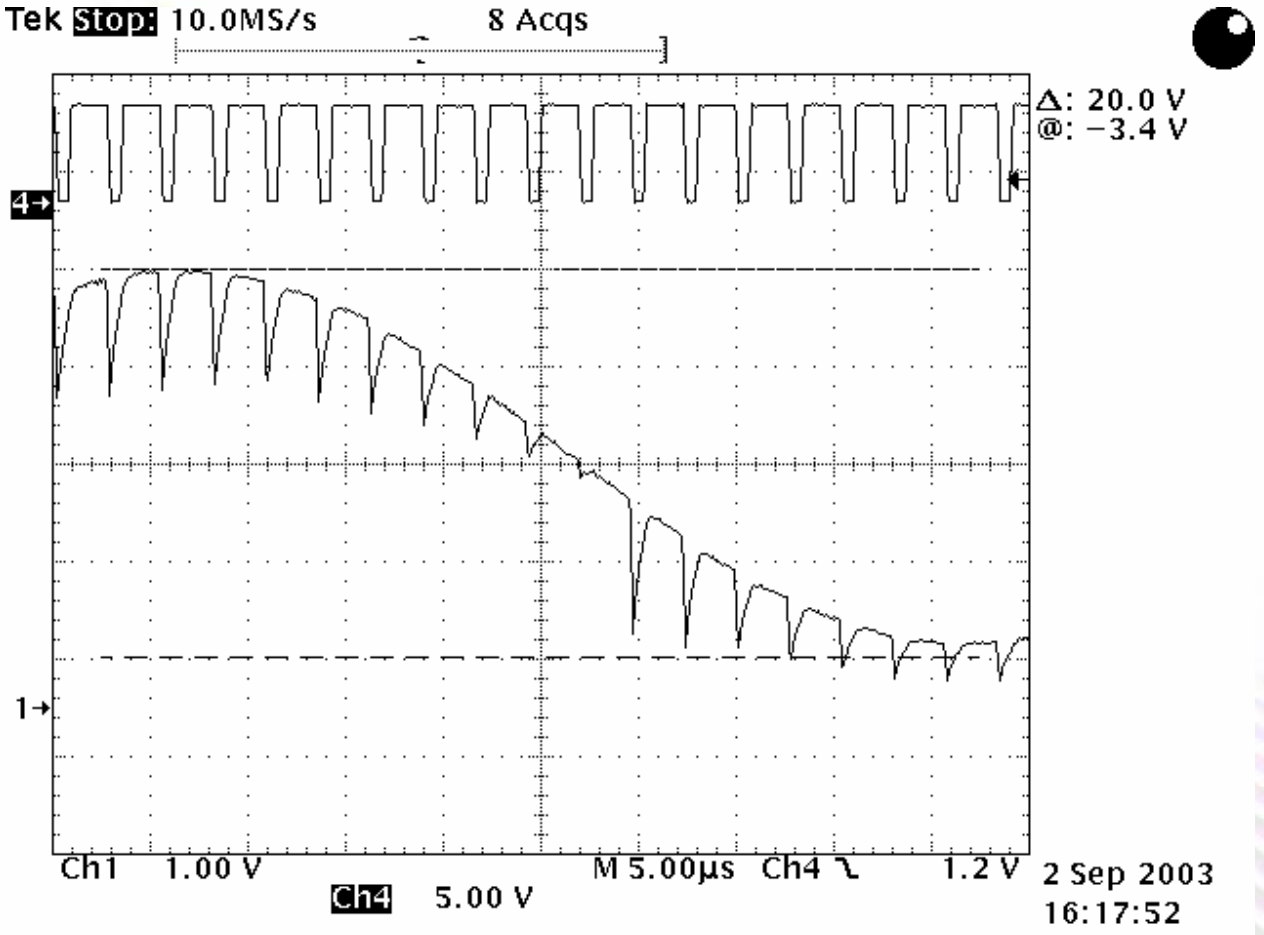


- Since op amp can only swing 4.8Vp-p.
- Set ADS FSR to 4.8V by reducing Refin to 2.4V.

Why the R/C Filter?



Charge Transients



R/C Component Selection

- Pick C_{flt} =20*C_{SH}
- R_{flt} Calculation
  - $t_{flt_settle} = t_{ACQ} = 12\ \tau_{FLT}$
    Theoretical Minimum

Practical Results:

- Use t =18τ_{FLT} margin for:
  - Op amp output load transient
  - Op amp output small signal settling time
- $R_{flt} = t_{ACQ}/18\ C_{flt}$

Settling Time vs. Resolution

Number of bits	0.5LSB	Time Constants
10	0.0488281%	8
12	0.0122070%	9
14	0.0030518%	11
16	0.0007629%	12
18	0.0001907%	13
20	0.0000477%	15
22	0.0000119%	17
24	0.0000030%	18

In Summary

- Choose the right ADC for your system input requirements
  - Single-ended
  - Pseudo-differential
  - Differential
- Buffer op amp
  - Rail-to-Rail considerations
  - Settling times and drive capability
- RC circuit
  - Use the starting criteria established here.
  - Experiment to optimize.

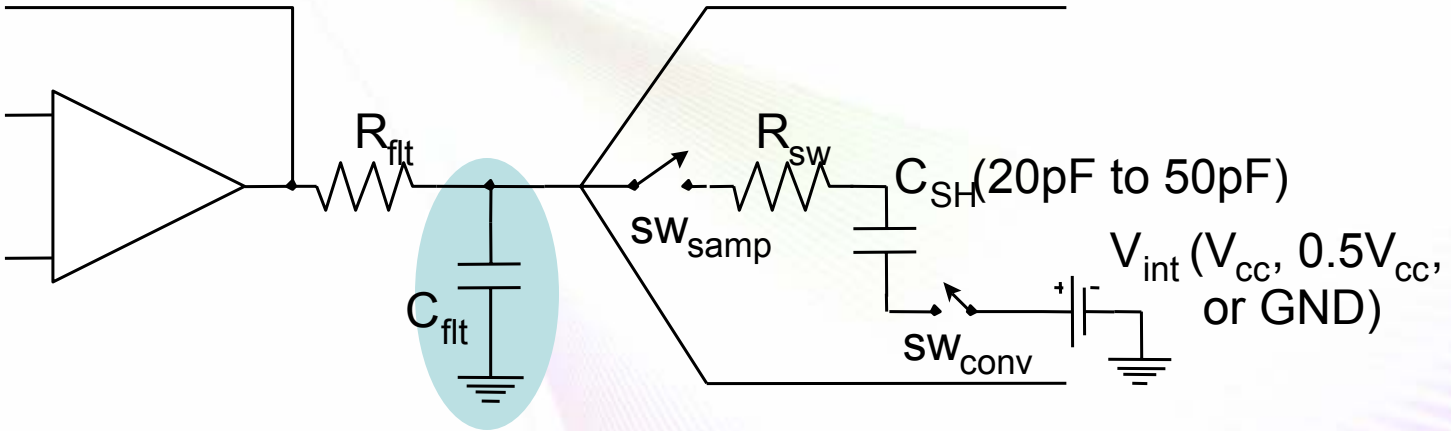
Balancing Cost and Performance

- What does the system really need?
- But I already have an on-board ADC…
- How to improve performance of an embedded converter.

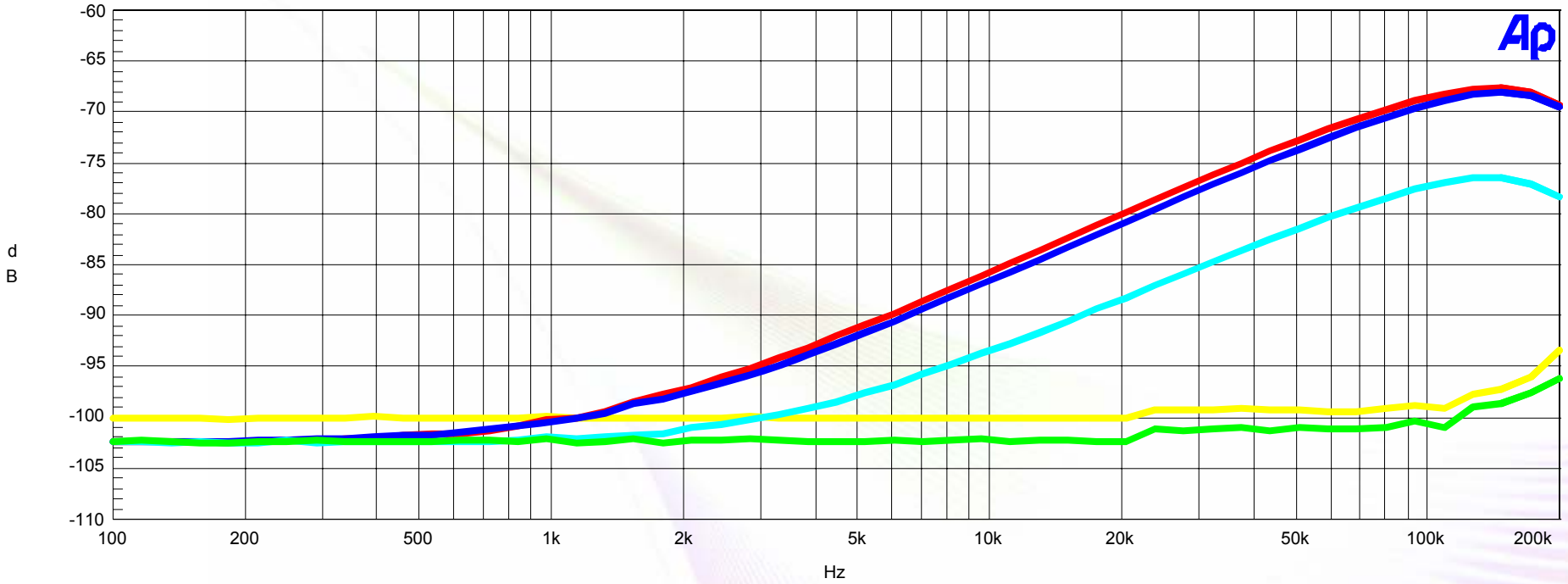
System Input Requirements

- Component selection: choice does matter!
- What performance level are you looking for?
- Does the embedded ADC give the required accuracy?
- Does the on-board reference support the required accuracy?

Capacitor Choice Is Important!



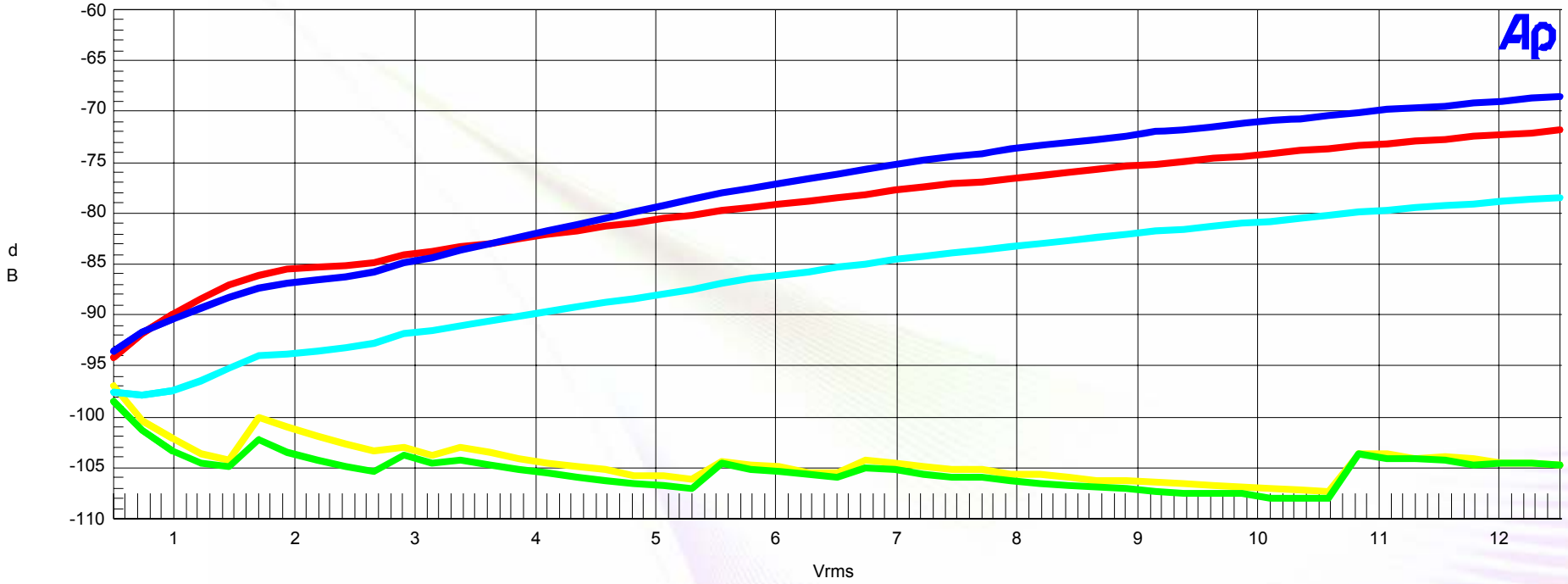
THD+N vs. Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	C = 0
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	C1
3	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	C2
4	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	C3
5	1	Green	Solid	1	Anlr.THD+N Ratio	Left	C4

R = 100 ohm, C = 3.3 nF, Vp-p = 5V f(-3dB) = 482 kHz

THD+N vs. Voltage



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	C = 0
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	C1
3	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	C2
4	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	C3
5	1	Green	Solid	1	Anlr.THD+N Ratio	Left	C4

R = 100 ohm, C = 3.3 nF, f = 10 kHz, f(-3dB) = 482 kHz

What ‘C’ Type Should I Use?

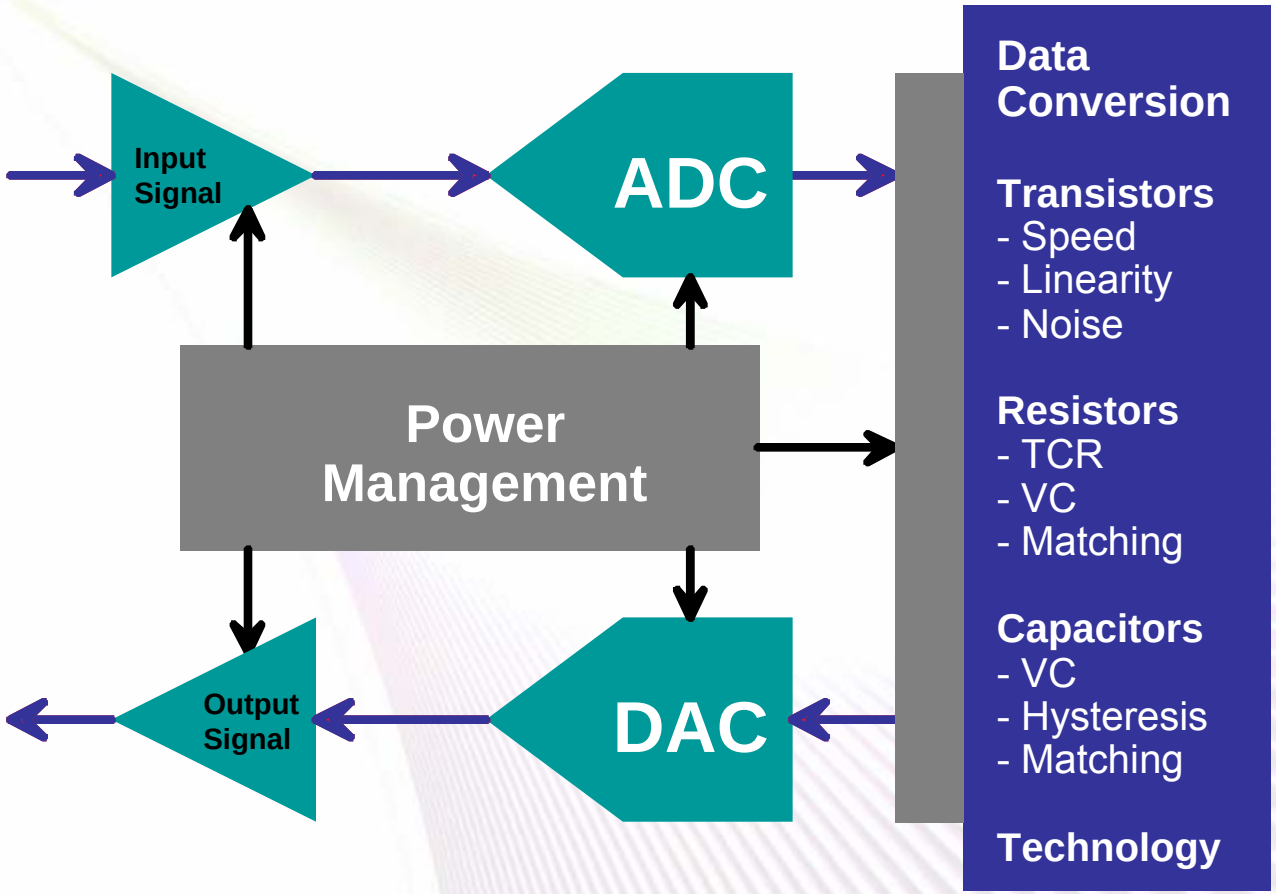
- Best performance:
  - Silver Mica or C0G(NPO)
- Avoid others.
- Others may cost less and be smaller but can distort the input signal.

Embedded Processor ADCs

- Performance vs. cost
- Process issues
  - Digital process, analog application…
- How to improve on-board converter accuracy
  - Try an external precision reference!

DAQ Signal Chain

- Temp
- Pressure
- Speed
- Humidity
- Position
- Flow
- Light



Minds in Motion

Specifications to Watch for

- Speed: How fast is the converter?
- Resolution: What is the ENOB?
- INL: Integral non-linearity
- DNL: Differential non-linearity
- Offset: Error (in LSBs) regarding offset
- Gain: Error (in %FSR) regarding gain

Important Parameters

		ADS7829		ADS7866		ADS7886		56F807	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max
Speed	kSPS		125		100		1000		714*
Resolution		12		12		12		12	
INL (@12bit)	LSB	±0.4	±1.25	±1	±1.5	±0.6	±1.5	±2.5	±4
DNL	LSB	±0.4	+1.25/-1	±0.8	+1.5/-0.9	±0.75	+1.5/-0.9	±0.9	±1
Offset	mV	±0.18	±1.83	±0.5	±0.87	±0.31	±0.92	-25	+10/-90
Gain	%	±0.007	±0.05	±0.007	±0.05	±0.012	±0.04	±0	+8/-7

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to 85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8361 MIN	ADS8361 TYP(1)	ADS8361 MAX	UNITS
ANALOG INPUT						
Full-Scale Range(2)	(FSR)	+IN – (–IN)			$\pm V_{REF}$	V
Operating Common-Mode Signal			2.2		2.8	V
Input Switch Resistance		–IN = V_{REF}		20		Ω
Input Capacitance		–IN = V_{REF}		25		pF

Datasheet Specs…

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to 85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.

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ANALOG INPUT						
Full-Scale Range(2)	(FSR)	+IN – (–IN)			$\pm V_{REF}$	V
Operating Common-Mode Signal			2.2		2.8	V
Input Switch Resistance		–IN = V_{REF}		20		Ω
Input Capacitance		–IN = V_{REF}		25		pF
Input Leakage Current		–IN = V_{REF}		±1		nA
Differential Input Switch Resistance				40		Ω
Differential Input Capacitance				15		pF
Common-Mode Rejection Ratio	(CMRR)	At DC		84		dB
		V_{IN} = ±1.25Vp-p at 50kHz		80		dB
DC ACCURACY						
Resolution			16			Bits
No Missing Code	(NMC)		14			Bits
Integral Linearity Error	(INL)			±3	±8	LSB(3)
Integral Linearity Match		Channel 0/1, Same A/D		4		LSB
Differential Nonlinearity	(DNL)			+1.5(4)		LSB
Bipolar Offset Error	(V_{OS})			±0.5	±2	mV
Bipolar Offset Error Match		Channel 0/1, Same A/D		0.5	1	mV
Bipolar Offset Error Drift	(TCV_{OS})			0.4		ppm/°C
Gain Error(6)	(G_{ERR})			±0.05	±0.5	%
Gain Error Match				0.05	0.15	%
Gain Error Drift	(TCG_{ERR})			20		ppm/°C
Noise				60		µVrms
Power-Supply Rejection Ratio	(PSRR)	4.75V < AV_{DD} < 5.25V, with External Reference, at DC		–70		dB
SAMPLING DYNAMICS						
Conversion Time per A/D	(t_{CONV})	100kHz ≤ f_{CLK} ≤ 10MHz	1.6		160	µs
Acquisition Time	(t_{AQ})	f_{CLK} = 10MHz	400			ns
Throughput Rate					500	kSPS

NOTES: (1) All Values are at T_A = 25°C. (2) Ideal input span; does not include gain or offset error. (3) LSB means Least Significant Bit, with V_{REF} equal to +2.5V; 1LSB = 76µV. (4) Specified for 14-bit no missing code. (5) Specified for 15-bit no missing code. (6) Measured relative to an ideal, full-scale input (+IN – (–IN)) of 4.9999V. Thus, gain error does not include the error of the internal voltage reference.

ADC's performance over temperature at specified speed

Ensured values based on tests in production

Clear test conditions for specified parameters

No hidden and unclear limitations

Read the Fine Print!

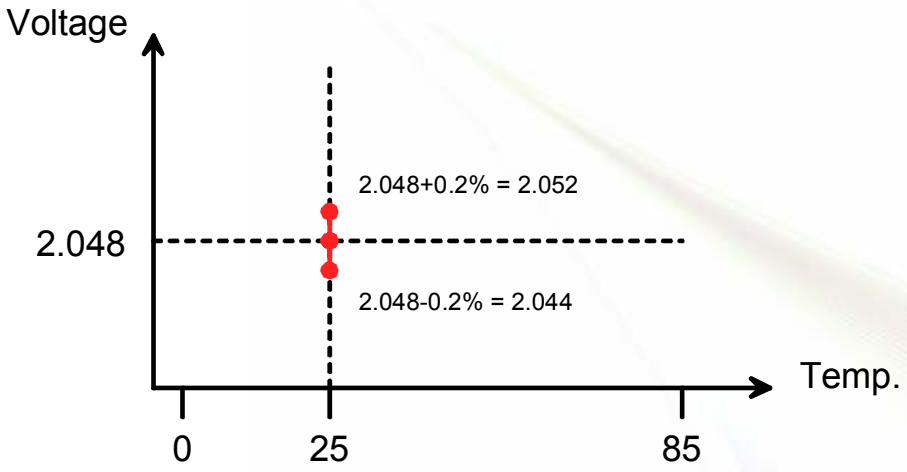
Table 35. ADC Characteristics

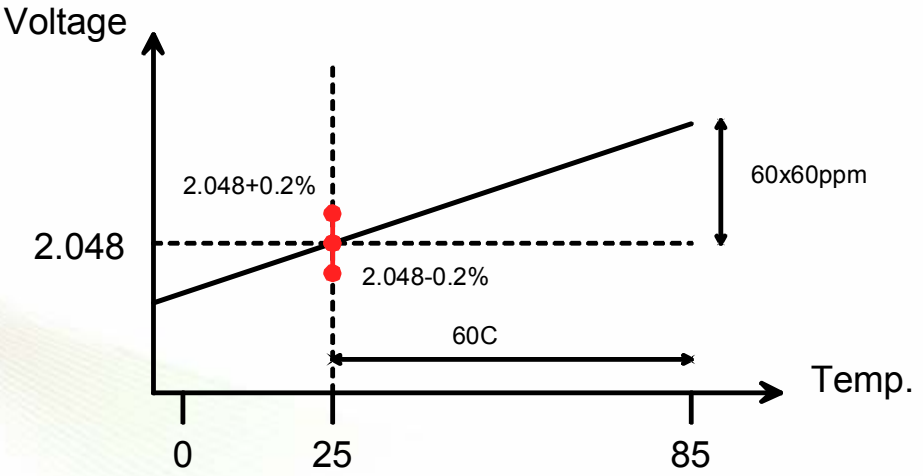
Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $V_{REF} = V_{DD}$-0.3V, ADCDIV = 4, 9, or 14, (for optimal performance), ADC clock = 4MHz, 3.0–3.6 V, $T_A = -40°$ to +85°C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/- 2.5	+/- 4	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[4]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	0.93	1.00	1.08	—

1. For optimum ADC performance, keep the minimum V_{ADCIN} value ≥ 25mV. Inputs less than 25mV may convert to a digital output code of 0.
2. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.

Reference Voltage Accuracy

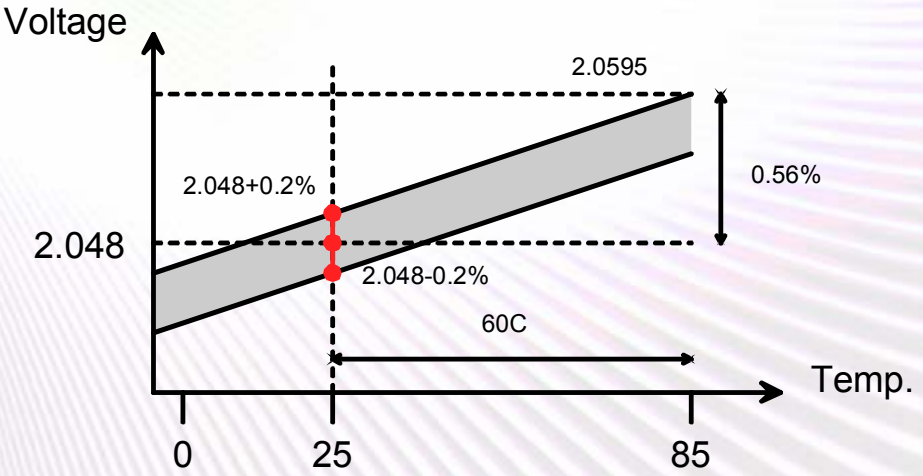




- Initial accuracy: ±0.2%
- Temp. coefficient: 60ppm/°C
- Range of interest: 60°C
- Insured accuracy: ±0.56%

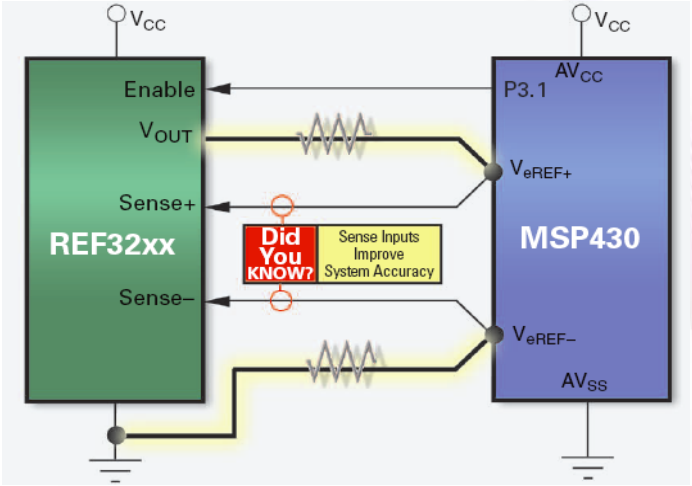
  0.2%+(60*60)ppm=

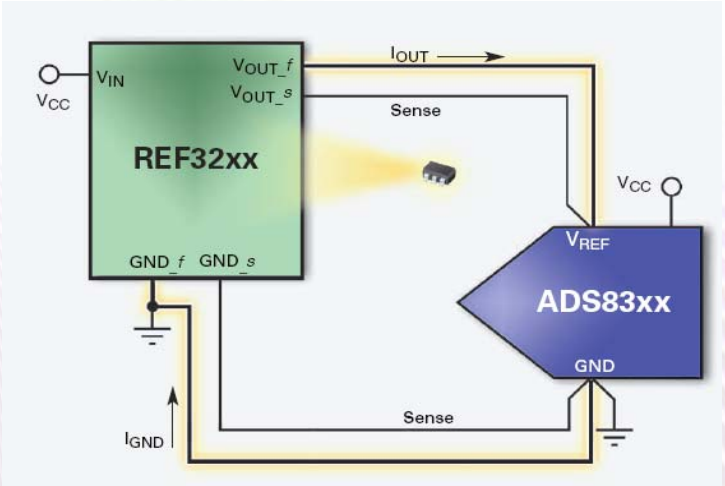
  0.2%+0.36%=0.56%



Minds in Motion

Device	Initial Accuracy (%)	Tmp.Coef. (ppm/°C)		Total Accuracy (%)	
	Max	Typ	Max	Typ	Max
MSP430F167	±4	_	±100*	_	±4.60
56F807	_	_	_	_	_
F2808	_	±50	_	?	_
ADS7829	_	_	_	_	_
ADS7866	_	_	_	_	_
ADS1203	±2	±20	_	±2.12	_
ADS8361	±1	±20	_	±1.12	_
REF29xx	±2	±35	±100	±2.21	±2.60
REF30xx	±0.2	±20	±50	±0.32	±0.50
REF31xx	±0.2	±5	±15	±0.23	±0.29
REF32xx	±0.2	±4	±7	±0.22	±0.24





Minds in Motion

PCB Layout Issues

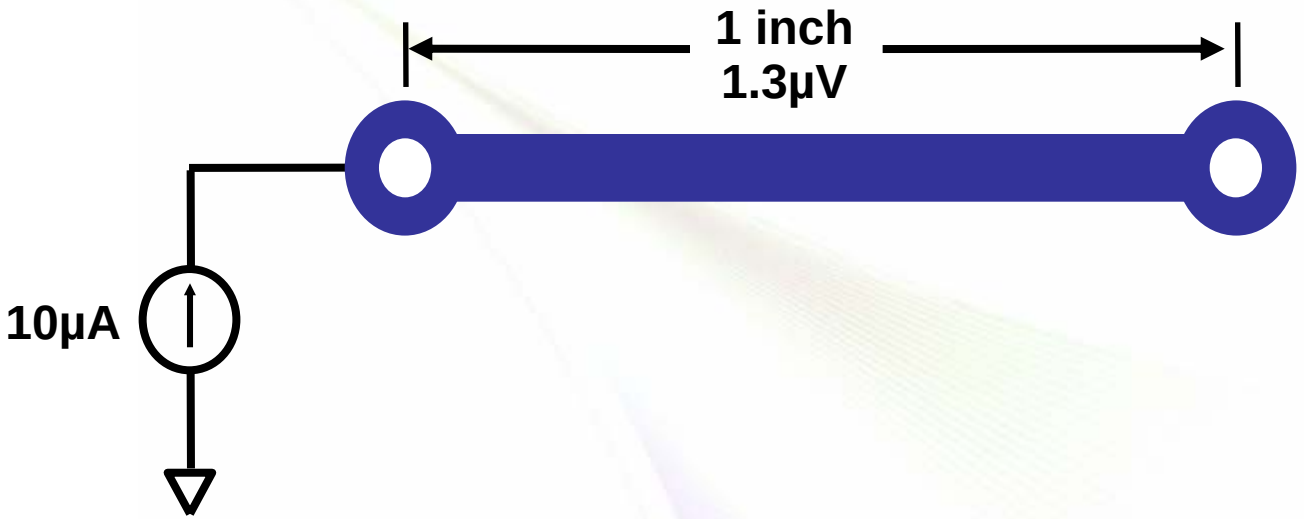
- LSB size
  - Affects your layout decisions.
- Basic PCB Design Principles
  - Care must be exercised for high resolution!
- PCB Layout Reviews
  - Learn from others! Ask your co-workers what worked and what did not. Better yet: Ask us!

LSB Size

Signal range is critical

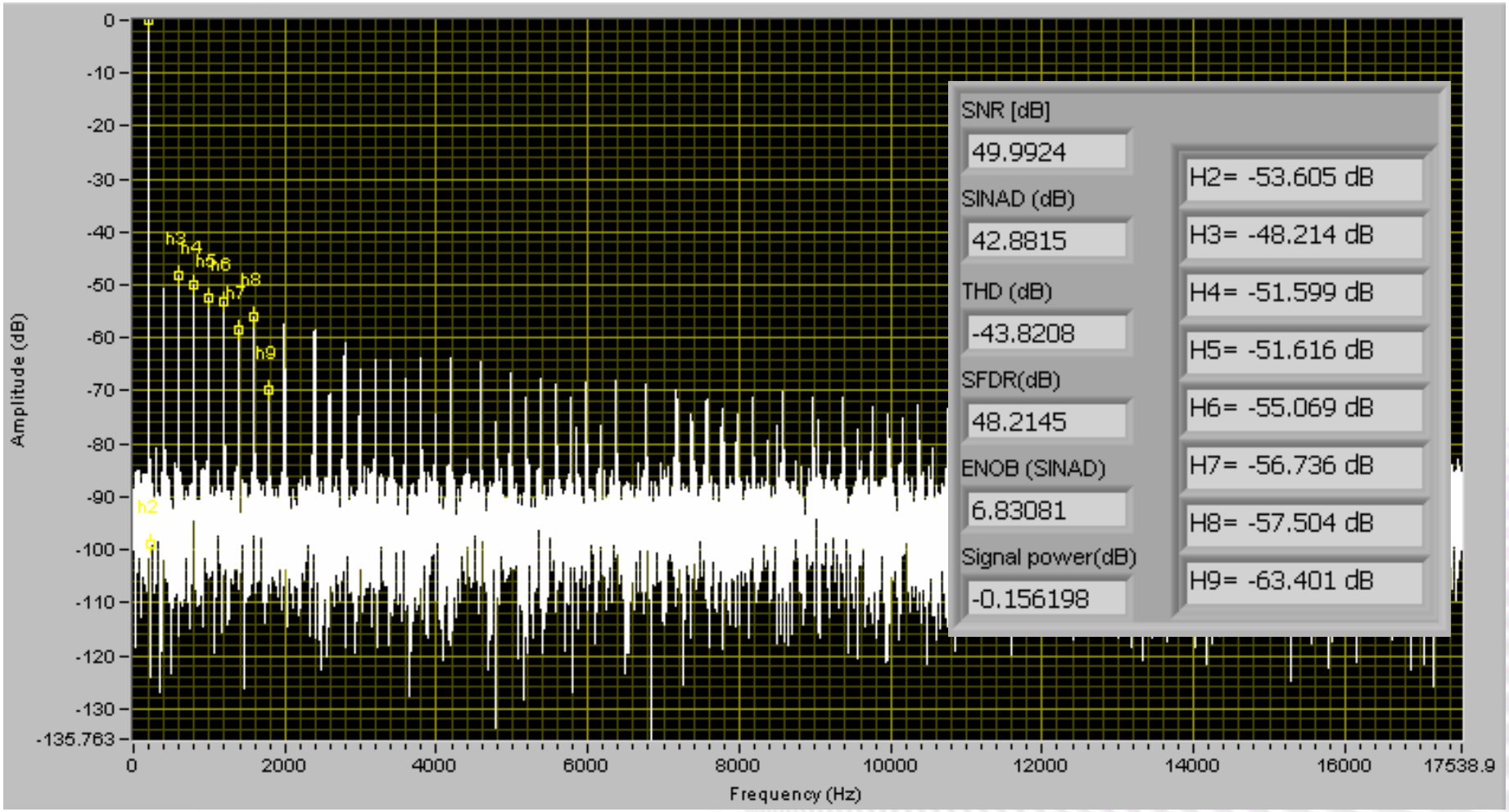
- ±10V is a FSR of 20V
  - 16 bits: 20V/65,536 = 305µV per LSB
  - 24 bits: 20V/16,777,216 = 1,192nV per LSB
- ±2.5V is a FSR of 5V
  - 16 bits: 5V/65,536 = 76.3µV per LSB
  - 24 bits: 5V/16,777,216 = 298nV per LSB
- ±0.020V is a FSR of 0.040V
  - 16 bits: 0.040v/65,536 = 0.610µV per LSB
  - 24 bits: 0.040V/16,777,216 = 2nV per LSB

Trace Length/Width Concerns

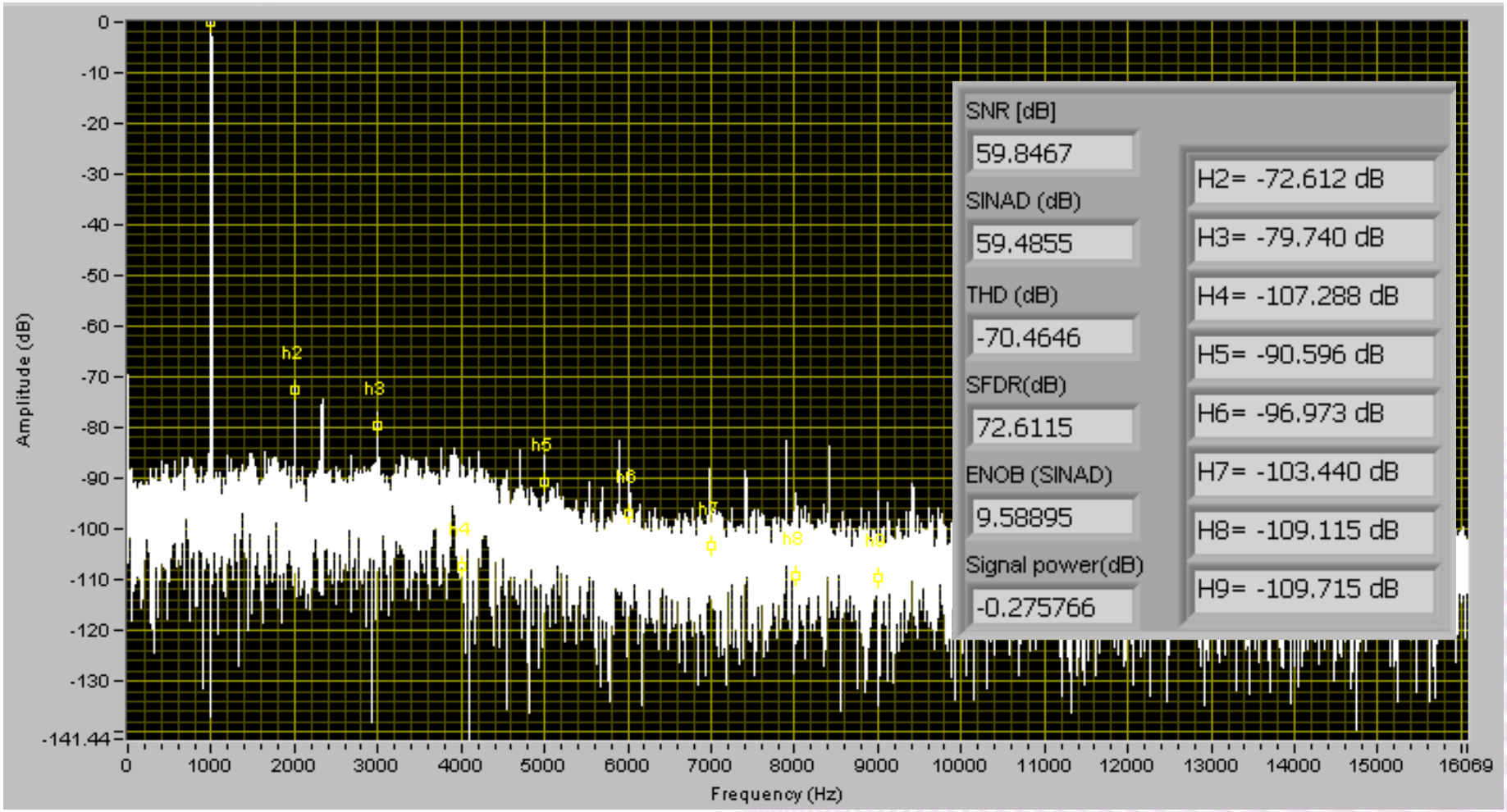


- 1 inch (7 mil) trace of 1/2 oz copper with 10µA of current => voltage drop of 1.3µV.
- This is 4 LSBs at 24 bits!

AC Performance vs. Layout



With Short Traces



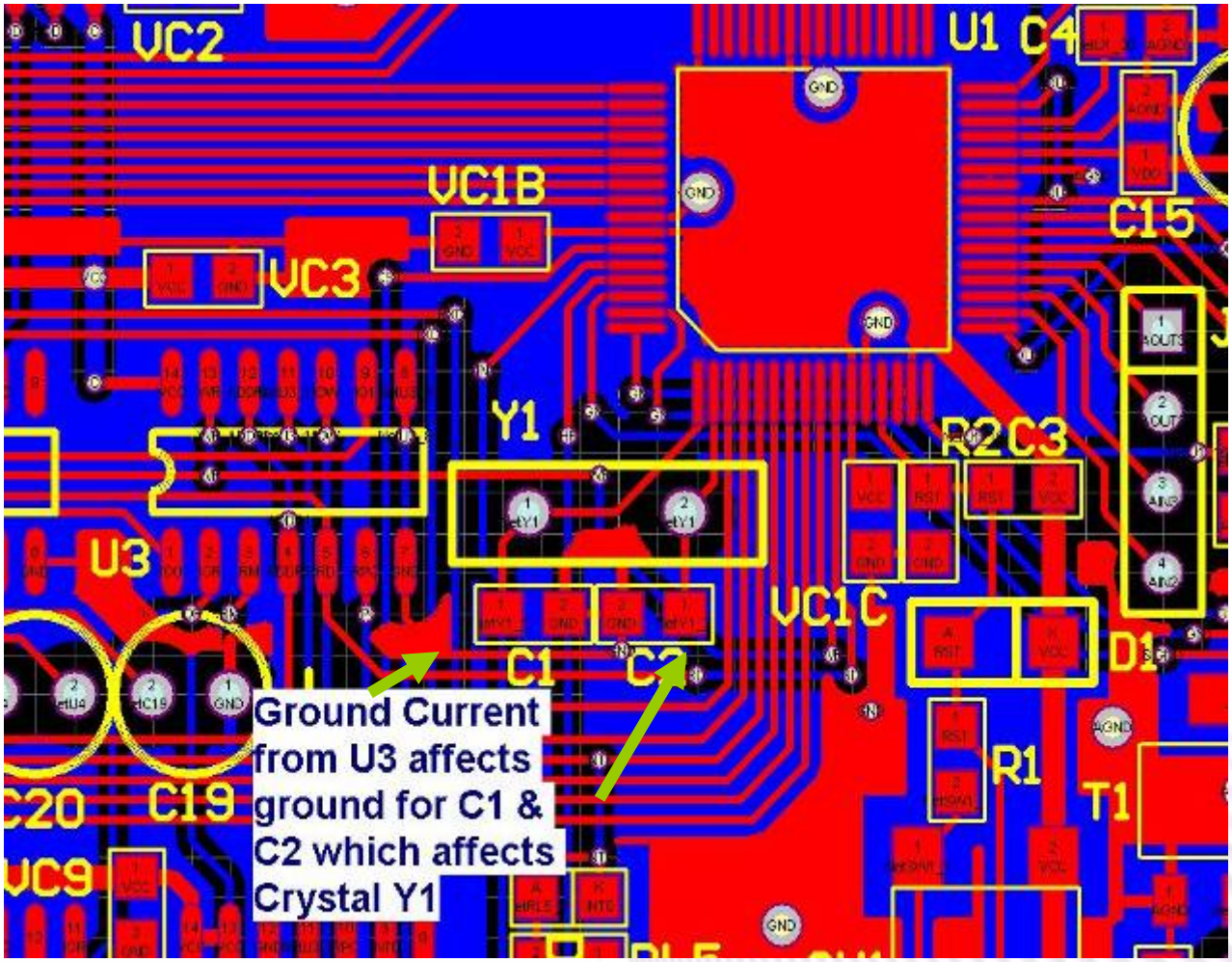
Basic Layout Issues

- Separate analog and digital signals
- AGND and DGND connected at ADC/DAC
- Provide good ground return paths
- High-frequency bypassing
- Minimize inductance
- Differential signal measurements
  - Route in pairs

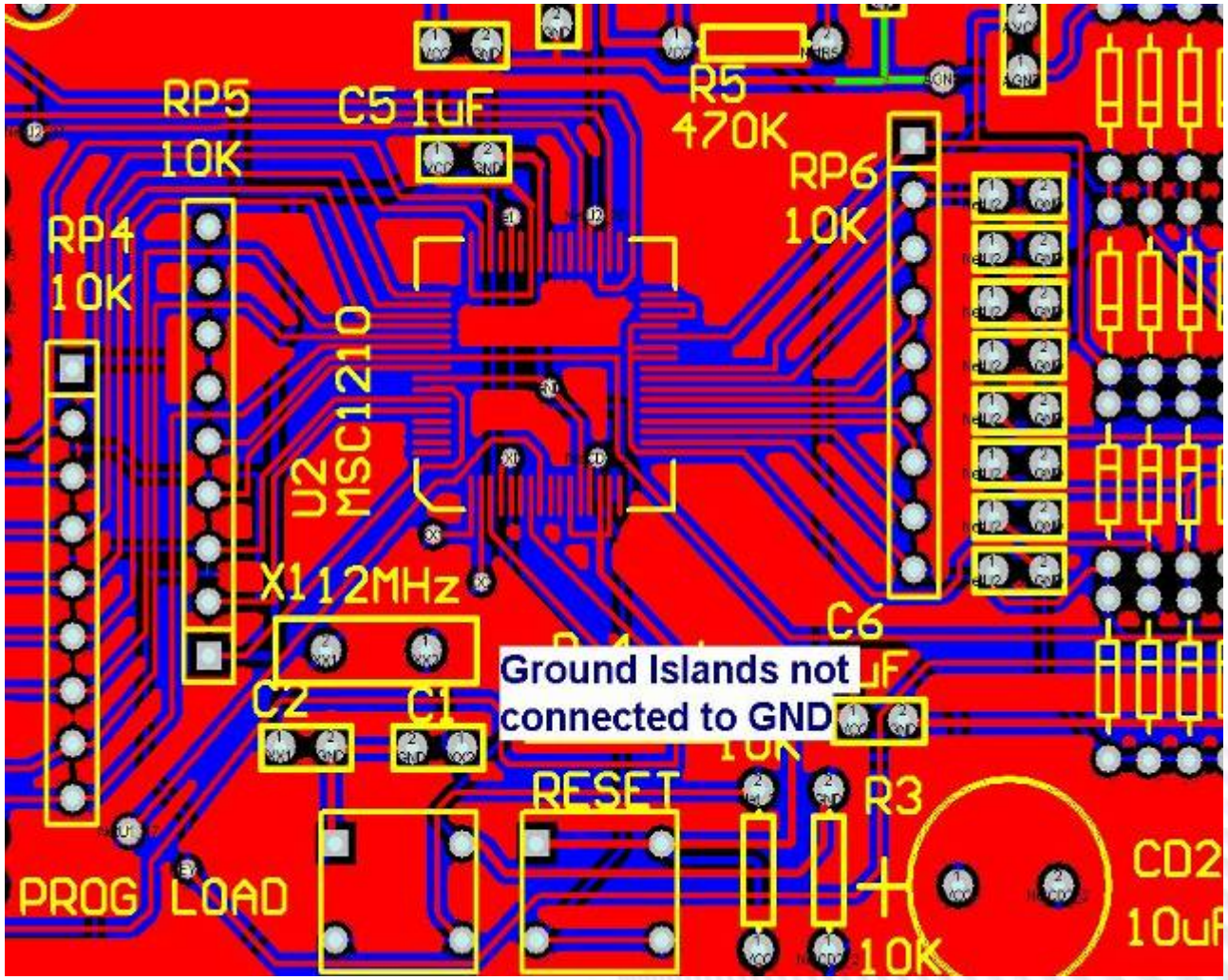
Avoid 'Auto Routing'

- Auto routers do not handle analog signals very well!
- Route critical signals by hand for best performance – this is imperative.
- Route "like" channels in similar fashion.
- Remember to tie grounds locally at the most critical circuit – usually the ADC.

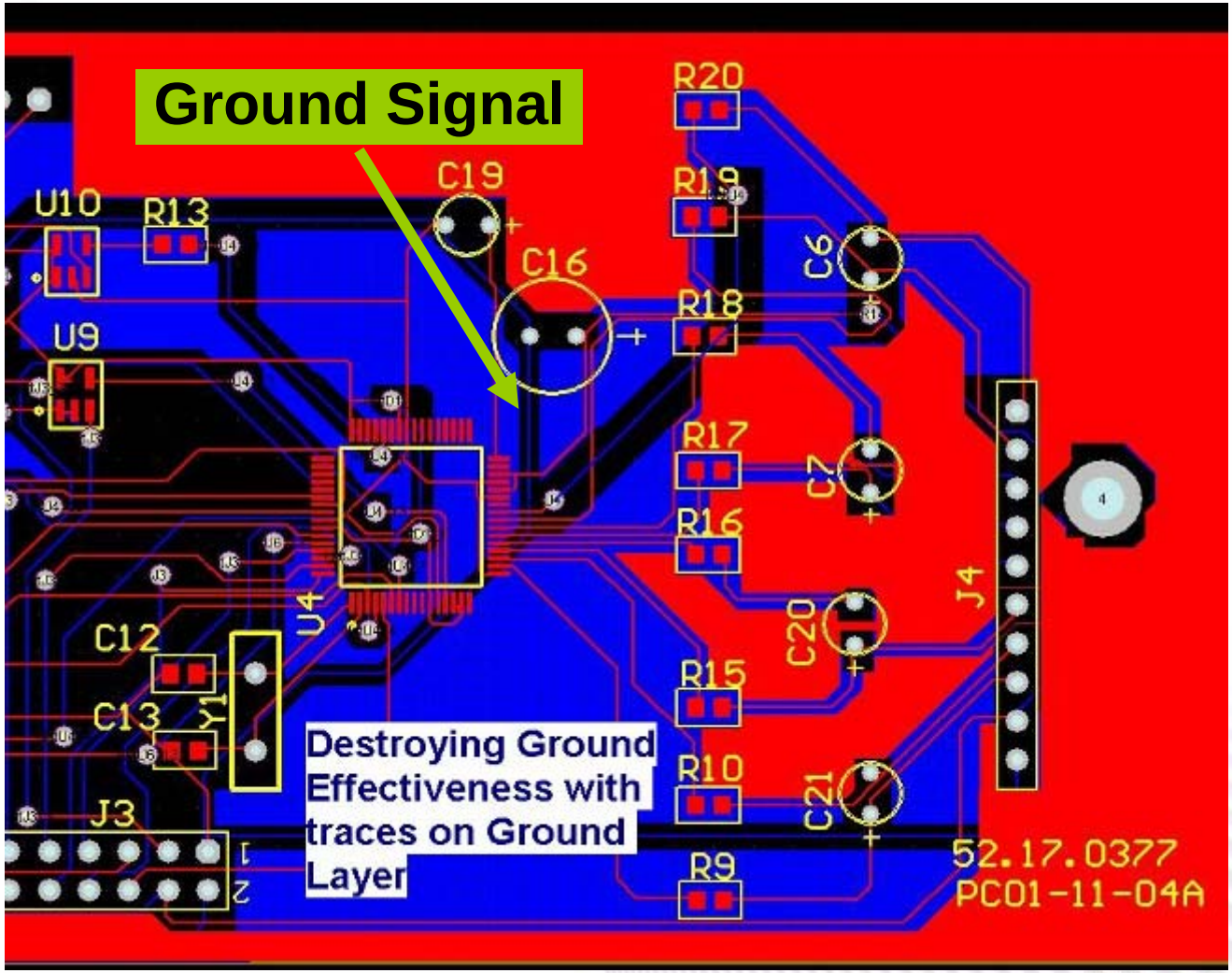
PCB Layout


VC2
U1
C4
VC1B
C15
VC3
Y1
R2
C3
U3
VC1
C
D1
C1
C2
Ground Current
from U3 affects
ground for C1 &
C2 which affects
Crystal Y1
C20
C19
R1
T1
VC9
GND
AGND

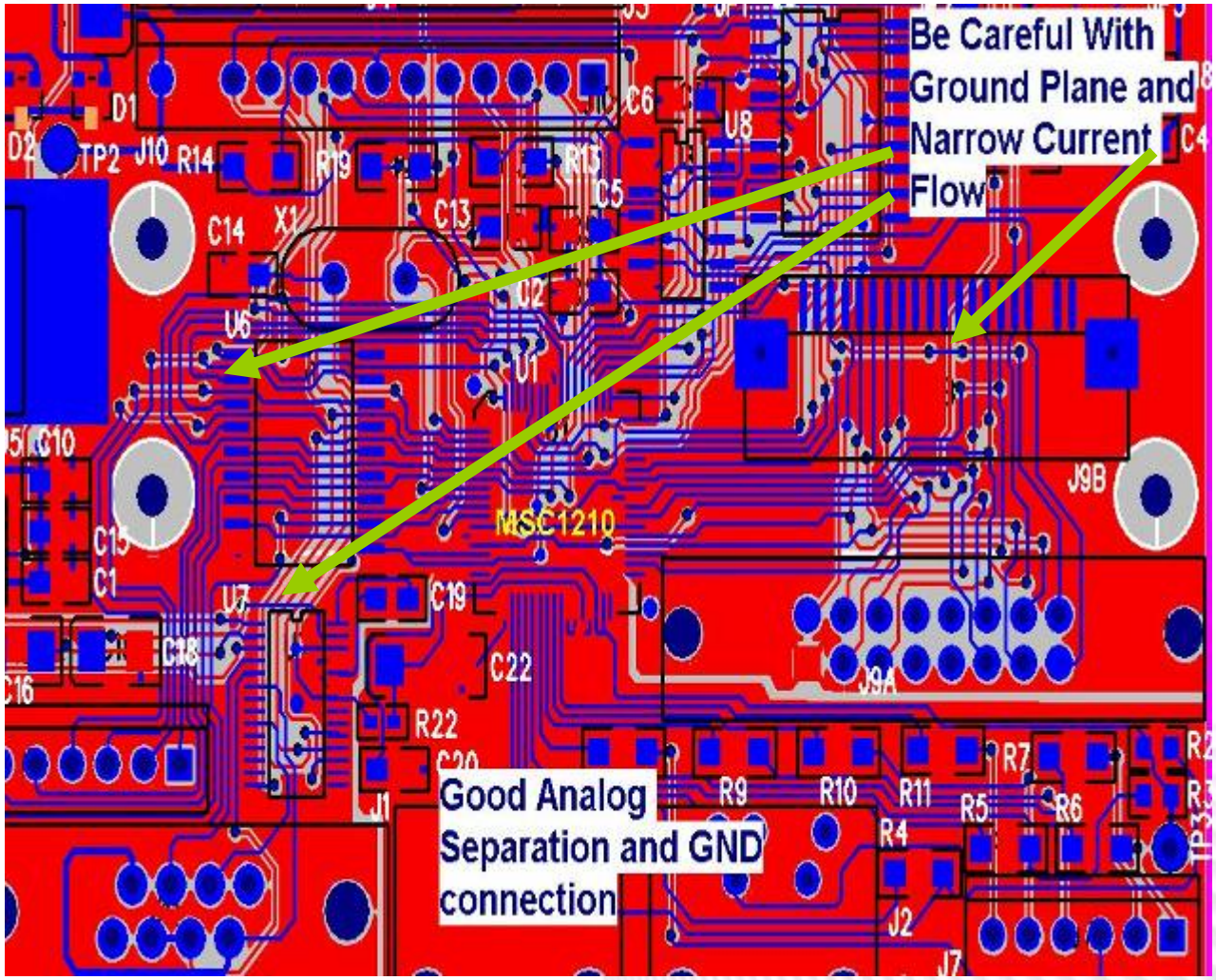
PCB Layout


RP5
10K
C5 1uF
R5
470K
RP6
10K
RP4
10K
U2
MSC1210
X1 12MHz
C6
Ground Islands not
connected to GND
C2
C1
RESET
R3
PROG
LOAD
CD2
10uF
10K

PCB Layout


Ground Signal
R20
C19
R19
U10
R13
C16
C6
R18
U9
R17
C7
R16
J4
U4
C20
C12
R15
C13
Y1
Destroying Ground Effectiveness with traces on Ground Layer
R10
C21
J3
R9
52.17.0377
PC01-11-04A

PCB Layout

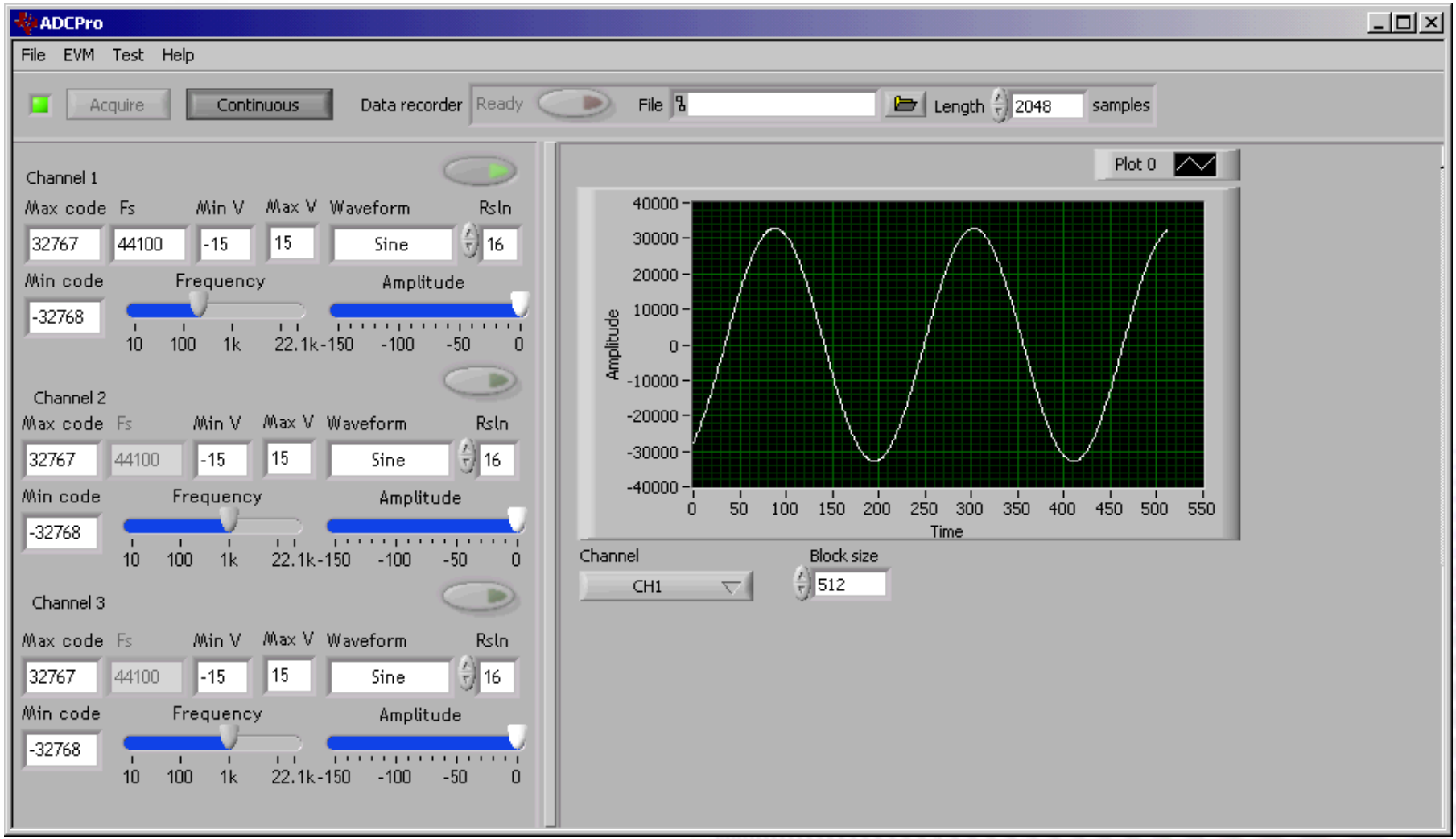


Minds in Motion

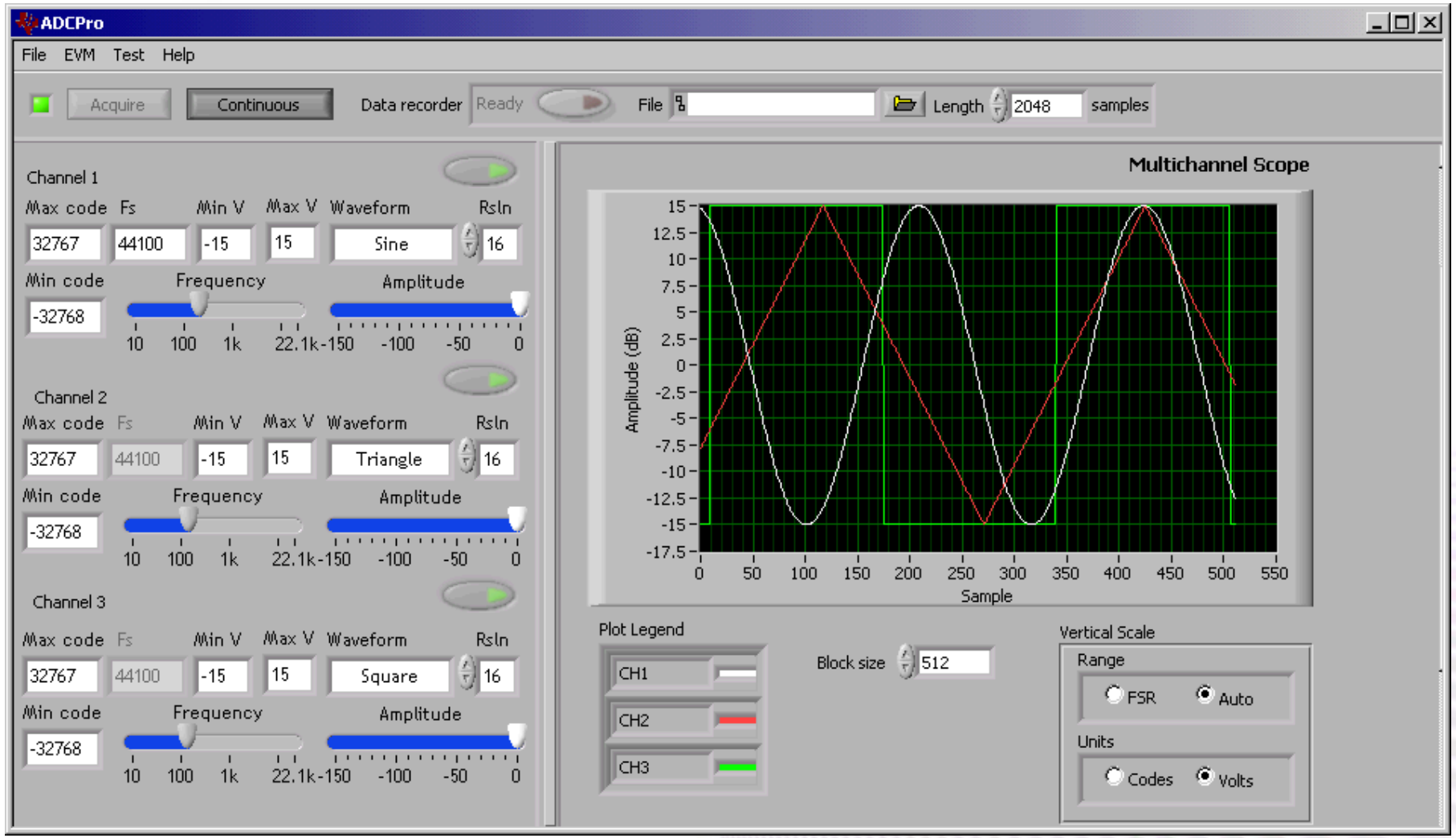
Demo Time!

- Software Tools
  - ADC Pro
  - Code Composer Studio™, Embedded Workbench™
- Hardware Tools
  - Analog EVMs
  - DSP starter kits
- Where to get more
  - App notes
  - Code examples

ADC Pro


ADCPro
File EVM Test Help
Acquire
Continuous
Data recorder
Ready
File
Length
2048
samples
Channel 1
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Sine 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Channel 2
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Sine 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Channel 3
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Sine 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Plot 0
Amplitude
40000 30000 20000 10000 0 -10000 -20000 -30000 -40000
0 50 100 150 200 250 300 350 400 450 500 550
Time
Channel
CH1
Block size
512

ADC Pro


ADCPro
File EVM Test Help
Acquire
Continuous
Data recorder
Ready
File
Length
2048
samples
Channel 1
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Sine 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Channel 2
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Triangle 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Channel 3
Max code Fs Min V Max V Waveform Rsln
32767 44100 -15 15 Square 16
Min code
Frequency
Amplitude
-32768
10 100 1k 22.1k -150 -100 -50 0
Multichannel Scope
Amplitude (dB)
15 12.5 10 7.5 5 2.5 0 -2.5 -5 -7.5 -10 -12.5 -15 -17.5
0 50 100 150 200 250 300 350 400 450 500 550
Sample
Plot Legend
CH1
CH2
CH3
Block size
512
Vertical Scale
Range
FSR
Auto
Units
Codes
Volts

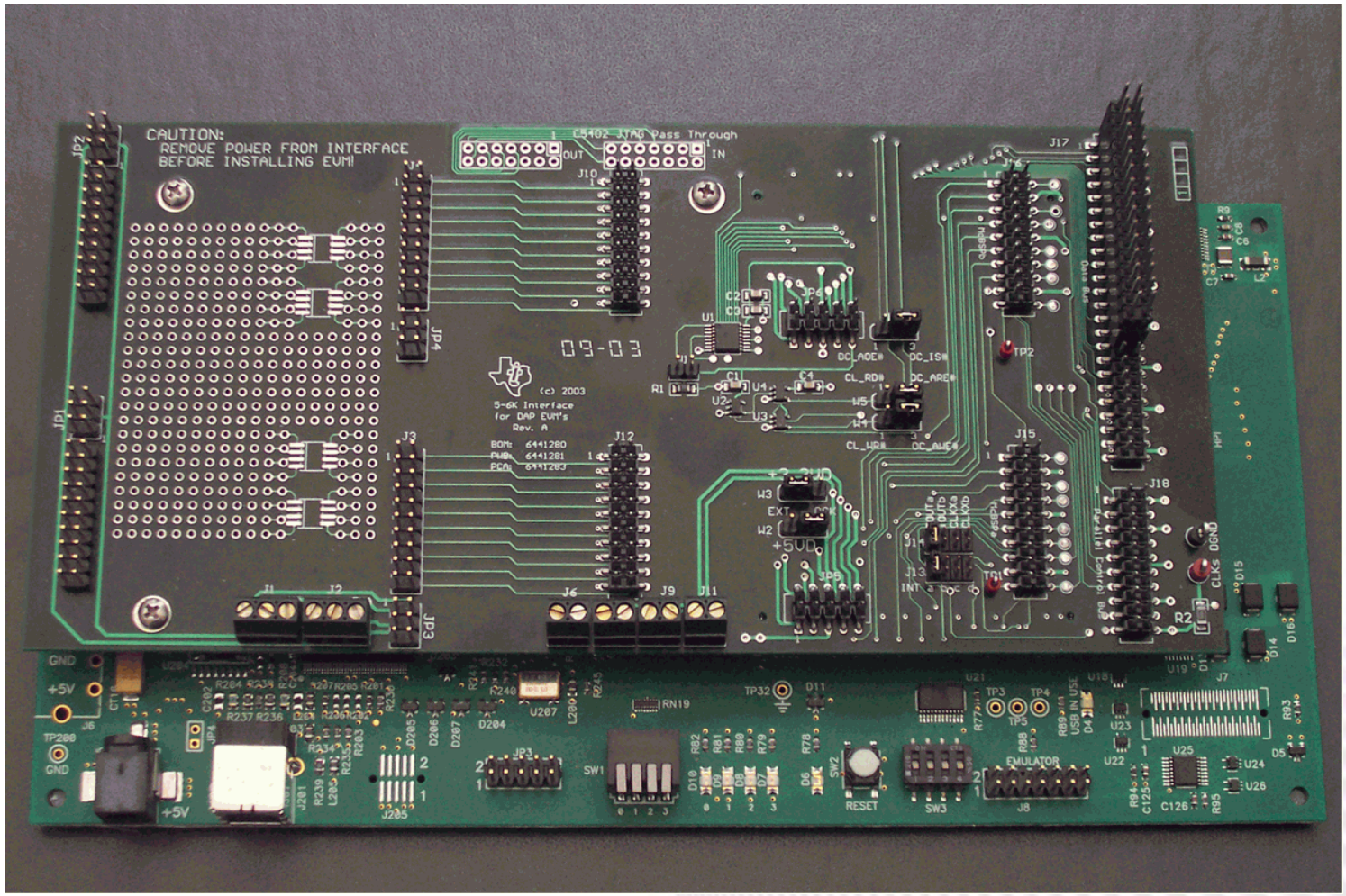
Writing Application Code

- Code Composer Studio IDE
  - Application design, code and build, debug
  - TMS320 and TMS470
- Code Composer Essentials
  - C compiler, assembler and linker
  - MSP430 ultra-low-power controllers
- IAR Embedded Workbench
  - IDE for embedded applications
  - MSP430 and TMS470

Code-Generation Tools

- Data converter “plug-in” tool for CCS
- Supports:
  - ADCs
  - DACs
  - CODECs
  - AMC
  - PCM

TMS320C6713 Hardware



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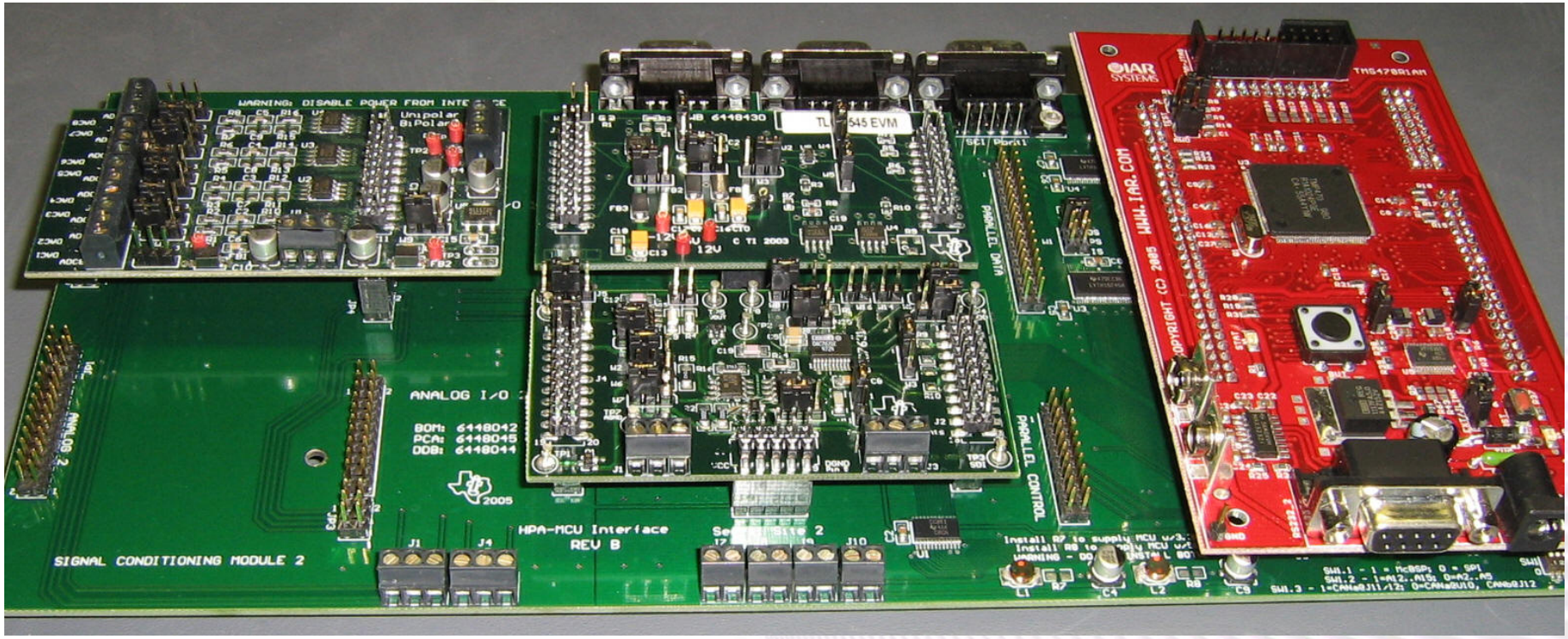
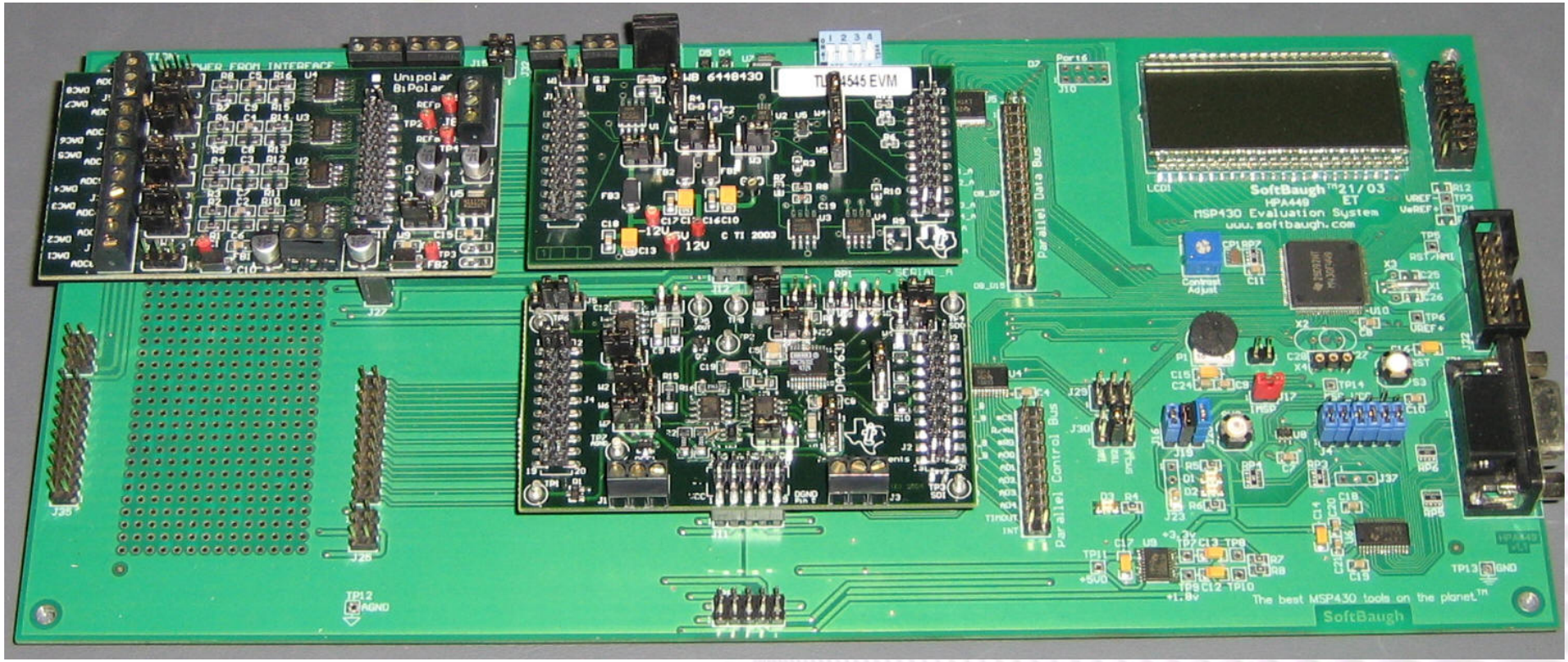
TMS470R1B1M Hardware



MSP430F449 Hardware



TI Developer Conference
March 7-9, 2007 • Dallas, TX

Minds in Motion

Evaluating Circuit Sensitivity in Analog Filters

Session ID: S284574

Wednesday at 4:10 p.m.

Mark Fortunato
Texas Instruments, Inc.

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Real World Analog Solutions for Your Processor Applications

Session ID: S283976
Thursday at 4:10 p.m.

Bonnie Baker
Texas Instruments, Inc.

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Data Converter Basics

How to Use and Test Data-Acquisition Products

Tom Hendrick
t-hendrick@ti.com

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