TEXAS INSTRUMENTS

Power Supply Design Seminar

Constructing your power supply - layout considerations

John Dorosa

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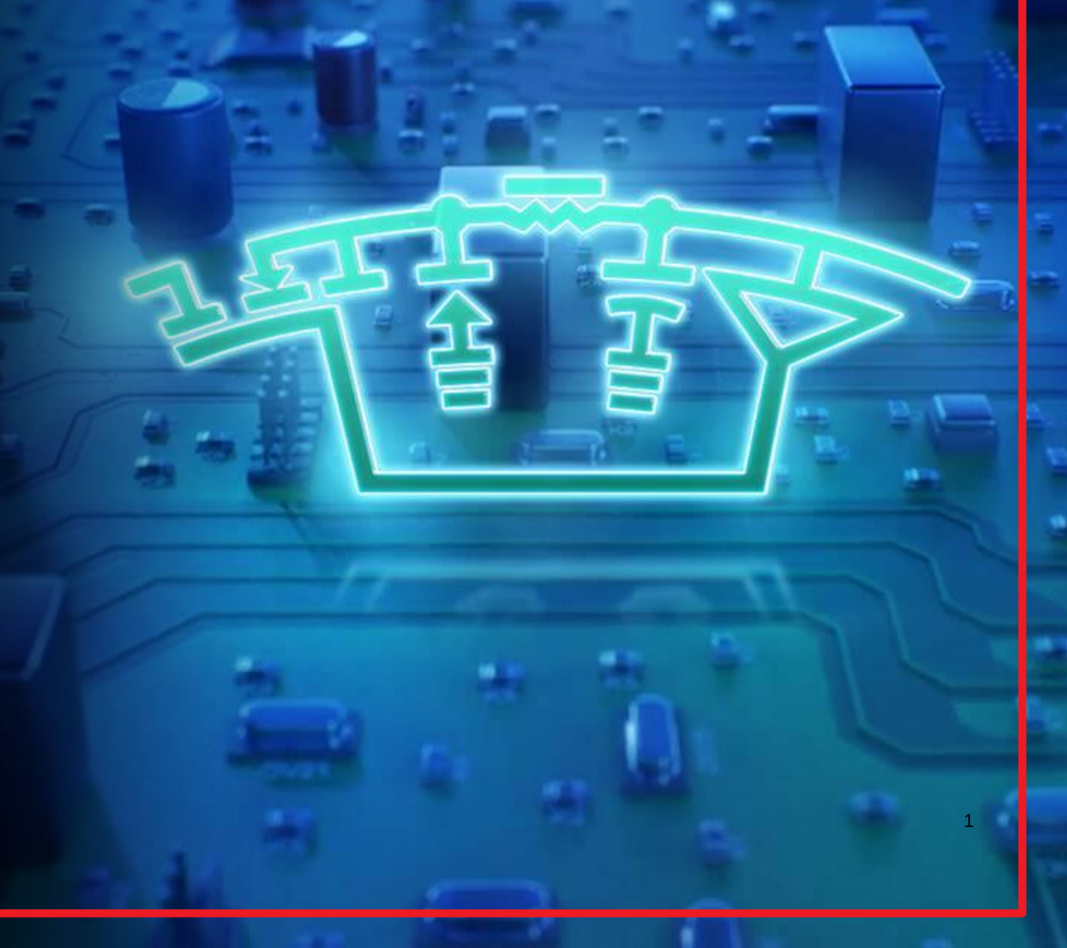

Agenda

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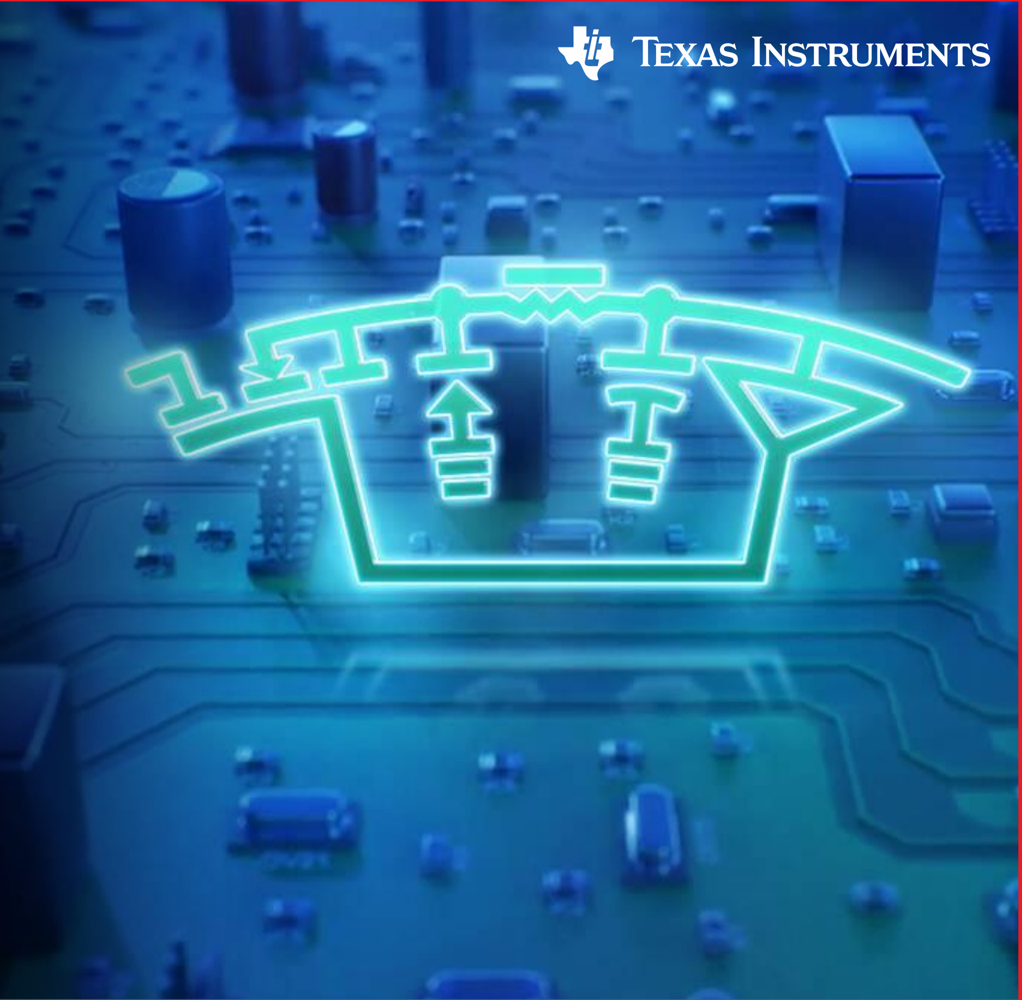
Introduction

Feature presentation

Live Q&A session

Enter questions into chat at any time



2025 Power Supply Design Seminar

Texas Instruments

Webinar Series

April 30	Common mistakes in DC/DC converters and how to fix them
May 28	Survey of resonant converter topologies
June 25	Power Factor Correction (PFC) circuit basics
July 30	Power-conversion techniques for complying with automotive emissions requirements
August 27	Switch-mode power converter compensation made easy
September 24	**Constructing your power supply – layout considerations**

Last Wednesday of every month
8:00AM & 8:00PM (US Central Time Zone)

Welcome to the PSDS 2025 webinar series!

Texas Instruments

The history of Power Supply Design Seminar

- In 1977 Bob Mammano, the "Father of PWM Industry," started the seminar
- 47+ years
- 26+ seminars
- 100+ technical topics
- 50,000+ customers
- A comprehensive archive of white papers, presentations and videos

Power supply industry legends associated with PSDS:
Bob Mammano, Lloyd Dixon, Bill Andreycak, Robert Kollman, Laszlo Balogh

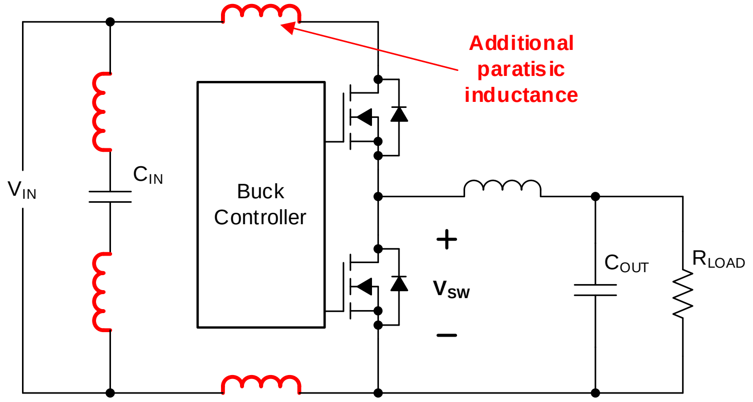
WWW.TI.COM/PSDS for all prior content

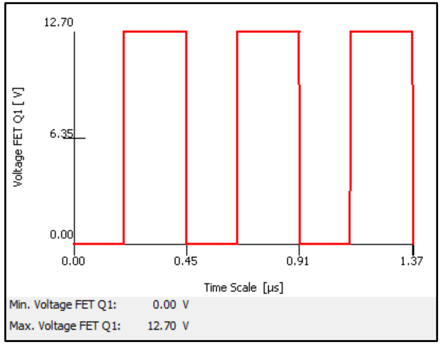
Agenda

- **DC Parasitics**
- AC Parasitics
- Grounds and Grounding
- Thermal Considerations

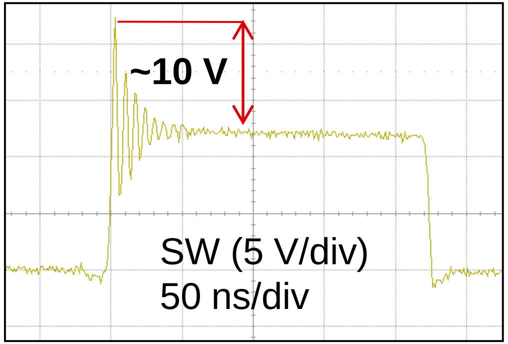
From schematic to PCB

- **Parasitic elements** (or parasitics)
  - Additional resistance, inductance and/or capacitance created from the physical construction of a component *(including the PCB itself!)*
  - Unintended effects:
    - Poor regulation
    - Lowered efficiency
    - EMI/ringing
    - Weak drive signals
    - Noise coupling
    - Instability





Nominal V_{SW} stress



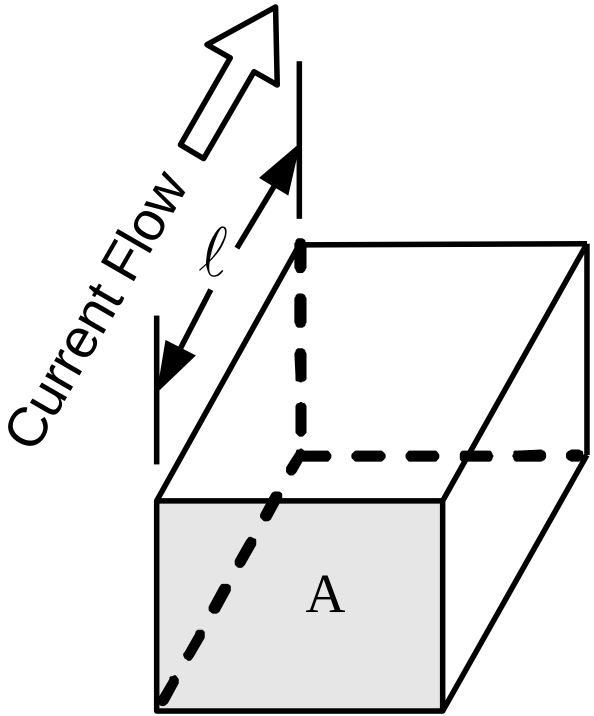
Measured V_{SW} stress

DC parasitics (resistance)

- ***You mean copper is not a perfect conductor?***
- Since it is not, it impacts
  - Regulation
  - Efficiency
  - Temperature rise

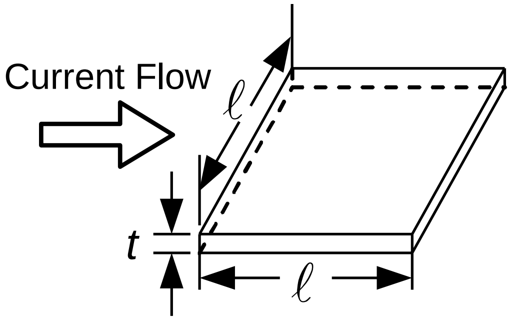
$$R = \frac{\rho \times l}{A}$$

  - Where ρ is resistivity of material
    - Copper = 17 µΩ·mm
    - Copper plating = 60 µΩ·mm



Count squares to estimate trace resistance

- Setting width = length:

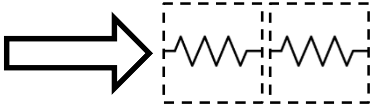


$$R = \frac{\rho \times l}{t \times l}$$

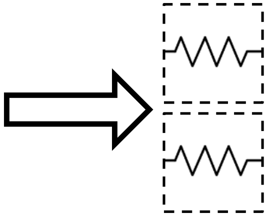
$$\boldsymbol{R = \frac{\rho}{t}}$$

- Simplifies analysis by counting squares in series or in parallel

$$R_{series} = n \cdot R$$



$$R_{parallel} = \frac{R}{n}$$



Copper weight (oz)	Thickness (mm)	mΩ per square (25°C)	mΩ per square (100°C)
1/2	0.02	1.0	1.3
1	0.04	0.5	0.65
2	0.07	0.2	0.26

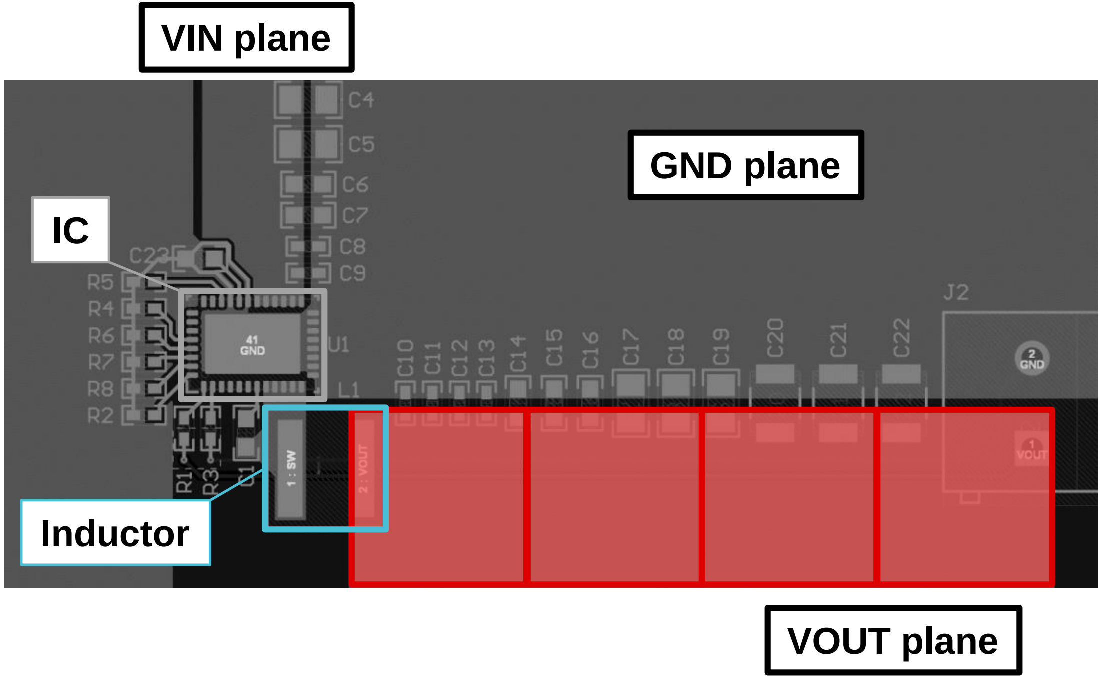
Counting squares example

- Synchronous buck converter
  - 1V output, 25A max loading
  - 1oz. copper layers
- Estimating four squares between inductor and output connector:

$$R_{plane} = n \cdot R_{1oz.cu}$$
$$R_{plane} = 4 \cdot 0.5m\Omega$$
$$R_{plane} = \mathbf{2m\Omega}$$

- At max loading:

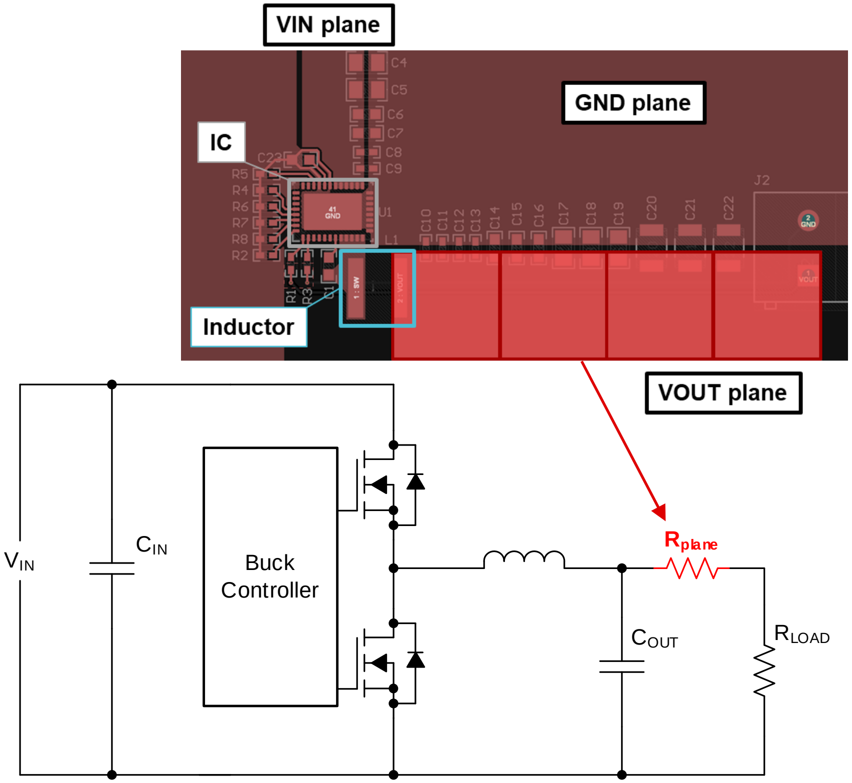
$$V_{drop} = I_{load} \cdot R_{plane}$$
$$V_{drop} = 25A \cdot 2m\Omega$$
$$V_{drop} = 50mV$$



5% regulation drop across load

Impacts of additional voltage drops

- Plane adds resistance between the inductor and load
  - Increases conduction loss
  - Can impact regulation at heavy load
  - Duty cycle will be wider than expected
- **Minimize resistance** for high current DC planes
  - Increase width as much as possible
  - Use thicker copper for power planes
  - Stitch multiple layers with vias



Vias have resistance too

- Same base equation:

$$R = \frac{\rho \times l}{A}$$

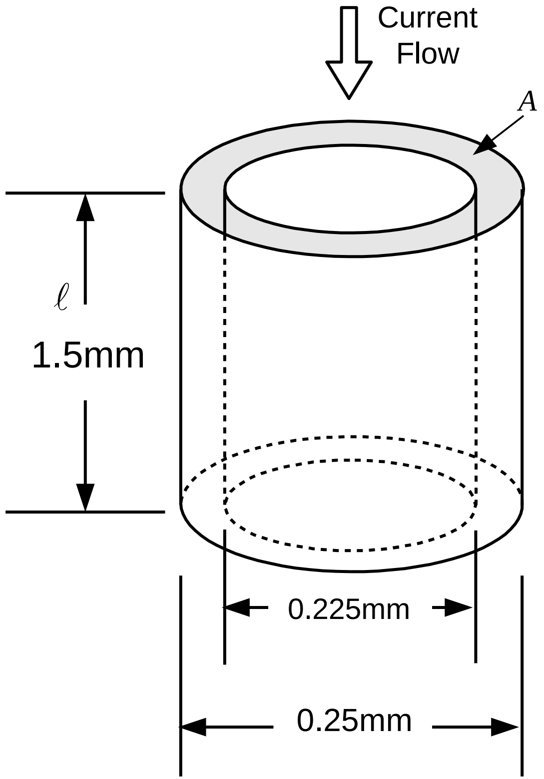
$$R = \frac{\rho \times l}{\pi(r_o^2 - r_i^2)}$$

- Using resistivity for copper plating

$$R = \frac{(60 \times 10^{-6}) \times 1.5}{\pi(0.25^2 - 0.225^2)}$$

$$\boldsymbol{R = 2.4m\Omega}$$

- *Note: include resistivity of filler material if used to lower resistance*



Agenda

- DC Parasitics
- **AC Parasitics**
- Grounds and Grounding
- Thermal Considerations

Parasitic inductance

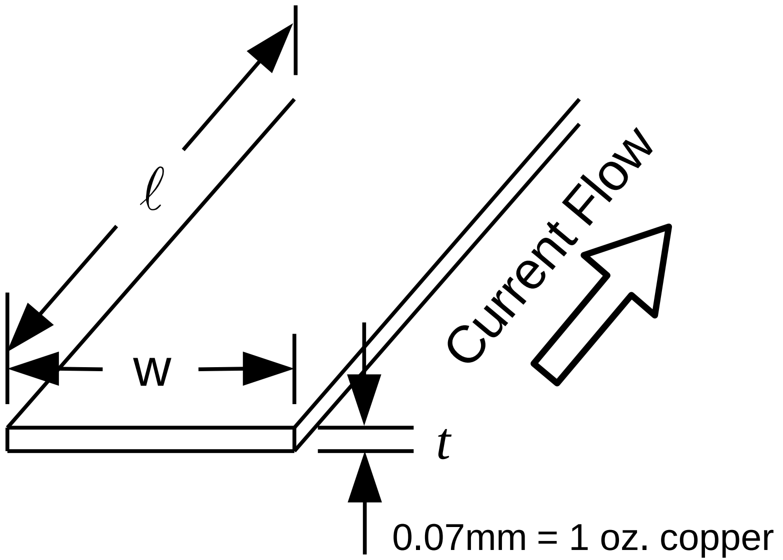
- Assuming free-space, the self inductance of copper traces:

$$L = 2l\left(ln\left(\frac{l}{t+w}\right)+\frac{1}{2}\right)nH$$

Where l is trace length in cm

w (mm)	T (mm)	Approximate Inductance (nH/mm)
0.25	0.07	1.0
2.5	**0.07**	**0.6**
12.5	0.07	0.2

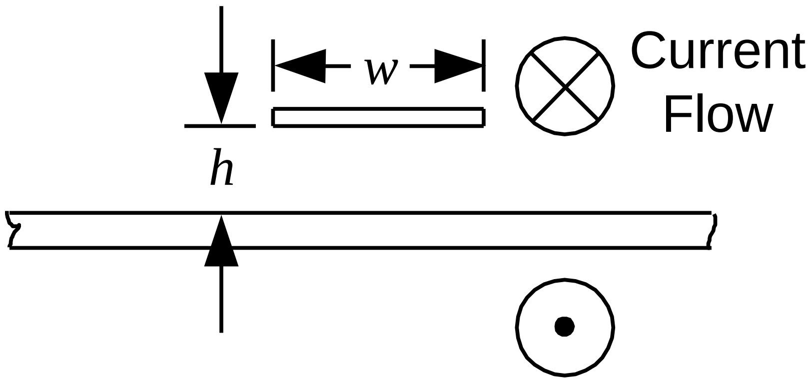
Note, large changes in width needed to see impact on inductance



PCB traces over ground planes

- Assuming a loop formed by a trace over an infinitely wide plane:

$$L = \frac{2hl}{w} nH/cm$$

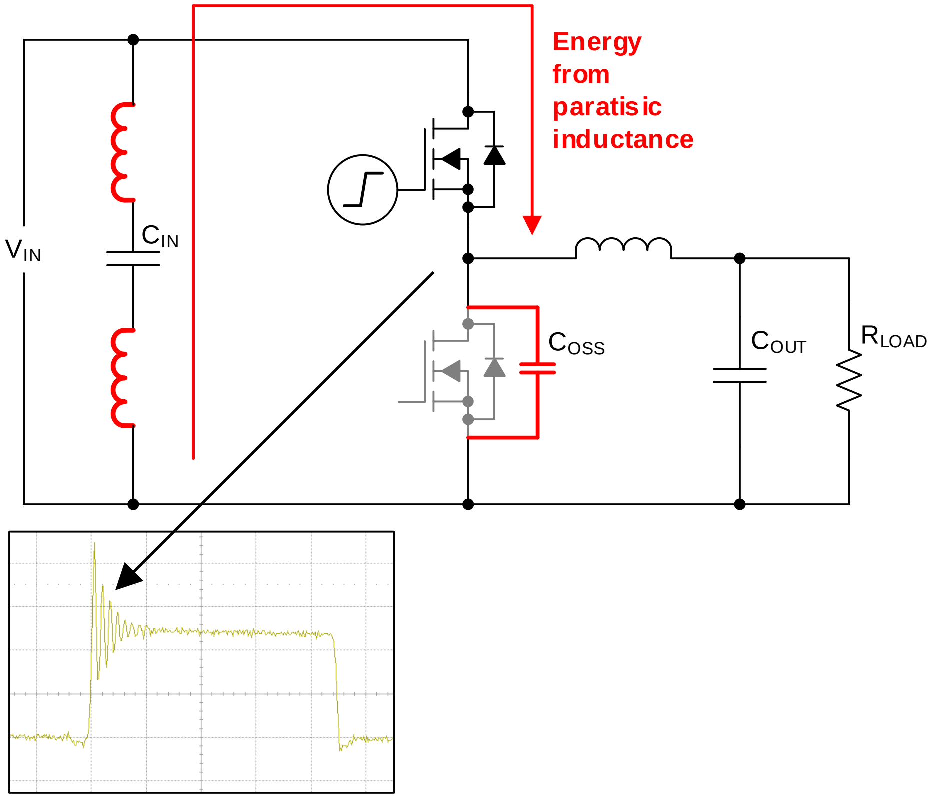


h (mm)	w (mm)	Inductance (nH/cm)
0.2	0.5	0.8
0.2	**2.5**	**0.16**
1.0	2.5	0.8

- Wide ground planes for return paths!
  - Reduction in inductance per length
  - **Proportional relationship** between inductance, length, width and height
- PCB core is typically thicker than prepeg layers

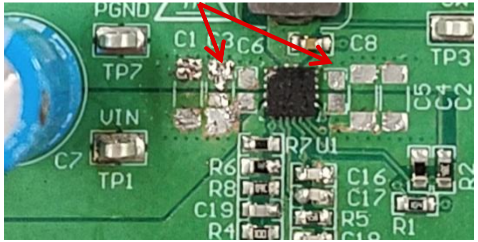
Loop inductance in buck power stage

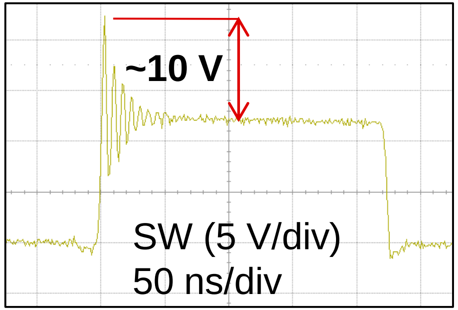
- High di/dt loop formed by FETs and input capacitor of buck converter
- Energy caught in parasitic inductance shows up as ringing at transitions
- Actual voltage stress seen by FET may be higher than expected!



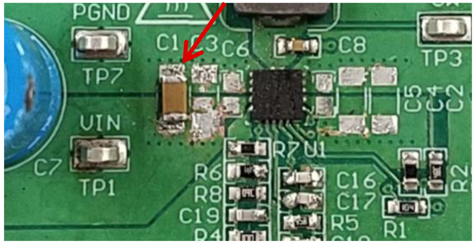
Closer C_{IN} placement, less L_{PAR}

No nearby input caps

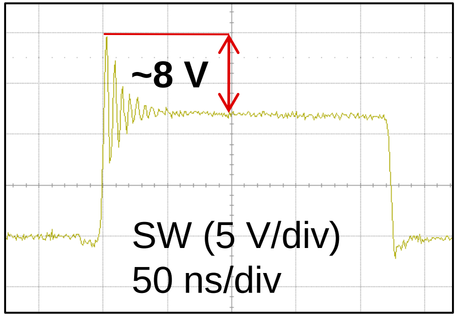




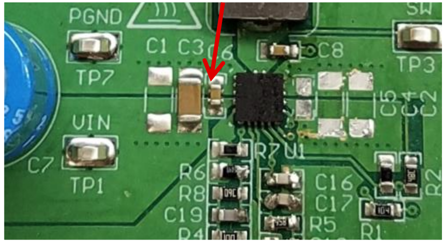
One far input cap



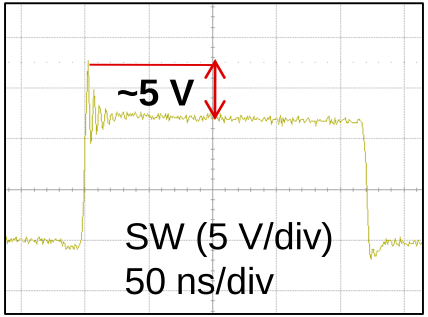
10 µF, 1206



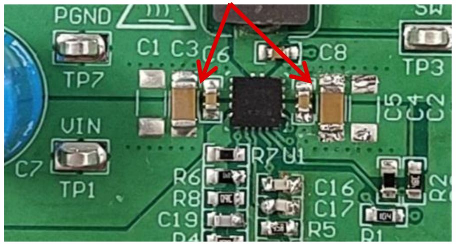
Two close caps



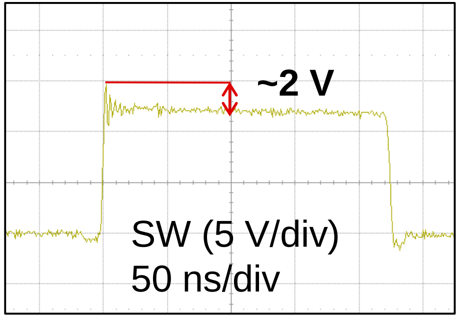
10 µF, 1206
0.1 µF, 0603



Two-sided, close caps



2 x 10 µF, 1206
2 x 0.1 µF, 0603



Parasitic capacitance

- Mutual capacitance of two planes:

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{l}$$

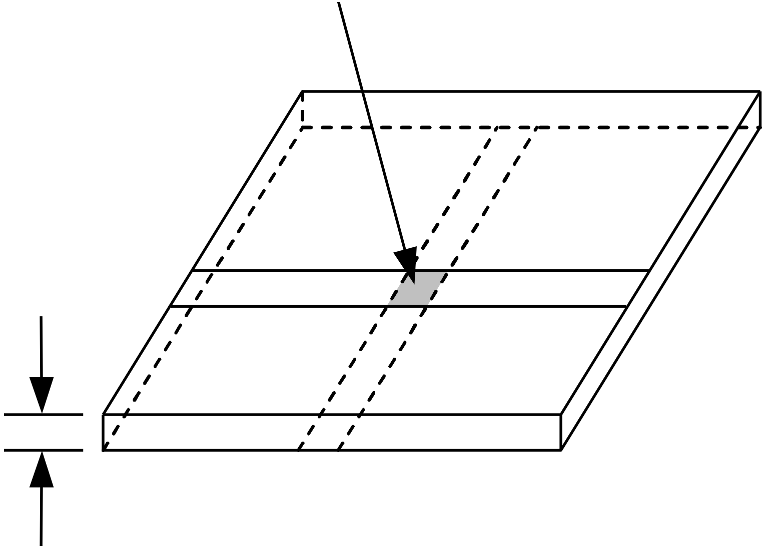
  - Where ε is material permittivity

- Two 0.25mm traces intersecting on adjacent layers, 0.25mm apart:

$$C = \frac{3.93 \times 10^{-14} \times 0.25^2}{0.25}$$

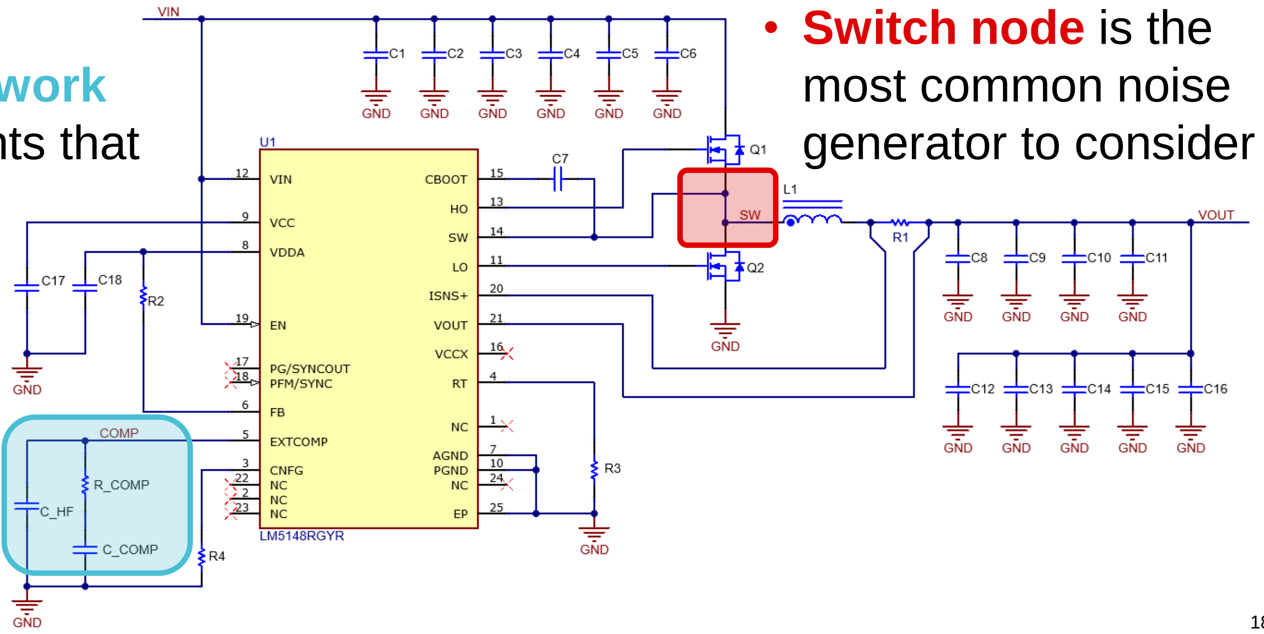
$$\boldsymbol{C = 0.01pF}$$

- Intersecting at 90º angles minimizes capacitance between adjacent traces



Identify sensitive and noisy nodes

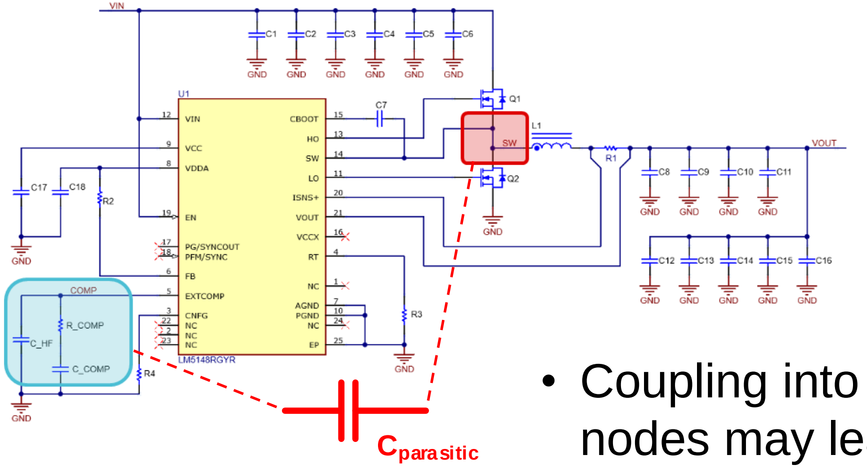
- Connections to high-impedance nodes are susceptible to noise
- Example **COMP network** has many components that may introduce large parasitic capacitance
- 5x pads can add at least 1pF to node



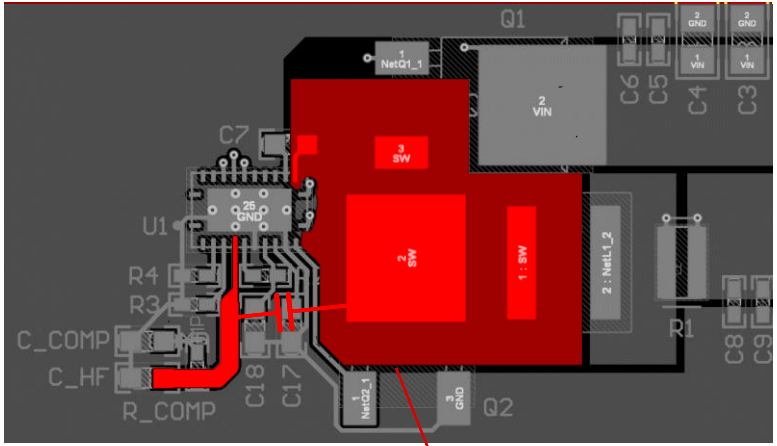
- Noise is generated by dV/dt nodes
- **Switch node** is the most common noise generator to consider

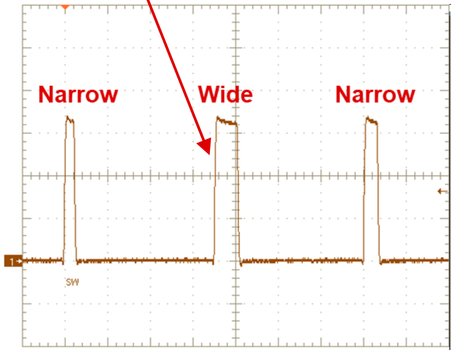
Chaos created by noise injection

- Large copper planes and close proximity increase parasitic capacitance



- Coupling into sensitive nodes may lead to unexpected instability





Agenda

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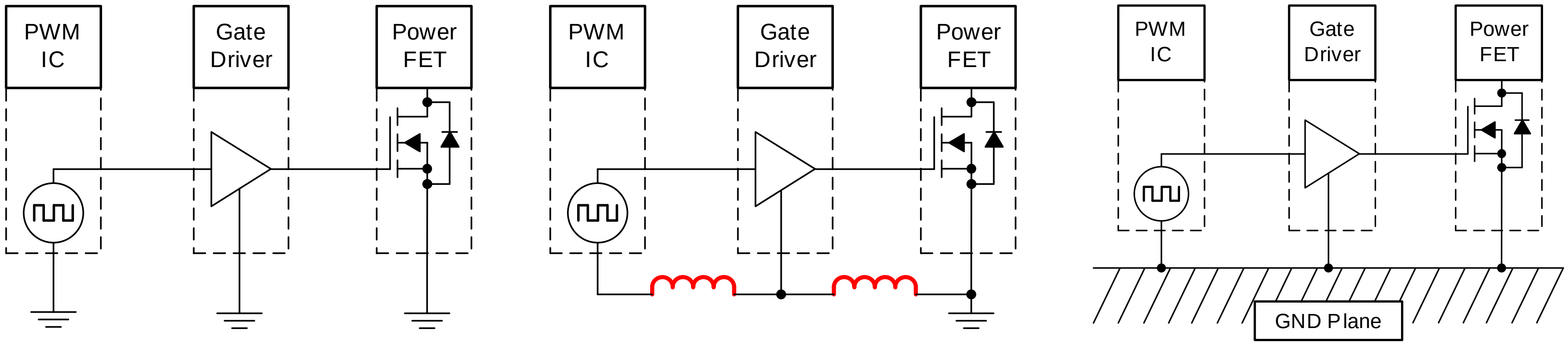
- AC Parasitics
- **Grounds and Grounding**
- Thermal Considerations

Ground and grounding



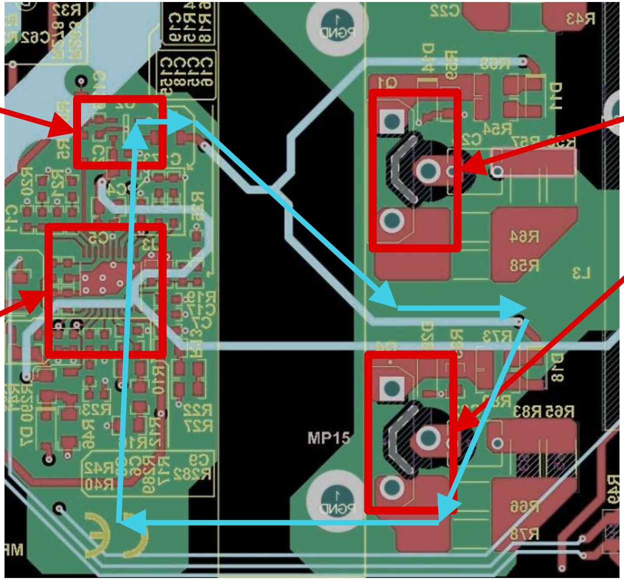
- Many components in a system connect electrically to ground
- Ground connections generate parasitics like any other trace
  - Increased inductance, susceptible to noise, slower di/dt
- Large ground plane
  - Provides low impedance between circuits
  - Minimize potential differences

Planning return paths

- Overlapping loops can lead to signals interfering with each other
  - Example: gate driver placed far away from Power FET
  - Return path of gate drive spans PCB

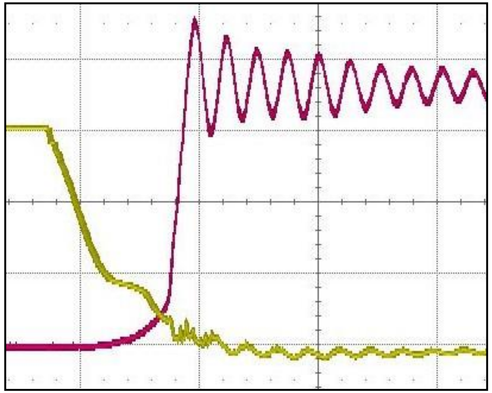
Gate Driver

PWM IC



Power FETs

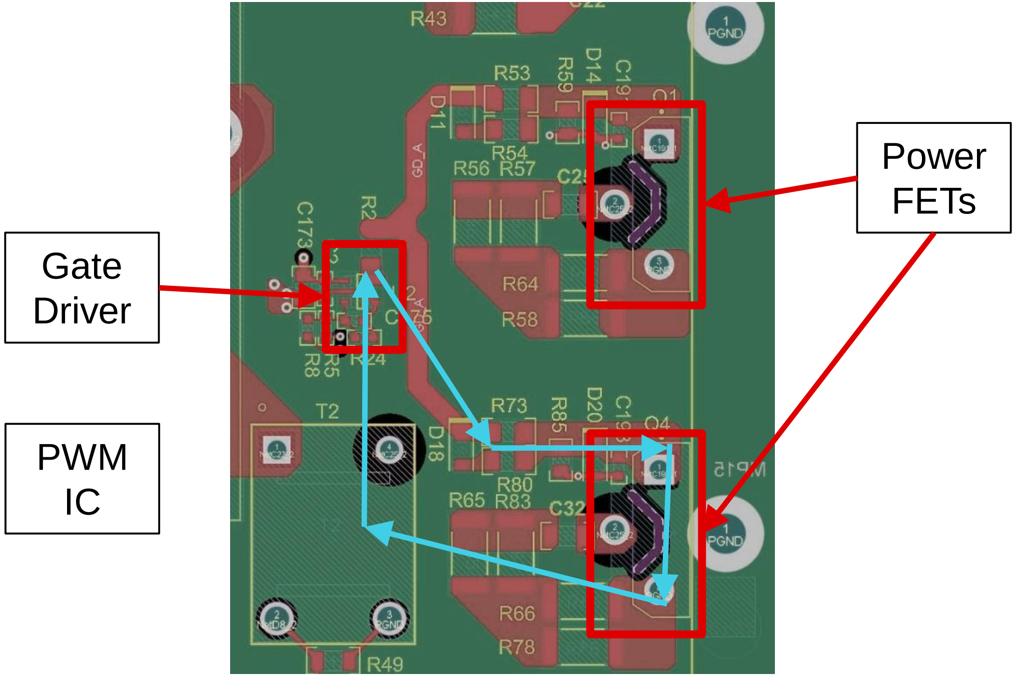
Switch node
Excessive ringing



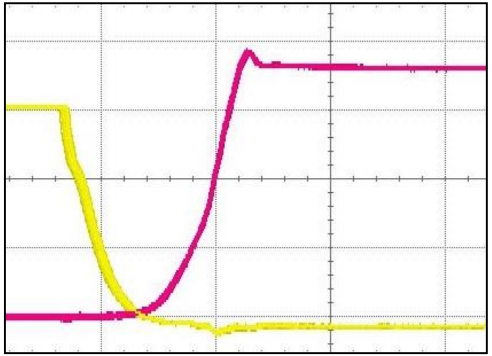
FET Vgs
Notch in waveform, poor driver performance

Reduce overlap of current loops

- Minimizing return path for gate drive
  - Goal is to contain high di/dt within power circuits and away from sensitive areas



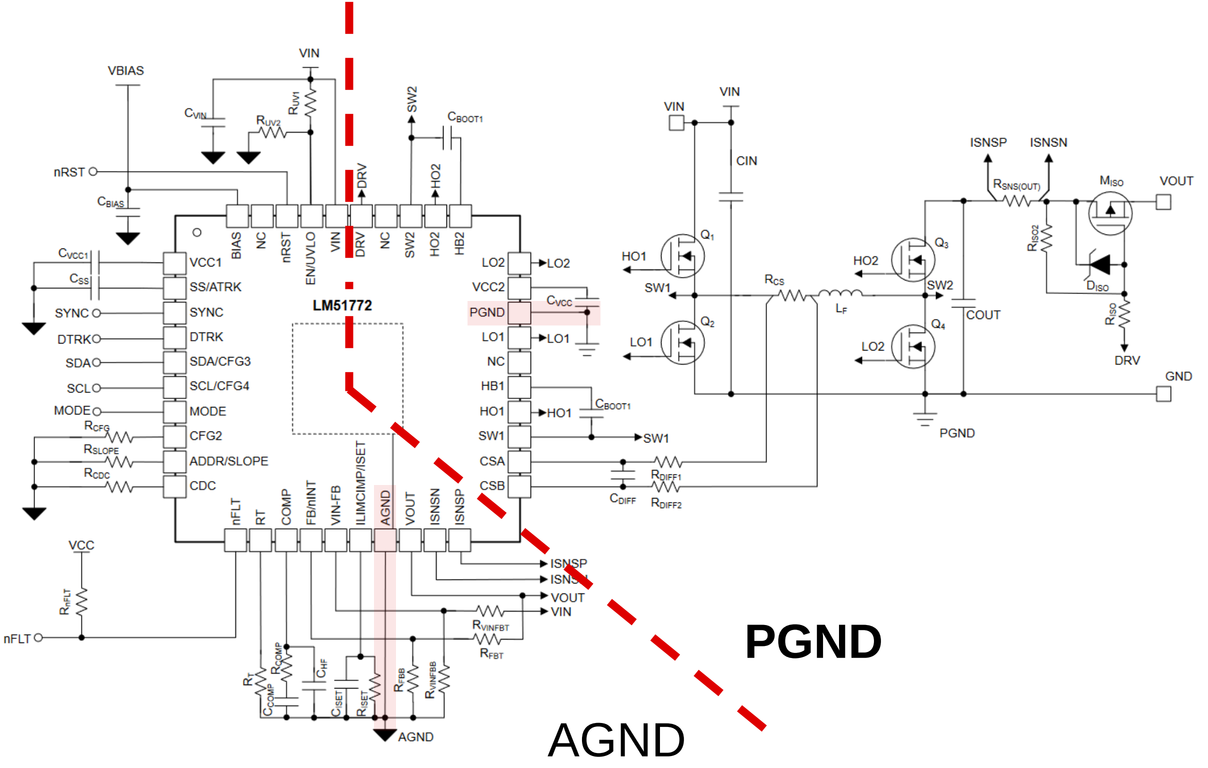
Switch node
Less ringing



FET Vgs
Clean drive signal

Partitioning circuits

- Many control IC's plan pin out to separate noisy/quiet circuit areas
  - Some provide separate power and analog ground pins
  - Refer to specific datasheet for guidelines
- Good practice plans layout around pin out and return path



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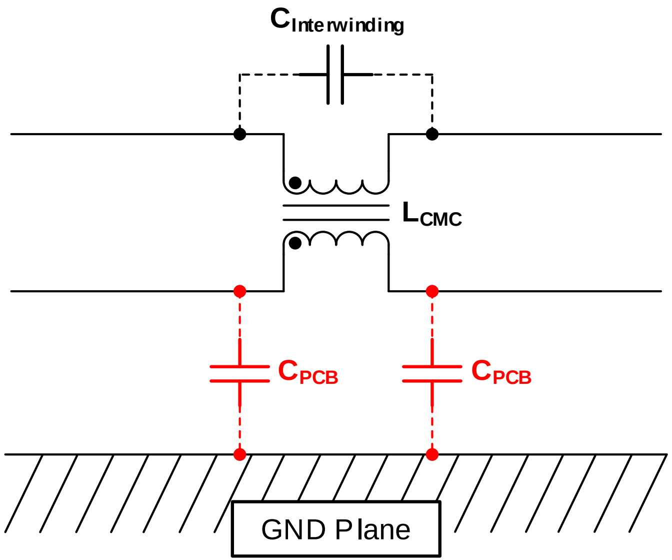
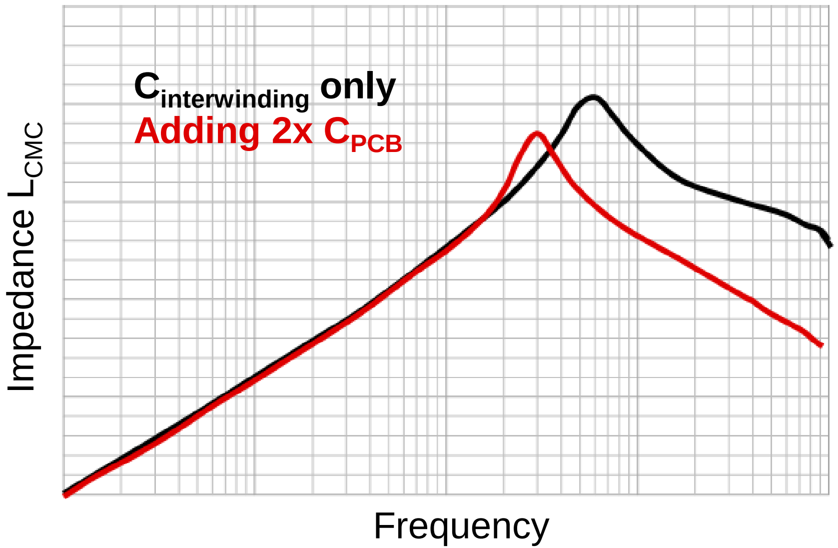
Ground plane drawbacks

- Large copper pours may introduce more parasitic capacitance
  - Common chokes are susceptible



- C_{PCB} from a large plane is often larger than $C_{interwinding}$
  - – Lowers effective self-resonant frequency



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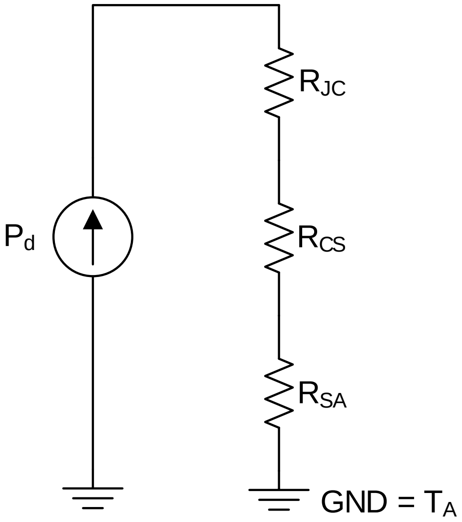
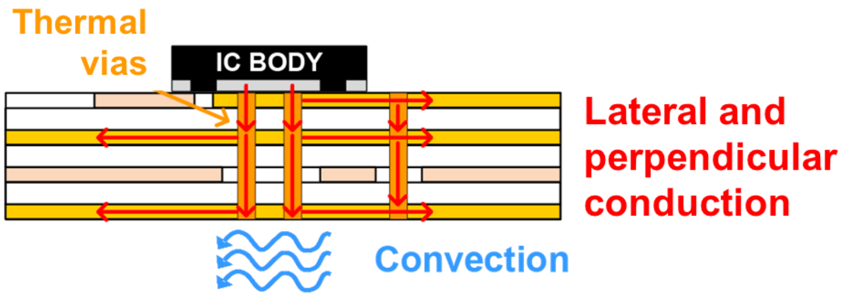
- **Thermal Considerations**

Thermal considerations

- Power dissipation can be modeled as a current source
- Conduction and convection paths form the thermal resistances
  - **R_{JC}**: Junction to case thermal resistance
  - **R_{CS}**: Interface resistance, specified for heat sink insulators, negligible for solder
  - **R_{SA}**: Sink to ambient resistance, specified for heatsinks
- Temperature rise can be estimated as:

$$\Delta T = P_d \times (R_{JC} + R_{CS} + R_{SA}) + T_A$$



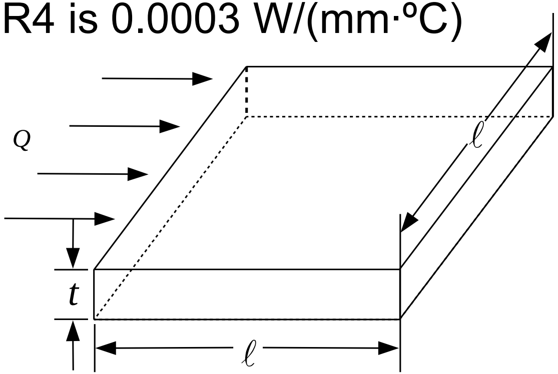


Lateral conduction

- Heat flow and thermal resistance akin to electrical current and resistance

$$R = \frac{l}{\sigma \times A}$$

  - Where σ is the material's thermal conductivity
    - Copper is 0.36 W/(mm·ºC)
    - FR4 is 0.0003 W/(mm·ºC)



- Using "counting squares" method:

$$R = \frac{l}{\sigma \times l \times t}$$

$$R = \frac{1}{\sigma \times t}$$

- For 2oz copper (t=0.07mm):

$$R = \frac{1}{0.36 \times 0.07}$$

$$\boldsymbol{R = 40ºC/W}$$

- For 1.57mm thick FR4:

$$R = \frac{1}{0.0003 \times 1.57}$$

$$\boldsymbol{R = 2,100ºC/W}$$

Break in copper plane

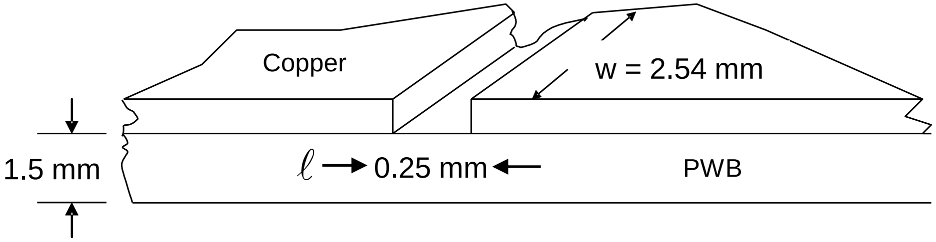
- Consider a cut in a copper plane:

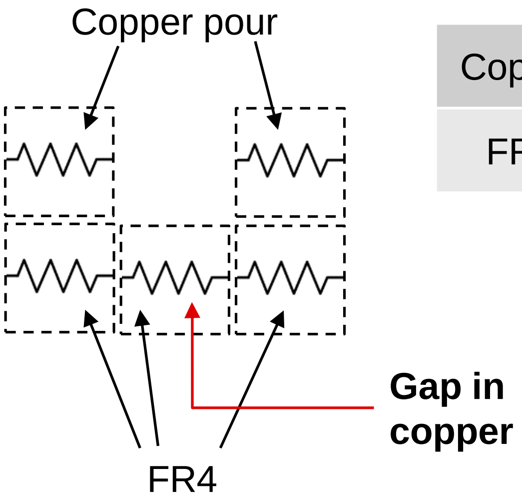
$$R = \frac{l}{\sigma \times w \times t}$$

$$R = \frac{0.25}{0.0003 \times 25.4 \times 1.5}$$

$$\boldsymbol{R = 23^{o}C/W}$$

- A thin cut added a significant amount of thermal resistance
- One way around this issue is to use buried planes on other layers to bridge the gap





Copper	$40^{o}C/W$ per square
FR4	$2,100^{o}C/W$ per square

Perpendicular conduction

- Conducting heat *through* PCB board
- Rearranging resistance equation:

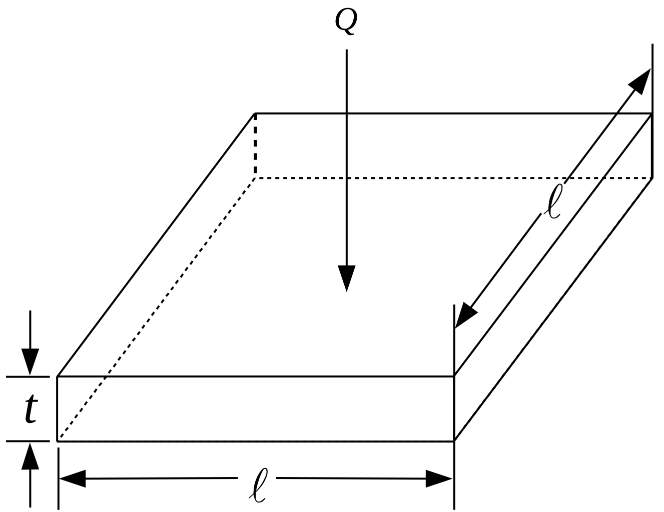
$$R = \frac{t}{\sigma \times l^2}$$

- For a 25mm × 25mm square of FR4:

$$R = \frac{1.57}{0.0003 \times 25^2}$$

$$\boldsymbol{R = 8.4ºC/W}$$

- Huge improvement over lateral conduction!
- Requires copper pour to cover a wide surface area to be effective



Thermal vias improve perpendicular conduction

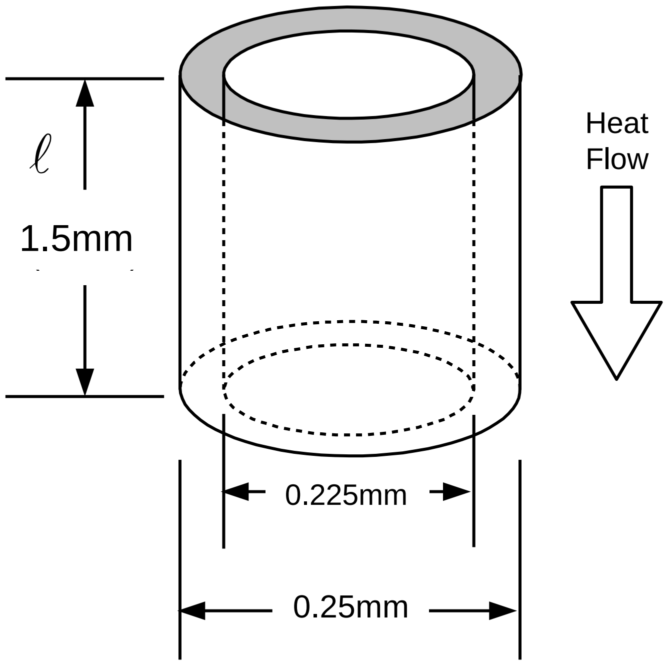
- For a via 0.5mm outer diameter, 0.45mm diameter hole

$$R = \frac{l}{\sigma \times \pi \times (r_o^2 - r_i^2)}$$

$$R = \frac{1.5}{(60 \times 10^{-6}) \times \pi(0.25^2 - 0.225^2)}$$

$$\boldsymbol{R = 100^{\circ}C/W}$$

- About 12 vias in parallel would **halve** the thermal impedance through PCB
- **Solder** filling or **plating** can further improve impedance



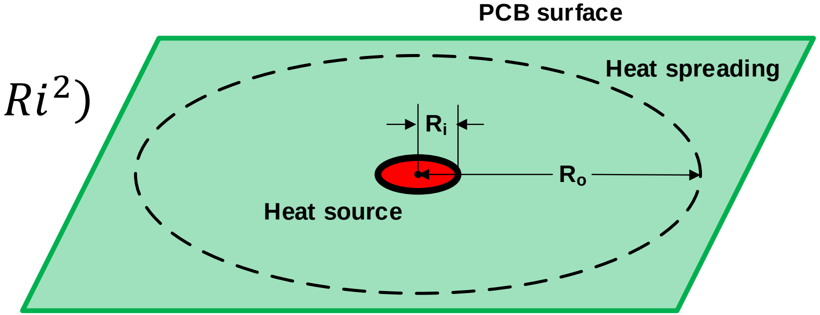
Heat dissipation

- [3] A simplified expression heat transfer considering typical conduction and convection in a PCB:

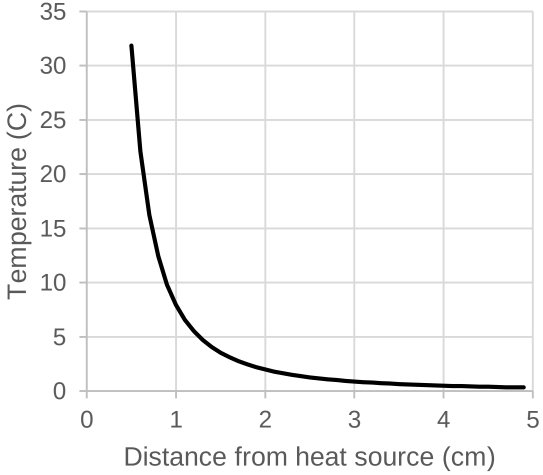
$$\Delta T = P_d^{0.8} \times \frac{K'}{A^{0.7}}$$

  - Where K' represents ability to transfer heat in mm^2·ºC/W
- A circular heat source on large copper plane:

$$A = \pi(Ro^2 - Ri^2)$$



- Plotting ΔT vs. Ro
  - Most of heat is close to component
  - Separation between multiple heat sources helps with overall cooling



Heat dissipates radially

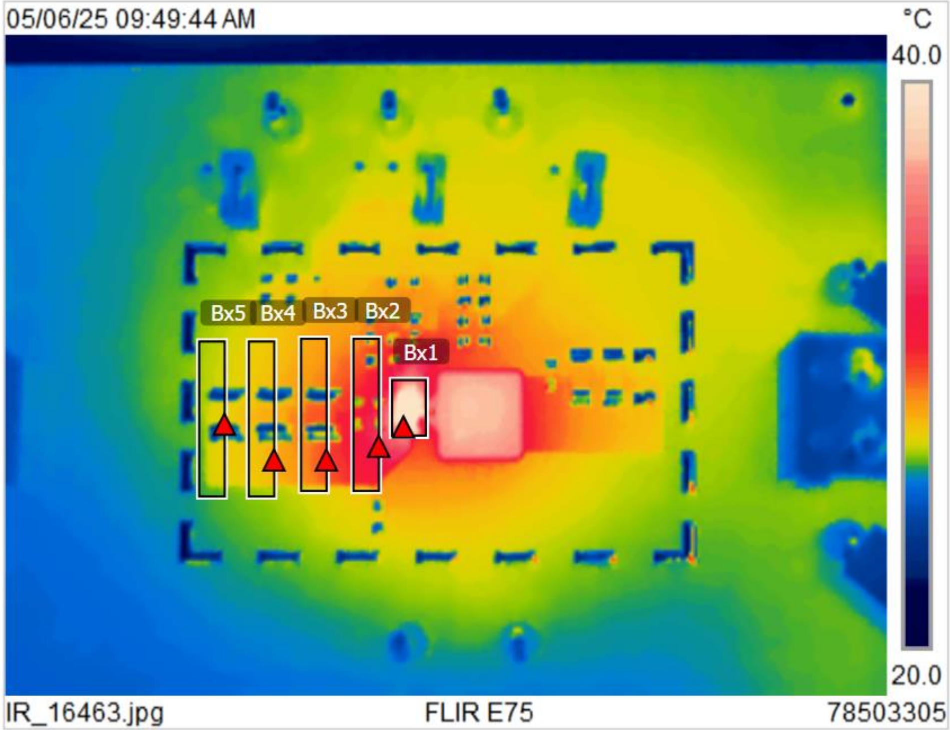
- 1W of power loss on a buck converter EVM
- Temperature rise drops off quickly away from converter

Measurements

Bx1	Max	53.2 °C
Bx2	Max	33.9 °C
Bx3	Max	30.3 °C
Bx4	Max	28.6 °C
Bx5	Max	27.9 °C

Parameters

Emissivity	0.95
Refl. temp.	20 °C

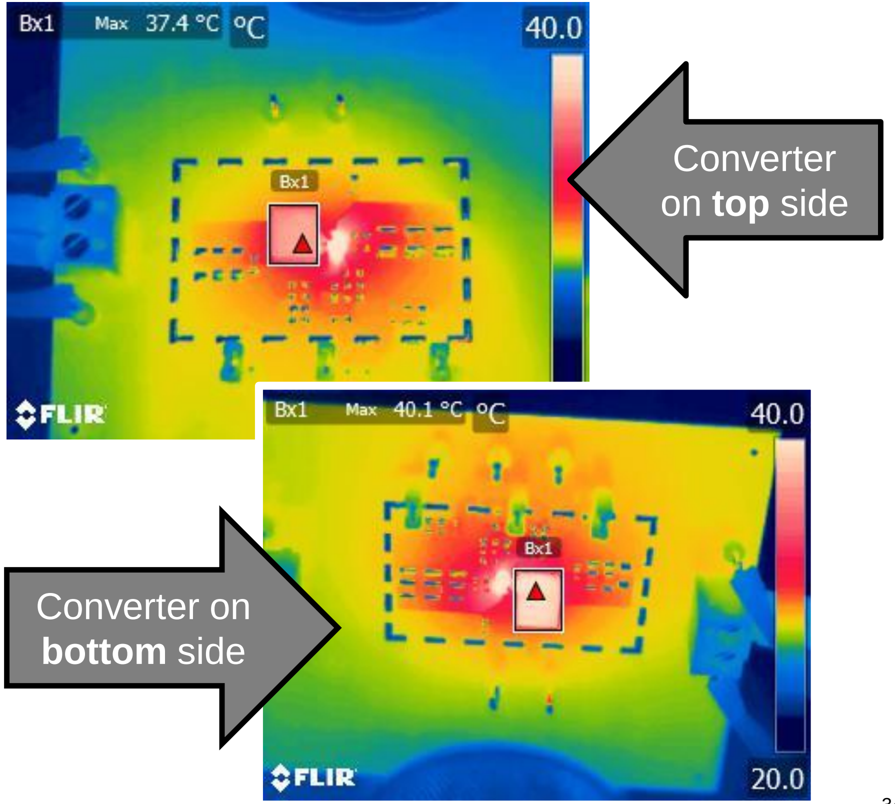


Orientation impacts passive convection

$$\Delta T = P_d^{0.8} \times \frac{K'}{A^{0.7}}$$

- Multiple factors considered in K’
- In a zero airflow environment, passive convection works to remove heat from PCB

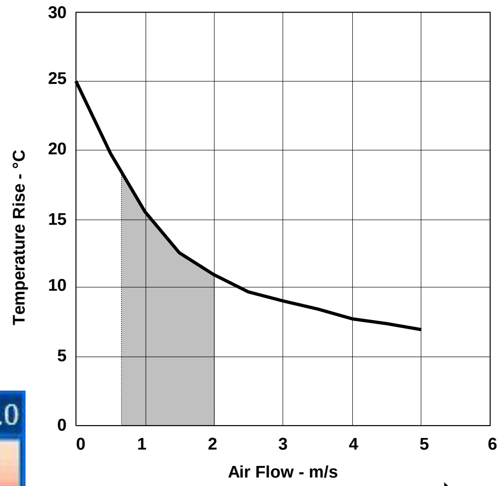
Surface orientation	K’
Vertical	650
Horizontal plane, top surface	675
Horizontal, bottom surface	1,375

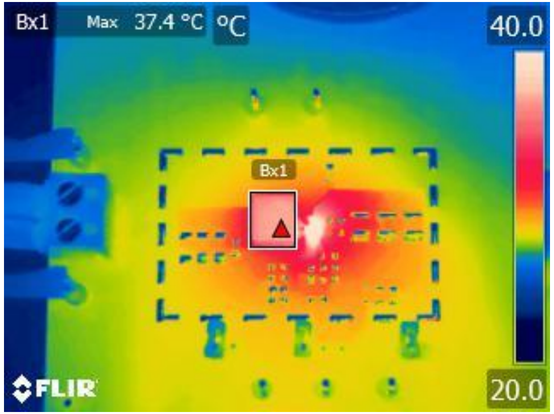


Texas Instruments

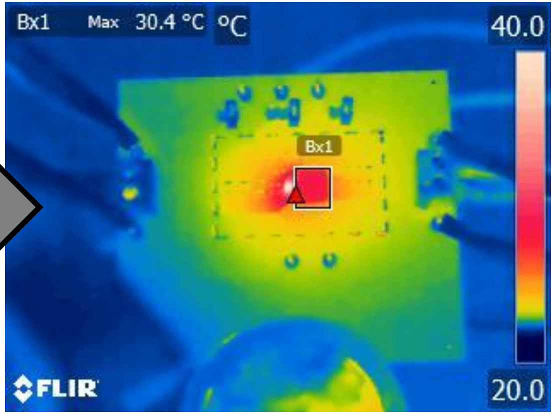
Even a whisper of air can reduce temperatures

- System airflow yields 20% to 60% drops in temperature rise





Same operating conditions, adding airflow



Texas Instruments

PCB cooling strategy

- Use **large copper planes** to distribute heat across PCB surface
  - Often runs opposed to noise reduction strategy
  - Maximize the thermal plane **wherever practical**
- Add **thermal vias** to carry dissipate though inner planes
  - Allows both sides of the board to cool
  - Provides substantial improvement over conducting through PCB
- Avoid having too many series impedances
  - **Breaks in planes** as they substantially degrade lateral heat flow
  - Buried planes can also improve the lateral heat flow

A good layout…

- **Makes for a successful design**
- Power supply layout is **as important** as any other design consideration
- The power supply engineer must be involved in parts placement and routing
- But it is not magic, it is an understanding of AC and DC parasitics, grounding, and cooling that makes a successful design

References

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4. IPC-2221A, *Generic Standard on Printed Board Design*, IPC, 2003
5. Abe Pressman, *Switching Power Supply Design*
6. Fredrick Grover, *Inductance Calculations, Working Formulas and Tables*, Dover, 1962
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Radiation heat transfer

- Heat flow due to radiation:

$$q = \sigma \times A \times F_{\varepsilon} \times F_{a} \times (T_1^4 - T_2^4)$$

- Where:
  - σ = constant
  - A = area
  - F_{ε} = emissivity factor
  - F_a = configuration factor
  - T = temperature °Kelvin
- In practice, **not an impactful way** to dissipate heat
  - Provides safety factor over convection calculations