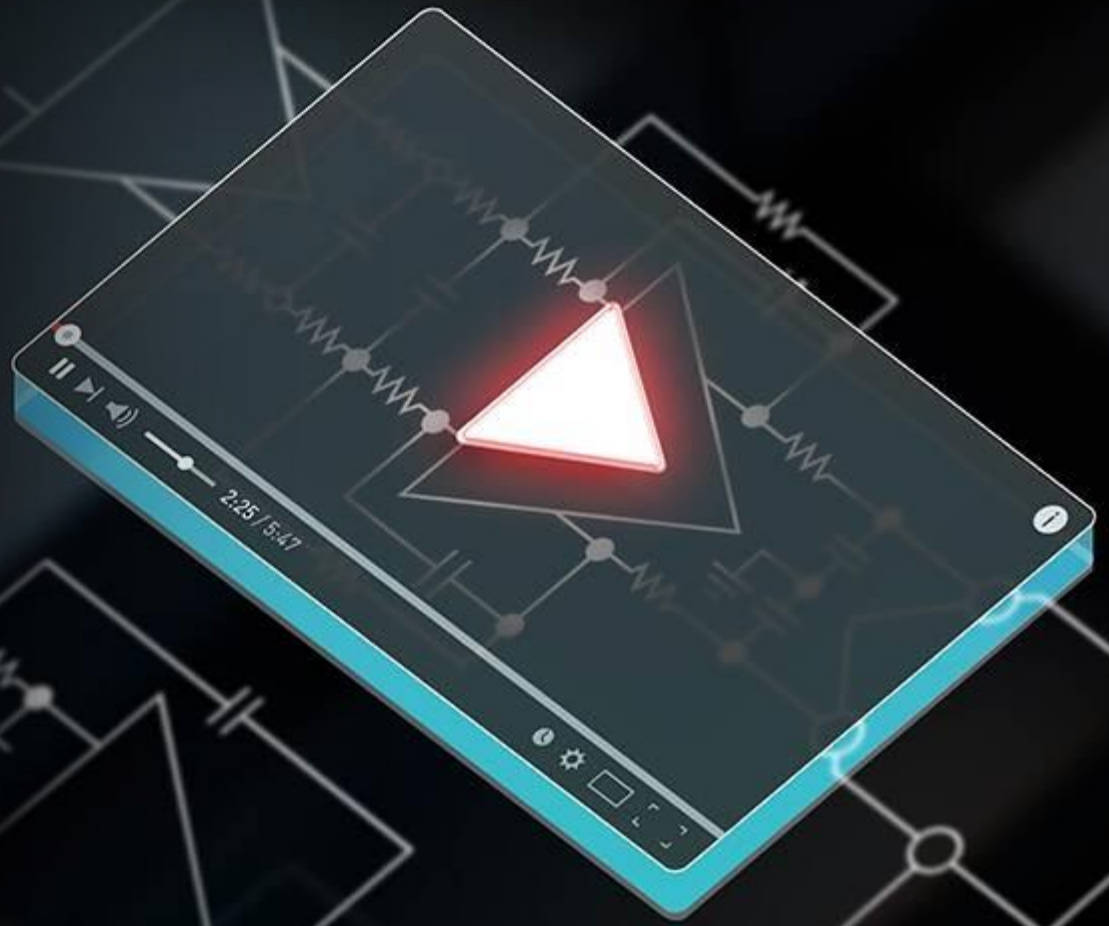
TI Precision Labs Seminar

Driving SAR and Delta-Sigma ADC Inputs

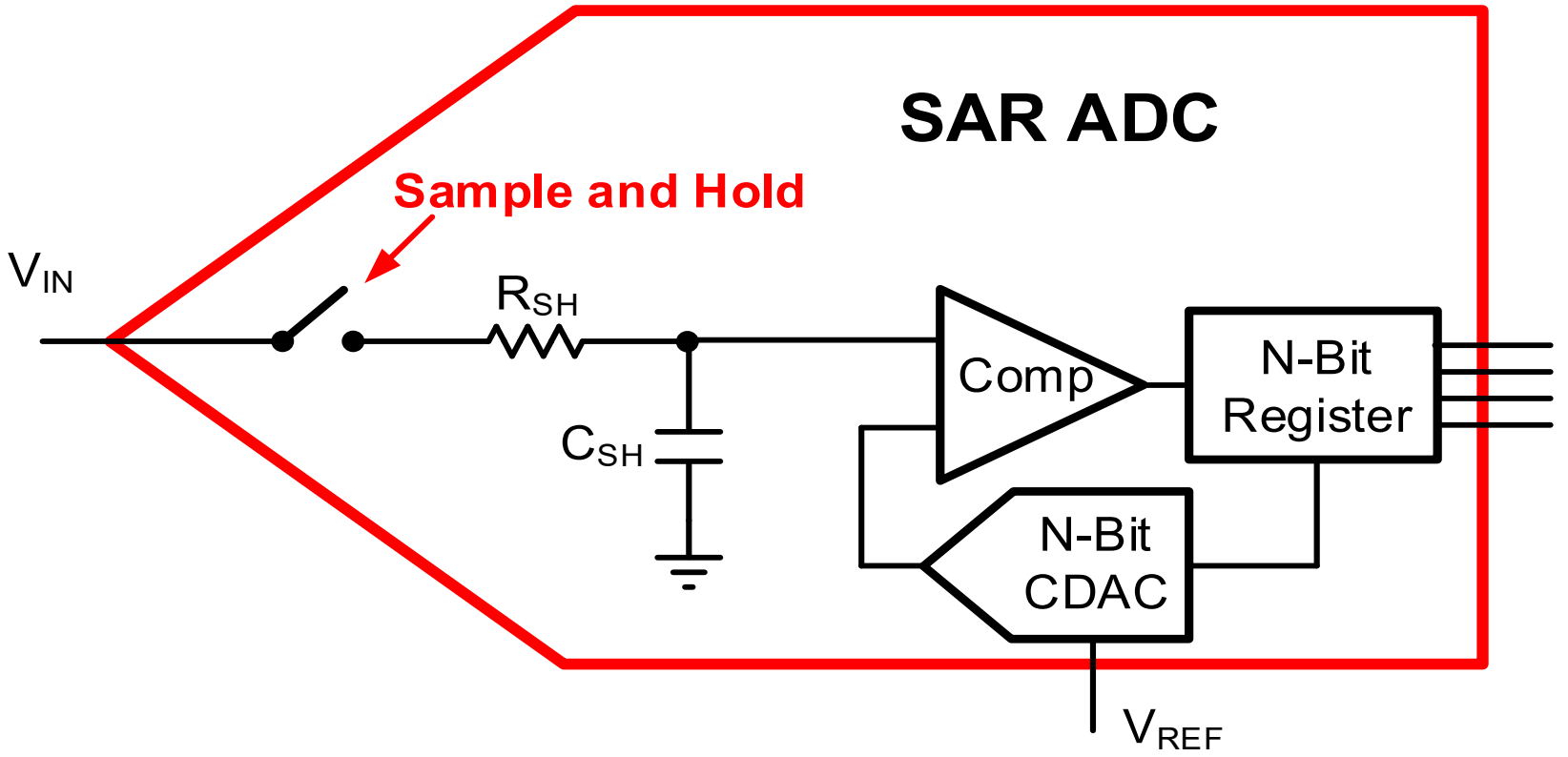


Objectives

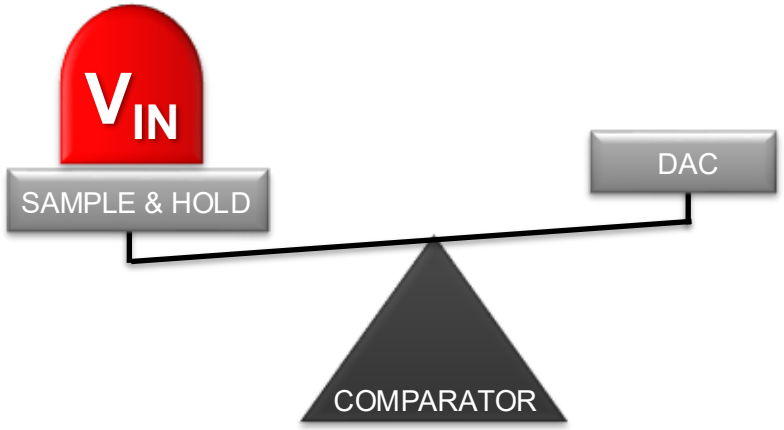
- Key considerations for driving a SAR ADC
  - RC charge bucket component selection
  - Driver op-amp need and selection
- Wideband Delta-Sigma ADC characteristics and input drive design considerations

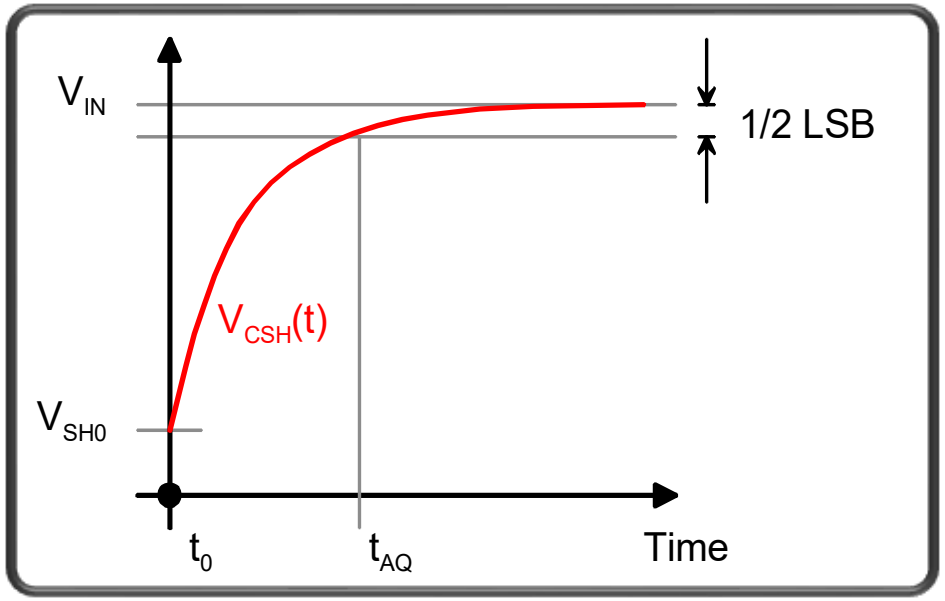
SAR ADC Drive

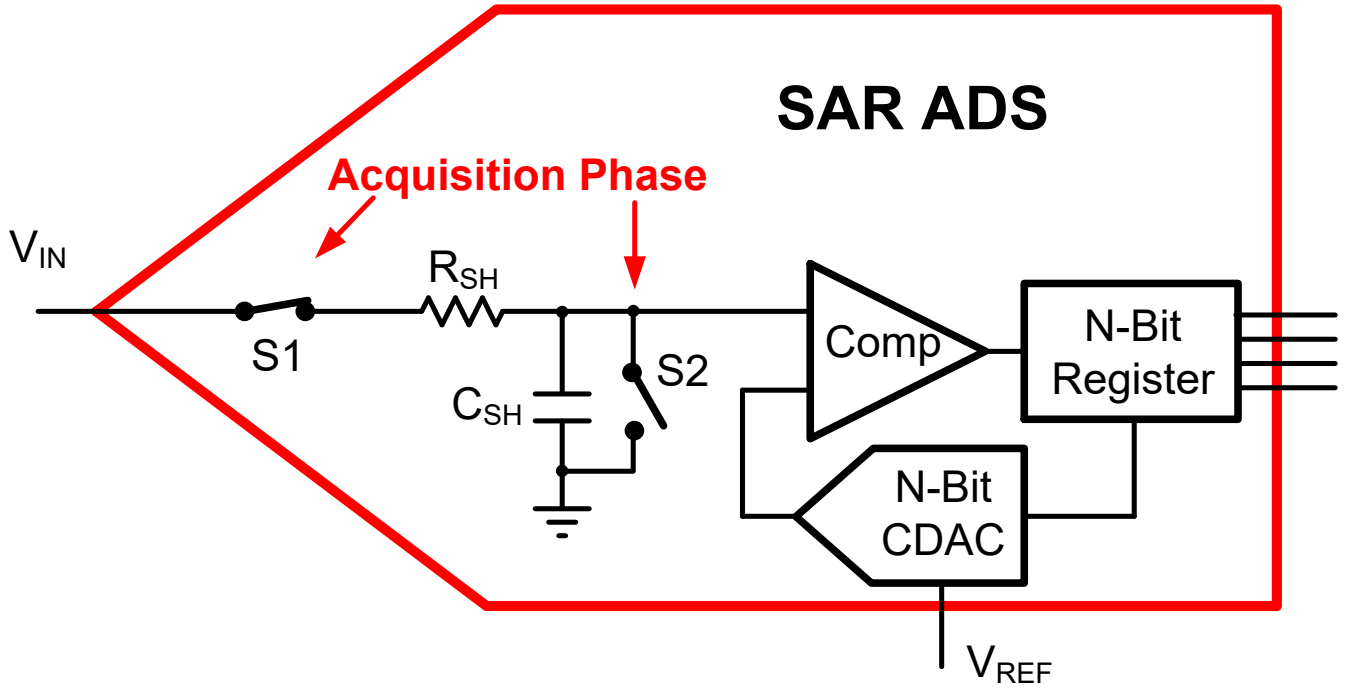
Basic diagram of SAR ADC
Successive Approximation Register



SAR ADC Acquisition & Conversion Phase



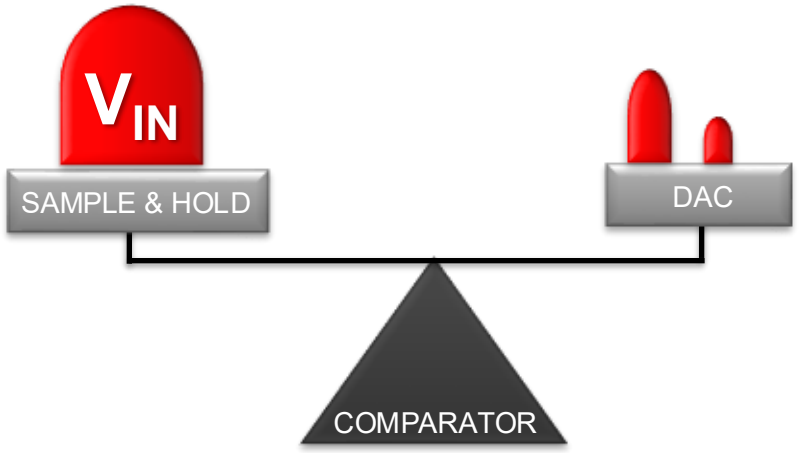


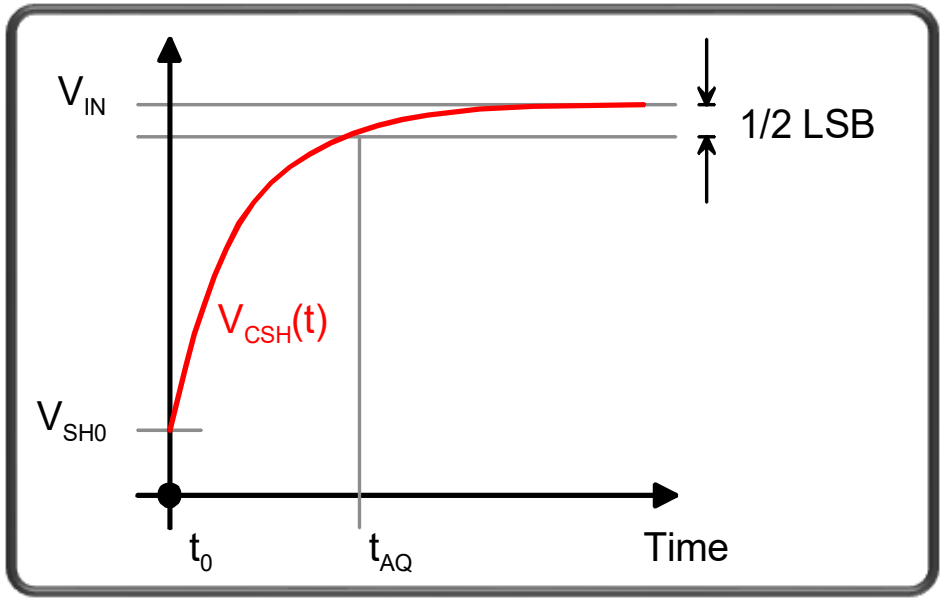


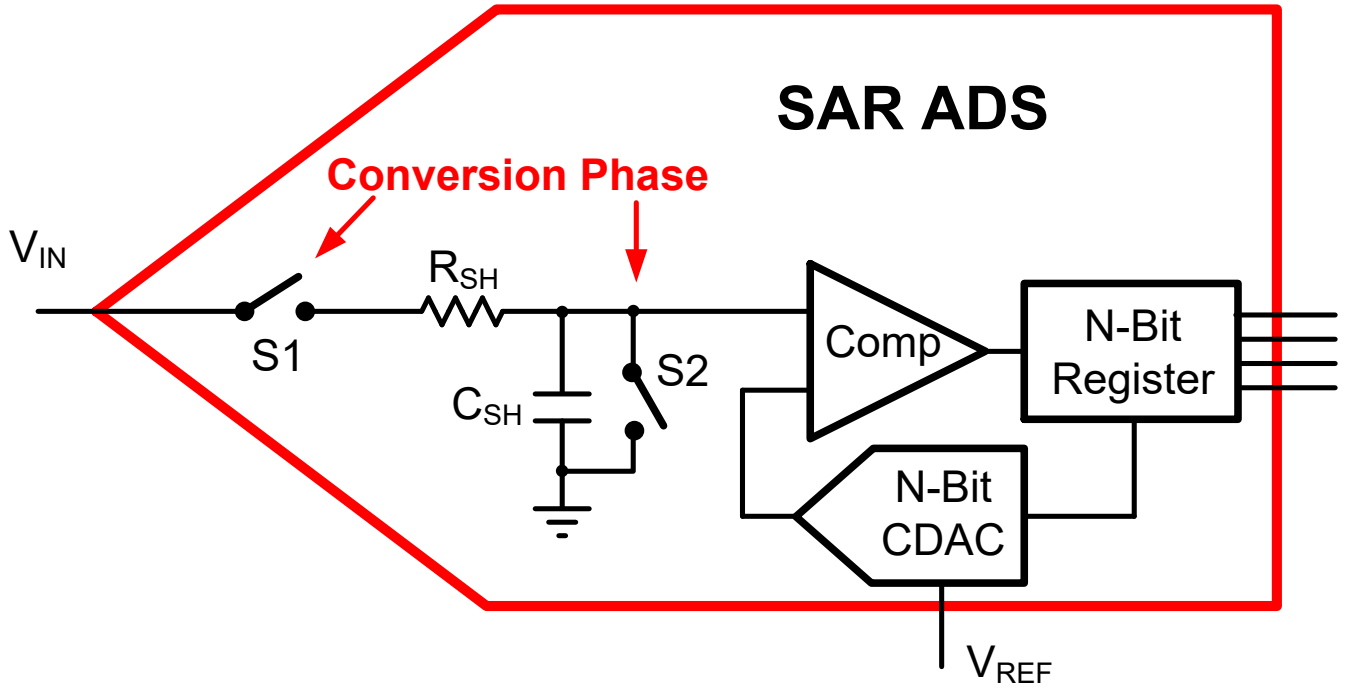
$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{SH} \times C_{SH}$$

SAR ADC Acquisition & Conversion Phase





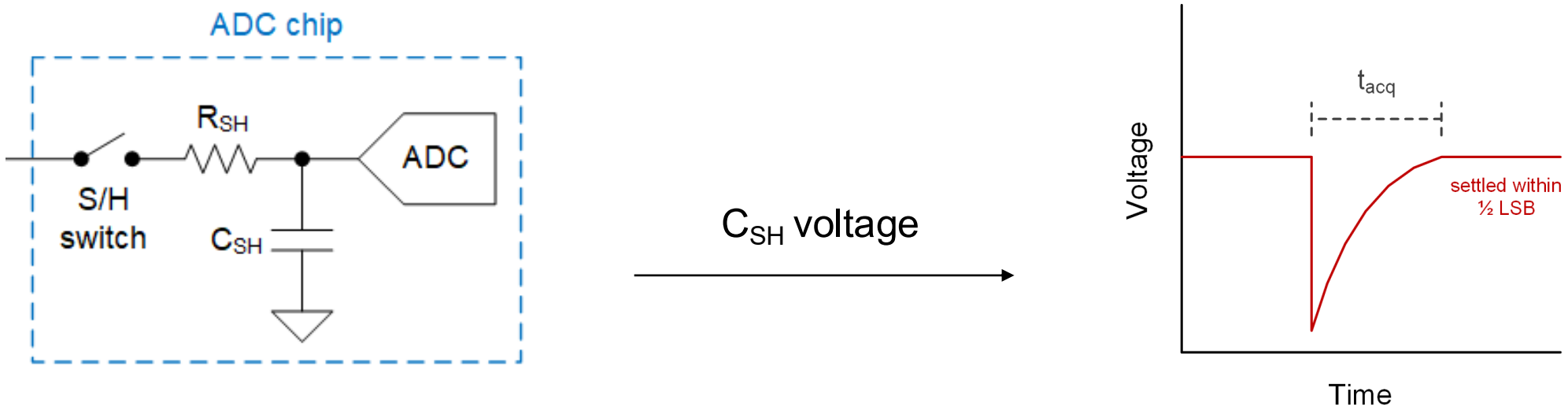


$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{SH} \times C_{SH}$$

Charging the C_{SH} Capacitor Within t_{acq}

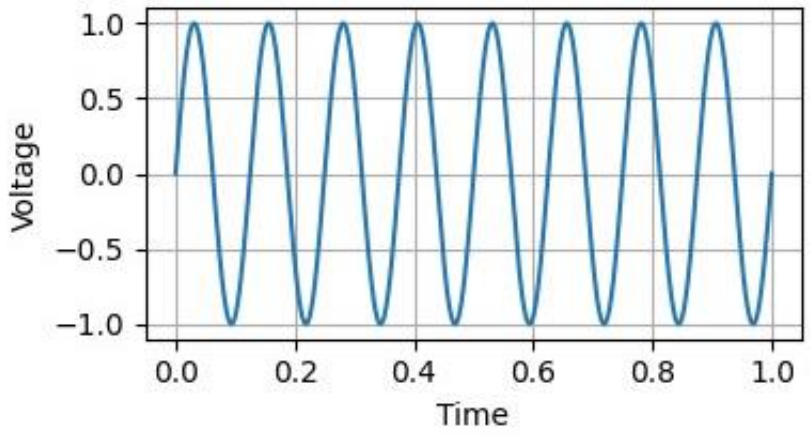
- The ADC's sample-hold capacitor (C_{SH}) needs to be settled to ½ LSB within the ADC's acquisition time (t_{acq}).
- where $t_{acq} = \left({}^{1}/_{f_{smpl}}\right) - t_{conv\_max}$



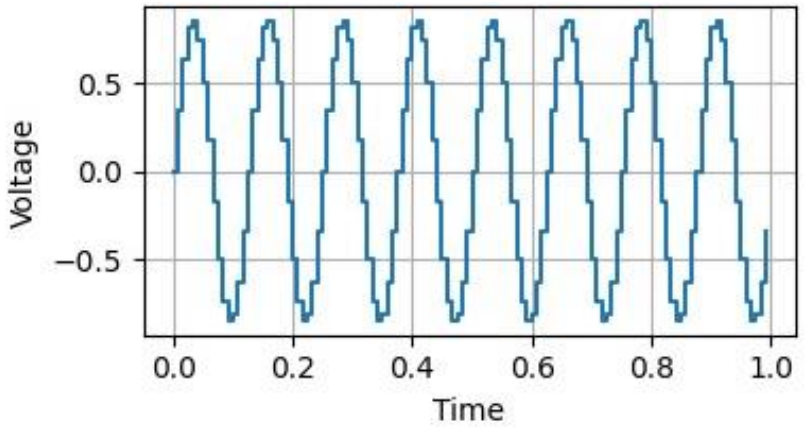
Why an ADC Driver Circuit is Needed

- If C_{SH} is not settled to ½ LSB within t_{acq}, the ADC's sampled waveform will be distorted and attenuated.

ADC Input Waveform

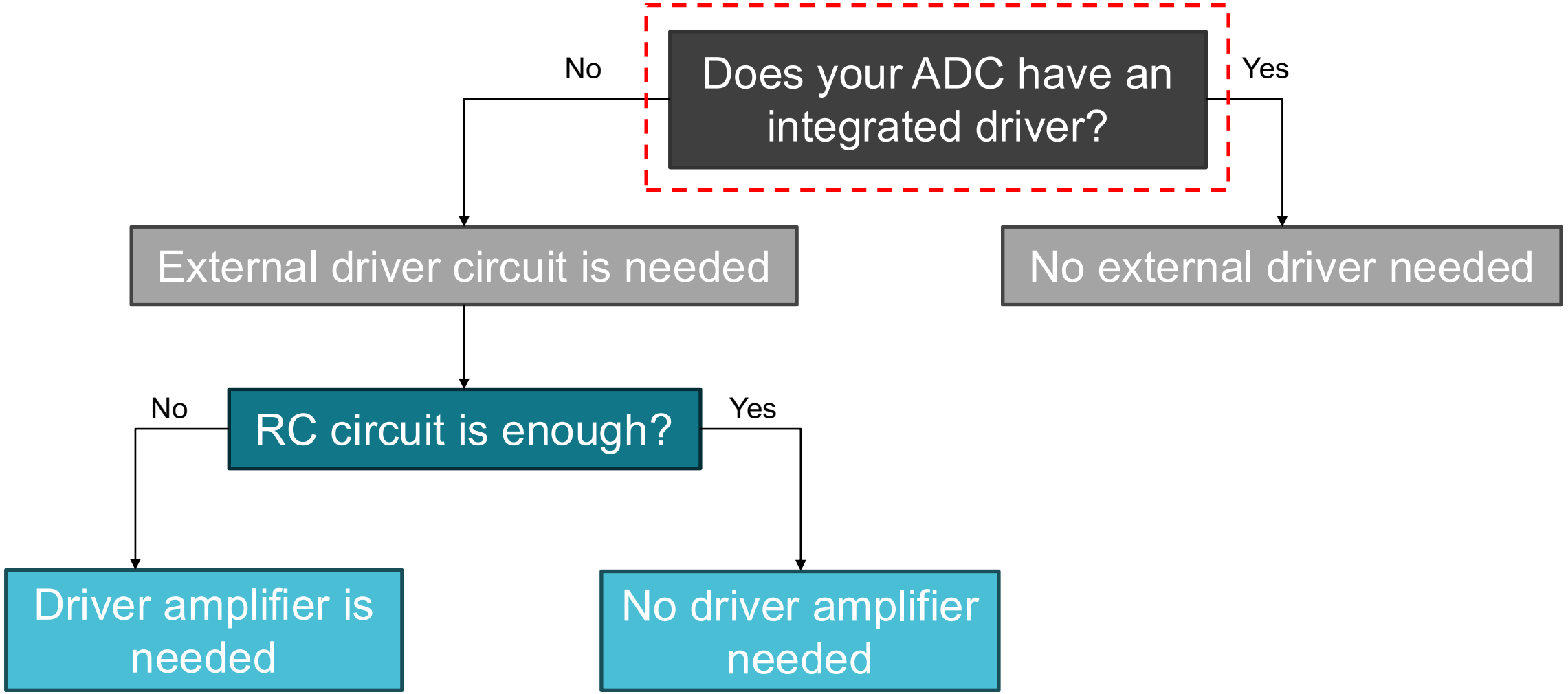


ADC Output Waveform



- An ADC driver circuit ensures fast and accurate settling of C_{SH}.

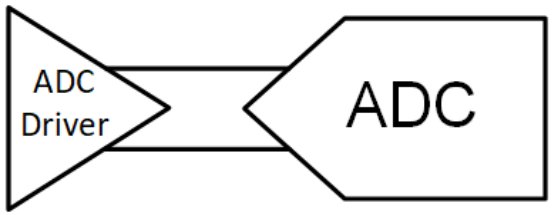
Do You Need an External ADC Driver Circuit?



Does Your ADC Have An Integrated Driver?

On the ADC datasheet:

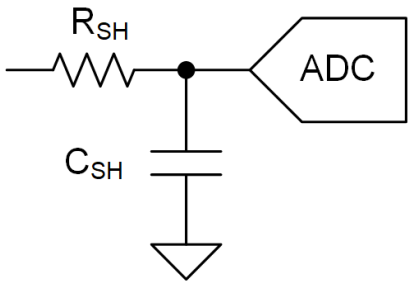
- Look for words like “integrated driver”.
- In the ADC block diagram, look for a driver block, like the one shown below:



Yes. External driver not needed.

On the ADC datasheet:

- Notice if there is a section on designing the drive circuit.
- Look for diagrams showing a switch-capacitor input structure, as below:



No. External driver is needed.

Example: Does ADS8860 Have An Integrated Driver?

For ADS8860:

- Check the datasheet for a block diagram.
- The block diagram shows a lack of an integrated driver.
- This ADC will require an external driver circuit.

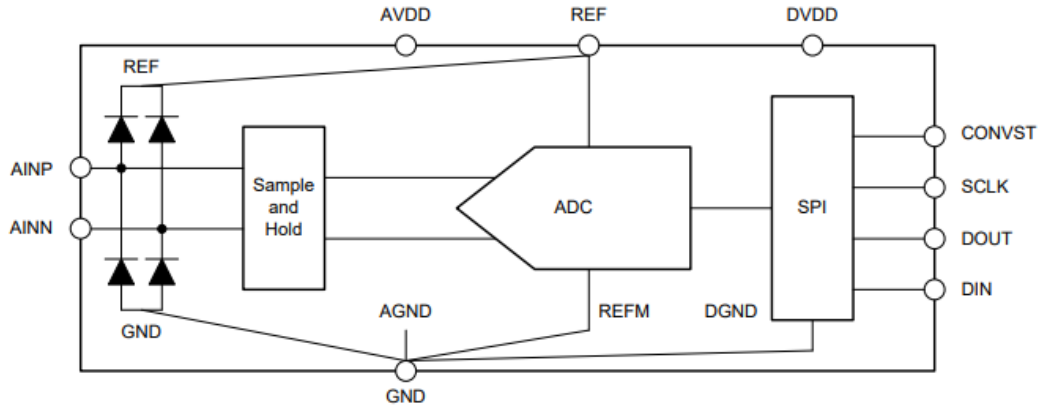
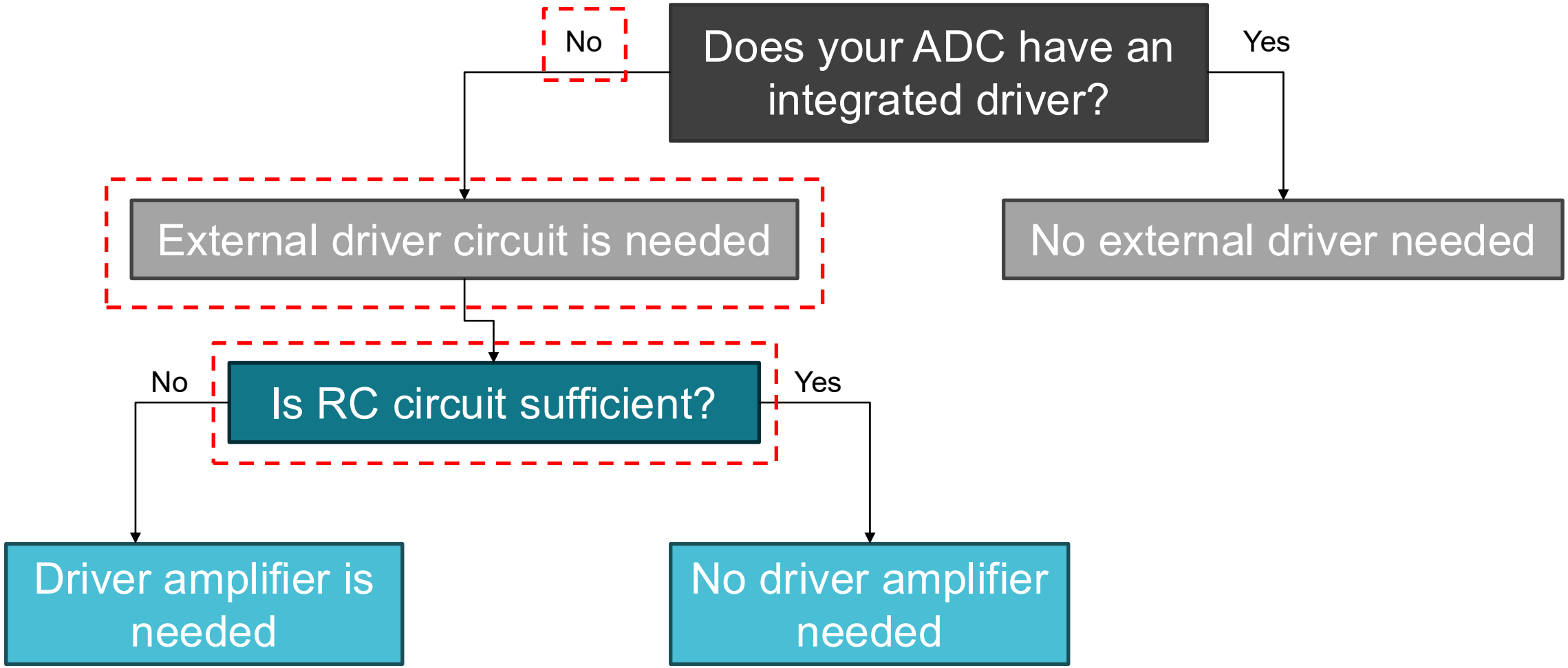


Figure 44. Detailed Block Diagram

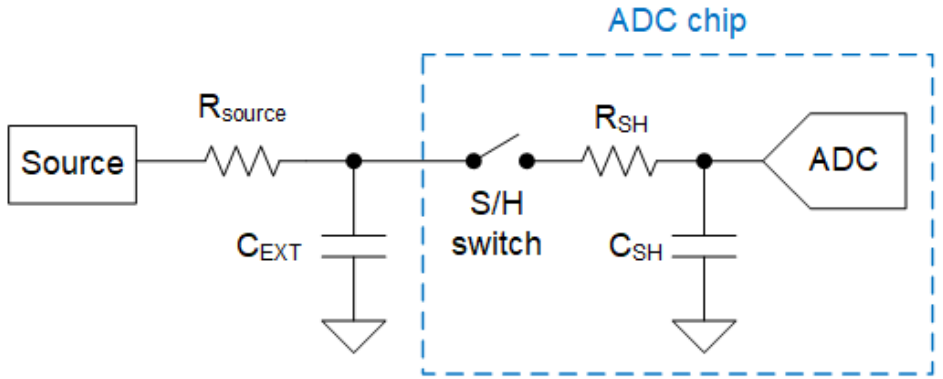
Do You Need an External ADC Driver Circuit?



Is RC Circuit Sufficient?

- C_{EXT} = 20 x C_{SH}
- Calculate the max R_{source} that may be interfaced with a given *n*-bit ADC:

1. $l = \ln 2^n$
2. $\tau = \frac{t_{acq}}{l}$
3. $R_{source} \leq \frac{\tau}{C_{EXT}}$



- If R_{source} is greater, then the ADC C_{SH} cannot settle within ½ LSB in the acquisition time t_{acq} without an external op-amp.

Example: Is RC Circuit Sufficient for ADS8860?

- From the ADS8860 datasheet:
  - C_{SH} = 55 pF
  - t_{acq} = 290 ns
  - n = 16
- Calculate $l = \ln 2^n = \ln 2^{16} = 11.09$
- Calculate τ, where $\tau = \frac{290*10^{-9}}{11.09} = 2.61 * 10^{-8}$
- Calculate max R_{source} using $R_{source} \leq \frac{2.61*10^{-8}}{55*10^{-12}} \leq 475.4\ \Omega$
- If R_{source} is larger than $475.4\ \Omega$, a driver amplifier will be needed.

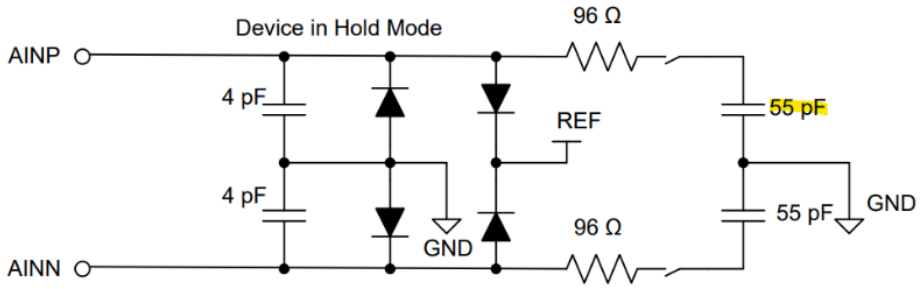


Figure 45. Input Sampling Stage Equivalent Circuit

t_{ACQ}	Acquisition time	290	ns

Factors Affecting Driver Circuit: R_{source} & t_{acq}

RC Circuit is Sufficient

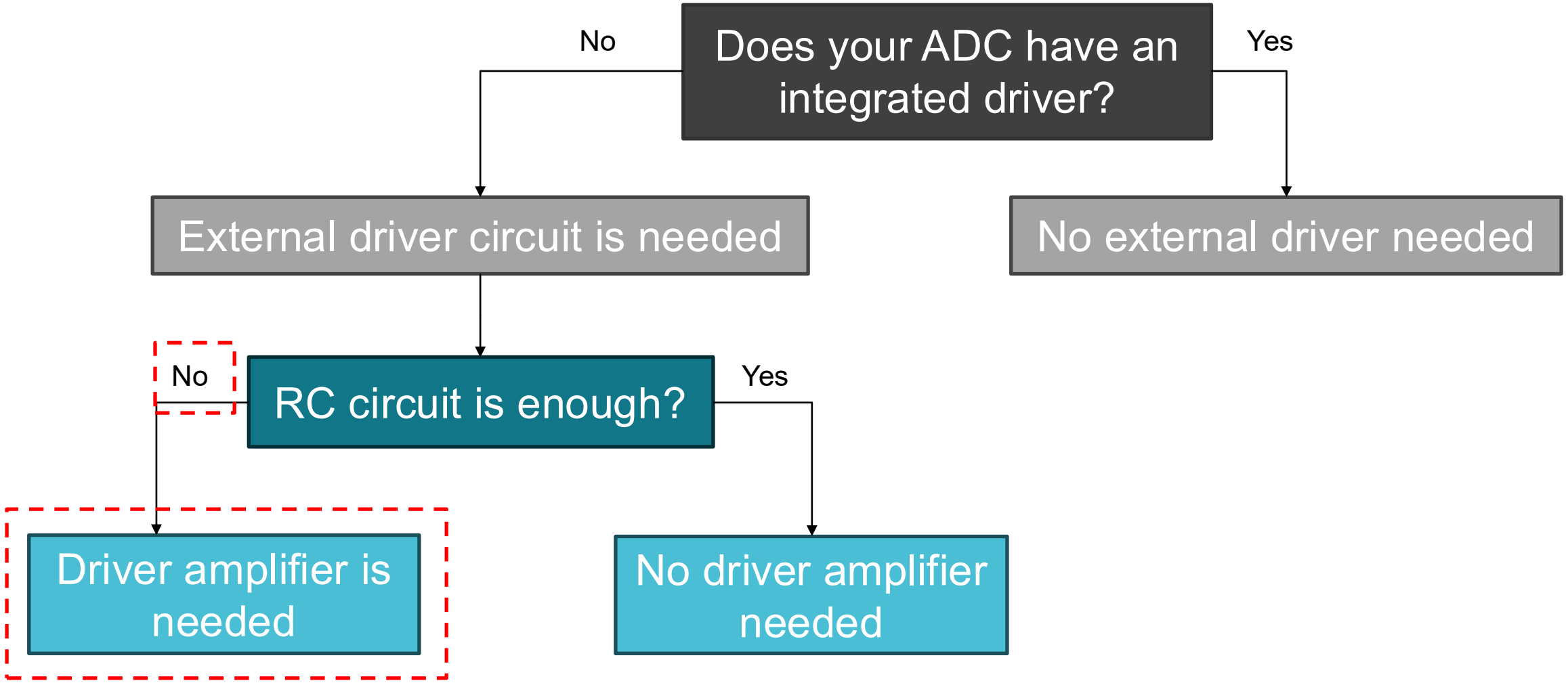
- If:
  - $R_{source} \leq 475.4\ \Omega$
  - $t_{acq} \geq 290\ ns$

Driver Amplifier is Required

- If:
  - $R_{source} > 475.4\ \Omega$
  - $t_{acq} < 290\ ns$

- For this example, assume $R_{source} = 1\ k\Omega$ – so, a driver amplifier will be needed.

Do You Need an External ADC Driver Circuit?



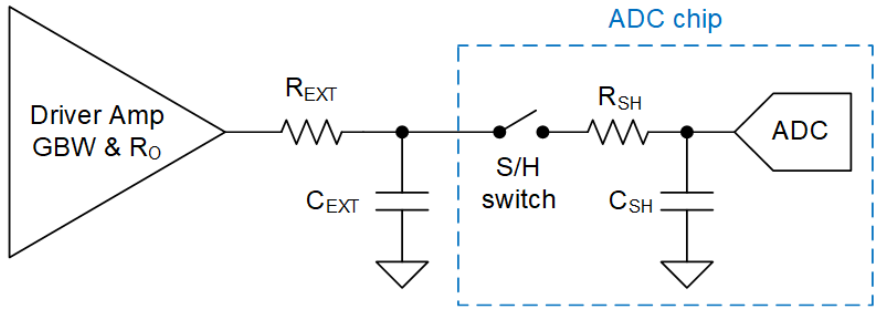
Select a Driver Amplifier

Find amplifier unity gain BW, f_U:

- $C_{EXT} = 20 \times C_{SH}$
- $K = ln\left[\frac{2^{N+1}}{\left(\frac{C_{EXT}}{C_{SH}}+1\right)}\right]$
- $f_Z = \frac{K}{2\pi \times t_{ACQ}}$
- $f_U \geq 4 * f_Z$

Find R_{EXT} and amplifier R_o:

- $R_{EXT} = \frac{1}{2\pi \times C_{EXT} \times f_Z}$
- $R_O \leq 9 \times R_{EXT}$



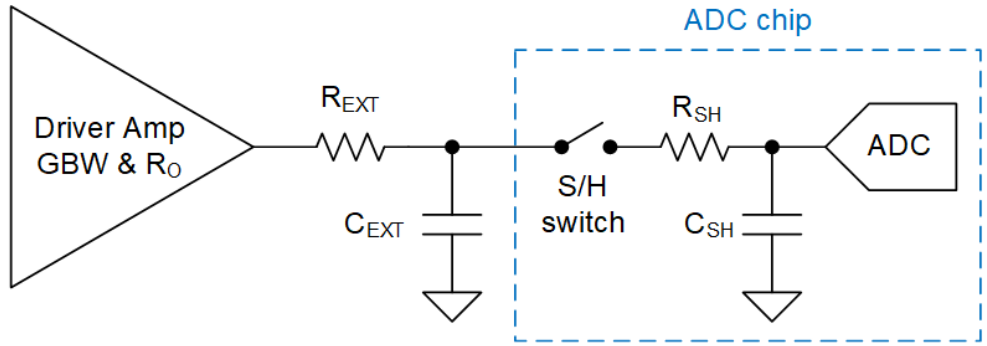
Example: Select a Driver Amplifier for ADS8860

Find amplifier unity gain BW, f_U:

- $C_{EXT} = 20 \times C_{SH} = 20 \times 55\text{pF} = 1.1\text{nF}$
- $K = \ln\left[\frac{2^{N+1}}{\left(\frac{C_{EXT}}{C_{SH}}+1\right)}\right] = \ln\left[\frac{2^{16+1}}{\left(\frac{1.1nF}{55pF}+1\right)}\right] = 8.74$
- $f_Z = \frac{K}{2\pi \times t_{acq}} = \frac{8.74}{2\pi \times 290ns} = 4.8\ MHz$
- $f_U \geq 4 * f_Z \geq 4 * 4.8\ MHz \geq 19.2\ MHz$

Find R_{EXT} and amplifier R_o:

- $R_{EXT} = \frac{1}{2\pi \times C_{EXT} \times f_Z} = \frac{1}{2\pi \times 1.1nF \times 4.8MHz} = 30.1\ \Omega$
- $R_O \leq 9 \times R_{EXT} \leq 9 \times 30.1 \leq 270.9\ \Omega$



Pick A Driver Amplifier

Selecting OPA836 to satisfy the requirements:

- $f_U = 10 \times 19.2\ MHz = 192\ MHz$
- $R_O \leq 270.9\ \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		205		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		100			
	V_{OUT} = 100 mV_{PP}, G = 5		28			
	V_{OUT} = 100 mV_{PP}, G = 10		11.8			
Closed-loop output impedance	f = 100 kHz		0.02		Ω	C

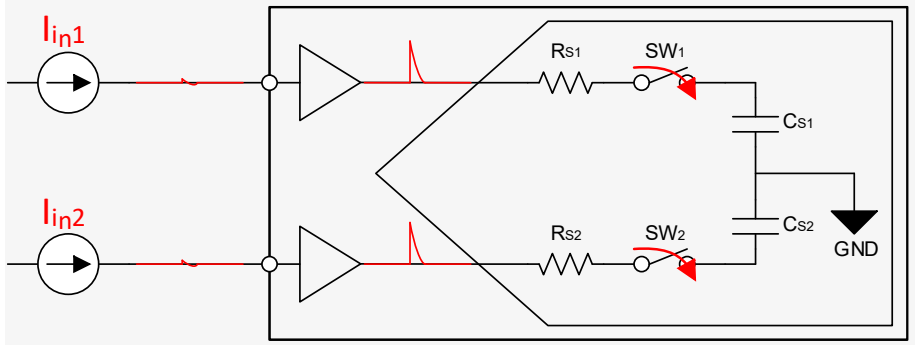
References

- https://www.ti.com/video/series/precision-labs/ti-precision-labs-analog-to-digital-converters-adcs.html
- https://e2e.ti.com/cfs-file/__key/CommunityServer-Discussions-Components-Files/14/7288.forum2_5F00_SAR_5F00_OPA.pdf

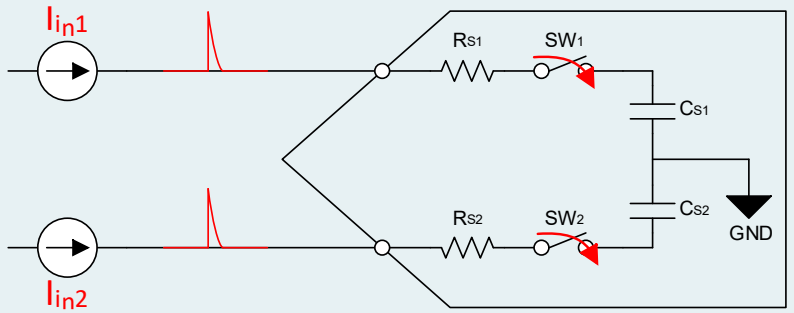
Buffered vs Unbuffered Architectures

Buffered vs. Unbuffered Architectures

Buffered



Unbuffered (Traditional)

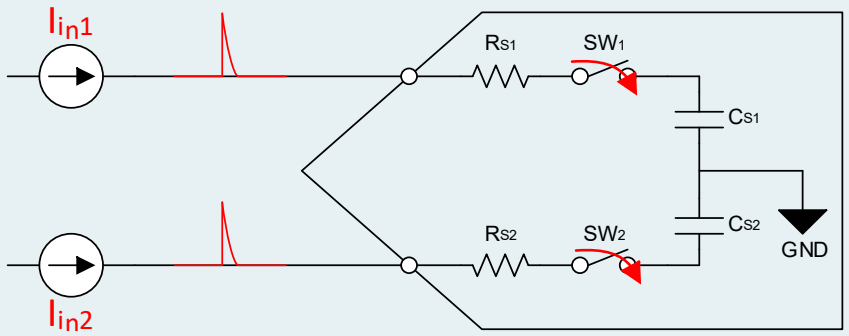


Feature	Buffered	Unbuffered (Traditional)
Input Structure	Integrated input buffer	Direct capacitor array connection
Input Impedance	High, constant impedance	Time-varying (switching)
Kickback	Minimal (isolated by buffer)	Significant charge injection
Driver Requirements	Simplified drive requirements	Must handle transient currents
Power Consumption	Higher (buffer active)	Lower (no buffer)
Settling Time	Relaxed requirements	Critical consideration

Understanding the Challenge:

Unbuffered Challenge

- SAR capacitor array switching during conversion
  - Creates transient input currents (kickback)
  - Driver must quickly settle these transients
- Input impedance varies with conversion phase

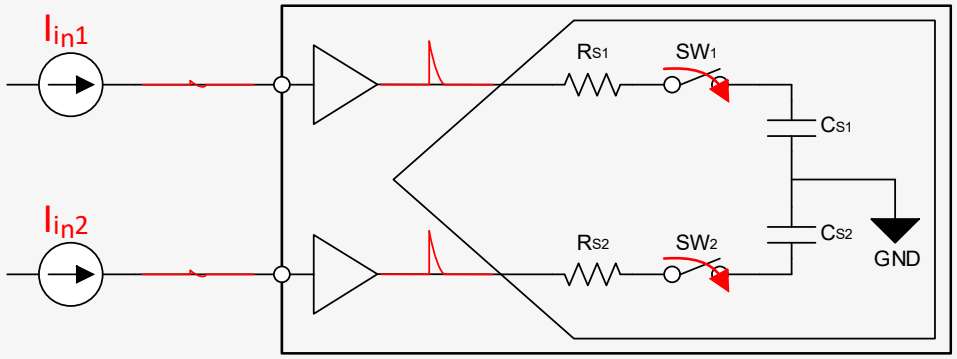


Impact on Driver:

- Requires low output impedance
- Must handle charge injection
- Needs adequate bandwidth for fast settling
- Complex input filter design (Charge-Bucket + Anti-Aliasing)

Buffered Benefits

- Buffer isolates capacitor array from input pins
  - Eliminates kickback to driver circuit
  - Simplifies anti-aliasing filter design
- Presents constant, high input impedance



Impact on Driver:

- Removed need to continuously charge sample and hold circuit.
- Anti-aliasing and signal bandwidth main priority

ADC Driver Design Process Steps

- Calculate Bandwidth Requirements
- Design Input Filter
- Set Common-Mode Voltage
- Analyze Noise

As an example, we will compare drivers for:

- ADS9227 – 16-bit, 5MSPS, SAR ADC with Buffered Input
- ADS9327 – 16-bit, 5MSPS, SAR ADC unbuffered
- Signal chain bandwidth: 100kHz
- Gain = 1V/V

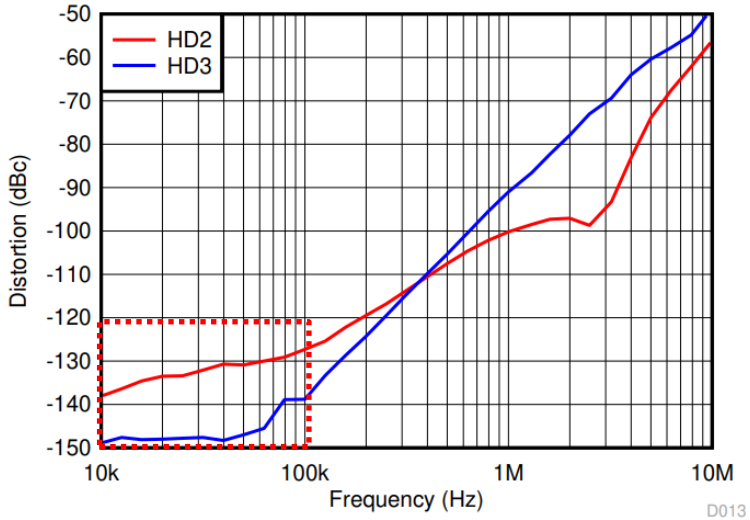
ADC Driver Design: Bandwidth

Unbuffered (ADS9327)

- Driver must settle to 16-bit accuracy to 1/2 LSB
- Settling time < acquisition time + margin
- **Bandwidth Calculation:**
  - **Rule of Thumb:**
    - For N-bit accuracy: $BW \approx \frac{\ln 2^N}{2\pi * t_{settle}}$
    - For 16-bit: $BW \approx \frac{11}{2\pi * t_{settle}}$
  - **For 5 MSPS with 70ns acquisition:**
    - Required closed-loop BW ≈ **25 MHz min**
    - Added margin in consideration for signal BW and input RC filter
    - *simulating RC combo still recommended

Buffered Benefits (ADS9227)

- Driver priority: signal fidelity
  - Select Driver with low distortion to desired input signal range (100kHz)
  - THS4551 (150MHz GBW):



G = 1 V/V, V_{OUT} = 2 V_{PP}

Figure 7-13. Harmonic Distortion vs Frequency

Step 2 - Input Filter Design

Anti-Aliasing Filter

- Main purpose: Low-pass filter to block frequencies above Nyquist frequency
  - $Nyquist = \frac{f_s}{2}$

Charge-Bucket Filter

- Main purpose: handle the "kickback" current when a SAR ADC sampling switch closes, quickly charge, and must be optimized for settling time.

Ideal goal (Traditional SAR): Find a balance between both

Limitations:

- Depends on ADC input and driver capabilities'
- Charge bucket filter might not effectively stop aliasing
- Pure anti-aliasing filter might not be fast enough to settle the input.

→ **For buffered ADCs charge bucket *not* needed.**

ADC Driver Design: Input Filter Design

Unbuffered (ADS9327)

- Priority: charge reservoir + anti-kickback
- Pick $C_{FLT} \geq 20 * C_{SH} \geq 20 * 18pF \geq 360pF$
  - 470pF standard value
- R_{FLT} calculation:
  - Practical $t_{FLT_{settle}} = t_{ACQ} = 12 * \tau_{FLT}$
  - $R_{FLT} = \frac{t_{ACQ}}{12 * C_{FLT}} \cong 12\Omega^*$

**confirming RC combination + driver in simulation recommended*

**Driver with higher* GBW → allows for improved Anti-Aliasing

**After simulation 10Ω & 1nF were found as best combination for driving and anti-aliasing*

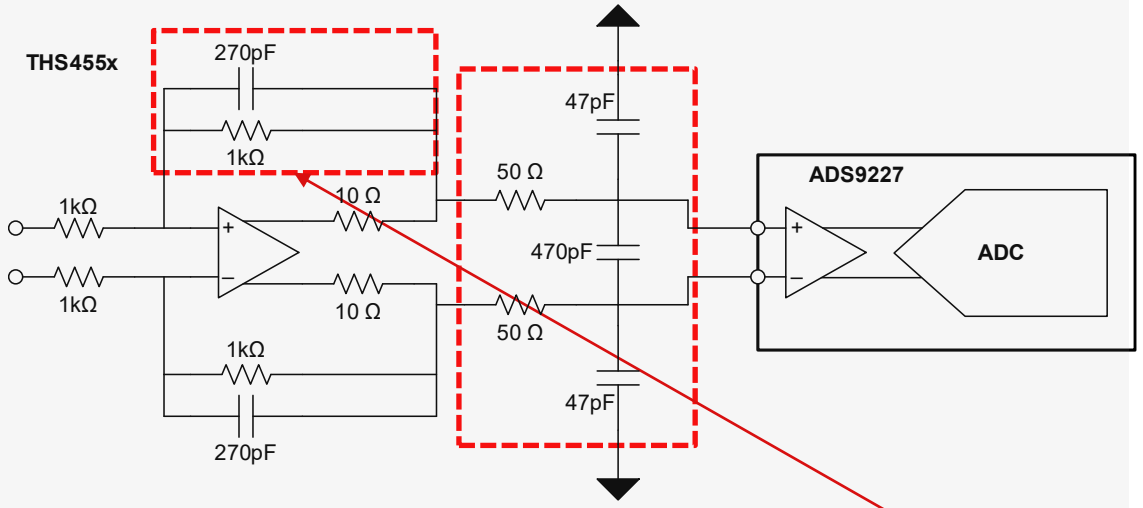
- Output filter $f_{-3dB} = \frac{1}{2\pi R_{FLT} C_{FLT}} \cong 16MHz$
- Minimum driver $GBW > 4 * \frac{1}{2\pi R_{FLT} C_{FLT}} \rightarrow \approx 60MHz$

Buffered Benefits (ADS9227)

- Priority: Anti-Aliasing
- Nyquist frequency $\frac{fs}{2} = 2.5MHz$
- $C_{diff} = \frac{1}{2\pi f_{Nyq} * 2R_{FLT}} = \frac{1}{2\pi * 2.5MHz * 2 * 50} \approx 646pF$
  - 470pF standard value
- $C_{cm} = \frac{C_{diff}}{10} = \frac{470pF}{10} = 47pF$

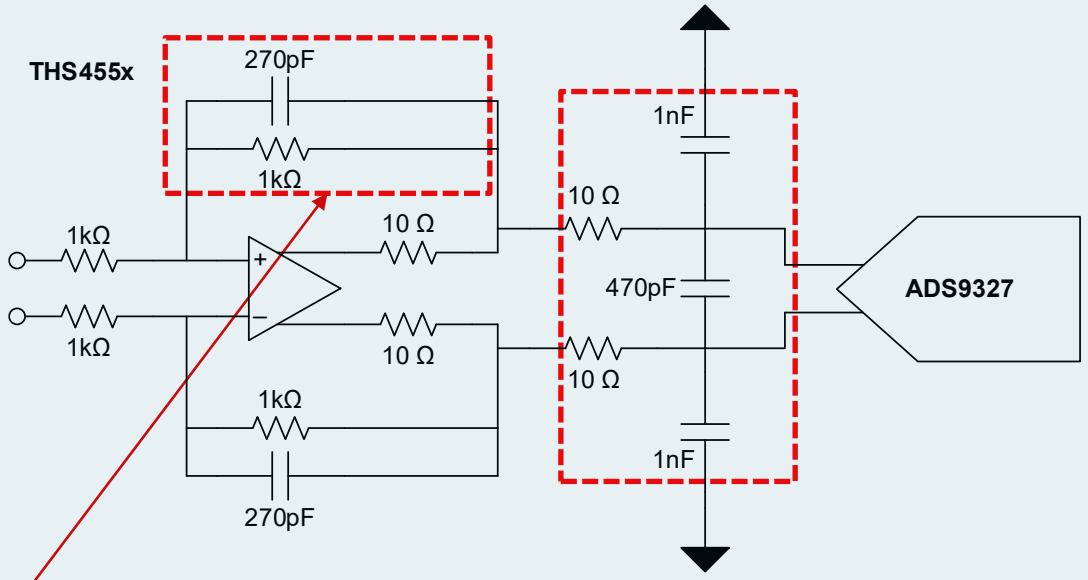
Step 2 - Input Filter Design

ADS9227 Circuit (from EVM):



Anti-Aliasing filter priority

ADS9327 Circuit (from EVM):



Charge Bucket Filter priority

- If ADC Driver bandwidth permits, additional filtering/bandwidth limitation can be added in the driver stage

Complete Design Comparison

Design Parameter	ADS9327 (Unbuffered)	ADS9227 (Buffered)
Min Driver BW	25-30 MHz (critical)	20-25 MHz (relaxed)
Filter Topology	Simple 1st-order RC	Simple 1st-order RC
Filter Cutoff	15 - 33 MHz (compromise)	5-10 MHz (better AA)
Series R	10-22 Ω (limits kickback)	22-50 Ω (flexible)
Shunt C	470 pF - 1 nF (limited)	470 pF - 2.2 nF (flexible)
Source Z	<10 Ω (critical)	<50 Ω (relaxed)
Design Complexity	Higher (settling critical)	Lower (isolated)
Power	Lower (no buffer)	~ 100-200 mW (buffer)
SNR	~91 dB	~90 dB

Which ADC to Choose?

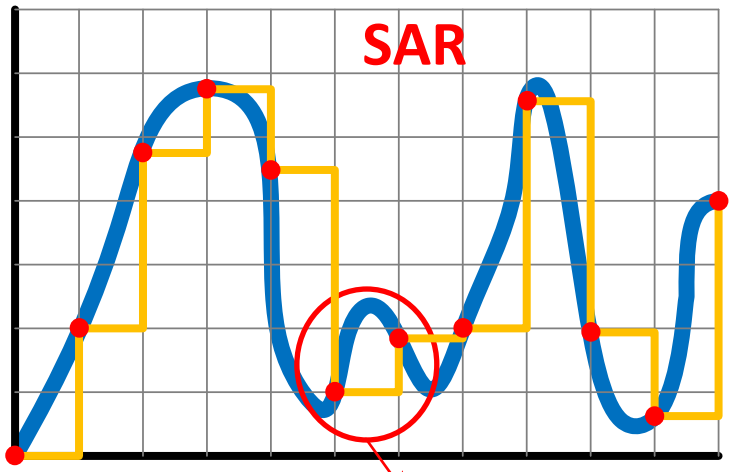
- **Choose ADS9227 (Buffered) When:** ✓ Ease of design is priority
  ✓ Need simplified filter design
  ✓ Driver has limited bandwidth/drive capability
  ✓ Power budget allows extra 100-200 mW
  ✓ Prototyping/quick time-to-market
  ✓ Multiple ADCs sharing same driver
- **Choose ADS9327 (Unbuffered) When:** ✓ Minimum power consumption required
  ✓ Maximum SNR performance needed (~1 dB better)
  ✓ Have experience with SAR ADC design
  ✓ Can provide low-impedance driver
  ✓ Willing to optimize settling/filtering

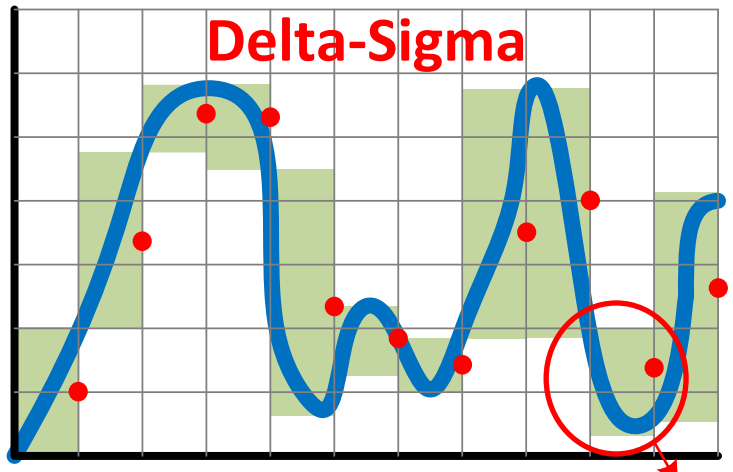
Driving High Speed Delta-Sigma ADC Inputs

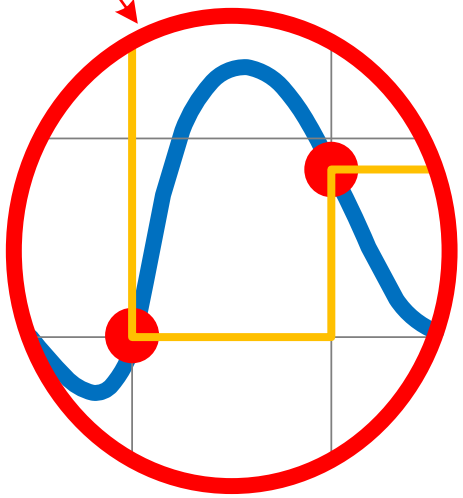
Agenda

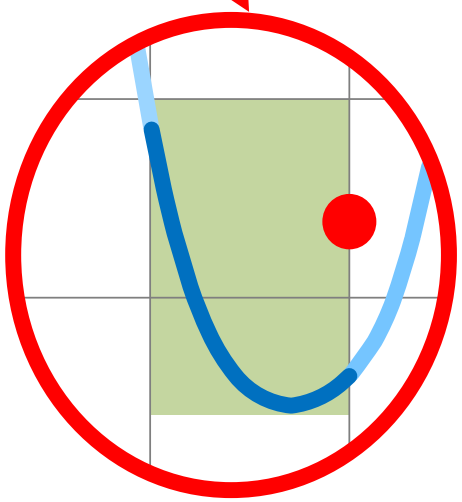
- Wideband Delta-Sigma ADC characteristics
  - ✓ Delta-Sigma ADC verses SAR ADC
  - ✓ Digital Filter characteristics
  - ✓ Anti-Alias Filter (AAF) requirements using wideband filter verses SAR
- Equivalent input model
- Input driver design procedure

SAR vs Delta-Sigma Sampling





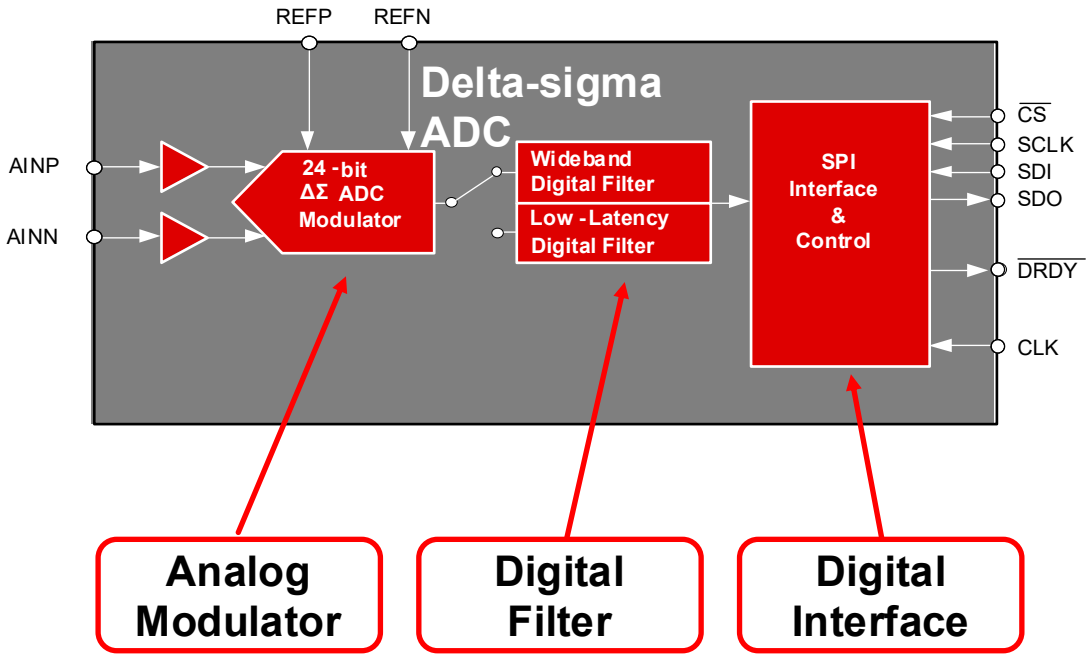




SAR:
Red dot indicates the "snap-shot" captured

Delta-Sigma:
Red dot indicates the average of the signal in the green sampling interval

High Speed Delta Sigma ADC

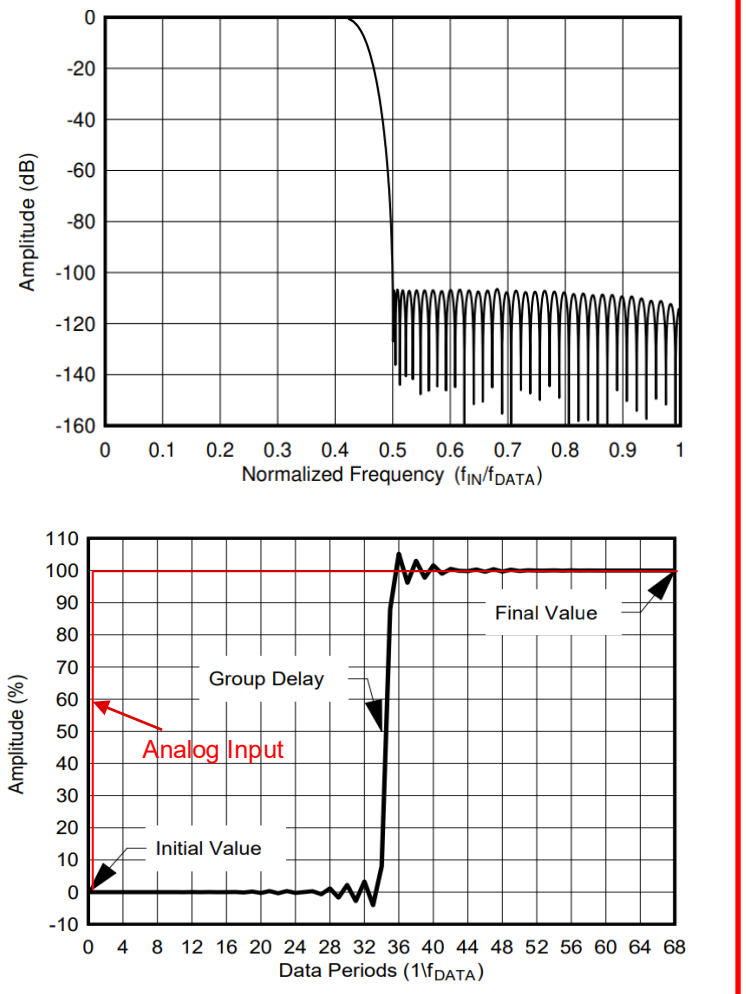


Simplified Model of Delta-Sigma ADC

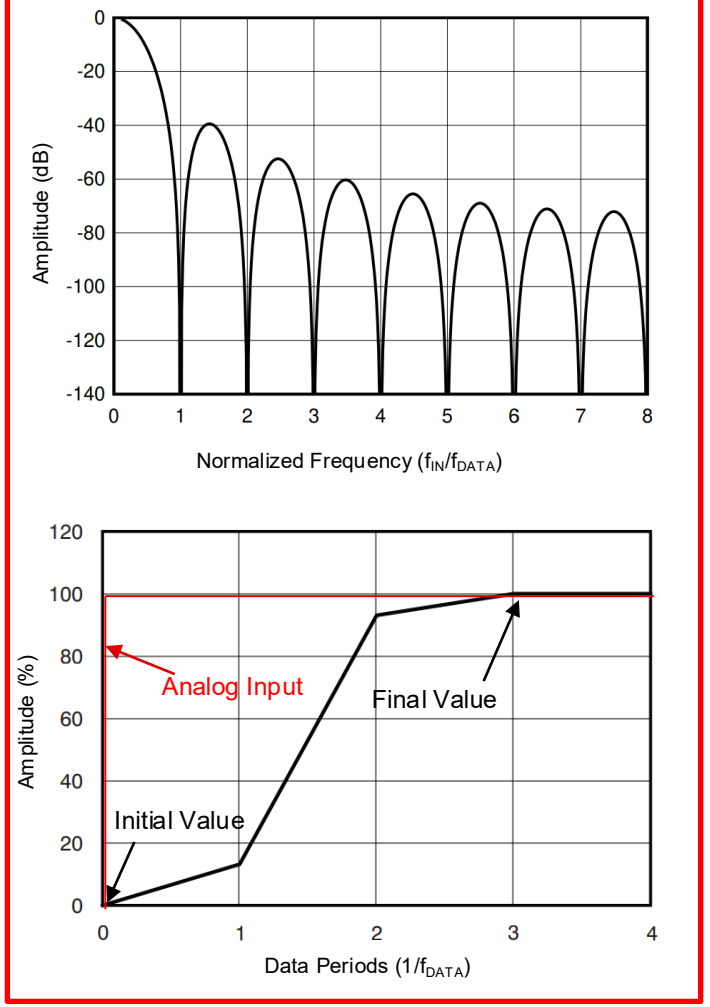
- Analog Modulator
  - ✓ Continuously captures data
  - ✓ Input sample rate (Modulator frequency) $\mathbf{f_{mod}}$
    - ➢ $\mathbf{f_{mod}}$ is directly proportional to clock frequency, $\mathbf{f_{clk}}$
- Digital Filter
  - ✓ Averages many input samples to produce a single output value, typically 24b or 32b
- Digital Interface
  - ✓ Typical interface options are SPI, Frame-sync
  - ✓ ADC requires a continuous clock (CLK) source
  - ✓ DRDY (Data Ready) indicates when the next conversion result is ready to read by the processor

High Speed Delta Sigma ADC

Typical Wideband Filter Response



Low-Latency SINC3 Filter Response



Digital Filter (continued)

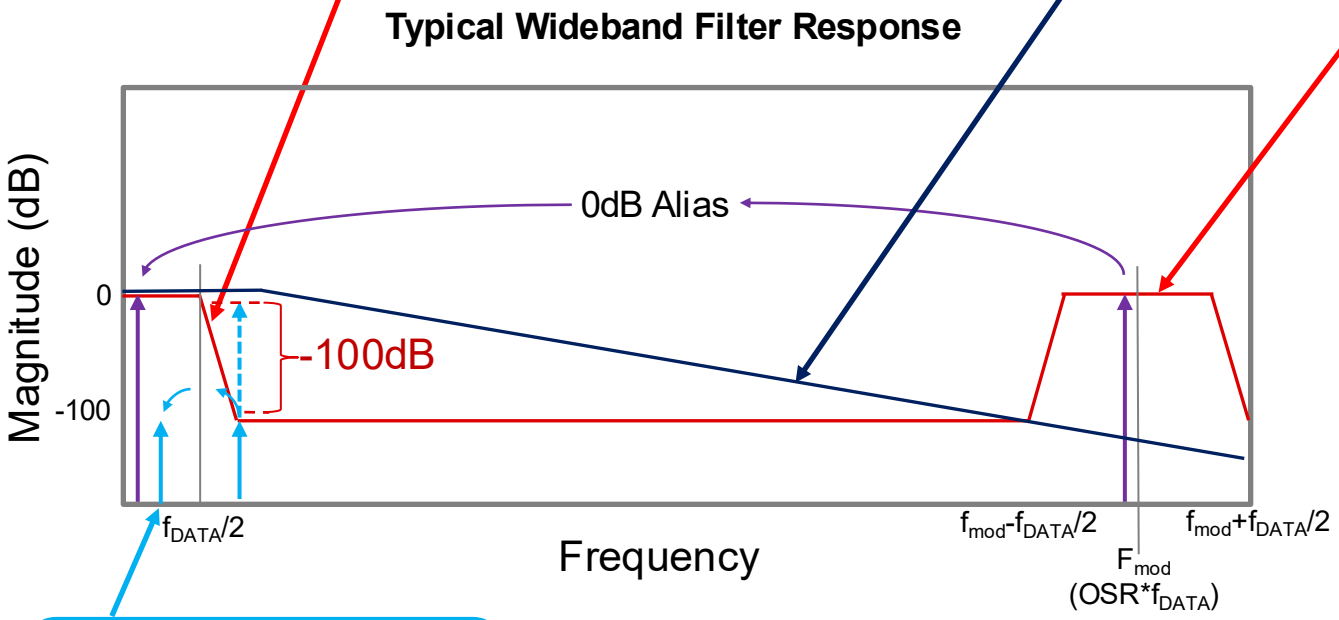
- Many Delta Sigma ADCs have multiple filter options
- Wideband filter maximizes input signal bandwidth
  - ✓ Usually very close to the Nyquist bandwidth ½*f_{DATA}
  - ✓ Very long settling time, >55 data rate periods are typical
- Low-latency filter
  - ✓ Usually a SINC filter, which is simply a moving average filter
  - ✓ Filter will attenuate input signal at very low frequency
  - ✓ Very fast settling times, 3 to 5 data rate periods

High Speed Delta Sigma ADC | Anti-Aliasing Filter

Digital filter attenuates signal by 100dB

Analog Anti-Alias filter attenuates signal by 100dB at f_{mod}-f_{DATA}/2

Digital filter has 0dB of attenuation in this frequency range

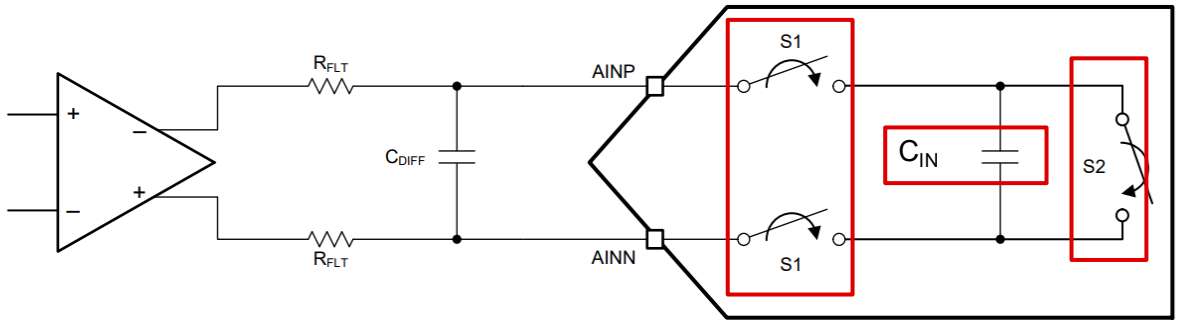


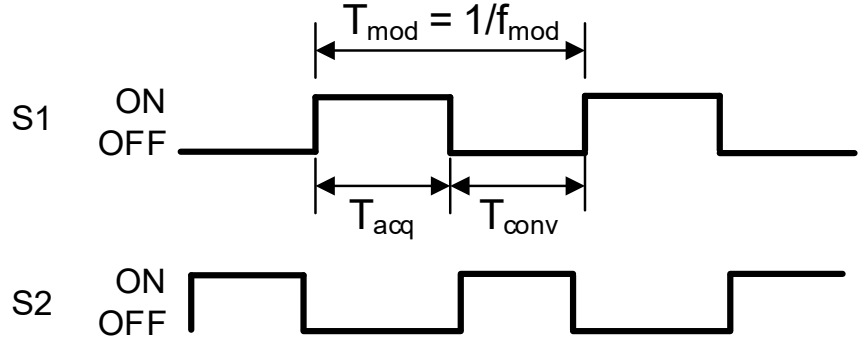
- Input signal aliasing occurs for any input frequency greater than f_{DATA}/2 (Nyquist frequency)
- The digital filter in a Delta-sigma ADC will attenuate the aliased signal frequency up to f_{mod}-f_{DATA}/2.
- Any signal in the range of f_{mod}±f_{DATA}/2 will have little or no attenuation by the digital filter.
- An external anti-alias filter is required to attenuate signals greater than f_{mod}-f_{DATA}/2

Input signal Aliases, but attenuated -100dB by digital filter

High Speed Delta Sigma ADC

Equivalent Analog Input Circuit Model

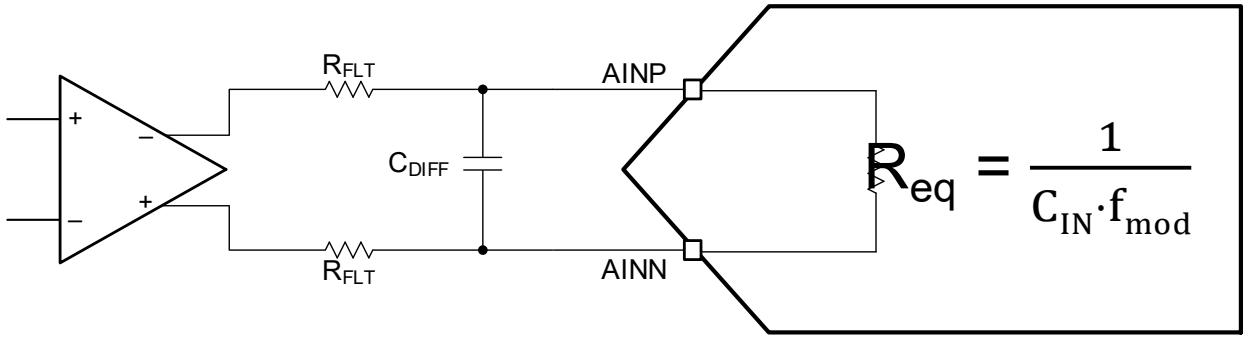




C_{IN},ADC sampling capacitor

- ✓ S1 closed during the acquisition period T_{acq}, $C_{IN} = V_{DIFF}$
- ✓ S2 closed during the conversion period T_{conv}, $C_{IN} = 0V$

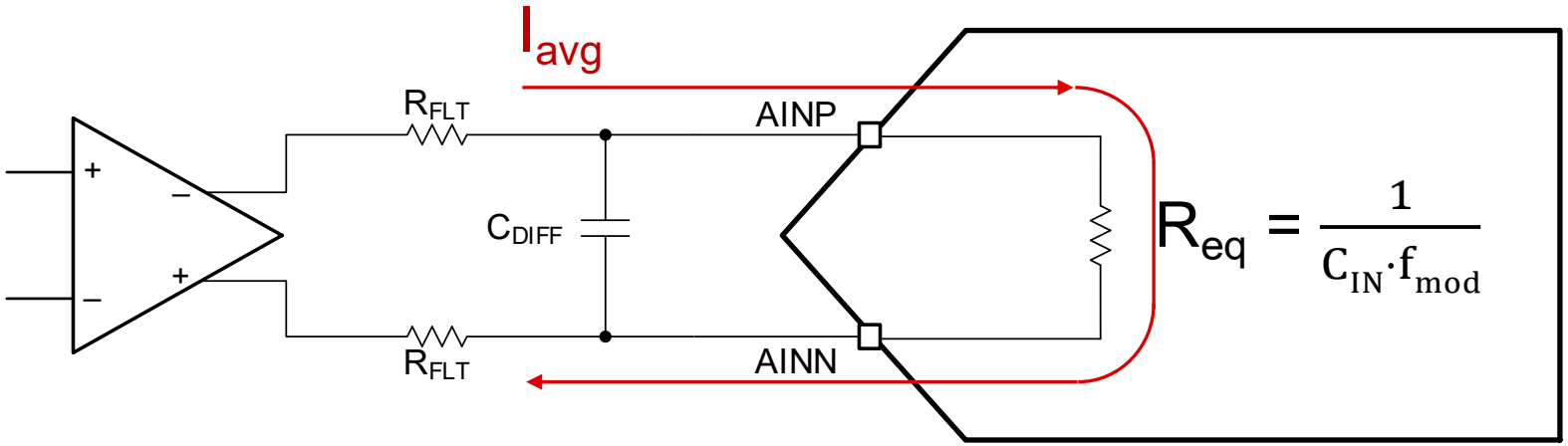
Average Input Circuit Model ($C_{DIFF} \geq 100 \times C_{IN}$)



Delta Sigma ADC input can be modeled as an input resistance

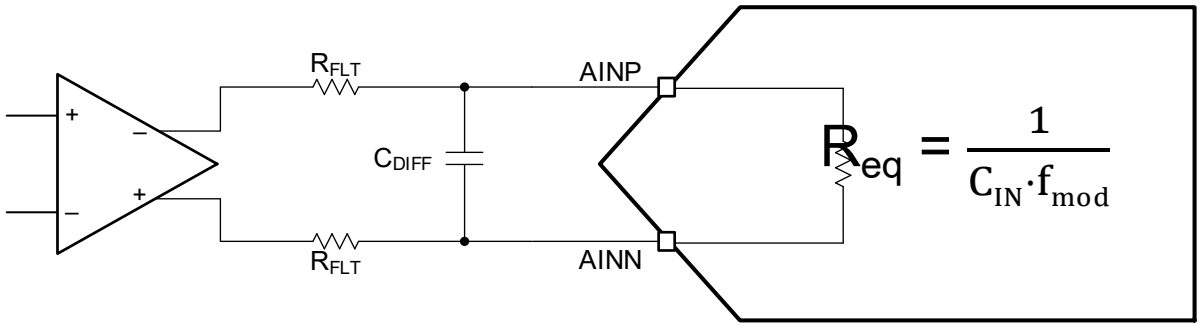
- ✓ Possible since input is continuously sampling
- ✓ $C_{DIFF} \geq 100 \times C_{IN}$

High Speed Delta Sigma ADC



- Using recommended values for the external RC input filter averages current transients required to charge the input sampling capacitor, resulting in a resistive amplifier load.
  - ✓ The amplifier only needs to drive the input filter and the ADC resistive load, allowing use of lower bandwidth amplifiers.
  - ✓ Many amplifiers in the 5MHz to 40MHz range can be used.
- A fully settled input driver design can be used but requires an input amplifier bandwidth approximately 20 times greater than the input sample rate.
  - ✓ Typical wideband delta-sigma ADC input sample rate is 10MHz, requiring an input amplifier bandwidth of 200MHz or higher to fully settle.

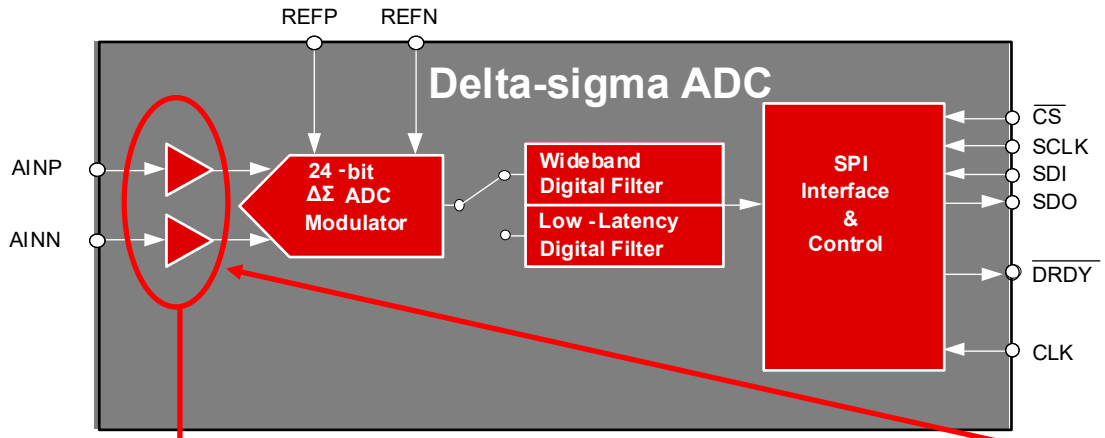
High Speed Delta Sigma ADC

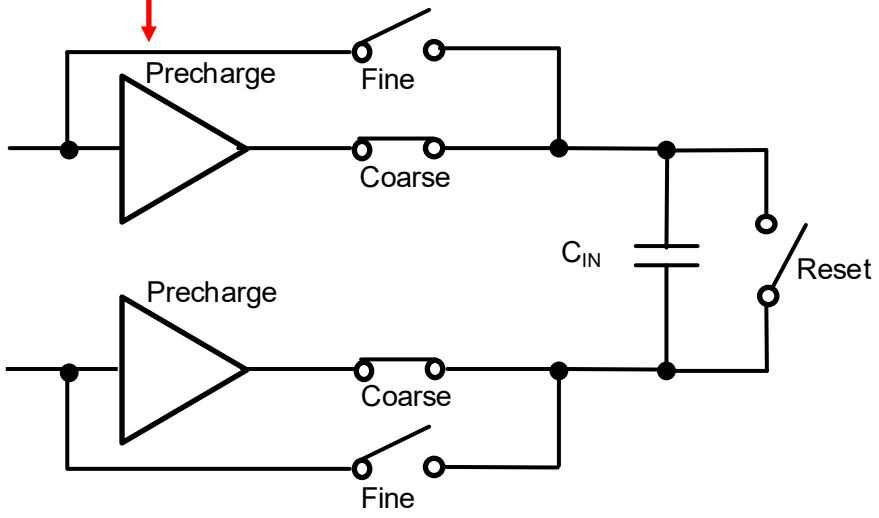


$$\text{Gain Error} = [1 - \frac{R_{eq}}{R_{eq} + 2 * RFLT}] * 100\%$$

- The disadvantage of using a large RC value to average the input current is a steady state gain error.
  - This error results from the average current flow through R_{FLT}.
- Using the simplified ADC input model, it is straightforward to calculate the gain error
  - ✓ The input filter resistors, R_{FLT} create a voltage divider with R_{eq}
- The Gain Error is the difference between an ideal gain of 1 and the voltage divider created by R_{eq} and R_{FLT}
  - ✓ Gain Error = $[1 - \frac{R_{eq}}{R_{eq} + 2 * RFLT}] * 100\%$

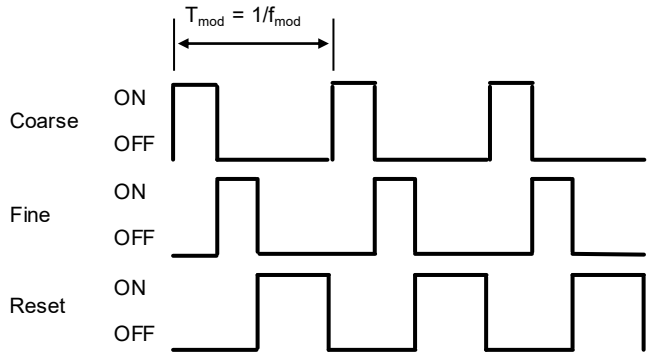
High Speed Delta Sigma ADC





Precharge buffers

- Latest generation high-speed Delta Sigma ADCs include input pre-charge buffers
- These buffers quickly charge the input capacitor C_{IN} to approximately 0.999 of the input value (coarse switch closed)
- After this pre-charge phase, the buffers are switched off, and the inputs are directly connected to the input capacitor (fine switch closed)
- This reduces the amount of average input current needed to charge the input capacitor C_{IN} by approximately 1000x



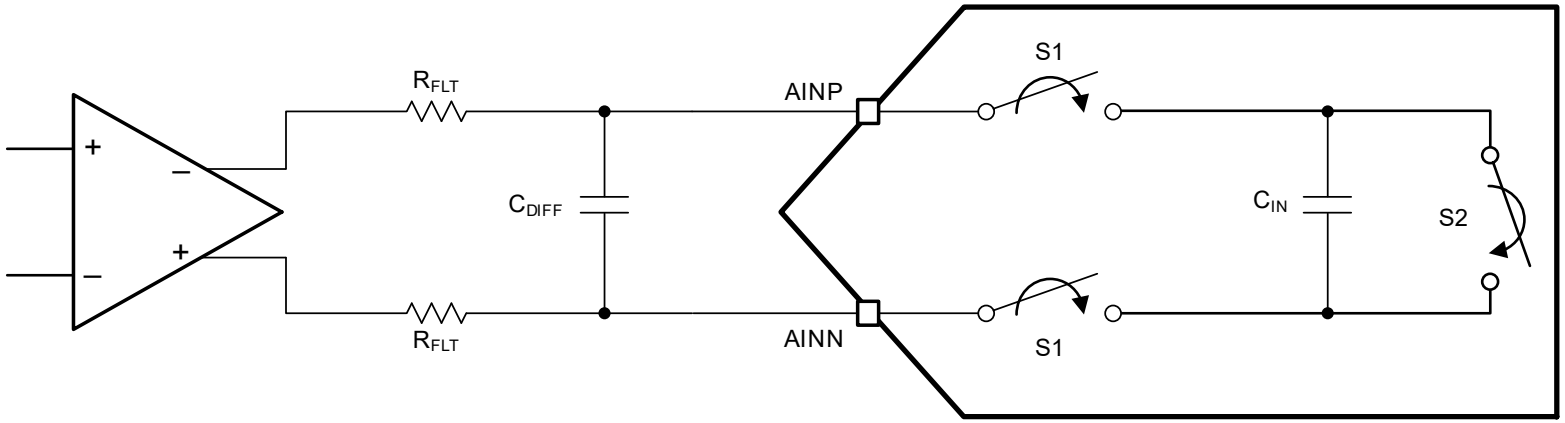
Precharge Buffers Enabled

$$R_{eq} = \frac{1000}{C_{IN} * fmod}$$

High Speed Delta Sigma ADC – ADC Input Filter

How to choose the ADC input RC capacitance

- C_{DIFF} should be in the range of 100·Cin up to 22nF
  - ✓ 22nF is a maximum practical limit to ensure amplifier stability
  - ✓ High value capacitors result in better low frequency performance (<10kHz) but cause amplifier distortion at high frequencies due to low impedance loading on amplifier outputs
  - ✓ Higher amplifier load current also results in higher power consumption

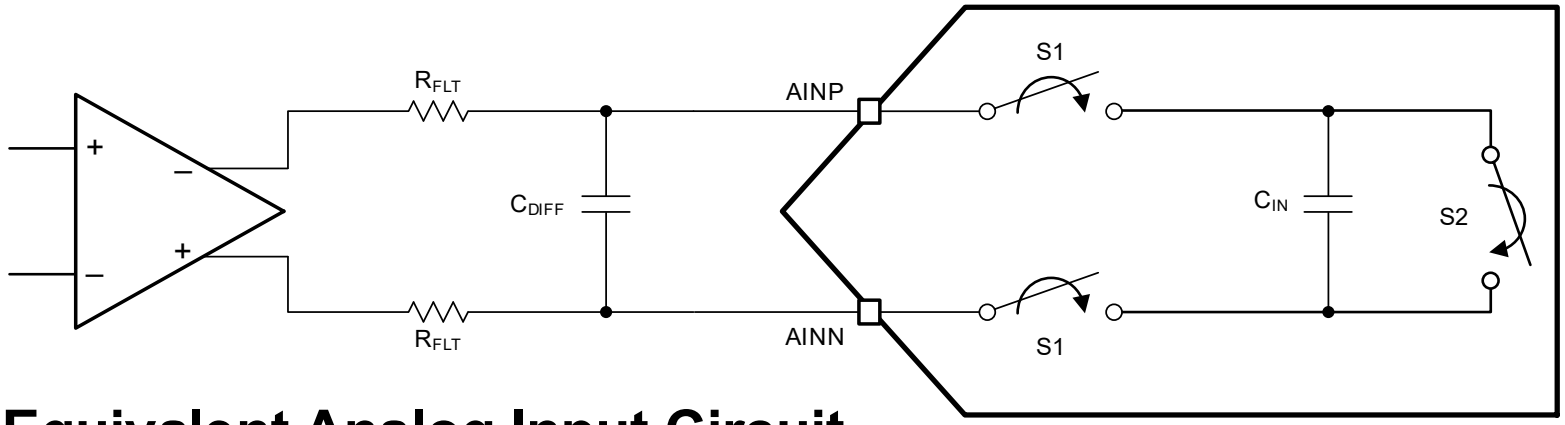


Equivalent Analog Input Circuit

High Speed Delta Sigma ADC – ADC Input Filter

How to choose the ADC input RC filter resistance

- R_{FLT} should be in the range of $1/(\pi \cdot f_{MOD} \cdot C_{DIFF})$ up to 100Ω maximum
  - ✓ Maximum 100Ω R_{FLT}
    - ✓ Minimizes offset voltage due to ADC input leakage current
    - ✓ Minimizes linearity errors due to nonlinear ADC input current flowing through R_{FLT}
  - ✓ Minimum R_{FLT} value sets the input RC filter corner frequency at a maximum of ¼· f_{MOD} frequency

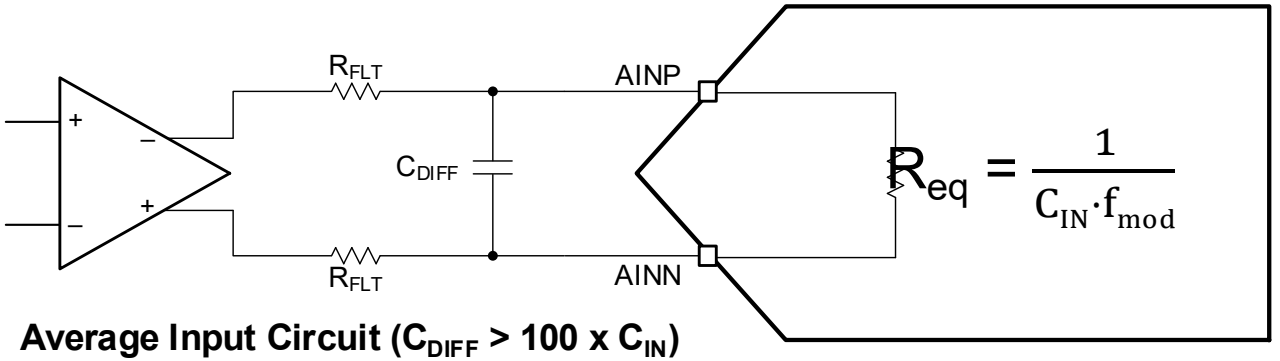


Equivalent Analog Input Circuit

High Speed Delta Sigma ADC – ADC Input Amplifier

How to choose Input amplifier Bandwidth

- The minimum bandwidth of the input amplifier should be GBW ≥ fmod/2
  - ✓ Higher amplifier bandwidth will support better THD performance
  - ✓ Higher bandwidth amplifiers will typically require lower R_{FLT} values to maintain stability, resulting in improved linearity and THD
- Simulate input amplifier, RC filter, and simplified ADC input impedance using SPICE to verify stability and proper settling
  - ✓ Most amplifiers have a complex, multi-order open loop output impedance making simple calculations for stability inaccurate
  - ✓ Modern amplifier SPICE models have very accurate output impedance and can be used to accurately simulate stability



Average Input Circuit (C_{DIFF} > 100 x C_{IN})

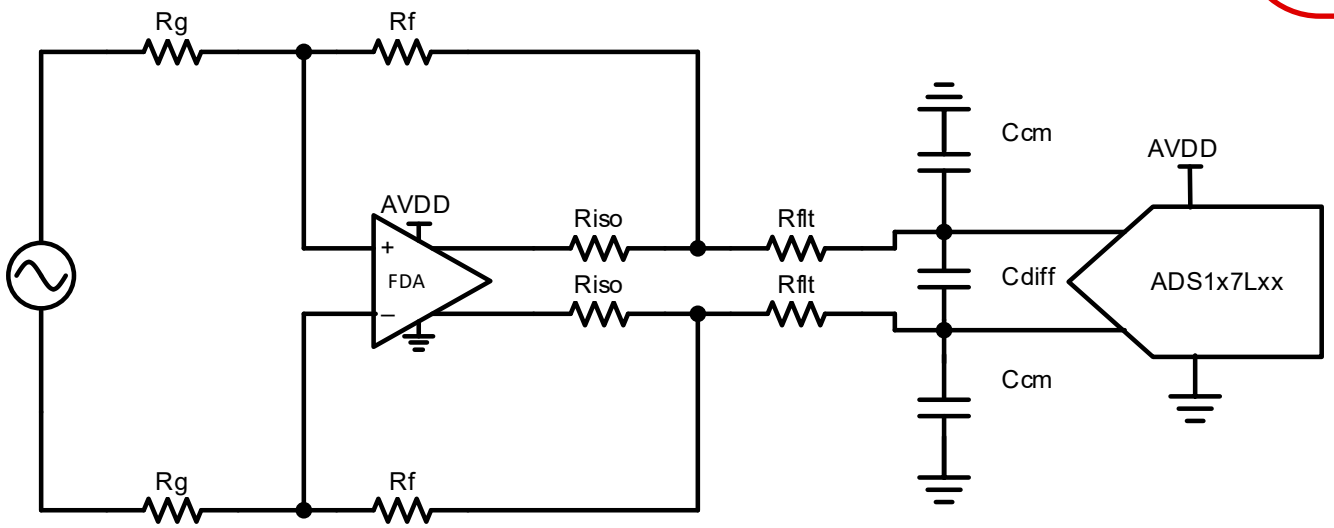
High Speed Delta Sigma ADC – Input Recommendations

Resistor Recommendations

- Rg, Rf, Riso and Rflt metal film
- 0.1% or better tolerance for good matching
- Rf and Rg set gain of input stage
- Riso used to improve amplifier stability

Capacitor Recommendations

- Low tc C0G/NP0 ceramic capacitors
- High-quality film capacitors
- 1% or better tolerance
- Optional common mode C_{CM} capacitors
  - ✓ $C_{CM} = 1/10 \times C_{DIFF}$



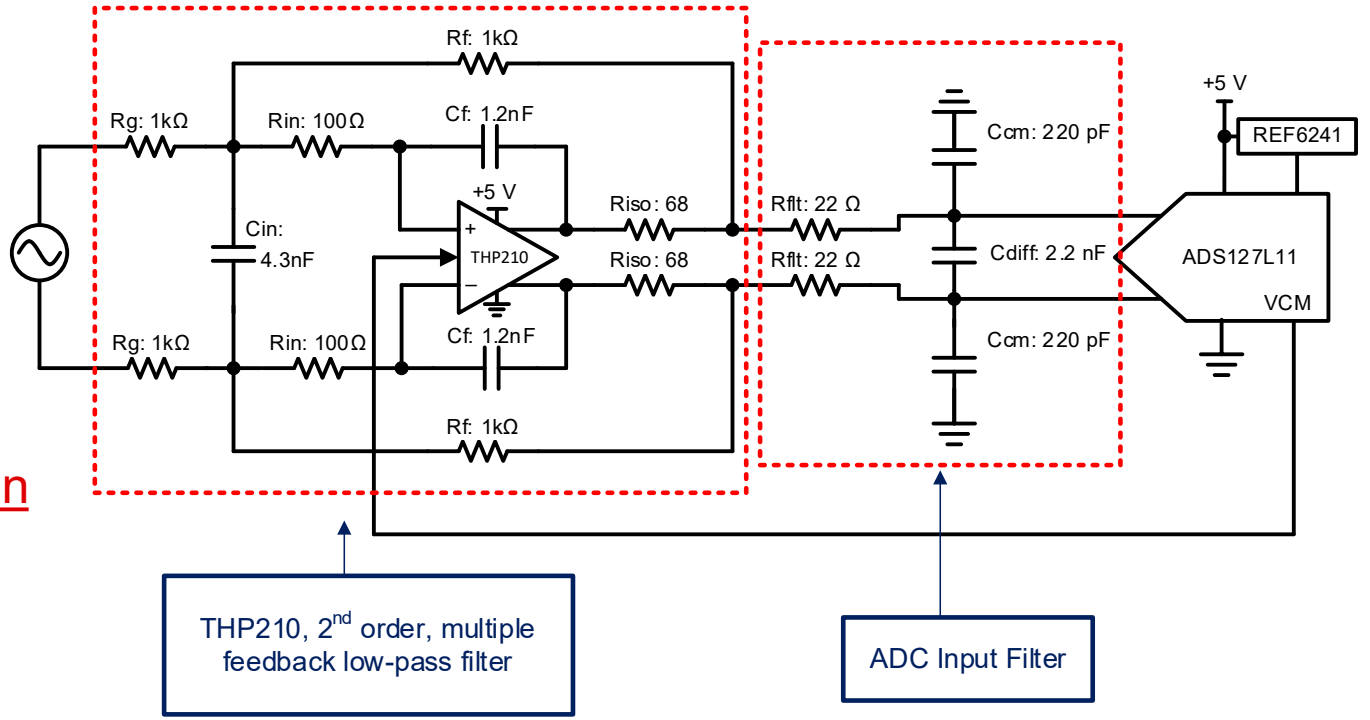
Amplifier Recommendations

- Fully Differential Amplifiers
  - ✓ THP210,THS4551,THS4561
- Differential output instrumentation
  - ✓ INA851, PGA854, PGA855
- Standard Operational Amplifiers
  - ✓ OPA325, OPA320, OPA328

THP210 + ADS127L11: General Purpose Data Acquisition Card Example

Example Design Steps:

- Select ADC input filter component values
- Select MFB filter component values
  - ✓ Use MFB filter Equations
    Design Methodology for MFB Filters in ADC Interface Applications
  - ✓ Alternative: Use filter tool
    FilterPro3.1 Link
- Verify AC Performance using SPICE
  - ✓ Stability Analysis
  - ✓ System Noise
  - ✓ AC Freq Response Analysis
  - ✓ ADC Transient Settling



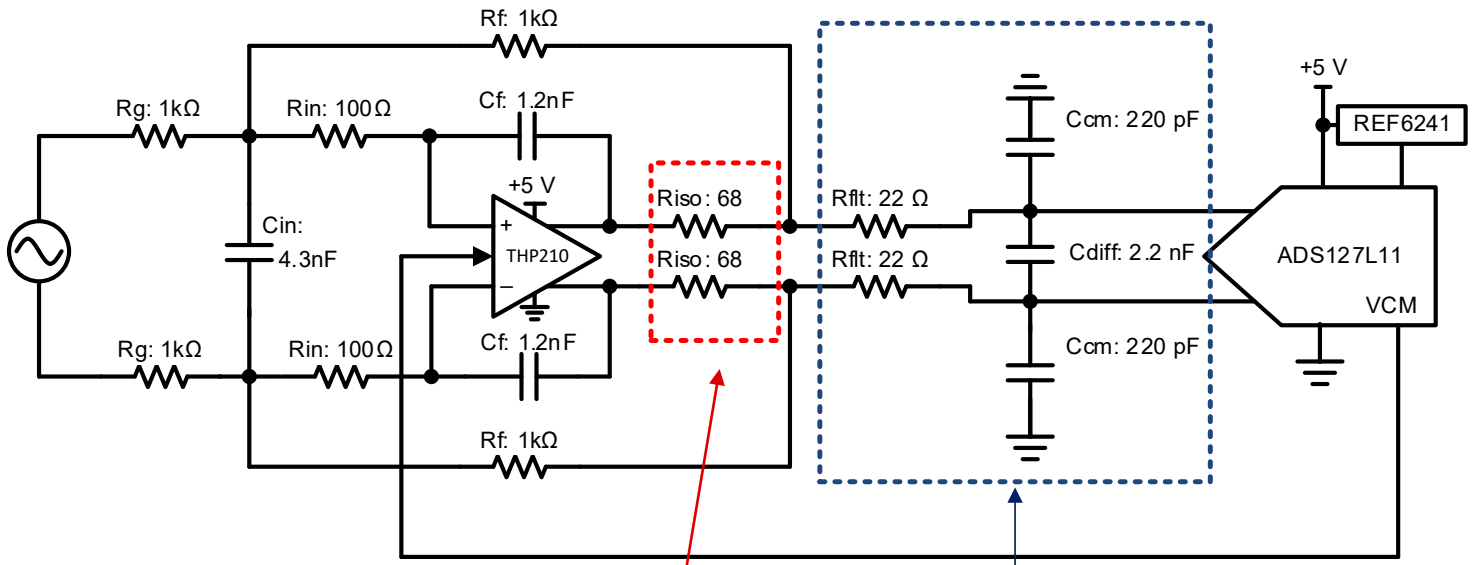
Example Critical Specs:

- BW: f(-3dB) = 150kHz, f(-0.2dB) = >20kHz
- Attenuation: -90dB at f_{MOD}= 12.8MHz
- Noise/SNR: 106-dB

THP210 + ADS127L11: Select ADC input filter Components

ADC RC filter at the ADC inputs serves two purposes:

- Provides a third pole, increases filter roll-off.
- Charge reservoir to filter the sampled input of the ADC



Riso resistors inside FB loop help further isolate the amplifier outputs, to improve filter phase margin

ADC Input Filter

ADC input filter selection

- C_{diff} :
  - ✓ C_{DIFF} should be 100x or greater than Delta-Sigma C_{IN} sample-and-hold capacitor
  - ✓ ADS1x7Lxx C_{IN} = 7.4pF
  - ✓ Minimum C_{diff} 740pF up to 22nF
  - ✓ This example, C_{diff} = 2.2nF
- C_{cm} :
  - ✓ C_{CM} scale to 1/10 of C_{diff} for best common-mode noise rejection
- R_{flt} :
  - ✓ R_{flt} are outside the feedback loop, and works as an isolation resistor for amplifier to remain stable
  - ✓ R_{flt} <100Ω to avoid non-linearities and settling errors.
- R_{iso}:
  - ✓ Inside the loop improves stability: Typical range of 20Ω to 100Ω
- **Ensure to verify FDA stability and phase margin via simulation**

THP210 + ADS127L11: THP210 FDA Stability

Simulate Phase Margin on TINA-TI

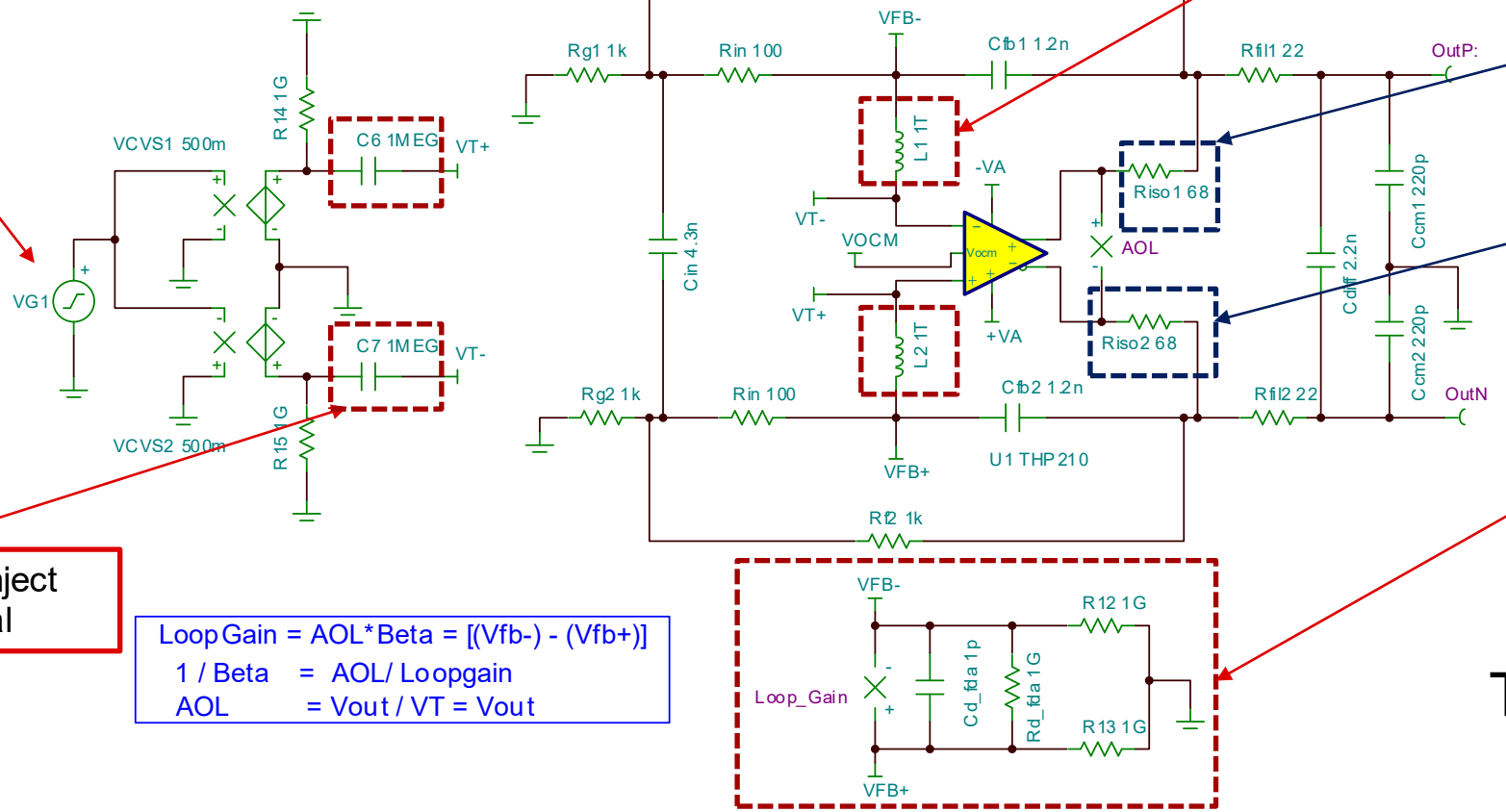
Large Inductors to Simulate Open-Loop

AC Small-Signal Test Source

Riso resistors inside loop:

Adjust to improve phase margin:

Riso = ~20Ω to ~100Ω



Large Capacitors to Inject Voltage AC Test Signal

Loop Gain = AOL*Beta = [(Vfb-) - (Vfb+)]
1 / Beta = AOL/ Loopgain
AOL = Vout / VT = Vout

Measure loop gain phase:

Loop-Gain $[(V_{FB-}) - (V_{FB+})]$

Reflect the Differential Input Impedance (data sheet values)

TINA-TI Simulation

TINA_THP210_MFB_Stability_ADS127Lxx.TSC

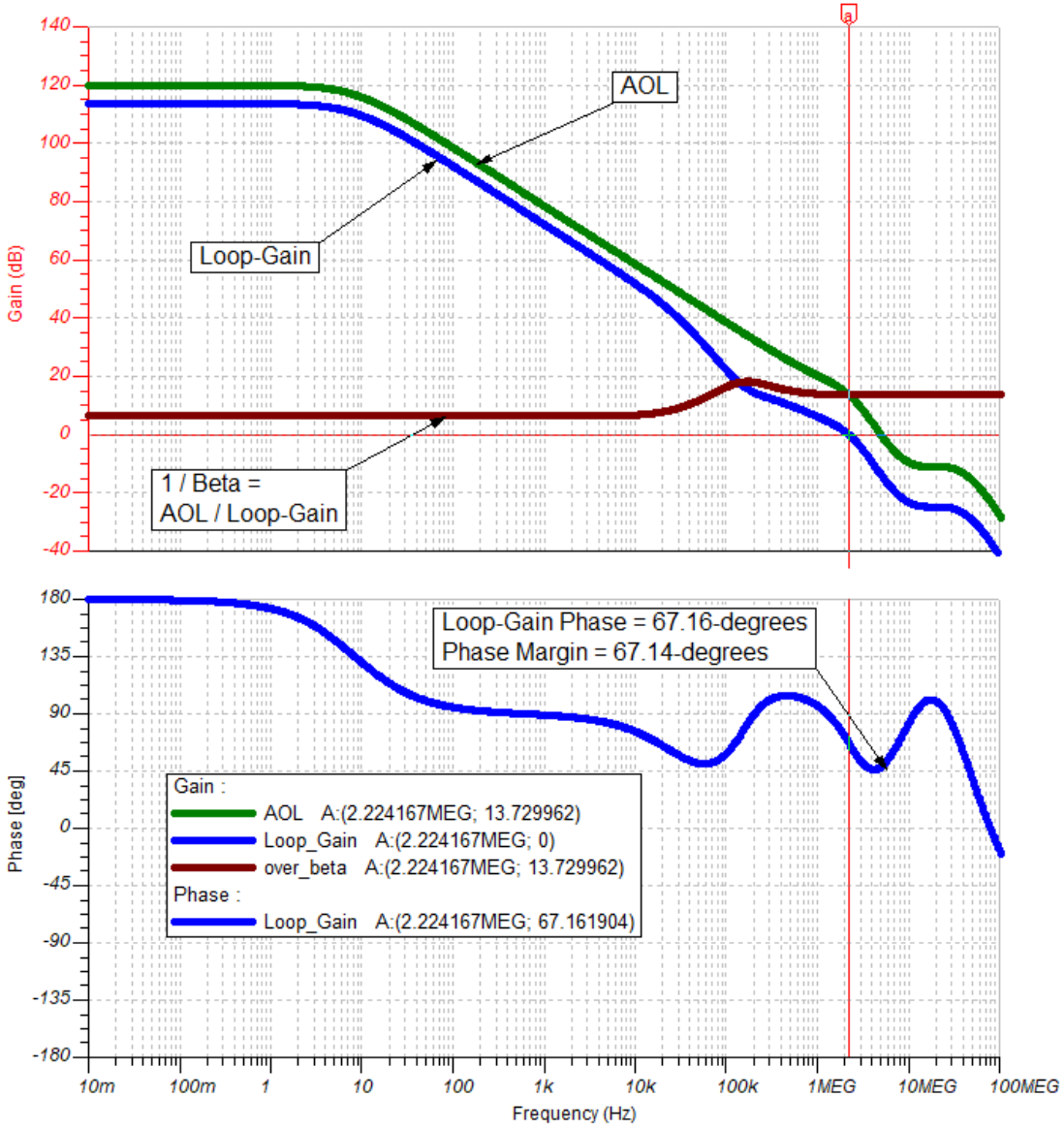
Input impedance differential mode	Input pins at $[(V_{S+})-(V_{S-})]/2$	1||1	GΩ || pF

THP210 + ADS127L11: THP210 FDA Stability

Simulate Phase Margin on TINA-TI

- AOL = Vout (differential FDA output pins)
- Loop-Gain = [(V_{FB-}) – (V_{FB+})]
  (see schematic)
- 1 / Beta = AOL / Loop-Gain
  (Use TINA-TI Post Processor)
- Phase Margin:
  - Monitor Phase Shift of Loop-Gain from low frequency (close to DC) to 1-decade above circuit GBW
  - Phase Margin at AOL and 1 / Beta intersection (or when Loop-Gain = 0-dB)
  - Allow a conservative >55° of phase Margin for MFB filters
  - In this Example: Phase Margin = 67°

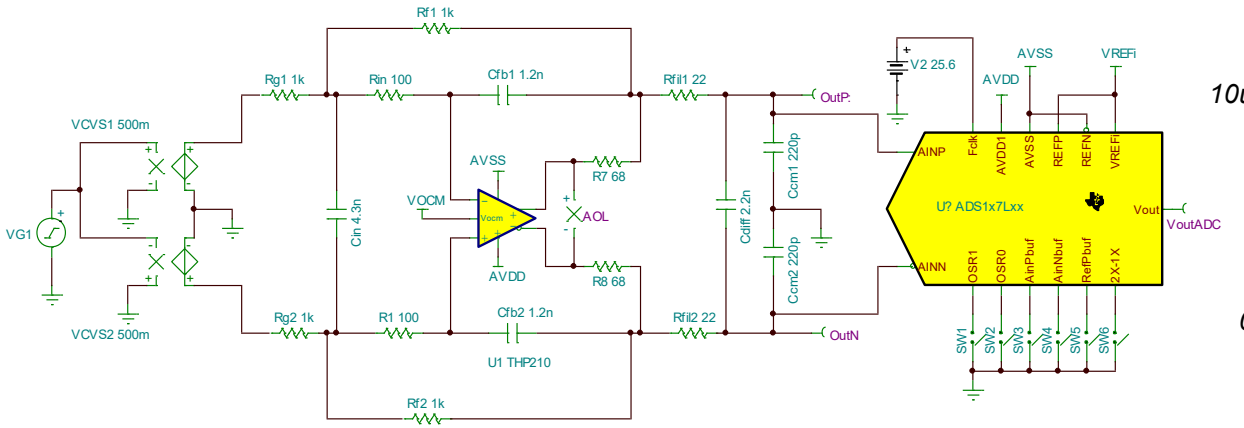
    Circuit is stable!!

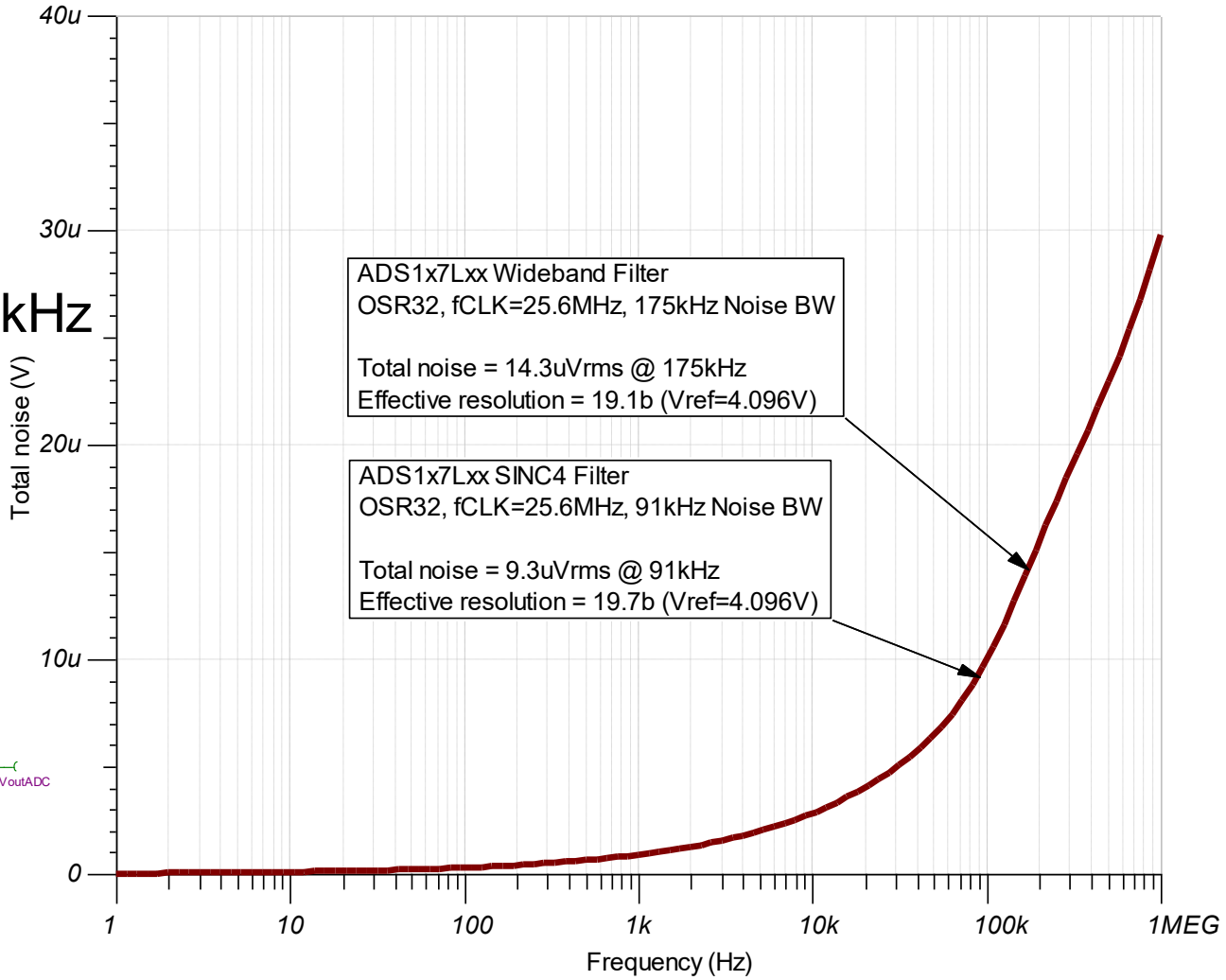


THP210 + ADS127L11: Total System Noise

Simulate Total Integrated Noise

- ADC noise only (Wideband Filter, 400ksps)
  - ✓ 10.6uVrms, Effective Resolution 19.5b
- Total system noise (including THP210)
  - ✓ 14.3uVrms, Dynamic Range 106.1dB
  - ✓ Noise limited by wideband filter at 175kHz
- Total system noise, SINC4 filter, 400ksps
  - ✓ 9.3uVrms, Effective Resolution 19.7b
  - ✓ Noise limited by SINC4 filter at 91kHz

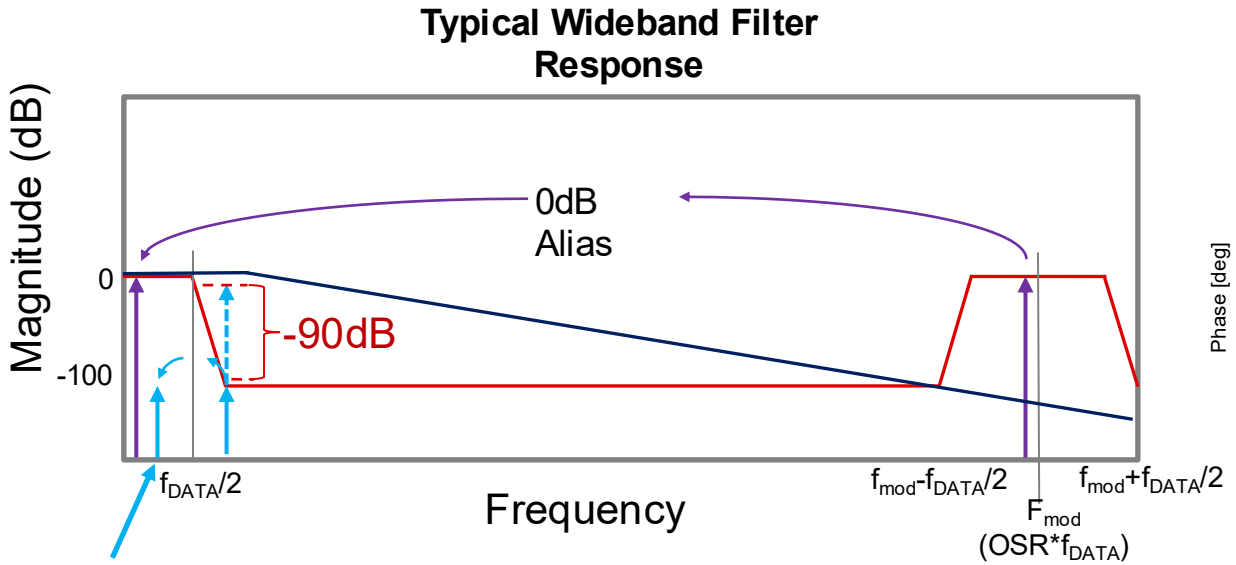


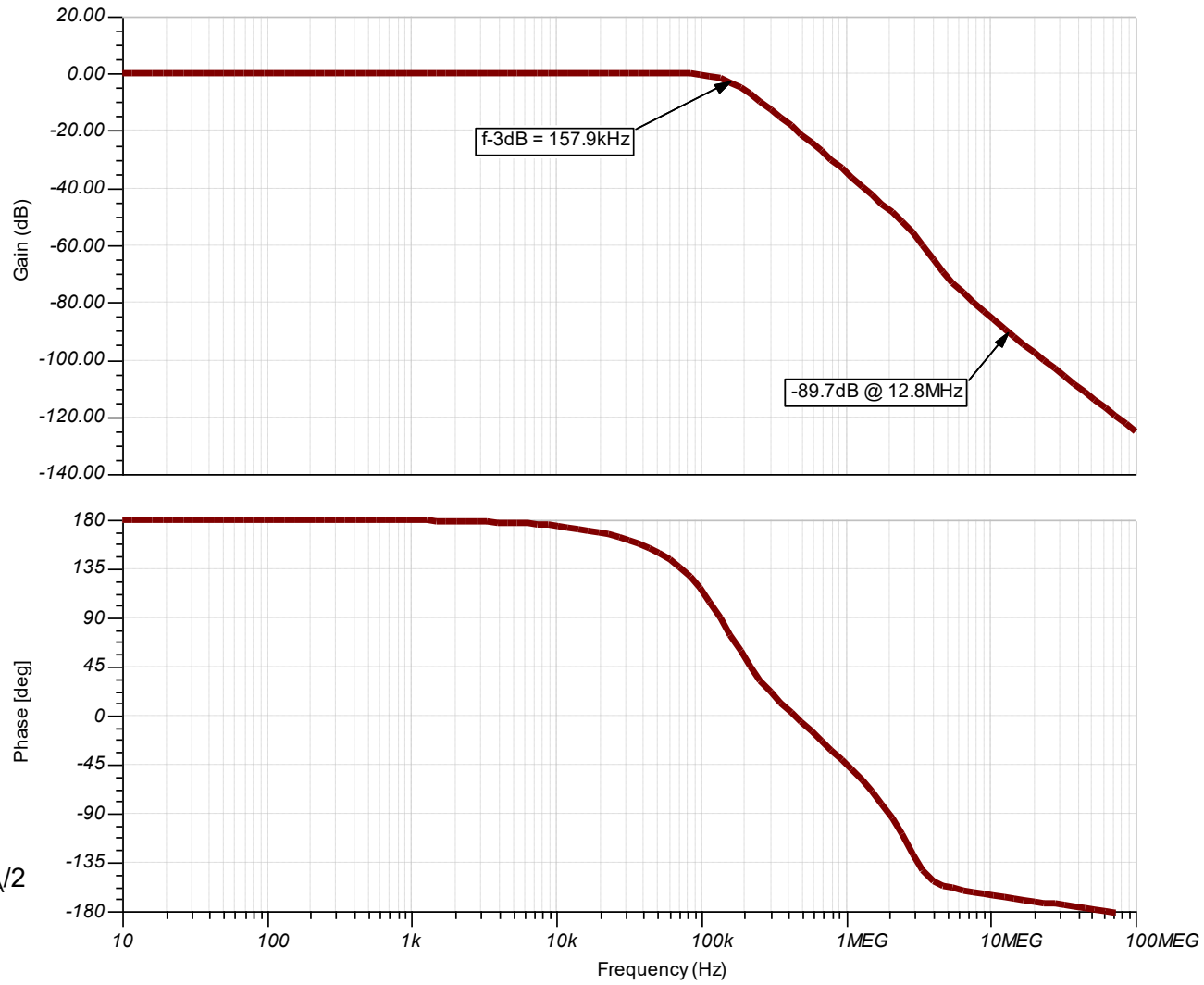


THP210 + ADS127L11: AC Response

Simulate AC Response

- -3dB bandwidth of 157.9kHz
  - ✓ Target BW>150kHz
- -90dB attenuation at modulator frequency
  - ✓ -89.7dB at 12.8MHz





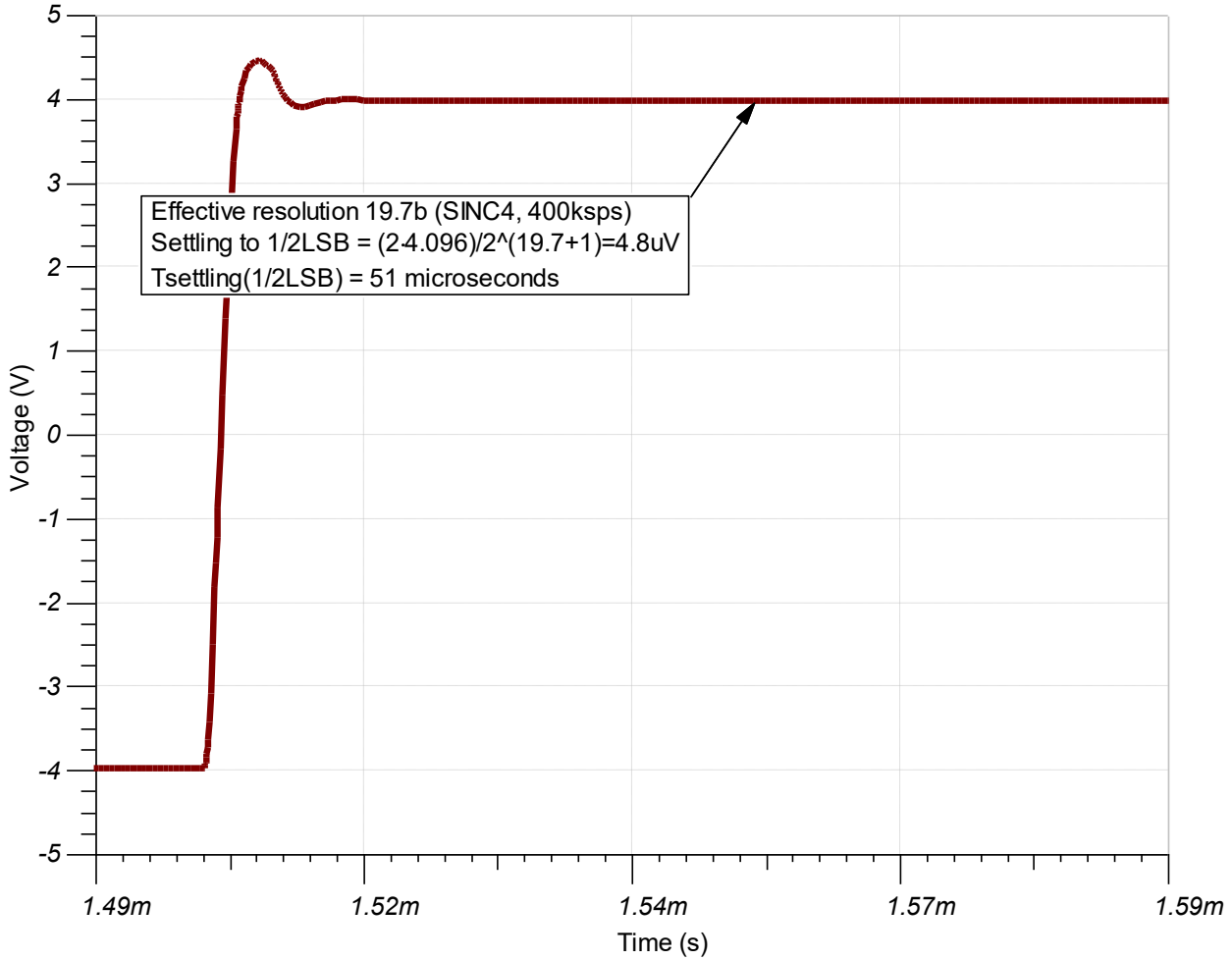
THP210 + ADS127L11: Step Input Settling Time using Low-Latency Filter

Simulate Transient Response of Step Input

- ADS1x7Lxx family includes low-latency filter
  - ✓ SINC4 filter settles in about 4 data cycles
  - ✓ 400ksps SINC4 latency (settling) time of 10.63µs
  - ✓ Input filter settling time to 19.7b of effective resolution
- Total settling time
  - ✓ THP210 AAF + ADS1x7Lxx SINC4
  - ✓ 51µs + 10.63µs = 61.63µs

TINA-TI Simulation

TINA_THP210_MFB_AC_Noise_Transient_ADS1x7Lxx.TSC



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