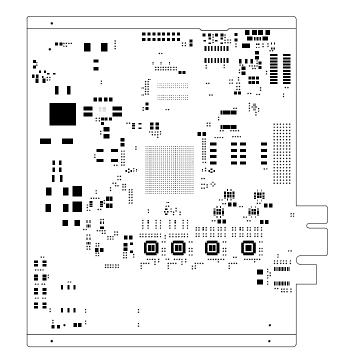
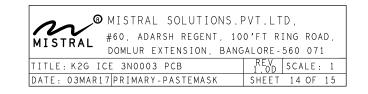


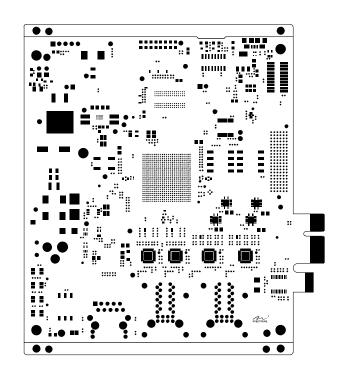
MISTRAL SOLUTIONS. F MISTRAL #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BANG	O'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV 1.0D SCALE: 1
DATE: 03MAR17 PRIMARY-SILKSCREEN	SHEET 02 OF 15

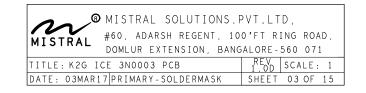
SPT Scale=0.65 Fri Mar 03 13:10:49 2017



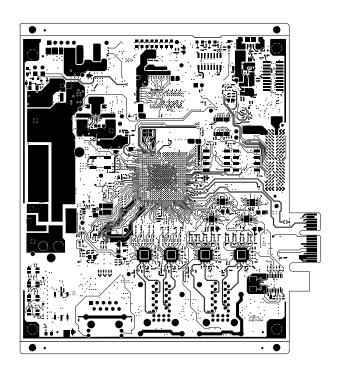


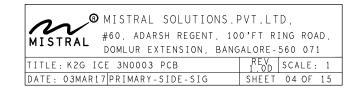
SMT Scale=0.65 Fri Mar 03 13:10:50 2017



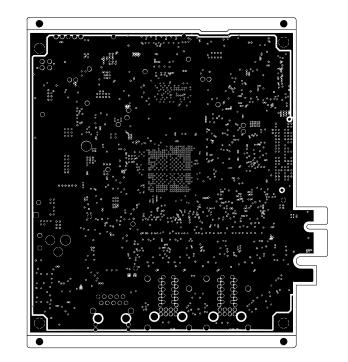


TOP Scale=0.65 Fri Mar 03 13:10:50 2017



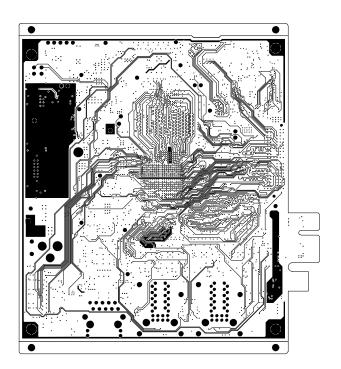


L2_GND1 Scale=0.65 Fri Mar 03 13:10:50 2017



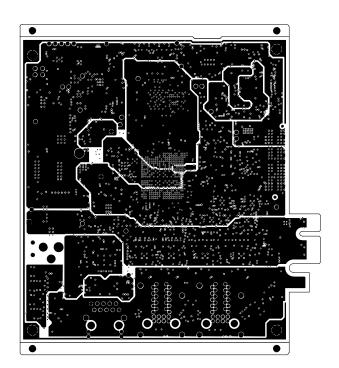
MISTRAL SOLUTIONS.I #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BANC)'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV 1.0D SCALE: 1
DATE: 03MAR17 GROUND-PLANE-01	SHEET 05 OF 15

L3_SIG1 Scale=0.65 Fri Mar 03 13:10:50 2017



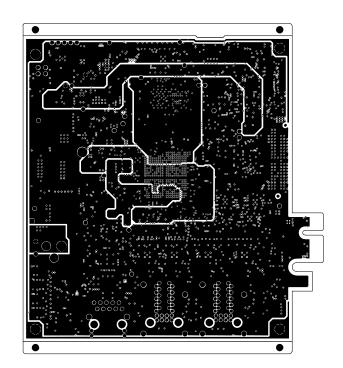
INTERNAL SOLUTIONS. MISTRAL SOLUTIONS. #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BANG	O'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV SCALE: 1
DATE: 03MAR17 INNER-SIGNAL-01	SHEET 06 OF 15

L4_PWR1 Scale=0.65 Fri Mar 03 13:10:50 2017



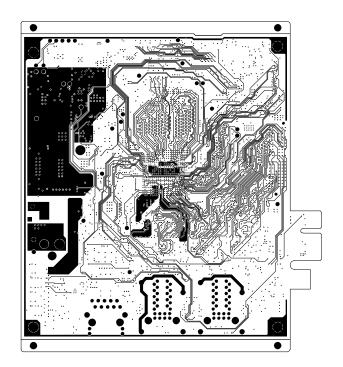
MISTRAL SOLUTIONS. MISTRAL #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BAN	O'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV 1.0D SCALE: 1
DATE: 03MAR17 POWER-PLANE-01	SHEET 07 OF 15

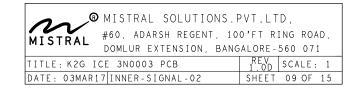
L5_PWR2 Scale=0.65 Fri Mar 03 13:10:50 2017



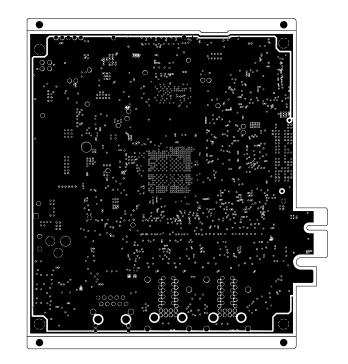
MISTRAL SOLUTIONS. #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BANG	O'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV 1.OD SCALE: 1
DATE: 03MAR17 POWER-PLANE-02	SHEET 08 OF 15

L6_SIG2 Scale=0.65 Fri Mar 03 13:10:50 2017



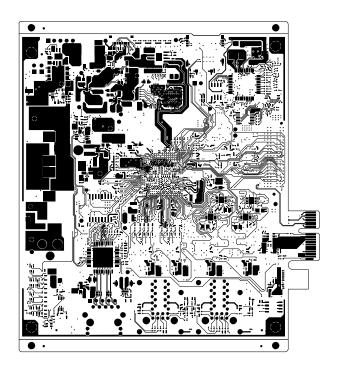


L7_GND2 Scale=0.65 Fri Mar 03 13:10:50 2017



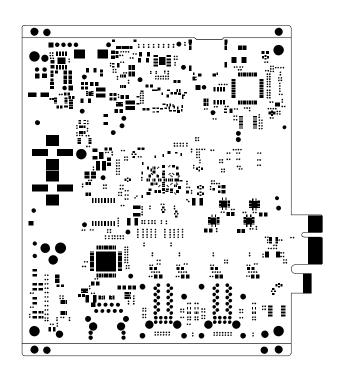
MISTRAL SOLUTIONS. #60, ADARSH REGENT, 10 DOMLUR EXTENSION, BANG	O'FT RING ROAD,
TITLE: K2G ICE 3N0003 PCB	REV 1.0D SCALE: 1
DATE: 03MAR17 GROUND-PLANE-02	SHEET 10 OF 15

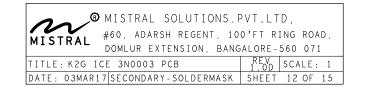
BOTTOM Scale=0.65 Fri Mar 03 13:10:51 2017



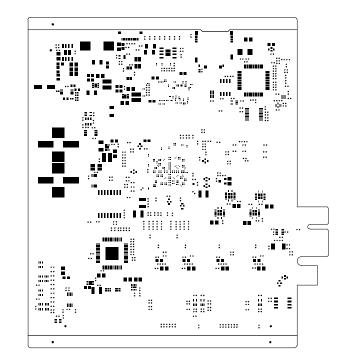


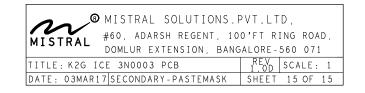
SMB Scale=0.65 Fri Mar 03 13:10:51 2017



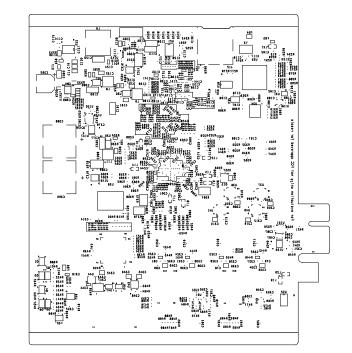


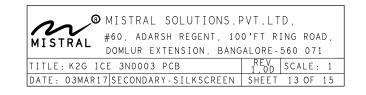
SPB Scale=0.65 Fri Mar 03 13:10:51 2017





SSB Scale=0.65 Fri Mar 03 13:10:51 2017





	DRILL CH	ART: TOP to BOT	ТОМ		
	ALL UN	IITS ARE IN MILS			
FIGURE	SIZE	TOLERANCE	PLATED	QTY	
	10.0	+2.0/-2.0	PLATED	2819	
•	35.0	+ 3 . 0 / - 3 . 0	PLATED	66	
•	40.0	+2.0/-2.0	PLATED	13	
۰	40.0	+3.0/-3.0	PLATED	22	
4	42.0	+3.0/-3.0	PLATED	2	
	50.0	+3.0/-3.0	PLATED	2	
۸	62.99	+3.0/-3.0	PLATED	8	
۲	67.0	+3.0/-3.0	PLATED	2	
8	120.0	+ 3 . 0 / - 3 . 0	PLATED	2	
C	138.0	+ 3 . 0 / - 3 . 0	PLATED	5	
N	140.0	+3.0/-3.0	PLATED	1	
0	50.0	+2.0/-2.0	NON-PLATED	2	
У	122.05	+2.0/-2.0	NON-PLATED	4	
¢	125.98	+2.0/-2.0	NON-PLATED	2	
\oplus	126.0	+ 3 . 0 / - 3 . 0	NON-PLATED	4	

FAB NOTES:

-

- 1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.
- THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2 AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2. CURRENT REVISIONS.
- 3. BOARD MATERIAL SHALL BE IT180A OR EQUIVALENT, ROHS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B. COLOR: NATURAL.
- 4. BOARD MATERIAL & CONSTRUCTION TO BE UL94V0 CERTIFIED AND MARKED ON TOP SIDE OF FINISHED BOARD.
- MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .002 INCH.
- 6. OVERALL BOARD THICKNESS TO BE .0625 +/- 10% AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
- 7. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
- 8. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-356 NETLIST.
- 9. ALL VIAS TO HAVE SOLDERMASK. VIAS ON THE PADS SHALL BE MASK OPENED.
- 10. ALL UNCONNECTED VIA/PADS SHALL BE SUPPRESSED IN THE INTERNAL LAYERS.
- 11. EDGE FINGER SHALL BE PLATED WITH HARD GOLD AS PER IPC 6012 CLASS 2.
- 12. THERE ARE 9 (NINE) INTENTIONAL SHORTS ON THE BOARD.

PROCESS NOTES:

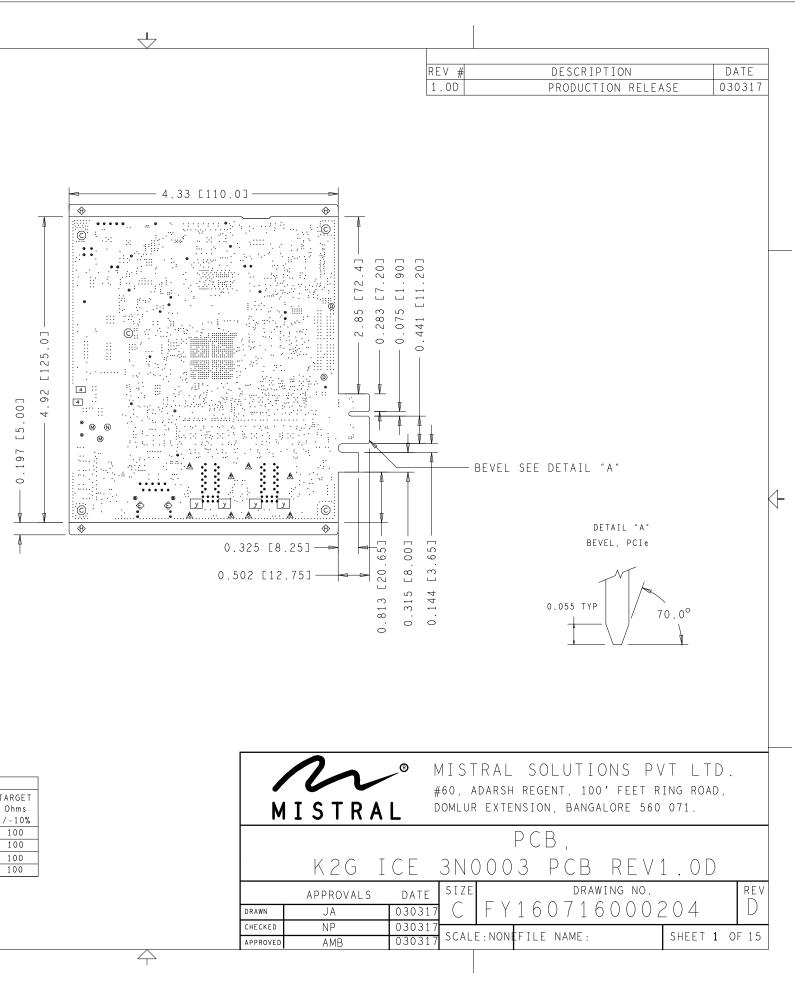
- 1. PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMMERSION GOLD, NICKEL 150 MICROINCHES THK MIN GOLD 2-8 MICROINCHES THK MIN.
- 2. APPLY LPI SOLDERMASK OVER BARE COPPER (SMOBC) COLOR: BLACK SOLDERMASK SHALL CONFORM TO IPC-SM-840, CLASS H. CURRENT REV.
- 3. SOLDERMASK ARTWORK HAS ZERO (0) OVERSIZED PADS. FABRICATION VENDOR IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS. 4. APPLY LPI SILKSCREEN OR EQUIVALENT PER THE ARTWORK.

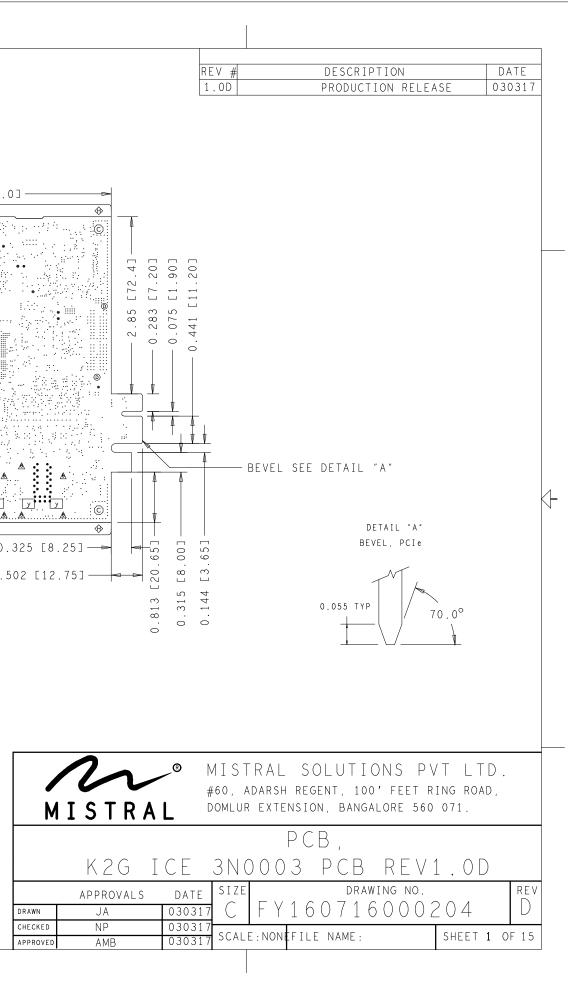
COLOR: WHITE.

	SINGLE - ENDED			EDGE-COUPLED DIFFERENTIAL						
LAYERS	TRACE WIDTH	TARGET Ohms	TRACE WIDTH	TARGET Ohms	TRACE WIDTH	TRACE SPACE	TARGET Ohms	TRACE WIDTH	TRACE SPACE	TARGET Ohms
	in mils	+/-10%	in mils	+/-10%	in mils	in mils	+/-10%	in mils	in mils	+/-10%
L1_TOP	6.11	50	-	-	4.5	4.5	90	4.0	6.0	100
L3_SIG1	5.5	50	-	-	-	-	-	4.0	8.5	100
L6_SIG2	5.5	50	-	-	-	-	-	4.0	8.5	100
L8_BOTTOM	6.11	50	-	-	4.5	4.5	90	4.0	6.0	100
	0.11					1.0			0.0	
NOTE :										

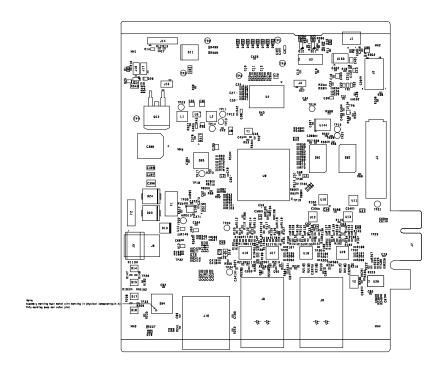
IMPEDANCE REQUIREMENT :- THIS DESIGN MAY NOT CONTAIN ALL THE FEATURES

LISTED IN THE ABOVE TABLE

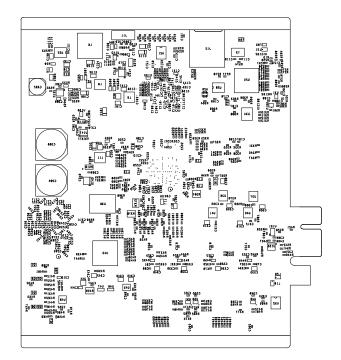




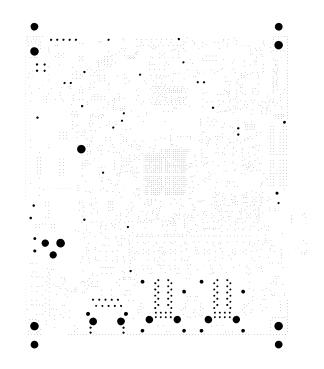
TASY Scale=0.65 Fri Mar 03 13:10:51 2017



BASY Scale=0.65 Fri Mar 03 13:10:51 2017



DRILL Scale=0.65 Fri Mar 03 13:10:51 2017



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